27.0   ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [†]

Ambient temperature under bias...-40°C to +125°C

Storage temperature ....-65°C to +150°C

Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) ....-0.3V to (VDD + 0.3V)

Voltage on VDD with respect to Vss ....-0.3V to +7.5V

Voltage on $\overline{MCLR}$ with respect to Vss **(Note 2)** ....0V to +13.25V

Total power dissipation **(Note 1)** 1.0W

Maximum current out of Vss pin ....300 mA

Maximum current into VDD pin ....250 mA

Input clamp current, IIK (VI < 0 or VI > VDD)..±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ....±20 mA

Maximum output current sunk by any I/O pin..25 mA

Maximum output current sourced by any I/O pin ....25 mA

Maximum current sunk by all ports ....200 mA

Maximum current sourced by all ports ....200 mA

Note 1:   Power dissipation is calculated as follows:
Pdis = VDD x {IDD − Σ IOH} + Σ {(VDD − VOH) x IOH} + Σ(VOL x IOL)

2:   Voltage spikes below Vss at the $\overline{MCLR}$/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$/VPP/RE3 pin, rather than pulling this pin directly to Vss.

40-Pin PDIP