Bilkent University

Department of Computer Engineering

CS 223 - Digital Design

Highway Racing

Şamil İraz (21501033)

Çağatay Sel (21502938)

Section-1

10.04.2017

Final Report

Block Descriptions

Clock Divider

Inputs : Clk_in, Basys3 clock.
Speed, Speed of the game. [7:0] Score, user score.
Output : Clk_out, clock that will be used for car generation, shifting and user input.

Description: Divides 100 Mhz clock signal of Basys3 and emits the clock signal that will be used for the game.

Car Generator

Inputs : Clk_out, reset

Output : [23:0] New_row, upcoming row of the game , [7:0] Obstacle Place

Description: This module will generate 24 bit outputs that represent a row of the dot matrix. 0's are available spaces and 1's are cars. Generation of the cars will be according to the pattern we will design. This pattern will repeat itself.

Dot Matrix Driver

Inputs : Clk_game; [7:0][23:0] positions, Positions of the cars.

Outputs: [7:0] rowSelector, Outputs used to light the leds. SH_CP,ST_CP,MR,OE,DS.

Description: This matrix gives inputs for the 8x8 RGD Matrix.

Shifter

Desciption: This module shifts each row to down and it also determines if we crash or not.

Inputs : clk_game, clk_matrix,[1:0]user_input, reset, [23:0] newRow, [7:0] obstaclePlace.

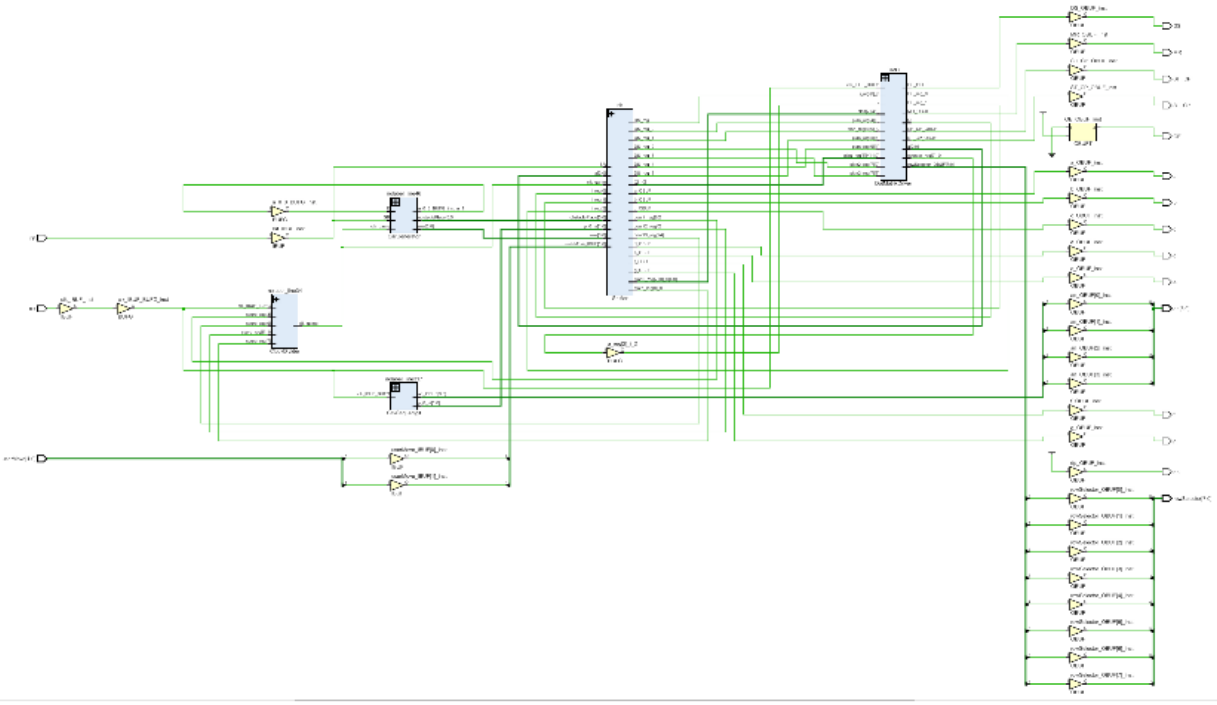
Output : [7:0][23:0] plan, [7:0] rowSelector, SH_CP,ST_CP,MR,OE,DS, [7:0] score.

SevSeg Display

Inputs: Clk, [3:0] in0, [3:0] in1, [3:0] in2, [3:0] in3.
Output: a,b,c,d,e,f,g,dp,[3:0] anode.

This module displays score on the Basys3.

Circuit Schematic



References

DotMatrixDriver: Taken from Serhat Akdağ.

SevSegDisplay: Taken from Lab5 Resources.