Assignment 4

CSE260: Digital Logic Design

Department of Computer Science and Engineering

Semester : Fall 25 **Marks: 5**

Graded (5 marks)

1. Short Questions:
   a. Explain the difference between a latch and a flip-flop. [0.5]
   b. Describe the working of a JK flip-flop and explain how it overcomes the undefined state of an SR flip-flop. [0.5]
   c. What is the importance of the clock signal in flip-flops? [0.5]
   d. Why do we need state diagrams to understand sequential circuits? [0.5]

2. Implement the following up/down counter using SR FF: 2 ↔ 4 ↔ 5 ↔ 6 ↔ 7 ↔ 2
   Note: Represent each number using ABC variables. Consider the selection bit as: M=0 (up) and M=1 (down). The order of the variables must be **MABC**. [1.5]

3. Convert the following circuit diagram to state diagram: [1.5]