BRAC UNIVERSITY

Department of Computer Science and Engineering

CSE 260: Digital Logic Design

Examination: Quiz III **Duration: 25min**
Semester : Fall 2025 **Full Marks: 15**

Name:	ID:	Section:

1	**Draw** a circuit using a 4-bit parallel adder that follows the following condition - If A is div by 4 and B is less or equal to 7, perform **A-B** - Else perform **A+B**	**4**
1	**Implement** XNOR gate using **one** 2:1 MUX only. You can not use multiple MUX.	**3**
2	Design a 4-to-2 **LSB** Priority Encoder that follows all general priority encoder rules, except for the special cases below: a. If two inputs are enabled, select the MSB among the enabled bits. b. If three inputs are enabled, select the middle enabled bit. c. In all other cases, it will work like an encoder that prioritizes the enabled LSB bit. **Draw** the truth table for the Encoder and **find** the simplified equation for the encoder using **Kmap** [4+4]	**8**

Rubric

Drew the PA correctly 1st condition is correct 2nd conditions are correct	1 1.5 1.5
MUX correct Table and output correct Correct inputs shown	0.5 1.5 1
Table correct Simplification correct	6 2