MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

EE 463 - Static Power Conversion II - Term Project

Simulation Report

Doge Power Inc.

12V - 100W Isolated DC-DC Converter

Mustafa Yıldız 2233013

Onur Öztaş 2330389

Table of Contents

Introduction

In electrical drivers, different power levels are required for different applications. Most of the small engines like window engine, wiper engine, air conditioner etc. requires 12V supply. The main power supply, whereas gives 400V input voltage for these applications. Therefore, designing a system that converts high input voltage to a low-level output voltage may need in here. Moreover, in order not to disturb the working performance of the other circuits from the faults may occur in somewhere, isolated systems are crucial. For that purpose, isolated power supplies are designed.

In this project, an isolated switched mode power supply design is conducted. This converter will be able to convert 220V to 400V input voltages to 12V 100W output voltage in a reasonable stability performance. The main duty in this job is to satisfy control loop in a way that system's both transient and steady state performances are quite good levels.

Throughout this report, first a topology selection is introduced. Then the subsystems of the project steps like controller design, snubber design, thermal design and magnetic design will be introduced one by one. At the end, by giving the simulation results the performance of the designed system can be evaluated.

1. Topology Selection

In this project 100W isolated dc-dc converter design is required. In the below, the project specifications are listed as follows:

- Minimum input voltage : 220V
- Maximum input voltage : 400V
- Output voltage : 12V
- Output Power : 100W
- Output voltage peak-peak ripple : 4%
- Line regulation : 3%
- Load regulation : 3%

For the design of such a system, first a suitable topology selection is required. Since the system should be an isolated system, the following topology alternatives can be chosen as follows:

- Flyback Converter
- Forward Converter
- Push – Push Converter
- Half Bridge
- Full Bridge

Flyback Converter:

Advantages of this converter are:

- No output inductance requirement
- Ability to supply multiple output voltages
- Less component requirement compared to the other converters

Disadvantages of this converter are:

- Closed loop bandwidth in CCM operation is narrow
- Large output capacitor requirement

Since our input margin is too large, this converter may not give good results in our conditions. Also, it is power ratings are top limit for our specifications. That may result in higher duty cycle requirement. For those reasons, this converter didn't select.

Forward Converter:

Advantages of this converter are:

- Drive circuit is simpler compared to other topologies
- One switching transistor is required

Disadvantages of this converter are:

- Transformer utilization is not sufficient compared to the push pull and bridge topologies. D_{max} is limited by 50%.

- Blocking voltage of the transistors are 2 times of the input voltage. That increases ratings of the component.
- It may go into DCM operation

In our design purposes, increasing transformer utilization is critical. Since this topology uses transformer insufficiently, it is not preferred in our design.

Half Bridge:

This topology presents best transformer utilization. It provides low cost and small space. However, when controller research is conducted, it is realized that the analog controllers for this topology is not applicable. Most of the controller stabilizes output voltage with respect to reference value. However, the input capacitance middle point is discarded almost all of the controllers. Therefore, due to the insufficient integrated circuits for this topology, it is not selected.

Full Bridge:

This topology generally preferred in larger than 500W applications. It has 4 transistors in the primary side of the topology. Since the input voltage level of this project is around 200-400V margin, selecting 4 transistors at those ratings will brings a lot of project costs. Therefore, for that reason this topology is discarded.

Push – Pull Converter:

This topology uses 2 input switch and 2 output diodes. Moreover, additional LC filter to the output is required. Since its transformer utilization is good, the required transformer core size is relatively small compared to others, and transformer ratings are smaller compared to the Forward. Also, its filter requirement is small compared to the Flyback and Forward topologies. It is one the biggest disadvantage is central top transformer structure. However, while considering the other advantages this converter has more useful for this project. Therefore, this one is selected as a SPMS design application.

2. Analytical Calculations and Simulations

Since the topology is Push-Pull, duty cycle should be between 0 and 0.5 because D is used twice during a period. We would like to have charging and discharging durations to be

close to each other in order to stay away from discontinuous conduction mode. We set up an xlsx file in order to observe the change in circuit parameters due to frequency, desired duty cycle etc. We set a duty cycle for the input voltage which is the mean of maximum and minimum and calculated D_{max} and D_{min} accordingly.

$$\frac{0.6}{2} = 0.3$$

$$\frac{220 + 400}{2} = 310$$

$$V_o = V_{in} * 2 * \frac{N_2}{N_1} * D$$

$$12 = 310 * 2 * \frac{N_2}{N_1} * 0.3$$

$$\frac{N_2}{N_1} = \frac{1}{16}$$

Duty cycle will be the controlled parameter in order to keep the output voltage constant with changing input voltage. We calculated the interval of duty cycle.

$$V_o = V_{in} * 2 * \frac{N_2}{N_1} * D_{min}$$

$$12 = 400 * 2 * \frac{1}{16} * D_{min}$$

$$D_{min} = 0.24$$

$$12 = 400 * 2 * \frac{1}{16} * D_{max}$$

$$D_{max} = 0.4364$$

Since the output side of the push-pull topology is identical to buck converter, output voltage ripple has the same characteristics with half of the period.

$$\frac{\Delta V_o}{V_o} = \frac{(1 - 2 * D)(\frac{1}{f_s})^2}{8 * L * C}$$

$$D = 0.4364\ (Worst\ Case)$$

$$0.04 > \frac{(1 - 2 * 0.4364)(\frac{1}{2 * f_s})^2}{8 * L * C}$$

$$L * C * {f_s}^2 > 0.09943$$

As we increase the frequency, we can use smaller components for L and C and reduce the cost. We set the switching frequency at 100kHz.

$$L * C > \frac{0.09943}{(10 * 10^3)^2}$$

$$L * C > 9.943 * 10^{-12}$$

We set L value as 160µH, so C value is calculated as:

$$C > \frac{9.943 * 10^{-12}}{160 * 10^{-6}}$$

$$C > 62.15\ nF$$

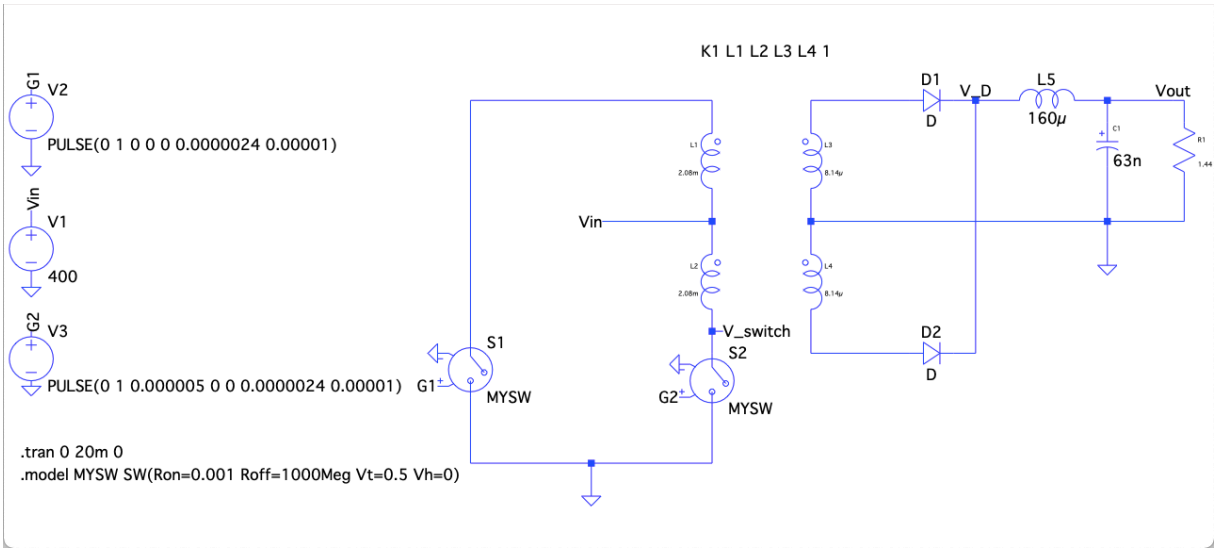


Figure 1. Circuit Schematic of Push-Pull Circuit without any Control

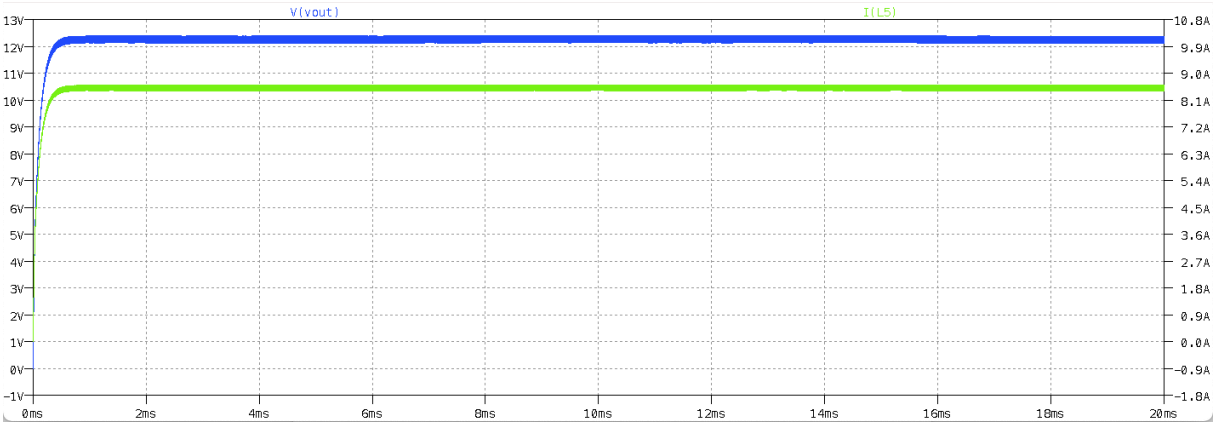


Figure 2. Output Voltage and Inductor Current Waveforms of Converter

As seen in Figure **2,** output voltage is in the limits of 4% ripple criteria. Maximum voltage rating of output capacitor should be higher than 12.48V. Maximum current flowing through output inductor should be higher than 8.333A, which can be also calculated as:

$$I_{L(out)-max} = \frac{100}{12}$$

$$I_{L(out)-max} = 8.333\ A$$

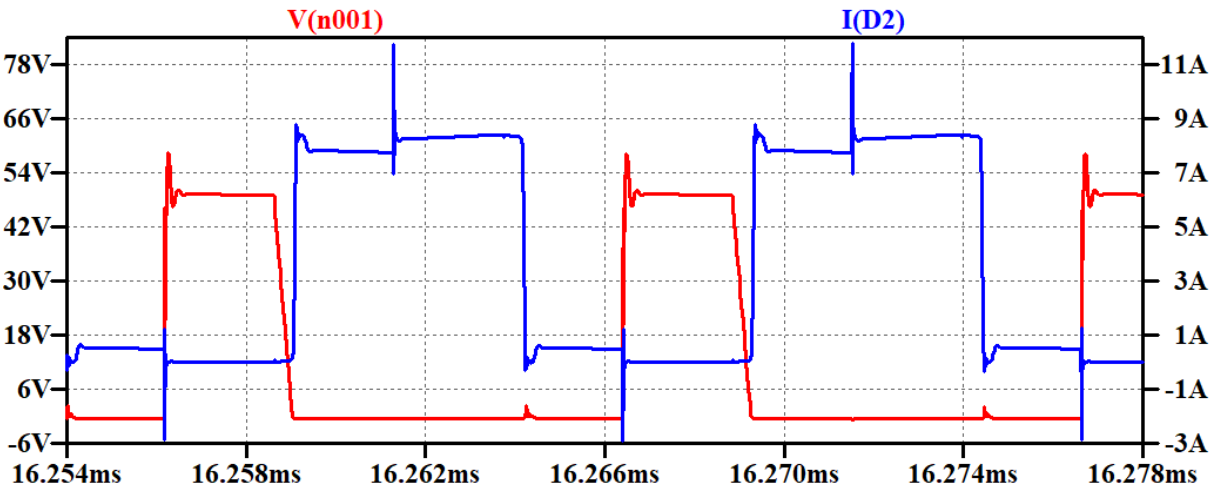


Figure 3. Voltage and Current Waveforms of DC Side Diodes at 400V Input Voltages

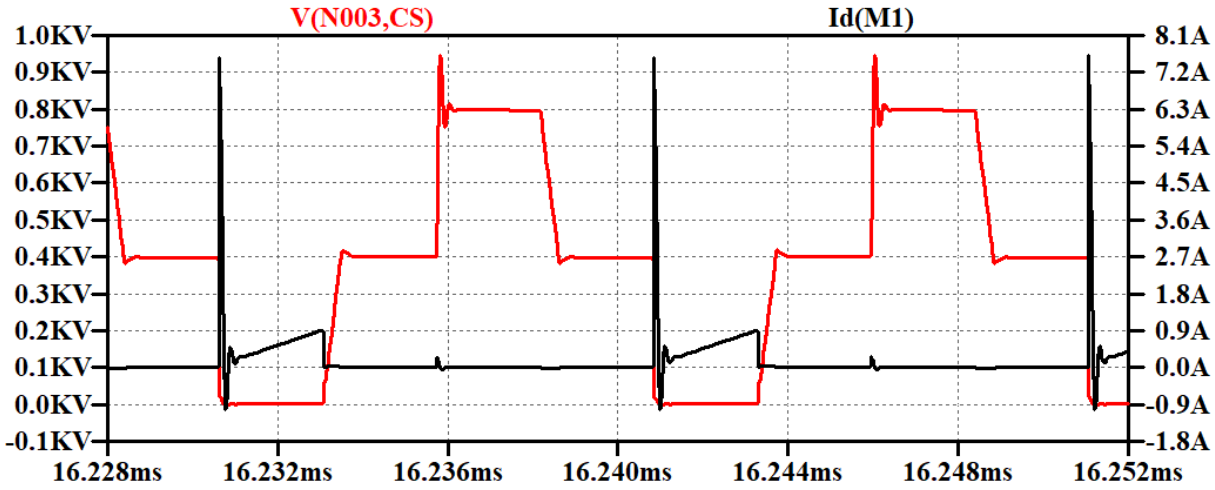


Figure 4. Voltage and Current Waveforms of Switches

As seen in Figure 3, diodes should be capable of handling 9A current and 50V reverse voltage. Switches should be able to block at least 800V and conduct more than 800mA according to Figure 4.

3. Controller Design

In this project, stable output is desired whereas input is changing from 220V to 400V. That yields a controller requirement. For this purpose, LT3723-1 current mode controller is selected as it will be expressed in component selection section. This controller can act both as controller and as gate driver for the MOSFETs. Therefore, it decreases the component requirement to a single component. However, the biggest drawback of this controller is that it does not satisfy the isolation criteria of the project. Therefore, in addition to this integrated circuit (IC) an opto coupler and opto coupler driver IC's is selected, which completes the isolation problem of this design. For opto-coupler MOC207M is selected, for its driver LT1431 IC is selected.

In designing controller, first the main IC should be programmed such that it suits in this application. For step by step improvement, the pin configuration and package information of this IC can be seen in Figure X.

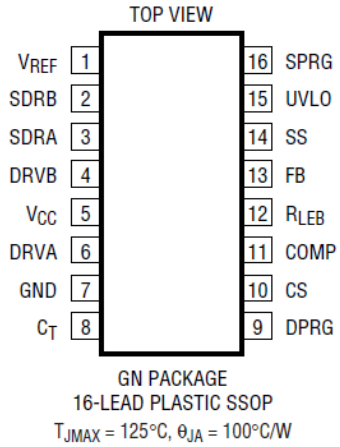


Figure 5. Pin configuration and packet information of LTC3723-1 IC

This project is designed with 100 kHz operating frequency. Selecting operating frequency high decreases, the size of the magnetic components and output filter components. However, while frequency increases the switching losses also increases. Therefore, that will yield less efficiency. Finding optimum point is crucial. For that purpose, 100kHz operating frequency is selected. In order to program IC to 100 kHz frequency, its C_T pin is used. The following formula programs the operating frequency of the IC by connecting capacitor from that pin to ground.

$$C_T = \frac{1}{2 * 14.8 * 10^3 * F_{OSC}}$$

$$C_T = 0.34\ nF$$

After inserting this capacitor, the frequency of the gate signals is measured as in Figure X.

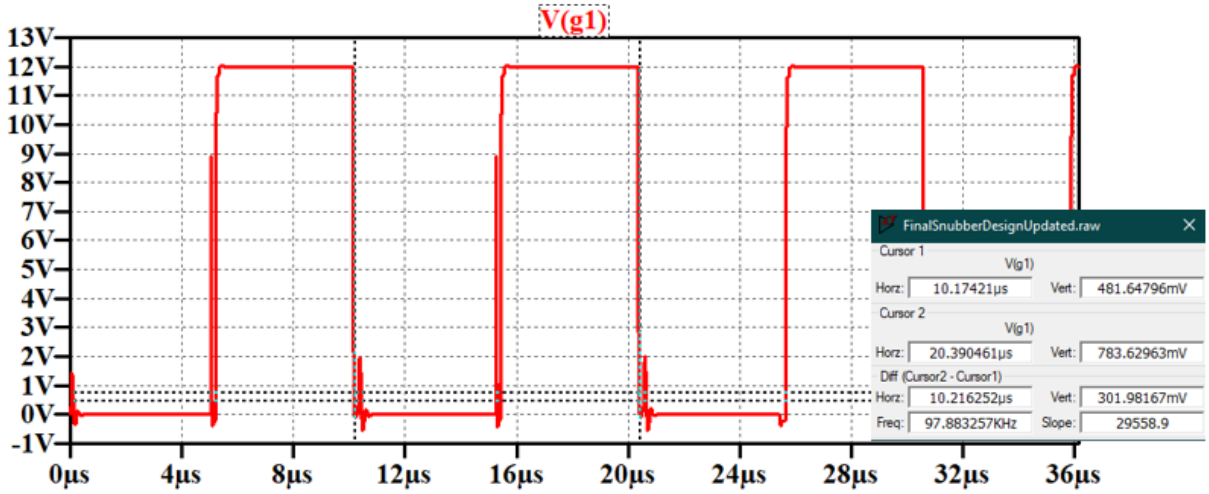


Figure 6. Frequency information of gate signals

Selecting capacitor value in large significant figures arranges the frequency exactly to the 100kHz. However, in practice it is not practical. Therefore, this amount is decided enough for this application.

In push pull topology, gates of the both MOSFETs are off during some time. That time is known as dead time. Dead time of this IC is programmed with connecting resistances to the SPRG and DPRG pins. The values are determined from the data sheet dead time plot. It is selected as higher as so that it suits in our application. They are selected as 250kΩ. That is enough to stabilize output in the 12V reference level.

Controllers provides controlled output by some external circuits constructed to the control pins. These circuits are known as ‘Compensator Circuits’. Since the control loop in this project is completed by using the opto-coupler circuits, the compensation circuits are constructed in the opto-coupler driver circuit pins. Also, feedback from the output is taken by the opto-coupler driver. Therefore, the feedback pin of the controller is connected to ground. It continuously provides output while compensation signal is provided. In the next subsection the compensator circuit design is explained in detail.

3.1. Compensator Circuit Design

The input voltage range in this application is quite large. Therefore, compensator circuit performance is crucial in order to stabilize output to 12V. There are 3 main compensator types, which are:

- Type I compensator
- Type II compensator
- Type III compensator

Type I is used for basic application. In SMPS designs, type II compensator is preferred generally. However, in large range application that may not be sufficient. In that cases, Type 3 compensator can be used. Since this project conducts in wide range input voltages, it is required to use type 3 compensator. In type 3 design, the following reference circuit configuration is referred.

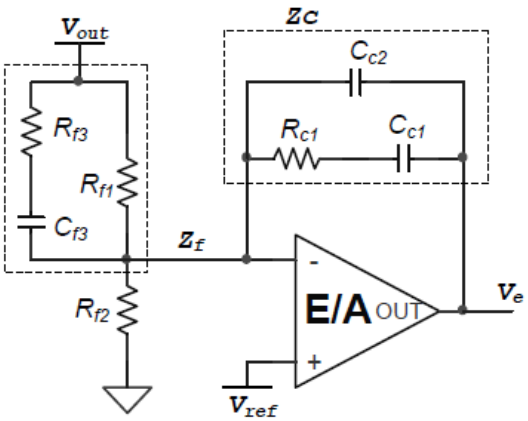


Figure 7. Type 3 compensator circuit configuration

In the design of these components, first pole zero locations are determined. For that purpose, the LC frequency of the output filter is calculated as:

$$F_{LC} = \frac{1}{2 * \pi * \sqrt{L * C}}$$

And, ESR frequency of the capacitor is calculated as:

$$F_{ESR} = \frac{1}{2 * \pi * R_{ESR} * C}$$

The pole-zero locations are selected by these frequencies accordingly as follows:

$$F_{Z2} = F_{LC}$$

$$F_{Z1} = 0.75 * F_{Z2} = 0.75 * F_{LC}$$

$$F_{P2} = F_{ESR}$$

$$F_{P3} = \frac{F_{sw}}{2}$$

$$F_0 \leq \frac{F_{sw}}{8}$$

Finally, these is a single pole at the origin, which is F_{p1}

The circuit components based on these formulas are calculated from the following formulas based on taking C_{f3} some suitable value, which can be 2.2nF as a good start. If not worked, it can be updated.

$$R_{f3} = \frac{1}{2 * \pi * C_{f3} * F_{p2}}$$

$$R_{f1} = \frac{1}{2 * \pi * C_{f3} * F_{z2}} - R_{f3}$$

$$R_{c1} = \frac{2 * \pi * F_0 * L_{out} * C_{out} * V_{osc}}{V_{in} * C_{f3}}$$

In here, the V_{osc} voltage is the oscillation voltage of the IC. It is 2.35V from datasheet.

$$C_{c1} = \frac{1}{2 * \pi * R_{c1} * F_{z1}}$$

$$C_{c2} = \frac{1}{2 * \pi * R_{c1} * F_{p3}}$$

These are the general formulas used in the design. However, finding values from these formulas generally not sufficient at first. It required fine tuning algorithms. Calculating again and again from at first step is a messy work. Therefore, as can be seen in Appendix A, a MATLAB m file is prepared.

When the first values are taken, they are simulated. They will stabilize at 12V output in both 220V and 400V input values. However, the final waveform of output voltage at steady state is not sufficient. It is oscillating very high. In order to solve this problem, the transfer function of the compensator circuit is extracted and written into the m file. Then, by plotting bode diagram of that transfer function, the effect of each component indicated above is observed one by one. It is crucial to obtain phase margin larger than 40 degrees. At first, it is around 40

degrees, and as said it is not good for output voltage stabilization. While observing each element effect to the bode plot, it is realized that increasing third pole frequency increases the phase margin of the system, and improves stability also. At final step third pole frequency is selected as:

$$F_{p3} = F_{sw} * 2.25$$

It results in -108 degrees phase at 100kHz frequency. It is phase margin is found as:

$$Phase_{margin} = Phase + 180$$

$$Phase_{margin} = -108 + 180 = 82\ degrees$$

The resulted phase margin is excellent for design. Its results are also very good both in terms of transient and in terms of steady state.

4. Snubber Circuit Design

In most of the industrial applications, designing circuits with low electromagnetic interference (EMI) is required. The reason for that is designing parts of a project in separately is not affected from this phenomenon because it has an effect to the neighboring components. They usually distort their operating frequencies and also operating performances. Higher EMI problems at some point also distort the operation performance of the product also. Therefore, suppressing those EMI spikes is critical. For that purpose, snubber circuits are preferred. There are 3 types of mostly used snubber circuit configurations. These can be order as:

- C snubber
- RC snubber
- R//D -C snubber

Inserting only C snubbers, decreases system operating speed. When system slows down, then it increases EMI radiation, which is also called ringings. To eliminate ringing R is inserted. In RC snubber that ringing also canceled. Therefore, it yields best result. In another application, resistor is parallel with diode and connected to capacitor in series. The purpose for this application decreasing resistive losses exists in the system. However, since this application works under 100kHz switching frequency, diode's switching losses are quite high. Also, the cost of the diodes will increase project costs. For that reasons, R-C snubber circuits are used.

Before starting the snubber circuit design, the drain-to-source voltage of MOSFET is observed as in Figure 8.

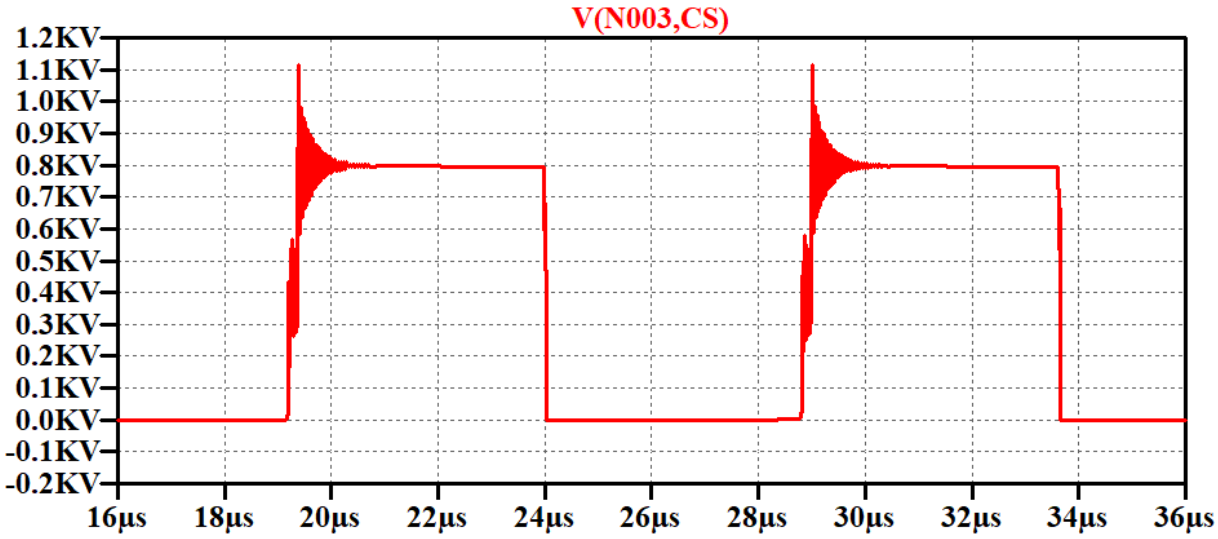


Figure 8. MOSFET drain-to-source voltage before snubber circuit

The effect of EMI radiations can be observed easily in this figure. Therefore, eliminating this is critical for SMPS design.

In the design of the snubber circuits, there is a guideline for the push-pull topology. Accordingly, first the resonance frequency of the spikes is measured as shown in Figure X.

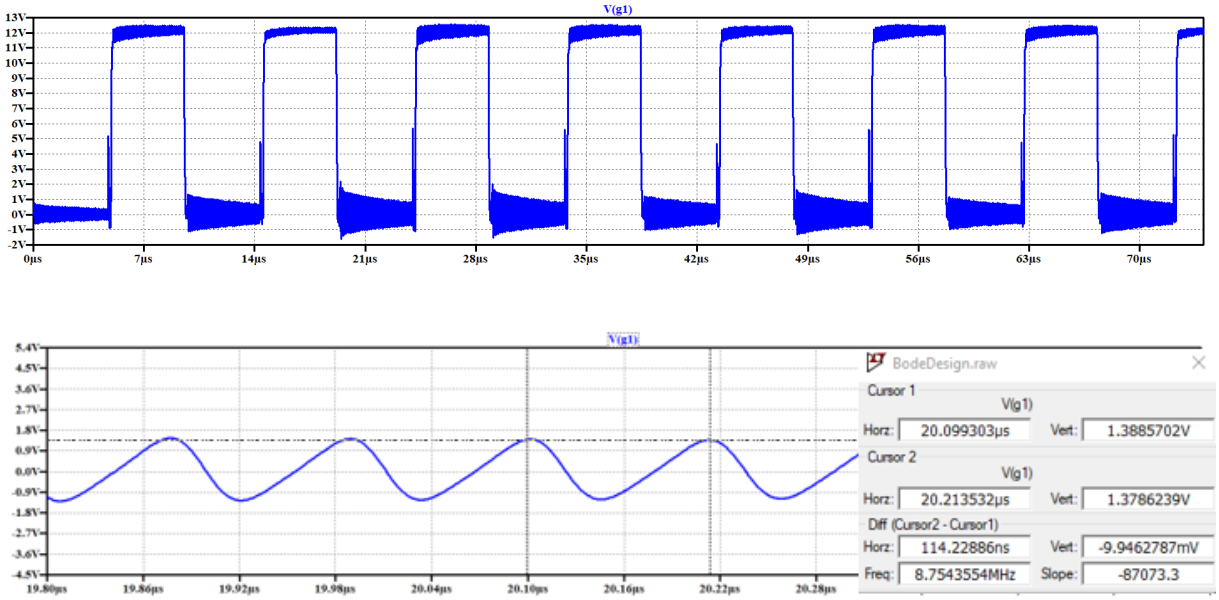


Figure 9. Gate signals and resonance frequency measurement for spikes

Resonant frequency is measured as 8.75 MHz Insert parallel capacitor to the MOSFET's drain to source legs so that that frequency drops half of it. The value of the inserted capacitor is 1100 pF that reduces spike frequency by a factor of two. That capacitance is the three times the value of the parasitic capacitance that created voltage spikes.

$$C_p = \frac{1100}{3}\, pF = 367\, pF\ (parasitic\ capacitance)$$

By using this value and the resonant frequency measured as above, the value of the parasitic inductance can be found as below.

$$L = \frac{1}{(2 * \pi * F_{res})^2 * C_p} = \frac{1}{(2 * \pi * 8.75 * 10^6)^2 * 367 * 10^{-12}} = 9 * 10^{-7} H$$

From these two found values, the characteristics impedance of the resonance can be found as below.

$$Z = \sqrt{\frac{L}{C}} = 49.52\ \Omega$$

From the calculated impedance and capacitor values, the RC snubber circuits component values can be chosen as;

$$R \cong Z \cong 49\ \Omega$$

$$4 * C_p < C < 10 * C_p$$

$$1468\, pF < C < 3670\, pF$$

While selecting the snubber capacitance value in found range, the gate signals waveforms observed as insufficient form when V_{in} is 400V. Therefore, in order to fix that problem snubber capacitor for MOSFET is selected as 500pF. It is decided with trial and error way around the found range. It is decided around 3 trial. Therefore, final selected values are:

$$C_{snubber}^{MOSFET} = 500\, pF$$

$$R_{snubber}^{MOSFET} = 45\ \Omega$$

After inserting snubber components the drain-to-source voltage of the MOSFET's is observed as in Figure 10.

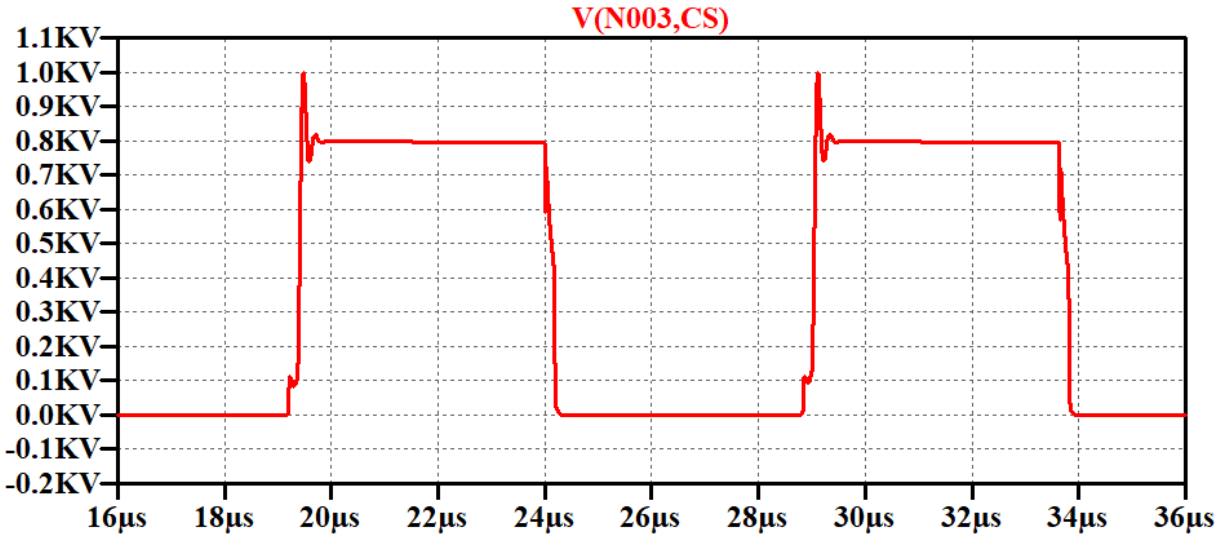


Figure 10. MOSFET drain-to-source voltage after snubber design

For diode, the same problem is existing. It is voltage waveform can be observed before inserting snubber circuits as in Figure 11.

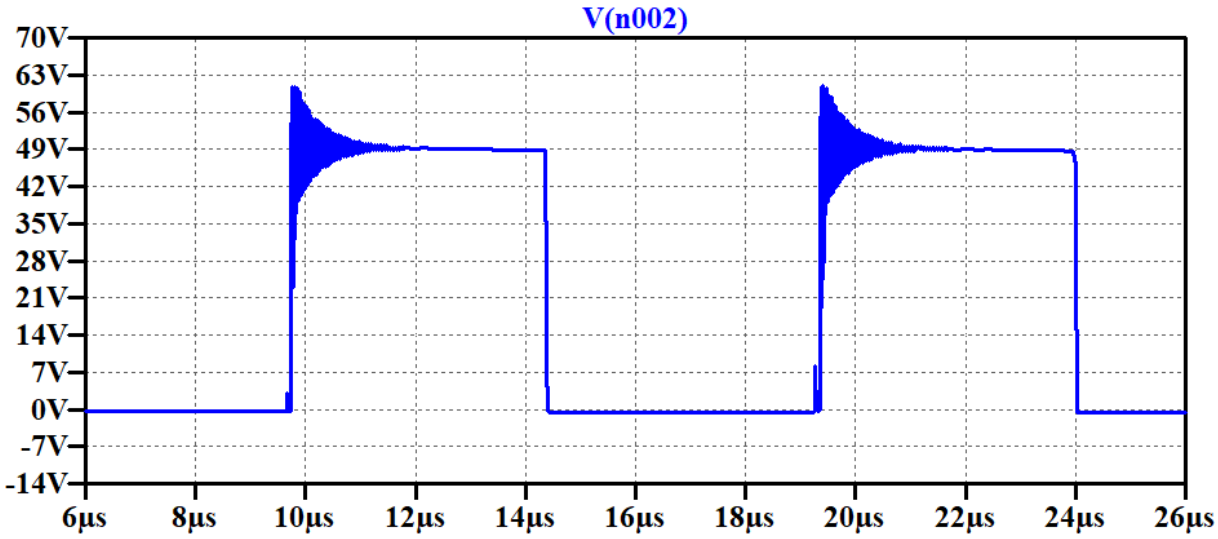


Figure 11. Diode voltage before snubber design

The same procedure applied to the MOSFET's can be applied for this component also. First resonance frequency of the spike is measured. It is found as 224 MHz Then, by connecting shunt capacitor the value of the parasitic capacitance is found in which the resonance frequency is reduced by a factor of two. Finally, by using the capacitance and resonance frequency values, inductance and reactance values can be found. At the end, almost same of the reactance is

selected as snubber resistance, and 200pF capacitance value is selected as the snubber capacitance.

$$f_{spike} = 224MHz$$

Capacitance value that reduces spike resonance frequency by half is 100pF. Then, the parasitic capacitance is:

$$C_p = \frac{C}{3} = \frac{100pF}{3} \cong 33pF$$

$$L = 1.53 * 10^{-8}\ H$$

$$Z = 21.53\ ohm$$

At this point, similar to the MOSFET design, resistor value is selected as found impedance value, and capacitor is selected as:

$$4 * C_p \leq C_{snubber} \leq 10 * C_p$$

$$132pF \leq C \leq 330pF$$

Selected exact values are:

$$C_{snubber}^{diode} = 200pF$$

$$R_{snubber}^{diode} = 22\Omega$$

After inserting snubber components, diode voltage waveform is observed as in Figure 12.

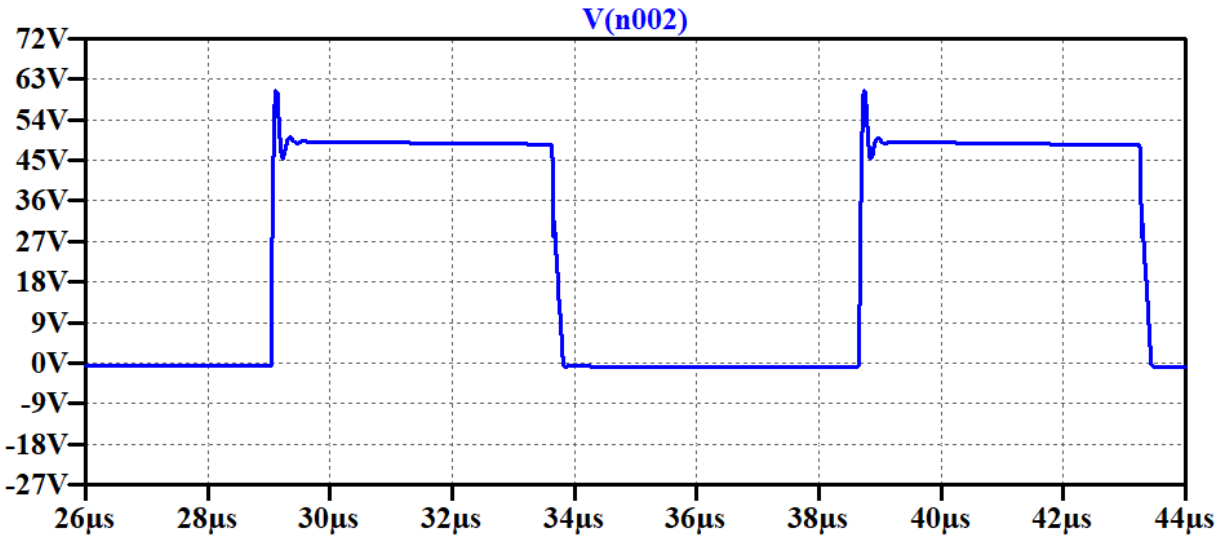


Figure 12. Diode voltage after snubber design

5. Magnetic Design

5.1. Transformer Magnetic Design

We set 16 as transformer turns ratio. Maximum input voltage is 400V, input frequency is 100kHz, maximum input current is 0.25A and maximum output current is 8.33A. A core should be selected due to stated specifications. We decided to use 2 EER ferrite cores. We checked several cores and calculated required and present window areas and chose PC47EER28-Z. We used AWG 25 for primary winding due to its maximum frequency rating and AWG 12 for secondary side in order to its current carrying capability. Primary and secondary winding turn numbers are calculated as:

$$n_1 > \frac{V_{i,max} * D_{max} * \frac{1}{f_s}}{B_{sat} * A_e}$$

$$n_1 > \frac{400 * 0.4364 * \frac{1}{100 * 10^{-3}}}{0.53 * 0.77 * 10^{-6}}$$

$$n_i > 42.76$$

$$n_1 = 48\ Turns$$

$$n_2 = \frac{48}{16}$$

$$n_2 = 3\ Turns$$

Required and present window areas are:

$$A_{req} = \frac{2 * 0.162 * 48 + 2 * 3.31 * 3}{0.6}$$

$$A_{req} = 59.02\ mm^2$$

$$A_w = \frac{(28.55 - 9.9)}{2} * 9.65 * 2$$

$$A_w = 179.9725\ mm^2$$

$$A_{req} < A_w$$

Magnetizing inductance of the transformer should be calculated. As long as we use 2 EER cores, we calculated the reluctance by combining several parts, and then we calculated the magnetizing inductance. Magnetizing inductance is calculated as:

$$\mu = \mu_0 * \mu_r$$

$$\mu = 2500 * 4 * \pi * 10^{-7}$$

$$\mu = 0.003142$$

$$R = \frac{\frac{14 + 9.65}{2} * 10^{-3} * 2}{\mu * \left(\frac{9.9}{2}\right)^2 * \pi} * \frac{\frac{\frac{21.2 + 3.4}{2} * 10^{-3} * 2}{\mu * 4.35 * 10^{-3} * 11.4 * 10^{-3}} + \frac{\frac{14 + 9.65}{2} * 10^{-3} * 2}{\mu * 3.4 * 10^{-3} * 11.4 * 10^{-3}}}{2}$$

$$R = 443821$$

$$L_m = \frac{N^2}{R}$$

$$L_m = \frac{48^2}{443821}$$

$$L_m = 5.19\ mH$$

The related skin depth analysis for this application can be conducted as:

$$Skin\ Depth(\delta) = \sqrt{\frac{\rho}{\pi * f_o * \mu_r * \mu_0}} = \sqrt{\frac{1.678 * 10^{-6}}{\pi * 100 * 10^3 * 0.999995 * 4 * \pi * 10^{-7}}}$$

$$= 206\mu m$$

In this design AWG25 and AWG12 cables are used. Their diameters are 0.455mm and 2.053mm respectively. Therefore, the skin depth exist which is 0.206mm will not create a problem for this design.

5.2. Inductor Magnetic Design

An output inductor is needed with capability of handling 8.33A and being larger than 160µH. We checked the cores from the smallest one in order to reduce costs and achieved our criterion at 0W41305TC. Calculations are as follows:

$$L > 160\ \mu H$$

$$n > \sqrt{\frac{160 * 10^{-6}}{4760 * 10^{-9}}}$$

$$n > 5.79$$

$$n = 6$$

$$L = 4760 * 10^{-9} * 6^2$$

$$L = 171.36\ \mu H$$

$$A_{req} = \frac{6 * 3.31}{0.6}$$

$$A_{req} = 33.1\ mm^2$$

$$A_w = 52.04\ mm^2$$

$$A_{req} < A_w$$

$$ESR_L = \frac{R_{per-km}}{10^6} * n * l_e$$

$$ESR_L = \frac{5.20864}{10^6} * 6 * (\pi * 5.08)$$

$$ESR_L = 0.499m\Omega$$

6. Component Selection

In the topology design there exist 3 main integrated circuits (IC), which are the main controller & gate driver, opto-coupler and opto-coupler driver.

For the main controller LTC3723-1 integrated circuit is selected. It can preserve both controller property and gate driver property. That will make design more systematic, cheaper and small size. This IC can drive two low side gate driver exists in the push pull topology according to the drive properties. At each switch cycle only one gate is driven and at some duration both gates are turned off, which is called dead time.

For the isolation, the controller IC doesn't preserve isolation. Therefore, an external isolation circuitry is required. For that purpose, an opto-coupler IC and its driver is used, which are MOC207 opto-isolator and LT1431 programmable reference. The compensation circuit is designed over the programmable reference pins. It preserves that duty for the general system performance. The necessary details about the compensation circuit design is explained in controller design section. In general, selected components can be seen in Table 1.

Table 1.Bill of Materials

Component	Serial Number	Price($) (unit price for purchase of 1000)
Controller	LTC3723EGN-1#PBF	6,48
C8	MA0805XR474K500	0,0095
C9	GMC04X5R683K16NT	0,0038
C7	MA0402XR331K500	0,00262
C10	GMC02X7R102M16NT	0,0019
C6	GMC04X7R151K16NT	0,0032
C1	337CKS025M	0,10051
C2	GMC04X7R222K50NT	0,0028
C3	GMC04CG120J25NT	0,0018
C4	GMC04X7R393K25NT	0,0048
C5	GMC04CG150J50NT	0,0019
C12	GMC21CG201J100NT	0,027
C13	GMC21CG201J100NT	0,027
C14	90150	0,1532

C16	90150	0,1532
C17	337CKS025M	0,10051
Transformer Core	PC47EER28L-Z	0,9576
D1	STPS30H100DJF-TR	0,4914
D2	STPS30H100DJF-TR	0,4914
Opto-isolator	MOC207M	0,25
Voltage Reference	LT1431CS8#TRPBF	2,58
C11	MC04X5R104K25NT	0,0045
Output Inductor Core	0W41305TC	2
M1	C3M0350120D	3,5
M2	C3M0350120D	3,5
Heatsink 1	513301B02500G	0,83992
Heatsink 2	513301B02500G	0,83992
Thermal Pad	Q3-0.005-00-114	0,05
Thermal Pad	Q3-0.005-00-114	0,05
Total		22,62848

We have selected necessary components for our converter application. Table 1 represents the used components and their prices. After choosing all the components, we calculated the losses and conducted detailed simulations which include all the non-idealities. Losses are calculated as follows.

Transformer:

$$P_{core} = 1.72\ W$$

Diodes (Calculated for One):

$$P_{loss} = I * V_f$$

$$P_{loss} = 8.333 * 0.56$$

$$P_{loss} = 4.67\ W$$

MOSFETs (Calculated for One):

$$P_{conduction} = I^2 * D * R_{DS}$$

$$P_{conduction} = 7^2 * 0.12 * 0.35$$

$$P_{conduction} = 2.058\ W$$

$$P_{switching} = \frac{1}{2} * V_{in} * I_{in} * (t_r + t_f) * f$$

$$P_{switching} = \frac{1}{2} * 400 * 7 * (16 + 17) * 10^{-9} * 100 * 10^{3}$$

$$P_{switching} = 4.62\ W$$

$$P_{gate} = V_{GS} * f * Q_g$$

$$P_{gate} = 20 * 100 * 10^{3} * 19 * 10^{-9}$$

$$P_{gate} = 0.038\ W$$

Output Inductor:

$$P_{loss} = I_o^2 * ESR$$

$$P_{loss} = 8.333^2 * 0.499 * 10^{-3}$$

$$P_{loss} = 0.035\ W$$

Integrated Circuits:

$$P_{total} = 0.42\ W$$

Thermal Circuit

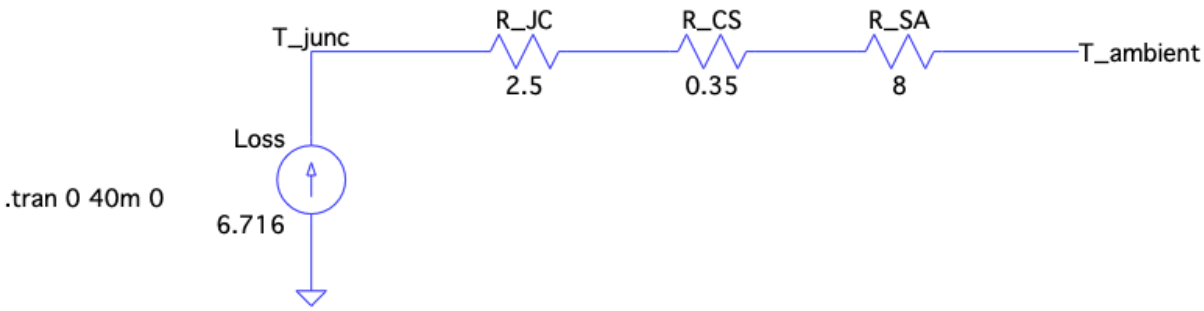


Figure 13. Thermal Circuit of MOSFET and Heatsink

Heatsink is needed for the MOSFETs. Maximum temperature for MOSFET operation is 150ºC according to datasheet and we want to have a smaller but close junction temperature in order to use a cheaper heatsink. We chose 513301B02500G model of Aavid, Thermal Division of Boyd Corporation which has 8ºC/W thermal resistance. Thermal circuit is shown in Figure 13. We are using natural cooling. Junction temperature is 98ºC with the heatsink.

$$T_{junction} = (8 + 0.35 + 2.5) * 6.716 + 25$$

$$T_{junction} = 97.87^{o}C$$

7. Detailed Simulation Results

This project design is completed over LTSpice simulation software. The designed circuit can be seen in sub-blocks as shown in Figure 14 to 16.

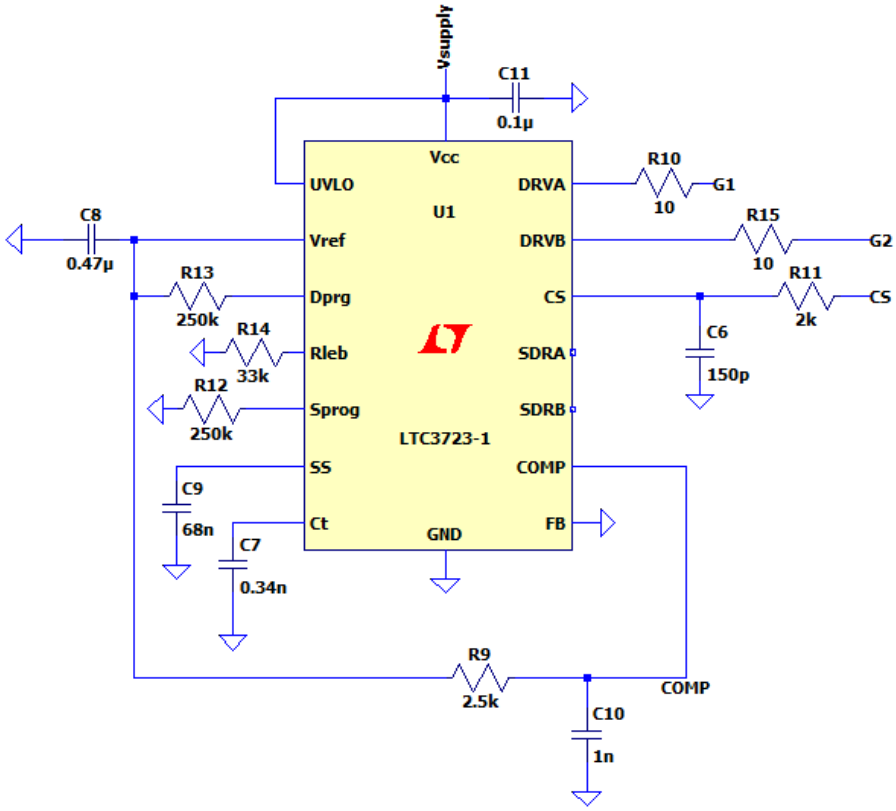


Figure 14. Controller IC setup circuit

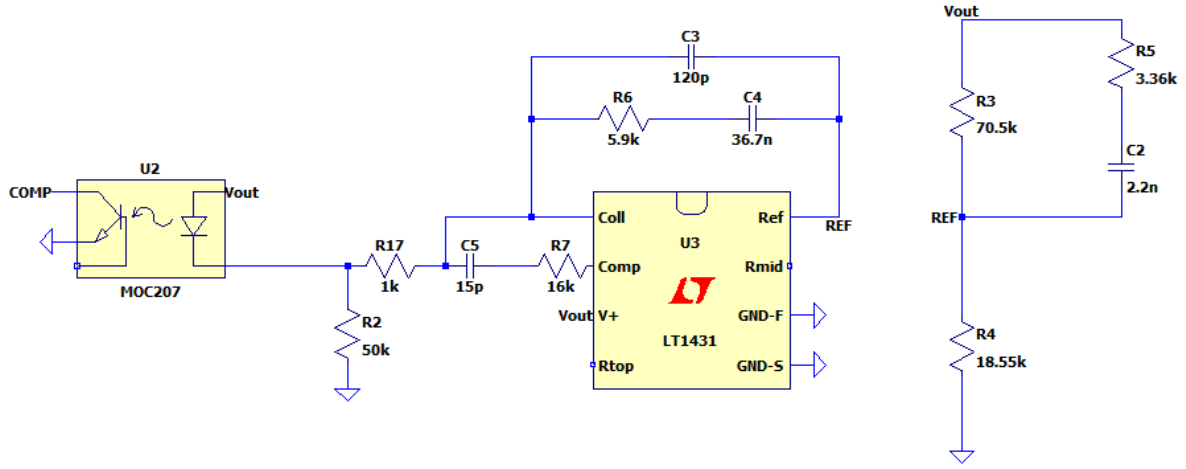


Figure 15. Opto-Coupler and it's driver circuit with reference voltage and compensator circuits

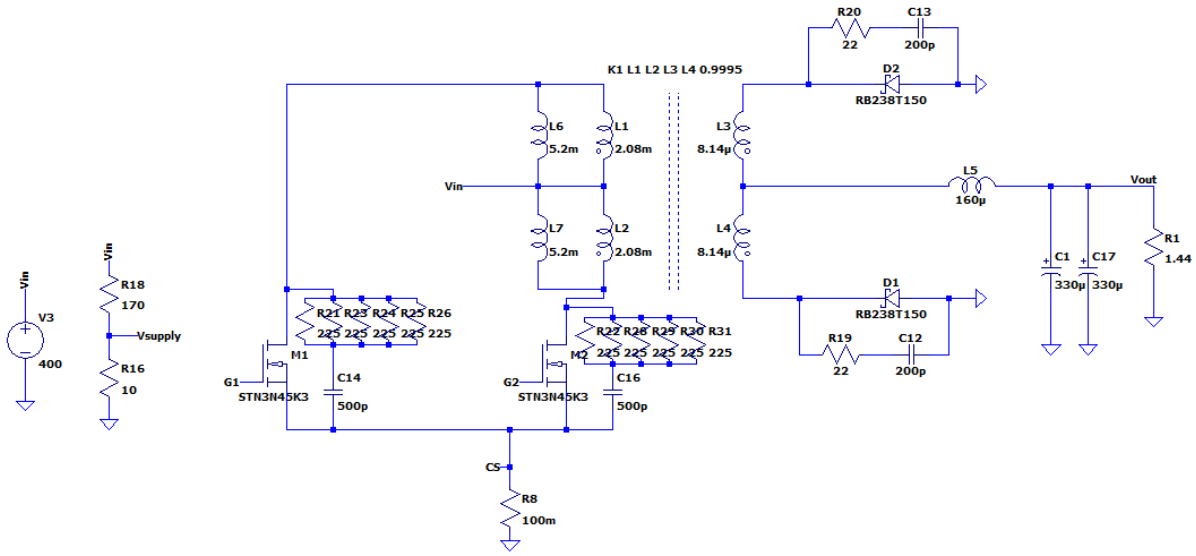


Figure 16. Main topology design and output filter part

As shown in Figures 14-16, system mainly consists of 3 sub-systems; topology design, controller design and opto-coupler design parts. With connecting these parts, overall system simulations are as followings.

Before starting any design, the output filter is simulated. With the entered below values the bode magnitude and phase diagrams are shown in Figure 18.

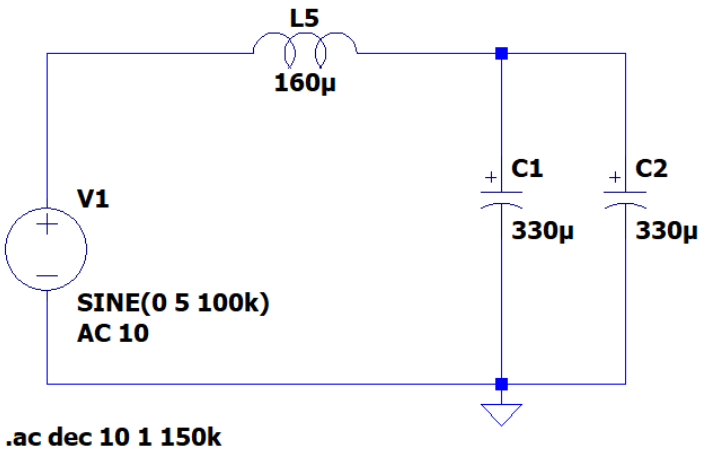


Figure 17. Output filter ac analysis circuit

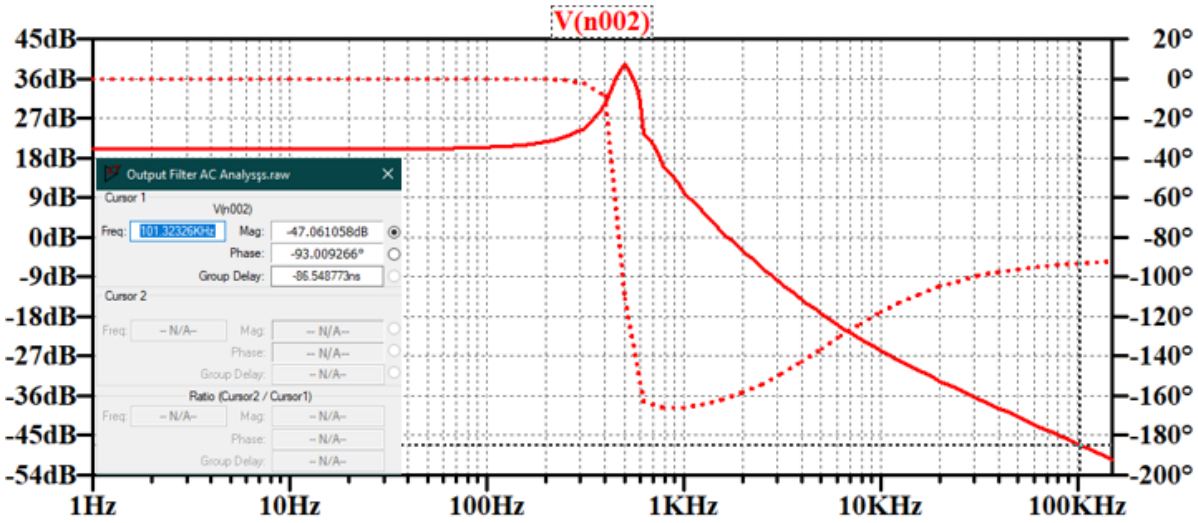


Figure 18. Magnitude and Phase Bode plots for output filter

As can be seen in Figure 18, the designed output filter has 87 degree phase margin at 100kHz operating frequency. Phase margin larger than 40 degree is preferred for stable closed loop systems.

When input voltage is 220V, the output voltage and power waveform is as shown in Figure 19.

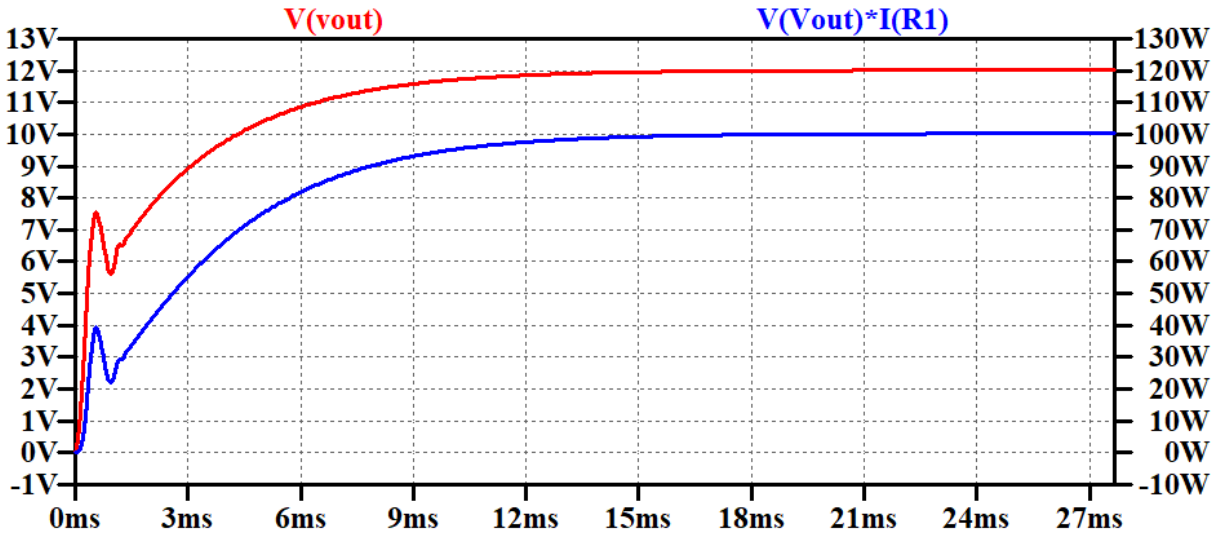


Figure 19. Output voltage and power waveforms when input voltage is 220V

Output voltage stabilizes at 12.02V. The output voltage ripple is measured as 0.297 mV as can be seen in Figure 20. It is 0.0025% of the output voltage.

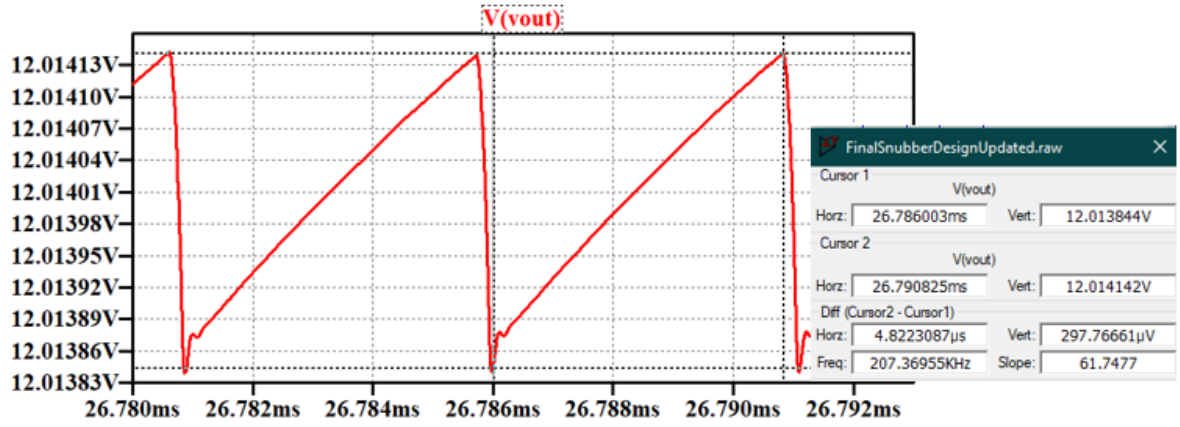


Figure 20. Output voltage ripple when input voltage is 220V

System's stability performance react to the load changes is critical for the design. The designed system's stability response to the load change from no load to full load can be seen in Figure 21.

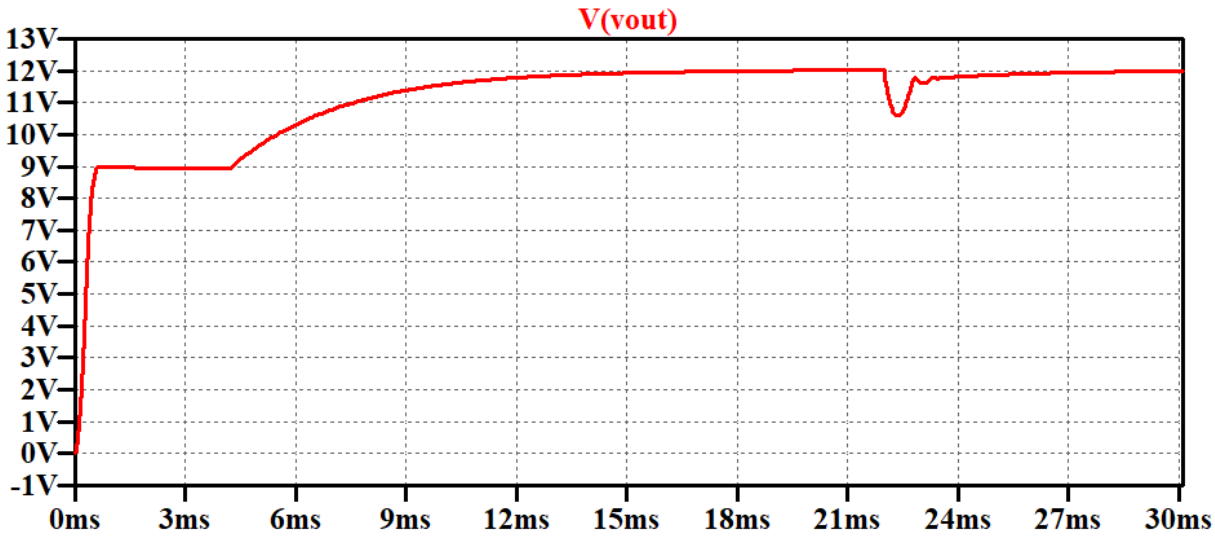


Figure 21. No load to full load stability performance when 220V input voltage exists

When input voltage is 400V, the output voltage and power waveform is as shown in Figure 22. Note that, the output voltage stabilizes at 12.0014V.

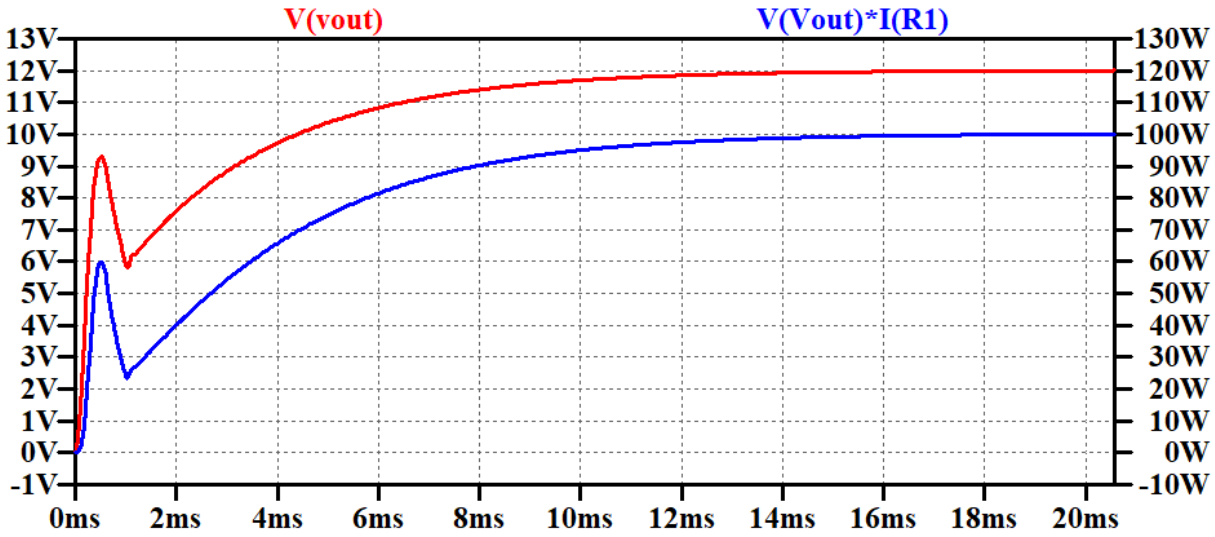


Figure 22. Output voltage and power waveforms when input voltage is 400V

The output voltage ripple is measured as 5.14mV as can be seen in Figure 23. That is 0.43% of the output voltage.

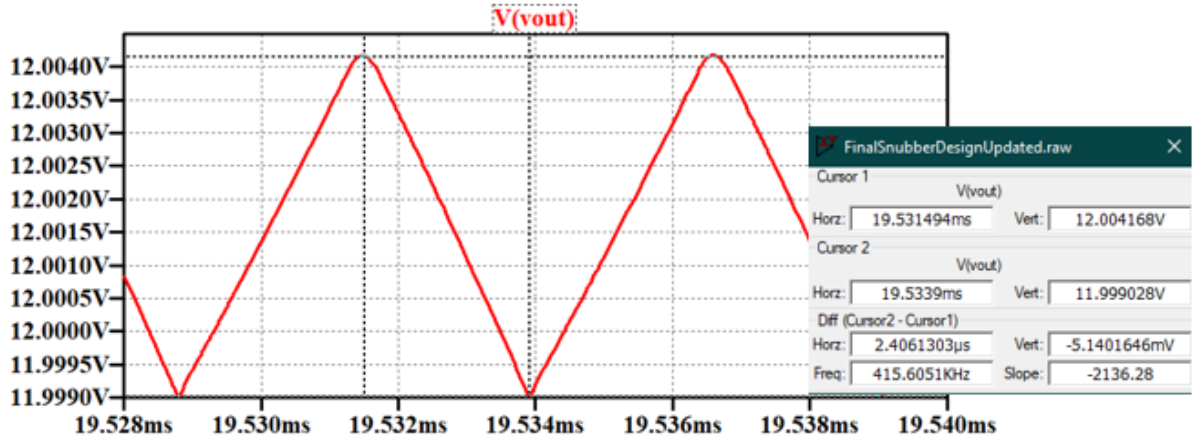


Figure 23. Output voltage ripple when input voltage is 400V

From no load to full load the output voltage waveform can be seen in Figure 24.

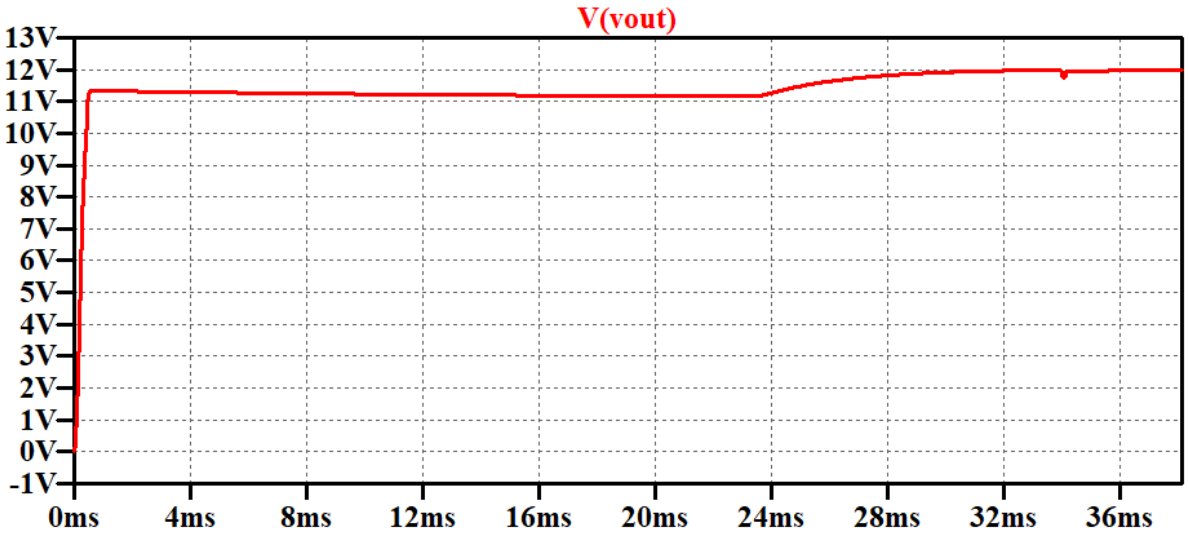


Figure 24. No load to full load stability performance when input voltage is 400V

The line regulation when input voltage changes from 220 V to 400 V can be calculated from the above results as:

$$Line_{reg} = \left(\frac{V_{out}^{220V} - V_{out}^{400V}}{V_{out}^{220V}}\right) * 100 = \frac{12.02 - 12.0014}{12.02} * 100 = 0.155\%$$

Conclusion

The aim of this project is to obtain 100W 12V DC output from a variable DC voltage source. In order to obtain required DC-DC converter first a suitable topology is selected. According to the evaluations described above, push pull topology is preferred. After selecting topology, the power transformer analysis is conducted. While proceeding with the calculations a suitable inductance, turns ratio etc. value ranges are determined, and then by using a PExprt power transformer design application a primary and secondary inductance values are found by entering the found transformer values.

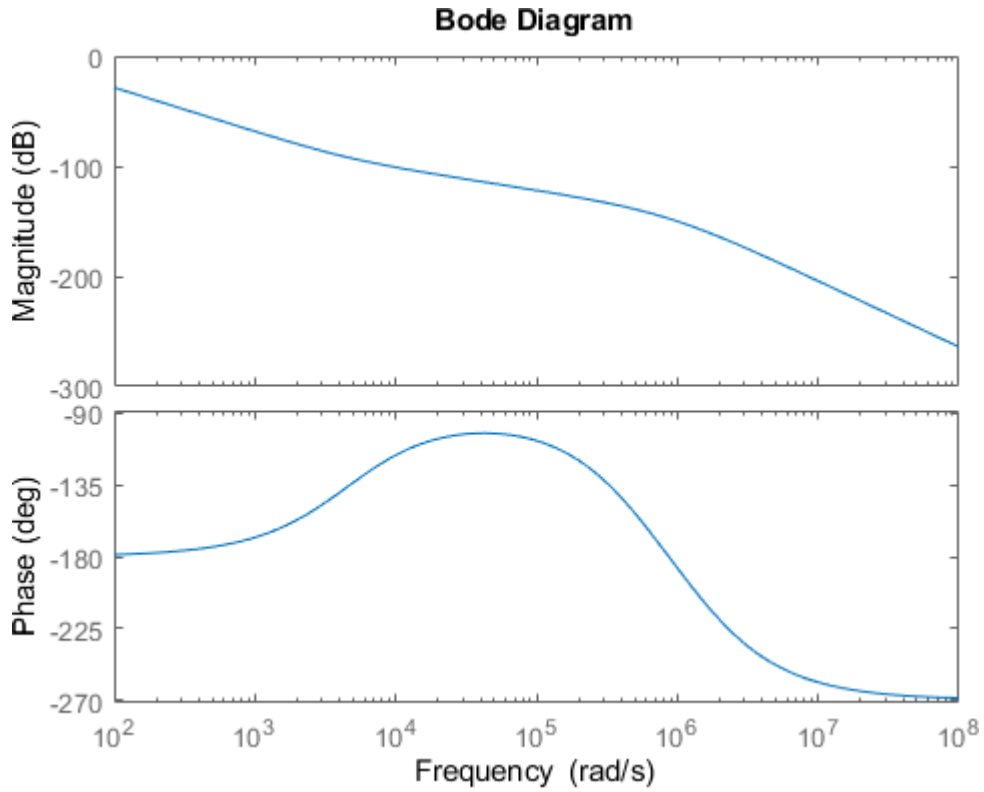
After finding transformer values, the system is performed in open loop. It gives 12V at 100W power in suitable pulse duty cycles. Next, selected integrated circuits are entered into the simulation, and system is run over closed loop design. At this stage, a compensator circuit is designed. For the system specifications, Type 3 compensator circuit is sufficient for system stability.

As a final step, filtering for the EMI effects is completed by designing snubber circuits. The power ratings of the snubber components are decreased by suitable number paralleling application. After completing the simulation step, a component selection is done, and a BOM is prepared.

As a result, in this project an isolated variable input constant output DC-DC switched mode power supply design is conducted with very small ripple ratings and strong stability performances. Overall cost for this project almost 22$ levels.

Appendix A – Compensation Circuit Design

```
%Doge Power Compensator Design File

L = 80e-6;                              %Output Inductance
C = 330e-6;                             %Output Capacitance
ESR = 56e-3;                            %Capacitor ESR value
F_lc = 1/(2*pi*sqrt(L*C));              %Filter frequency
F_esr = 1/(2*pi*ESR*C);                 %ESR frequency
Fsw = 100e3;                            %Switching frequency
Fzero = Fsw/10;                         %Center frequency

Vref = 2.5;                             %Driver reference voltage
Vout = 12;                              %Output voltage
Vosc = 2.35;                            %Peak-to-Peak
 oscillator amplitude voltage
Vin = 300;                              %Minimum input voltage

%Type 3 Compensator pole and zero frequencies
Fz2 = F_lc;                             %Second zero frequency
Fz1 = 0.75*F_lc;                        %First zero frequency
Fp2 = F_esr*10;                        %Second pole frequency
%Fp3 = Fsw/2;                           %Third pole frequency
Fp3 = Fsw*2.25;                         %Third pole frequency


%Type 3 Compansator Parameters
Cf3 = 2.2e-9;                           %Cf3 is selected then rest
 is calculated from it
Rf3 = 1/(2*pi*Cf3*Fp2);                 %Voltage division
compensator Rf1 = 1/(2*pi*Cf3*Fz2)-Rf3;   %Voltage division top
resistor Rf2 = (Rf1*Vref)/(Vout-Vref);%Voltage division bottom
 resistor
Rc1 =
(2*pi*Fzero*L*C*Vosc)/(Vin*Cf3); Cc1
= 1/(2*pi*Rc1*Fz1);
Cc2 = 1/(2*pi*Rc1*Fp3);


%Type 3 Compensator Transfer
Function s = tf('s');
H = tf([(Rc1*Cc1+Rc1*Cc1*Cf3*(Rf1+Rf3)) (1+Cf3*(Rf1+Rf3))],
[(Cc2*Rc1*Cf3*Rf3*Cc1*Rf1) (Cc1*Rf1*Rc1*Cc2+Cc1*Rf1*Rf3*Cf3)
(Cc1*Rf1)
 0 0]);
bode(H)
   ;
```



Published with MATLAB® R2020b

Appendix B – Circuit Parameter Decision Table

Inputs	
Vin_max	400
Vin_min	220
D center	0,3
L	0,000047
C	0,000047
fs	100000
L	0,0001

If you use these fs will be your output

If you use these L*C and C will be your output

Outputs	
N1/N2	16
D_max	0,436363636
D_min	0,24
L*C*fs*fs	0,099431818
fs	6709,108765
L*C	9,94318E-12
C	9,94318E-08