MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

EE 463 - Static Power Conversion II - Term Project

Final Report

Doge Power Inc.

12V - 100W Isolated Push-Pull DC-DC Converter

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Introduction

In electrical drivers, different power levels are required for different applications. Most of the small engines like window engine, wiper engine, air conditioner etc. requires 12V supply. The main power supply, whereas gives 400V input voltage for these applications. Therefore, designing a system that converts high input voltage to a low-level output voltage may need in here. Moreover, in order not to disturb the working performance of the other circuits from the faults may occur in somewhere, isolated systems are crucial. For that purpose, isolated power supplies are designed.

In this project, an isolated switched mode power supply design is conducted. This converter will be able to convert 220V to 400V input voltages to 12V 100W output voltage in a reasonable stability performance. The main duty in this job is to satisfy control loop in a way that system's both transient and steady state performances are quite good levels.

Throughout this report, first a topology selection is introduced. Then the subsystems of the project steps like controller design, snubber design, thermal design, magnetic design and PCB design will be introduced one by one. At the end, by giving the simulation results the performance of the designed system can be evaluated.

1. Topology Selection

In this project 100W isolated dc-dc converter design is required. In the below, the project specifications are listed as follows:

- Minimum input voltage : 220V
- Maximum input voltage : 400V
- Output voltage : 12V
- Output Power : 100W
- Output voltage peak-peak ripple : 4%
- Line regulation : 3%
- Load regulation : 3%

For the design of such a system, first a suitable topology selection is required. Since the system should be an isolated system, the following topology alternatives can be chosen as follows:

- Flyback Converter
- Forward Converter
- Push – Push Converter
- Half Bridge
- Full Bridge

Flyback Converter:

Advantages of this converter are:

- No output inductance requirement
- Ability to supply multiple output voltages
- Less component requirement compared to the other converters

Disadvantages of this converter are:

- Closed loop bandwidth in CCM operation is narrow
- Large output capacitor requirement

Since our input margin is too large, this converter may not give good results in our conditions. Also, it is power ratings are top limit for our specifications. That may result in higher duty cycle requirement. For those reasons, this converter didn't select.

Forward Converter:

Advantages of this converter are:

- Drive circuit is simpler compared to other topologies
- One switching transistor is required

Disadvantages of this converter are:

- Transformer utilization is not sufficient compared to the push pull and bridge topologies. D_{max} is limited by 50%.
- Blocking voltage of the transistors are 2 times of the input voltage. That increases ratings of the component.
- It may go into DCM operation

In our design purposes, increasing transformer utilization is critical. Since this topology uses transformer insufficiently, it is not preferred in our design.

Half Bridge:

This topology presents best transformer utilization. It provides low cost and small space. However, when controller research is conducted, it is realized that the analog controllers for this topology is not applicable. Most of the controller stabilizes output voltage with respect to reference value. However, the input capacitance middle point is discarded almost all of the controllers. Therefore, due to the insufficient integrated circuits for this topology, it is not selected.

Full Bridge:

This topology generally preferred in larger than 500W applications. It has 4 transistors in the primary side of the topology. Since the input voltage level of this project is around 200-400V margin, selecting 4 transistors at those ratings will brings a lot of project costs. Therefore, for that reason this topology is discarded.

Push – Pull Converter:

This topology uses 2 input switch and 2 output diodes. Moreover, additional LC filter to the output is required. Since its transformer utilization is good, the required transformer core size is relatively small compared to others, and transformer ratings are smaller compared to the Forward. Also, its filter requirement is small compared to the Flyback and Forward topologies. It is one the biggest disadvantage is central top transformer structure. However, while considering the other advantages this converter has more useful for this project. Therefore, this one is selected as a SPMS design application.

2. Analytical Calculations and Simulations

Since the topology is Push-Pull, duty cycle should be between 0 and 0.5 because D is used twice during a period. We would like to have charging and discharging durations to be close to each other in order to stay away from discontinuous conduction mode. We set up an xlsx file in order to observe the change in circuit parameters due to frequency, desired duty cycle etc. We set a duty cycle for the input voltage which is the mean of maximum and minimum and calculated D_{max} and D_{min} accordingly.

$$\frac{0.6}{2} = 0.3$$

$$\frac{220 + 400}{2} = 310$$

$$V_o = V_{in} * 2 * \frac{N_2}{N_1} * D$$

$$12 = 310 * 2 * \frac{N_2}{N_1} * 0.3$$

$$\frac{N_2}{N_1} = \frac{1}{16}$$

Duty cycle will be the controlled parameter in order to keep the output voltage constant with changing input voltage. We calculated the interval of duty cycle.

$$V_o = V_{in} * 2 * \frac{N_2}{N_1} * D_{min}$$

$$12 = 400 * 2 * \frac{1}{16} * D_{min}$$

$$D_{min} = 0.24$$

$$12 = 400 * 2 * \frac{1}{16} * D_{max}$$

$$D_{max} = 0.4364$$

Since the output side of the push-pull topology is identical to buck converter, output voltage ripple has the same characteristics with half of the period.

$$\frac{\Delta V_o}{V_o} = \frac{(1 - 2 * D)(\frac{1}{f_s})^2}{8 * L * C}$$

$$D = 0.4364\ (Worst\ Case)$$

$$0.04 > \frac{(1 - 2 * 0.4364)(\frac{1}{2 * f_s})^2}{8 * L * C}$$

$$L * C * {f_s}^2 > 0.09943$$

As we increase the frequency, we can use smaller components for L and C and reduce the cost. We set the switching frequency at 100kHz.

$$L * C > \frac{0.09943}{(10 * 10^3)^2}$$

$$L * C > 9.943 * 10^{-12}$$

We set L value as 68µH, so C value is calculated as:

$$C > \frac{9.943 * 10^{-12}}{160 * 10^{-6}}$$

$$C > 146.22\ nF$$

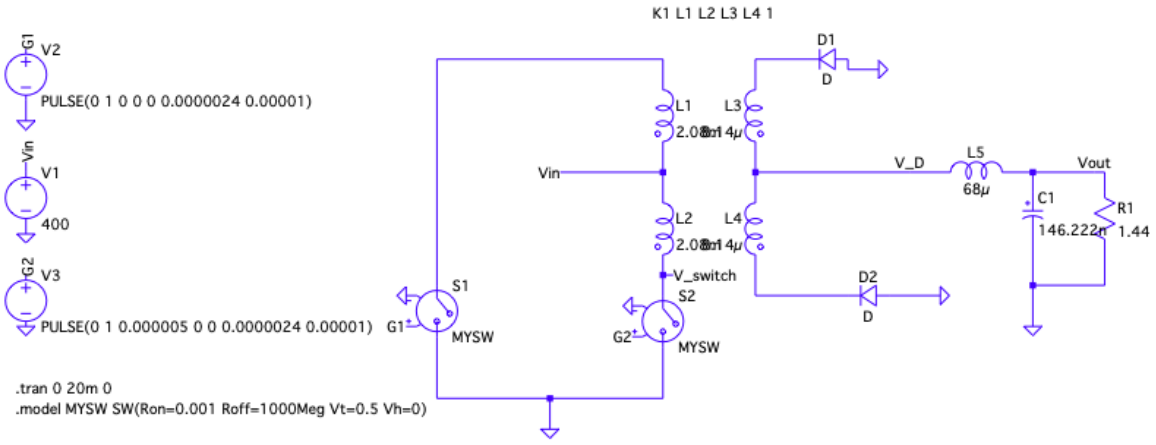


Figure 1. Circuit Schematic of Push-Pull Circuit without any Control

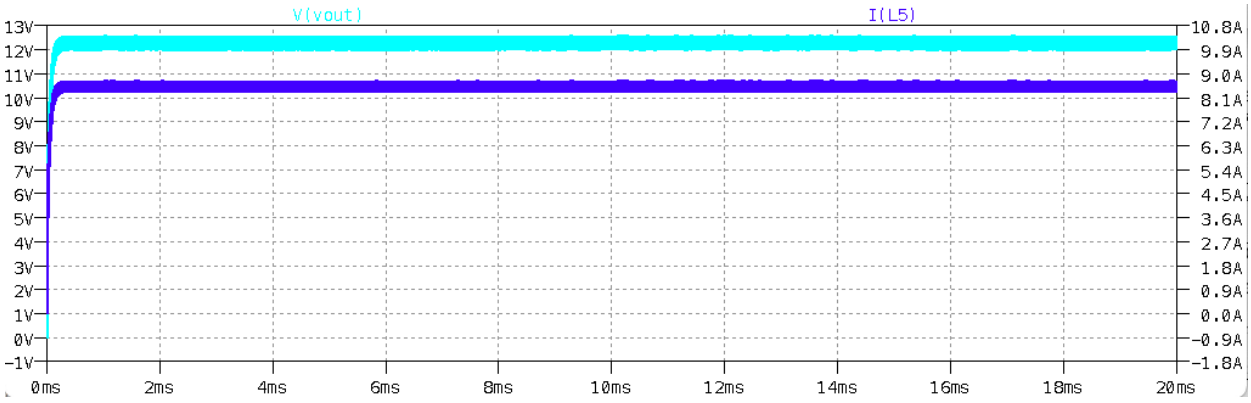


Figure 2. Output Voltage and Inductor Current Waveforms of Converter

As seen in Figure **2,** output voltage is in the limits of 4% ripple criteria. Maximum voltage rating of output capacitor should be higher than 12.48V. Maximum current flowing through output inductor should be higher than 8.333A, which can be also calculated as:

$$I_{L(out)-max} = \frac{100}{12}$$

$$I_{L(out)-max} = 8.333\ A$$

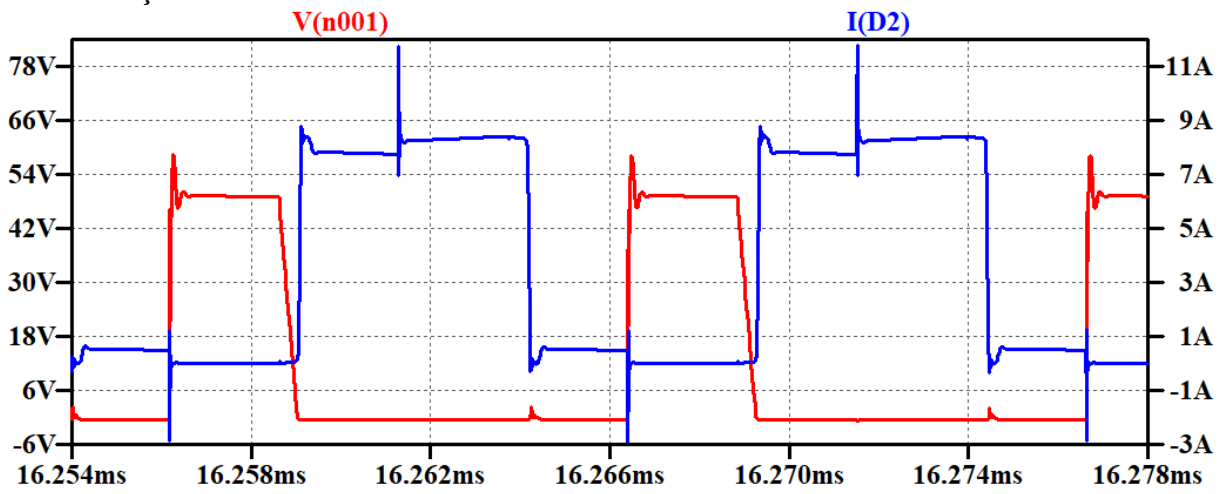


Figure 3. Voltage and Current Waveforms of DC Side Diodes at 400V Input Voltages

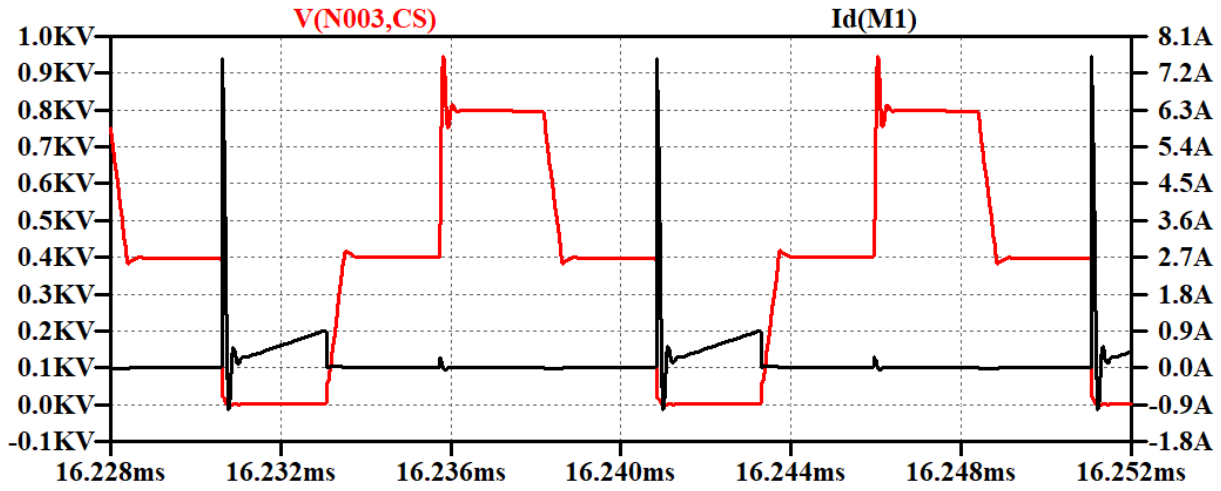


Figure 4. Voltage and Current Waveforms of Switches

As seen in Figure 3, diodes should be capable of handling 9A current and 50V reverse voltage. Switches should be able to block at least 800V and conduct more than 800mA according to Figure 4.

3. Controller Design

In this project, stable output is desired whereas input is changing from 220V to 400V. That yields a controller requirement. For this purpose, LT3723-1 current mode controller is selected as it will be expressed in component selection section. This controller can act both as controller and as gate driver for the MOSFETs. Therefore, it decreases the component requirement to a single component. However, the biggest drawback of this controller is that it does not satisfy the isolation criteria of the project. Therefore, in addition to this integrated circuit (IC) an opto coupler and

opto coupler driver IC's is selected, which completes the isolation problem of this design. For opto-coupler MOC207M is selected, for its driver LT1431 IC is selected.

In designing controller, first the main IC should be programmed such that it suits in this application. For step by step improvement, the pin configuration and package information of this IC can be seen in Figure X.

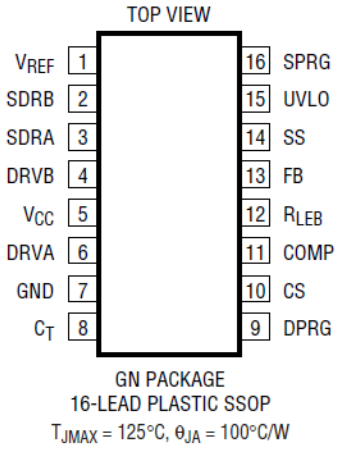


Figure 5. Pin configuration and packet information of LTC3723-1 IC

This project is designed with 100 kHz operating frequency. Selecting operating frequency high decreases, the size of the magnetic components and output filter components. However, while frequency increases the switching losses also increases. Therefore, that will yield less efficiency. Finding optimum point is crucial. For that purpose, 100kHz operating frequency is selected. In order to program IC to 100 kHz frequency, its C_T pin is used. The following formula programs the operating frequency of the IC by connecting capacitor from that pin to ground.

$$C_T = \frac{1}{2 * 14.8 * 10^3 * F_{OSC}}$$

$$C_T = 0.34\ nF$$

After inserting this capacitor, the frequency of the gate signals is measured as in Figure X.

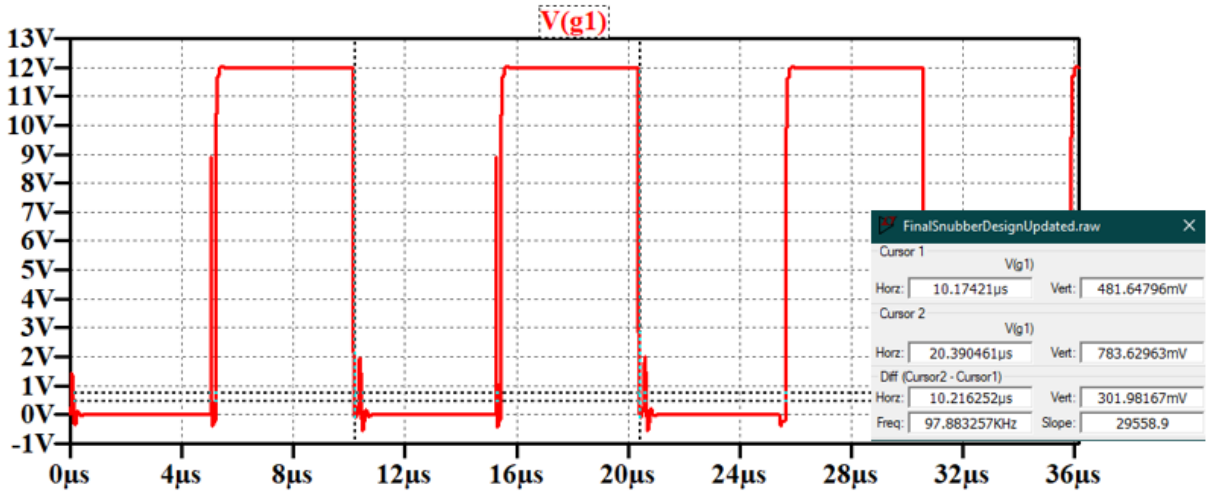


Figure 6. Frequency information of gate signals

Selecting capacitor value in large significant figures arranges the frequency exactly to the 100kHz. However, in practice it is not practical. Therefore, this amount is decided enough for this application.

In push pull topology, gates of the both MOSFETs are off during some time. That time is known as dead time. Dead time of this IC is programmed with connecting resistances to the SPRG and DPRG pins. The values are determined from the data sheet dead time plot. It is selected as higher as so that it suits in our application. They are selected as 250kΩ. That is enough to stabilize output in the 12V reference level.

Controllers provides controlled output by some external circuits constructed to the control pins. These circuits are known as ‘Compensator Circuits’. Since the control loop in this project is completed by using the opto-coupler circuits, the compensation circuits are constructed in the opto-coupler driver circuit pins. Also, feedback from the output is taken by the opto-coupler driver. Therefore, the feedback pin of the controller is connected to ground. It continuously provides output while compensation signal is provided. In the next subsection the compensator circuit design is explained in detail.

3.1. Compensator Circuit Design

The input voltage range in this application is quite large. Therefore, compensator circuit performance is crucial in order to stabilize output to 12V. There are 3 main compensator types, which are:

- Type I compensator
- Type II compensator
- Type III compensator

Type I is used for basic application. In SMPS designs, type II compensator is preferred generally. However, in large range application that may not be sufficient. In that cases, Type 3 compensator can be used. Since this project conducts in wide range input voltages, it is required to use type 3 compensator. In type 3 design, the following reference circuit configuration is referred.

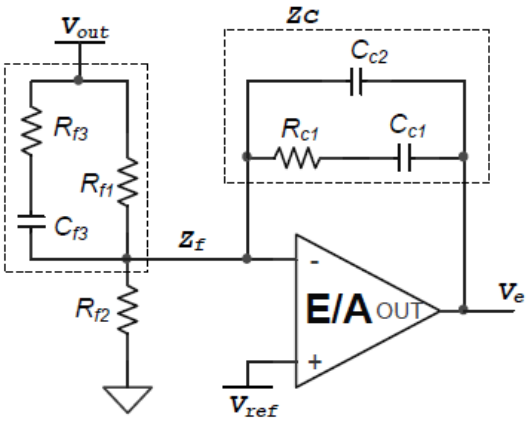


Figure 7. Type 3 compensator circuit configuration

In the design of these components, first pole zero locations are determined. For that purpose, the LC frequency of the output filter is calculated as:

$$F_{LC} = \frac{1}{2 * \pi * \sqrt{L * C}}$$

And, ESR frequency of the capacitor is calculated as:

$$F_{ESR} = \frac{1}{2 * \pi * R_{ESR} * C}$$

The pole-zero locations are selected by these frequencies accordingly as follows:

$$F_{Z2} = F_{LC}$$

$$F_{Z1} = 0.75 * F_{Z2} = 0.75 * F_{LC}$$

$$F_{P2} = F_{ESR}$$

$$F_{P3} = \frac{F_{sw}}{2}$$

$$F_0 \leq \frac{F_{sw}}{8}$$

Finally, these is a single pole at the origin, which is F_{p1}

The circuit components based on these formulas are calculated from the following formulas based on taking C_{f3} some suitable value, which can be 2.2nF as a good start. If not worked, it can be updated.

$$R_{f3} = \frac{1}{2 * \pi * C_{f3} * F_{p2}}$$

$$R_{f1} = \frac{1}{2 * \pi * C_{f3} * F_{z2}} - R_{f3}$$

$$R_{c1} = \frac{2 * \pi * F_0 * L_{out} * C_{out} * V_{osc}}{V_{in} * C_{f3}}$$

In here, the V_{osc} voltage is the oscillation voltage of the IC. It is 2.35V from datasheet.

$$C_{c1} = \frac{1}{2 * \pi * R_{c1} * F_{z1}}$$

$$C_{c2} = \frac{1}{2 * \pi * R_{c1} * F_{p3}}$$

These are the general formulas used in the design. However, finding values from these formulas generally not sufficient at first. It required fine tuning algorithms. Calculating again and again from at first step is a messy work. Therefore, as can be seen in Appendix A, a MATLAB m file is prepared.

When the first values are taken, they are simulated. They will stabilize at 12V output in both 220V and 400V input values. However, the final waveform of output voltage at steady state is not sufficient. It is oscillating very high. In order to solve this problem, the transfer function of the compensator circuit is extracted and written into the m file. Then, by plotting bode diagram of that transfer function, the effect of each component indicated above is observed one by one. It is crucial to obtain phase margin larger than 40 degrees. At first, it is around 40 degrees, and as said it is not good for output voltage stabilization. While observing each element effect to the bode plot, it is realized that increasing third pole frequency increases the phase margin of the system, and improves stability also. At final step third pole frequency is selected as:

$$F_{p3} = F_{sw} * 2.25$$

It results in -108 degrees phase at 100kHz frequency. It is phase margin is found as:

$$Phase_{margin} = Phase + 180$$

$$Phase_{margin} = -108 + 180 = 82\ degrees$$

The resulted phase margin is excellent for design. Its results are also very good both in terms of transient and in terms of steady state.

4. Snubber Circuit Design

In most of the industrial applications, designing circuits with low electromagnetic interference (EMI) is required. The reason for that is designing parts of a project in separately is not affected from this phenomenon because it has an effect to the neighboring components. They usually distort their operating frequencies and also operating performances. Higher EMI problems at some point also distort the operation performance of the product also. Therefore, suppressing those EMI spikes is critical. For that purpose, snubber circuits are preferred. There are 3 types of mostly used snubber circuit configurations. These can be order as:

- C snubber
- RC snubber
- R//D -C snubber

Inserting only C snubbers, decreases system operating speed. When system slows down, then it increases EMI radiation, which is also called ringings. To eliminate ringing R is inserted. In RC snubber that ringing also canceled. Therefore, it yields best result. In another application, resistor is parallel with diode and connected to capacitor in series. The purpose for this application decreasing resistive losses exists in the system. However, since this application works under 100kHz switching frequency, diode's switching losses are quite high. Also, the cost of the diodes will increase project costs. For that reasons, R-C snubber circuits are used.

Before starting the snubber circuit design, the drain-to-source voltage of MOSFET is observed as in Figure 8.

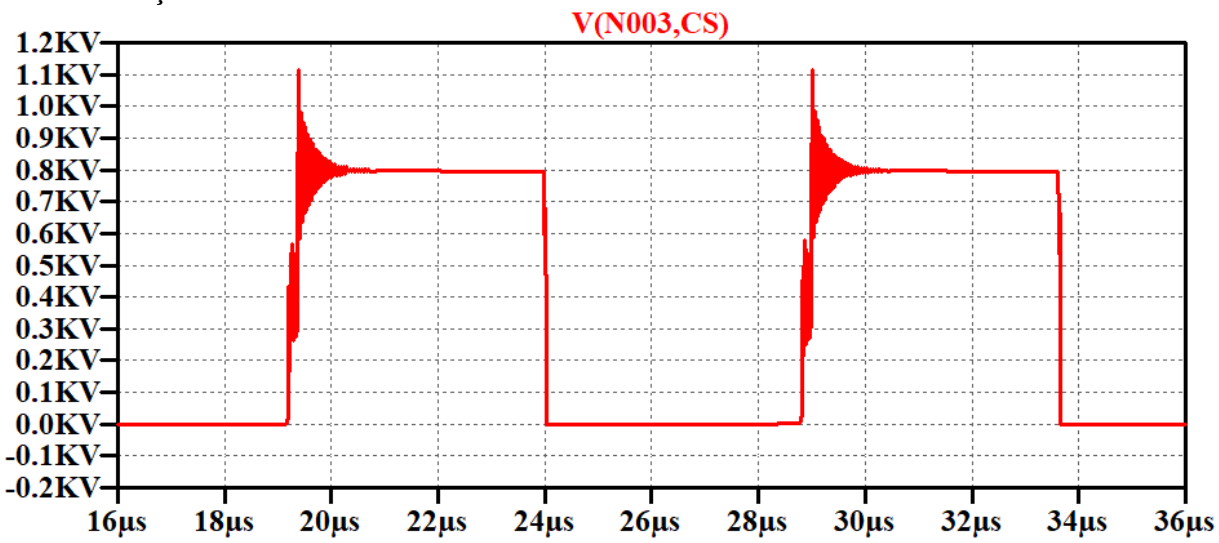


Figure 8. MOSFET drain-to-source voltage before snubber circuit

The effect of EMI radiations can be observed easily in this figure. Therefore, eliminating this is critical for SMPS design.

In the design of the snubber circuits, there is a guideline for the push-pull topology. Accordingly, first the resonance frequency of the spikes is measured as shown in Figure X.

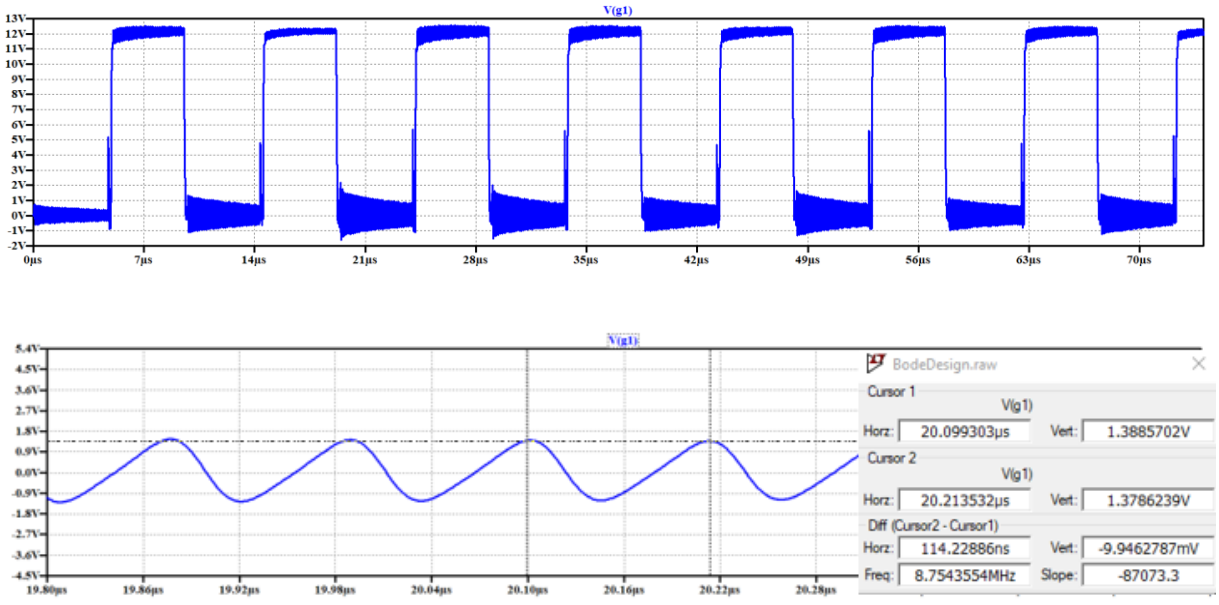


Figure 9. Gate signals and resonance frequency measurement for spikes

Resonant frequency is measured as 8.75 MHz Insert parallel capacitor to the MOSFET's drain to source legs so that that frequency drops half of it. The value of the inserted capacitor is 1100 pF that reduces spike frequency by a factor of two. That capacitance is the three times the value of the parasitic capacitance that created voltage spikes.

$$C_p = \frac{1100}{3}\ pF = 367\ pF\ (parasitic\ capacitance)$$

By using this value and the resonant frequency measured as above, the value of the parasitic inductance can be found as below.

$$L = \frac{1}{(2 * \pi * F_{res})^2 * C_p} = \frac{1}{(2 * \pi * 8.75 * 10^6)^2 * 367 * 10^{-12}} = 9 * 10^{-7} H$$

From these two found values, the characteristics impedance of the resonance can be found as below.

$$Z = \sqrt{\frac{L}{C}} = 49.52\ \Omega$$

From the calculated impedance and capacitor values, the RC snubber circuits component values can be chosen as;

$$R \cong Z \cong 49\ \Omega$$

$$4 * C_p < C < 10 * C_p$$

$$1468\ pF < C < 3670\ pF$$

While selecting the snubber capacitance value in found range, the gate signals waveforms observed as insufficient form when V_{in} is 400V. Therefore, in order to fix that problem snubber capacitor for MOSFET is selected as 500pF. It is decided with trial and error way around the found range. It is decided around 3 trial. Therefore, final selected values are:

$$C_{snubber}^{MOSFET} = 500\ pF$$

$$R_{snubber}^{MOSFET} = 45\ \Omega$$

After inserting snubber components the drain-to-source voltages of the MOSFETs' are observed as in Figure 10.

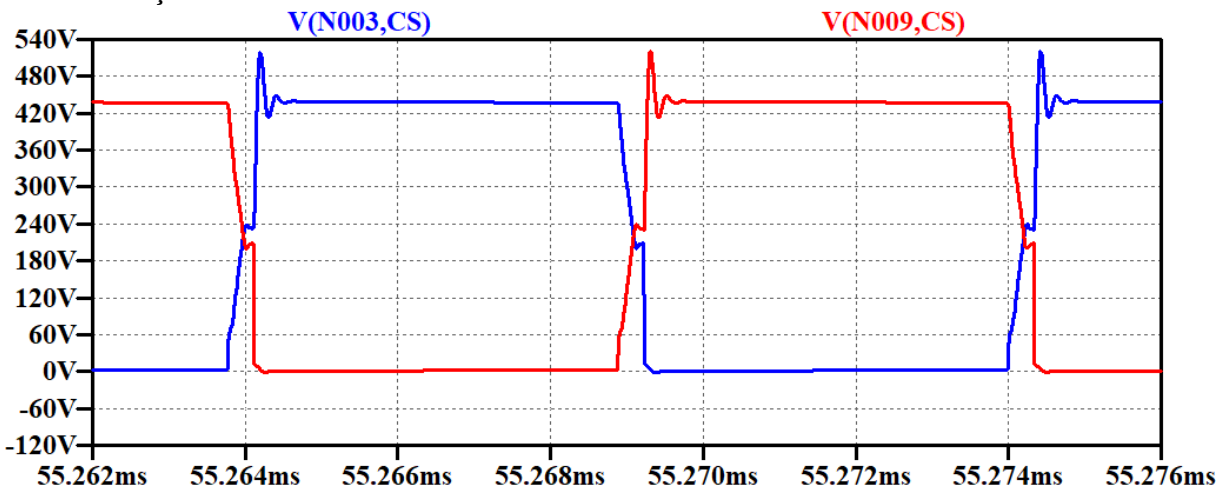


Figure 10. MOSFET drain-to-source voltage after snubber design

For diode, the same problem is existing. It is voltage waveform can be observed before inserting snubber circuits as in Figure 11.

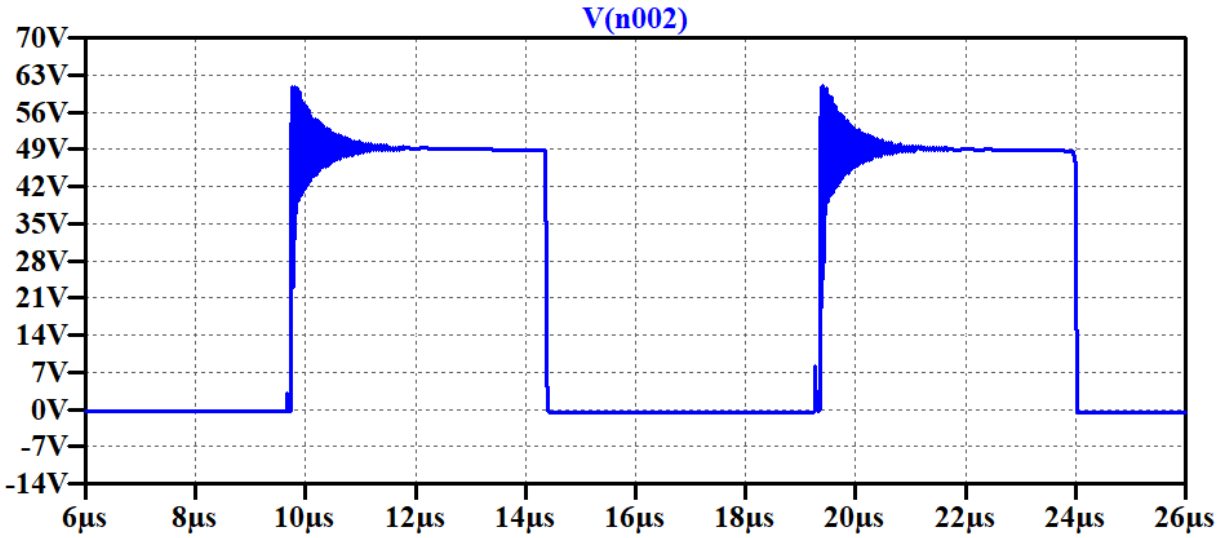


Figure 11. Diode voltage before snubber design

The same procedure applied to the MOSFET's can be applied for this component also. First resonance frequency of the spike is measured. It is found as 224 MHz Then, by connecting shunt capacitor the value of the parasitic capacitance is found in which the resonance frequency is reduced by a factor of two. Finally, by using the capacitance and resonance frequency values, inductance and reactance values can be found. At the end, almost same of the reactance is selected as snubber resistance, and 200pF capacitance value is selected as the snubber capacitance.

$$f_{spike} = 224MHz$$

Capacitance value that reduces spike resonance frequency by half is 100pF. Then, the parasitic capacitance is:

$$C_p = \frac{C}{3} = \frac{100pF}{3} \cong 33pF$$

$$L = 1.53 * 10^{-8}\ H$$

$$Z = 21.53\ ohm$$

At this point, similar to the MOSFET design, resistor value is selected as found impedance value, and capacitor is selected as:

$$4 * C_p \leq C_{snubber} \leq 10 * C_p$$

$$132pF \leq C \leq 330pF$$

Selected exact values are:

$$C_{snubber}^{diode} = 200pF$$

$$R_{snubber}^{diode} = 22\Omega$$

After inserting snubber components, diode voltage waveform is observed as in Figure 12.

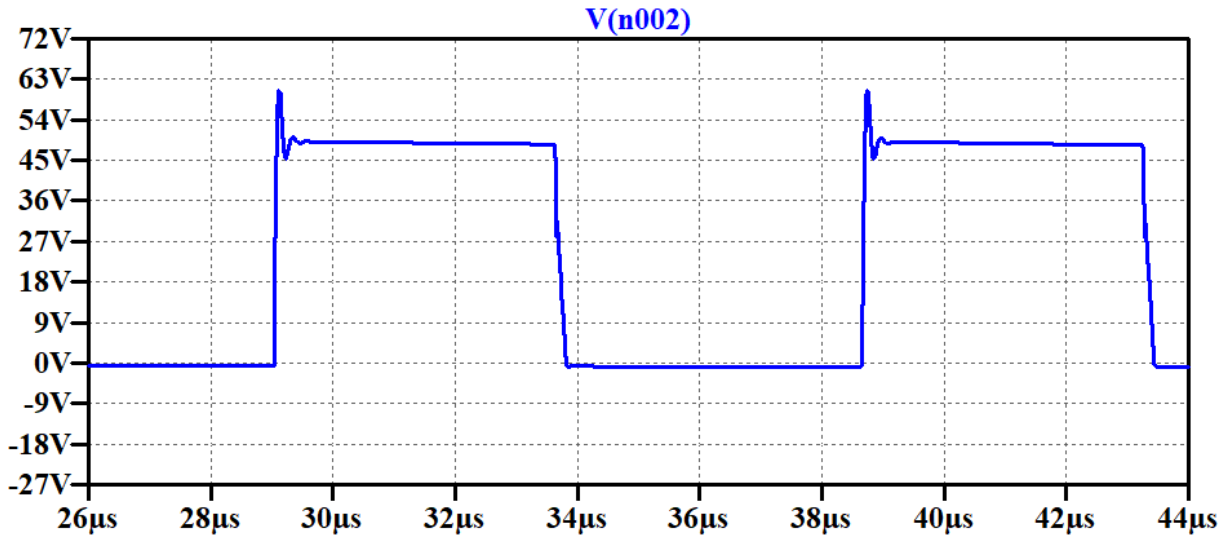


Figure 12. Diode voltage after snubber design

5. Transformer Magnetic Design

We set 16 as transformer turns ratio. Maximum input voltage is 400V, input frequency is 100kHz, maximum output current is 8.33A. A core should be selected due to stated specifications. There is no need for energy storing so we decided to use 2 E shape ferrite cores. Firstly, we calculated the area product for required core

$$W_a A_c = \frac{V_{pri} * I_{pri}}{2 * k_{cu} * J_{rms} * B_{ac} * f}$$

$$W_a A_c = \frac{100}{2 * 0.6 * 6 * 10^6 * 0.2 * 100000} * 10^8$$

$$W_a A_c = 0.0694\ cm^4$$

We checked E shaped ferrite cores and chose 0R42513EC core since it has the smallest area product which is larger than our minimum criteria. Primary and secondary winding turn numbers are calculated as:

$$N_{pri} > \frac{V_{in}}{4 * B_{ac} * A_{core} * f}$$

$$N_{pri} > \frac{400}{4 * 0.2 * 51.8 * 10^{-6} * 100000}$$

$$N_{pri} > 96.53$$

$$N_{pri} = 112\ Turns$$

$$N_{sec} = \frac{N_{pri}}{16}$$

$$N_{sec} = 7\ Turns$$

Magnetizing inductance of the transformer is calculated as:

$$L_m = A_L * {N_{pri}}^2$$

$$L_m = 1900 * 10^{-9} * 128^2$$

$$L_m = 23.834\ mH$$

RMS values of output and input currents should be calculated in order to make a cable selection.

$$I_{sec,rms} = \sqrt{D * I_{out,ave}^2 + 2D * \left(\frac{I_{out,ave}}{2}\right)^2}$$

$$I_{sec,rms} = \sqrt{0.4364 * 8.333 + 2 * 0.4364 * 8.333^2}$$

$$I_{sec,rms} = 6.742 \text{ A}$$

RMS value of primary side can be found from the turns ratio.

$$I_{pri,rms} = \frac{6.742}{16}$$

$$I_{pri,rms} = 0.421\ A$$

Required conductor areas can be found with rms values of the currents and predetermined current density.

$$A_{pri} = \frac{I_{pri,rms}}{J_{rms}}$$

$$A_{pri} = \frac{0.421}{6}$$

$$A_{pri} = \ 0.0702\ mm^2$$

$$A_{sec} = \frac{I_{sec,rms}}{J_{rms}}$$

$$A_{sec} = \frac{6.742}{6}$$

$$A_{sec} = \ 1.124\ mm^2$$

For secondary side AWG16 satisfies the cross-sectional area but it fails with the frequency, it will work with full skin depth causing large losses. As we include the effect of skin depth, we should use AWG26 according to its maximum frequency for 100% skin depth. AWG26 has a smaller skin depth, so we have to parallel them for the secondary.

$$N_{parallel,pri} > \frac{A_{pri}}{A_{AWG26}}$$

$$N_{parallel,pri} > \frac{0.0702}{0.128}$$

$$N_{parallel,pri} = \ 1$$

$$N_{parallel,sec} = \frac{A_{sec}}{A_{AWG26}}$$

$$N_{parallel,sec} > \frac{1.124}{0.128}$$

$$N_{parallel,sec} = 10$$

$$A_{window} = M * 2D$$

$$A_{window} = 5.35 * 2 * 8.7$$

$$A_{window} = 93.09mm^2$$

$$k_{cu} = \frac{2 * A_{copper,pri} + 2 * A_{copper,sec}}{A_{window}}$$

$$k_{cu} = \frac{2 * 112 * 0.128 + 2 * 7 * 10 * 0.128}{93.09}$$

$$k_{cu} = 50.1\%$$

The design of transformer is completed. Fill factor is satisfactory. Losses of this transformer should be calculated. Copper losses are calculated as follows.

$$MLT = 2\pi \frac{E - F}{2}$$

$$MLT = 2\pi \frac{17.5 - 7.5}{2}$$

$$MLT = 31.416\, mm$$

$$R_{pri} = \frac{N_p * MLT * R}{Number\ of\ parallel\ cables}$$

$$R_{pri} = \frac{112 * 31.416 * 133.8568 * 10^{-6}}{1}$$

$$R_{pri} = 471\ m\Omega$$

$$R_{sec} = \frac{N_p * MLT * R}{Number\ of\ parallel\ cables}$$

$$R_{sec} = \frac{7 * 31.416 * 133.8568 * 10^{-6}}{10}$$

$$R_{pri} = 2.944\ m\Omega$$

$$P_{cu,total} = 2 * P_{cu,pri} + 2 * P_{cu,sec}$$

$$P_{cu,total} = 2 * 0.421^2 * 471 * 10^{-3} + 2 * 8.333^2 * 2.994 * 10^{-3}$$

$$P_{cu,total} = 0.58W$$

Core loss is calculated as follows.

$$P_{core} = a * f^x * B^y * V_{core}$$

$$P_{core} = 0.036 * 100^{1.64} * 0.2^{2.68} * (2 * 2.99)$$

$$P_{core} = 2.63\ W$$

$$P_{transformer} = 0.58 + 2.63$$

$$P_{transformer} = 3.21\ W$$

The related skin depth analysis for this application can be conducted as:

$$Skin\ Depth(\delta) = \sqrt{\frac{\rho}{\pi * f_o * \mu_r * \mu_0}}$$

$$\delta = \sqrt{\frac{0.0171}{\pi * 100 * 10^3 * 0.999994 * 4 * \pi * 10^{-7}}}$$

$$\delta = 208\mu m$$

In this design only AWG26 cable is used. Diameter of this cable is 0.403mm. Therefore, the skin depth exist which is 0.208mm will not create a problem for this design.

6. Component Selection

In the topology design there exist 3 main integrated circuits (IC), which are the main controller & gate driver, opto-coupler and opto-coupler driver.

For the main controller LTC3723-1 integrated circuit is selected. It can preserve both controller property and gate driver property. That will make design more systematic, cheaper and small size. This IC can drive two low side gate driver exists in the push pull topology according to the drive properties. At each switch cycle only one gate is driven and at some duration both gates are turned off, which is called dead time.

For the isolation, the controller IC doesn't preserve isolation. Therefore, an external isolation circuitry is required. For that purpose, an opto-coupler IC and its driver is used, which are MOC207 opto-isolator and LT1431 programmable reference. The compensation circuit is

designed over the programmable reference pins. It preserves that duty for the general system performance. The necessary details about the compensation circuit design is explained in controller design section. In general, selected components can be seen in Table 2 in the cost analysis section.

We have selected necessary components for our converter application. Table 2 represents the used components and their prices. After choosing all the components, we calculated the losses and conducted detailed simulations which include all the non-idealities. Losses are calculated as follows.

Transformer:

$$P_{core} = 3.21\ W$$

Diodes (Calculated for One):

$$P_{loss} = I * V_f$$

$$P_{loss} = 8.333 * 0.56$$

$$P_{loss} = 4.67\ W$$

MOSFETs (Calculated for One):

$$P_{conduction} = I^2 * D * R_{DS}$$

$$P_{conduction} = 7^2 * 0.12 * 0.35$$

$$P_{conduction} = 2.058\ W$$

$$P_{switching} = \frac{1}{2} * V_{in} * I_{in} * (t_r + t_f) * f$$

$$P_{switching} = \frac{1}{2} * 400 * 7 * (16 + 17) * 10^{-9} * 100 * 10^3$$

$$P_{switching} = 4.62\ W$$

$$P_{gate} = V_{GS} * f * Q_g$$

$$P_{gate} = 20 * 100 * 10^3 * 19 * 10^{-9}$$

$$P_{gate} = 0.038\ W$$

Output Inductor:

$$P_{loss} = I_o^2 * ESR$$

$$P_{loss} = 8.333^2 * 26.2 * 10^{-3}$$

$$P_{loss} = 1.82\ W$$

Integrated Circuits:

$$P_{total} = 0.42\ W$$

Thermal Circuit

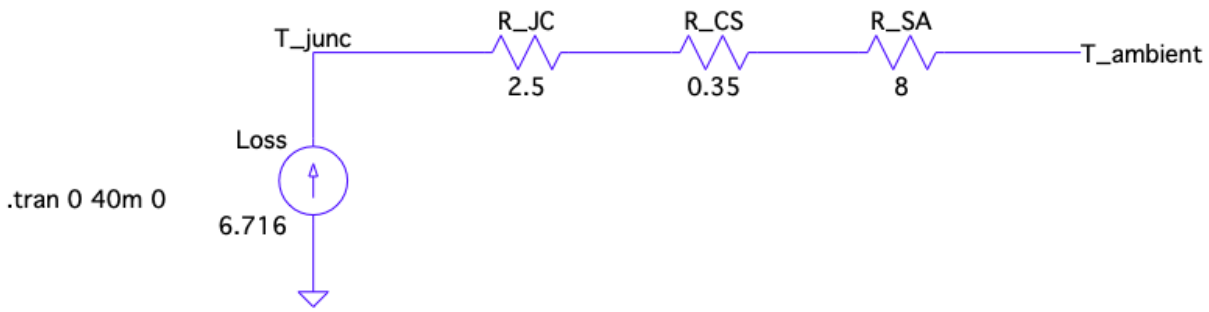


Figure 13. Thermal Circuit of MOSFET and Heatsink

Heatsink is needed for the MOSFETs. Maximum temperature for MOSFET operation is 150°C according to datasheet and we want to have a smaller but close junction temperature in order to use a cheaper heatsink. We chose 513301B02500G model of Aavid, Thermal Division of Boyd Corporation which has 8°C/W thermal resistance. Thermal circuit is shown in Figure 13. We are using natural cooling. Junction temperature is 98°C with the heatsink.

$$T_{junction} = (8 + 0.35 + 2.5) * 6.716 + 25$$
$$T_{junction} = 97.87^{o}C$$

However, when we compare the cases which adding heatsink to the MOSFETs or using the box as a heatsink. Using the box as a heatsink and connecting MOSFETs' and Diodes' pads to the box will cool down our system. Therefore, there is no need to buy additional heatsink under these conditions.

Efficiency:

$$P_{total} = 16.836\ W$$

$$efficiency = \frac{100}{116.836} = 86\%$$

7. Detailed Simulation Results

This project design is completed over LTSpice simulation software. The designed circuit can be seen in sub-blocks as shown in Figure 14 to 16.

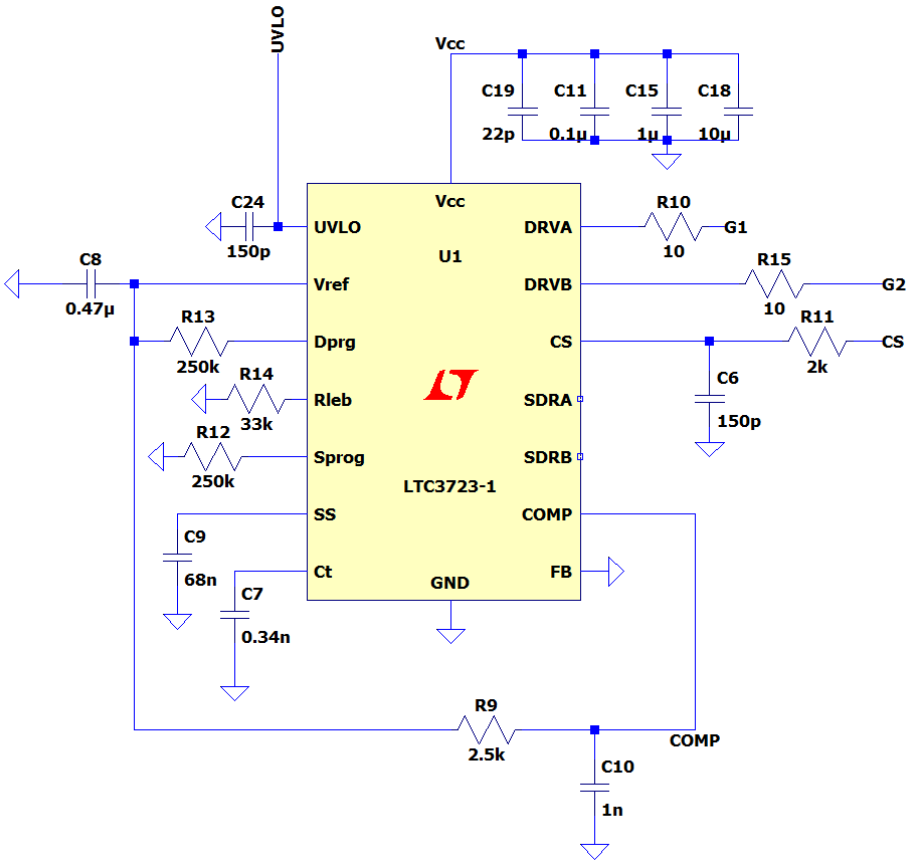


Figure 14. Controller IC setup circuit

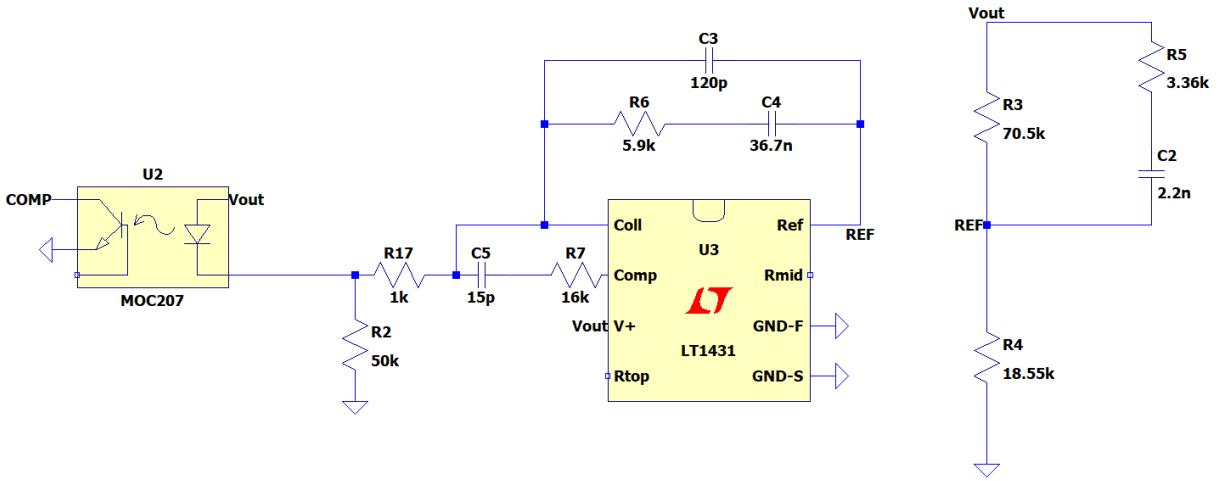


Figure 15. Opto-Coupler and it's driver circuit with reference voltage and compensator circuits

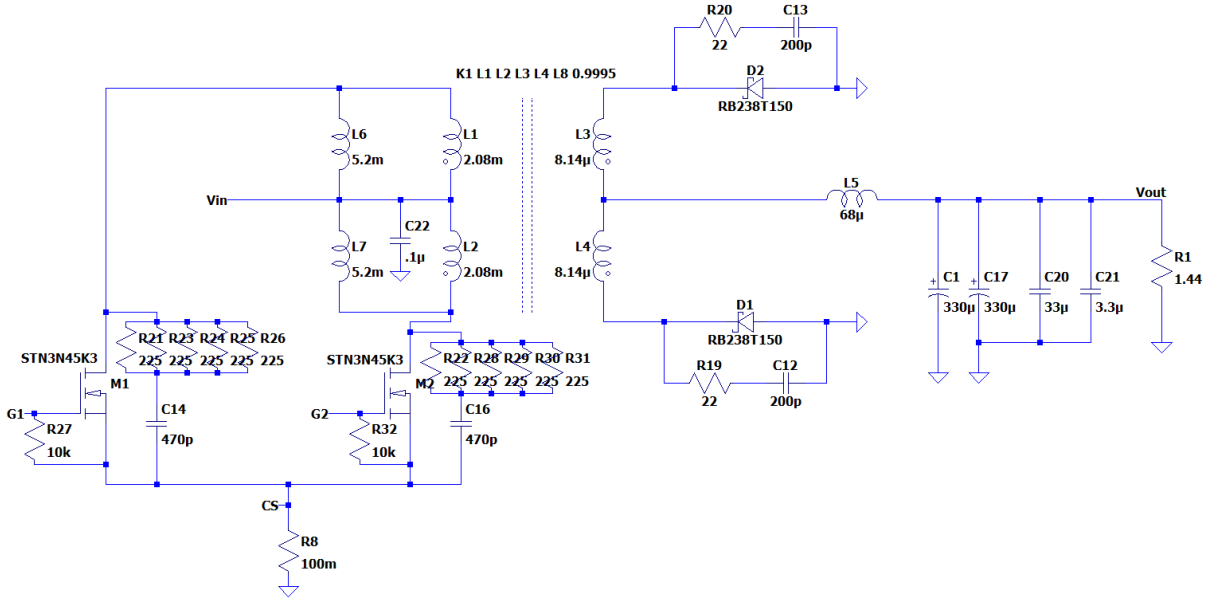


Figure 16. Main topology design and output filter part

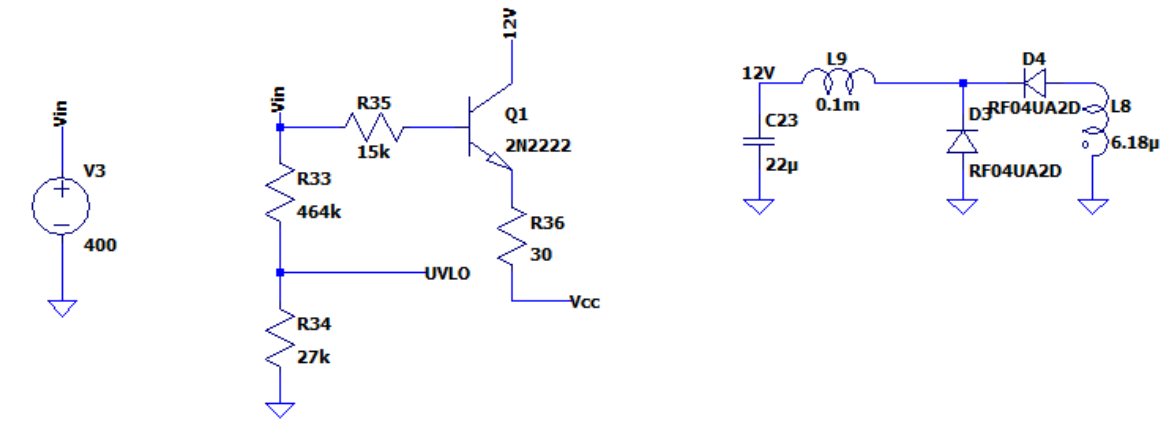


Figure 17. Auxilary winding and startup circuit design for controller supply voltage

As shown in Figures 14-17, system mainly consists of 3 sub-systems; topology design, controller design and opto-coupler design parts. With connecting these parts, overall system simulations are as followings.

Before starting any design, the output filter is simulated. With the entered below values the bode magnitude and phase diagrams are shown in Figure 18. Later, in the closed loop performance the inductor and capacitor values can be updated.

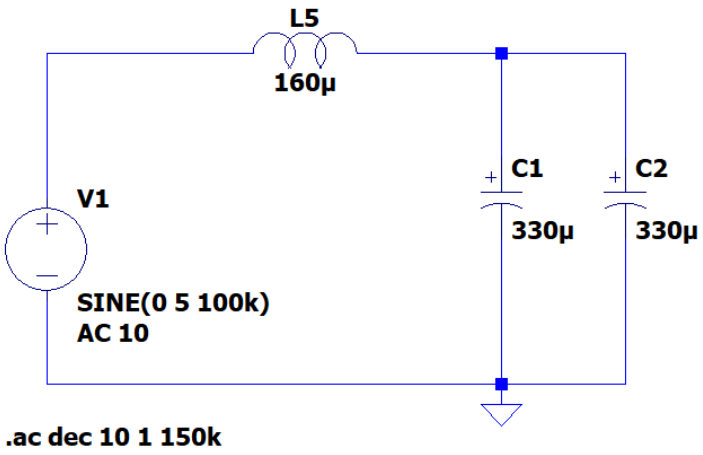


Figure 18. Output filter ac analysis circuit

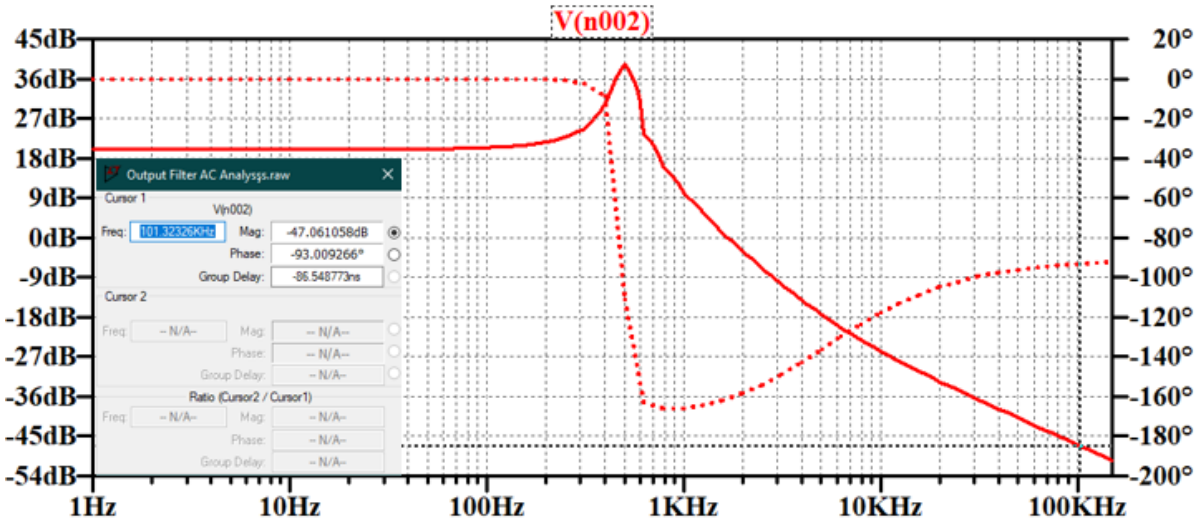


Figure 19. Magnitude and Phase Bode plots for output filter

As can be seen in Figure 18, the designed output filter has 87 degree phase margin at 100kHz operating frequency. Phase margin larger than 40 degree is preferred for stable closed loop systems.

When input voltage is 220V, the output voltage and power waveform is as shown in Figure 20.

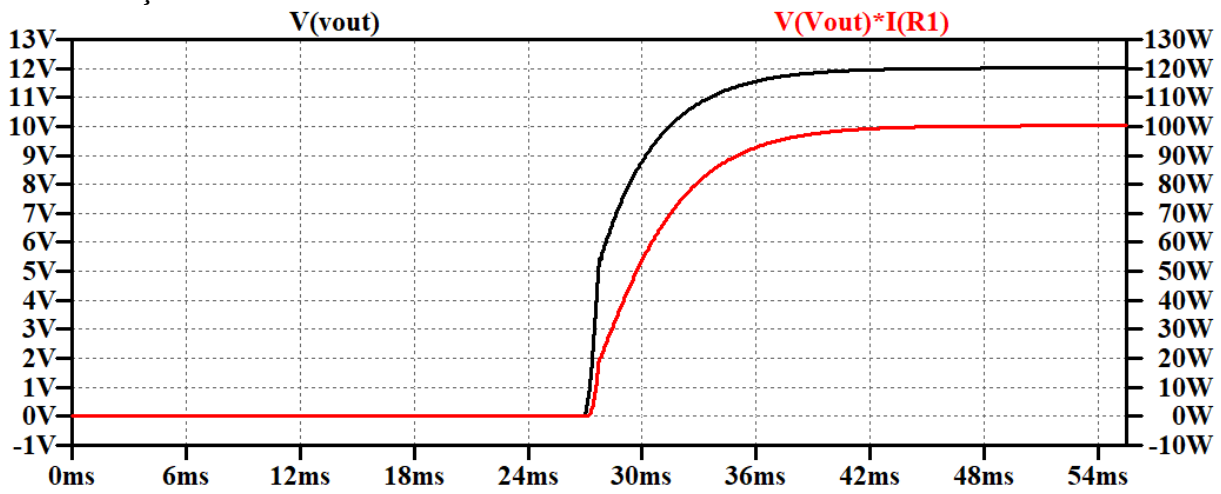


Figure 20. Output voltage and power waveforms when input voltage is 220V

Output voltage stabilizes at 12.014V. The output voltage ripple is measured as 0.66 mV as can be seen in Figure 21. It is 0.0025% of the output voltage.

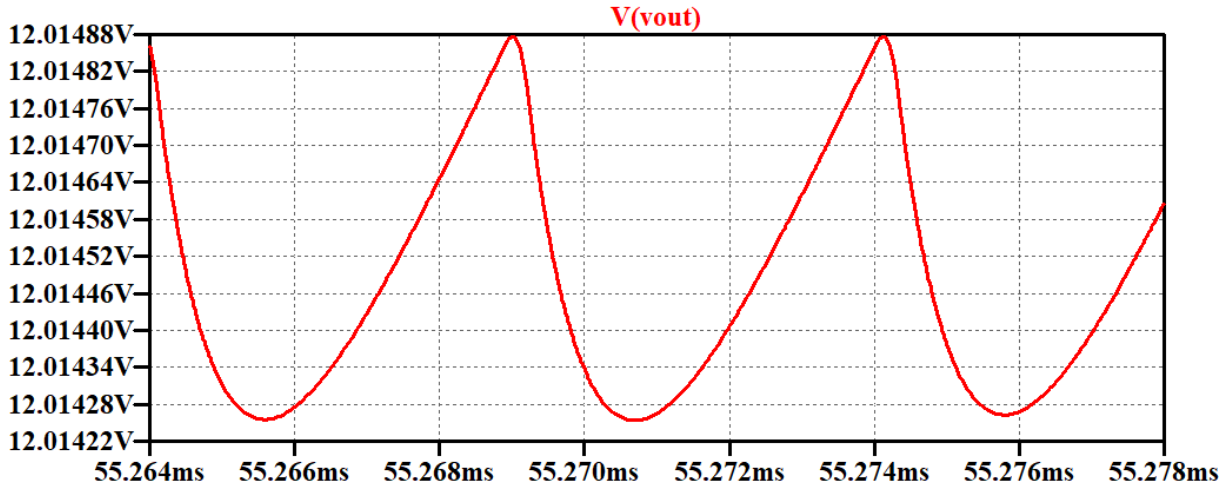


Figure 21. Output voltage ripple when input voltage is 220V

System's stability performance react to the load changes is critical for the design. The designed system's stability response to the load change from no load to full load can be seen in Figure 22.

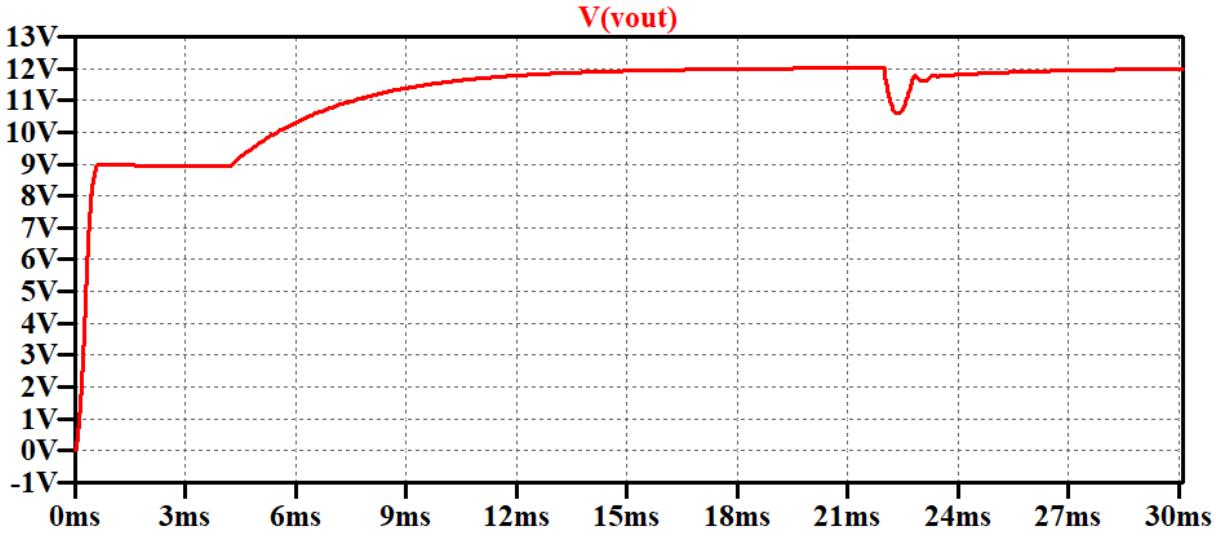


Figure 22. No load to full load stability performance when 220V input voltage exists

The inductor current in the steady state can be seen in Figure 23.

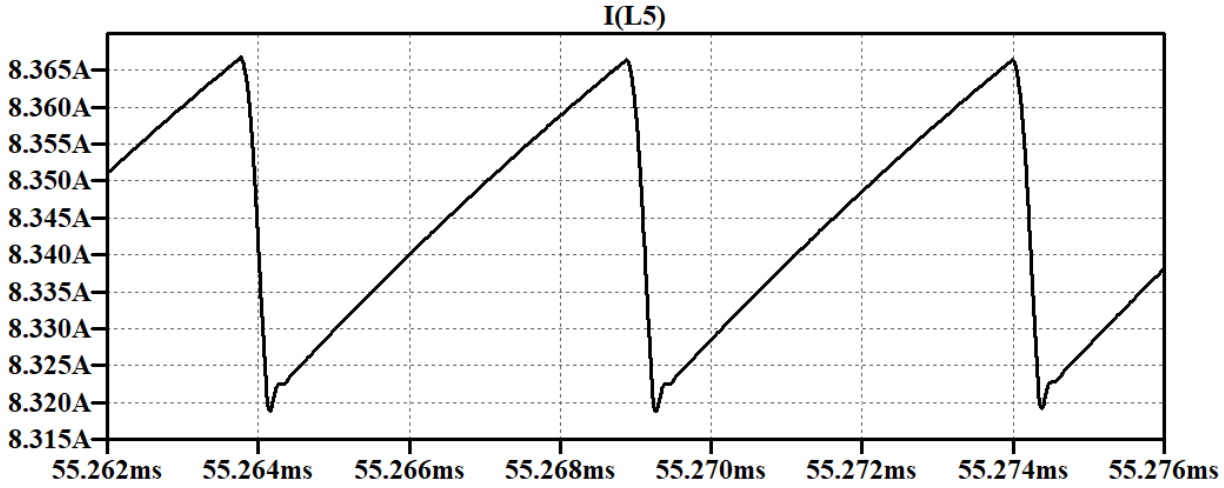


Figure 23. Inductor current waveforms when input voltage is 220V

The gate signals of the MOSFETs' can be analyzed in Figure 24.

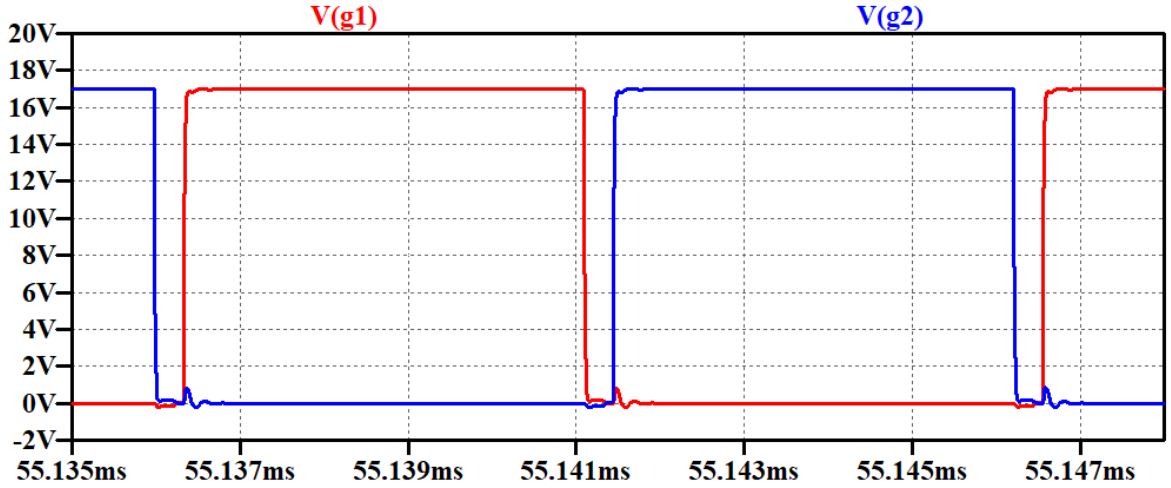


Figure 24. MOSFETs' gate signals when input voltage is 220V

When input voltage is 400V, the output voltage and power waveform is as shown in Figure 25. Note that, the output voltage stabilizes at 12.0014V.

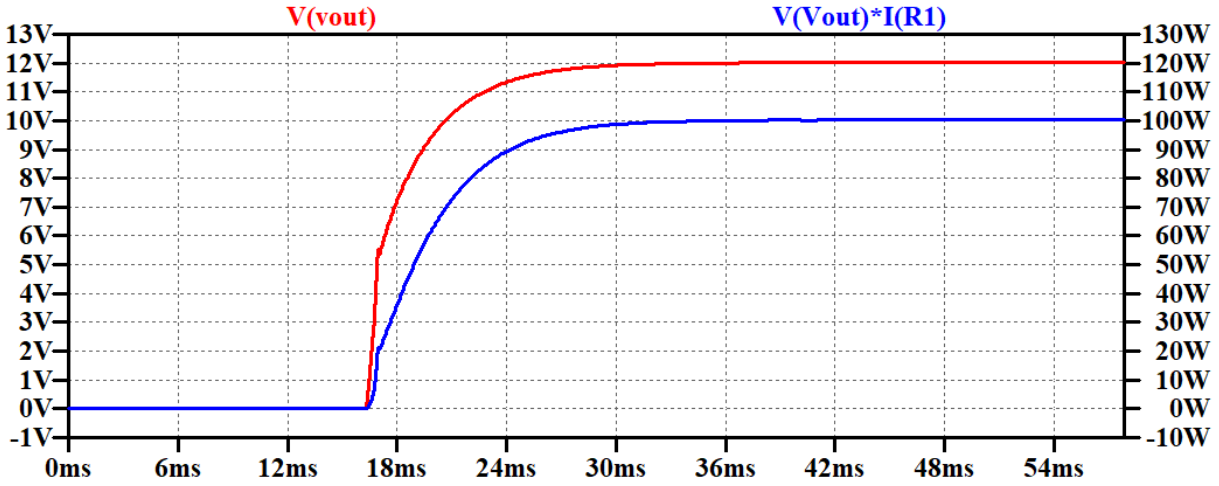


Figure 25. Output voltage and power waveforms when input voltage is 400V

The output voltage ripple is measured as 7.2mV as can be seen in Figure 26. That is 0.43% of the output voltage.

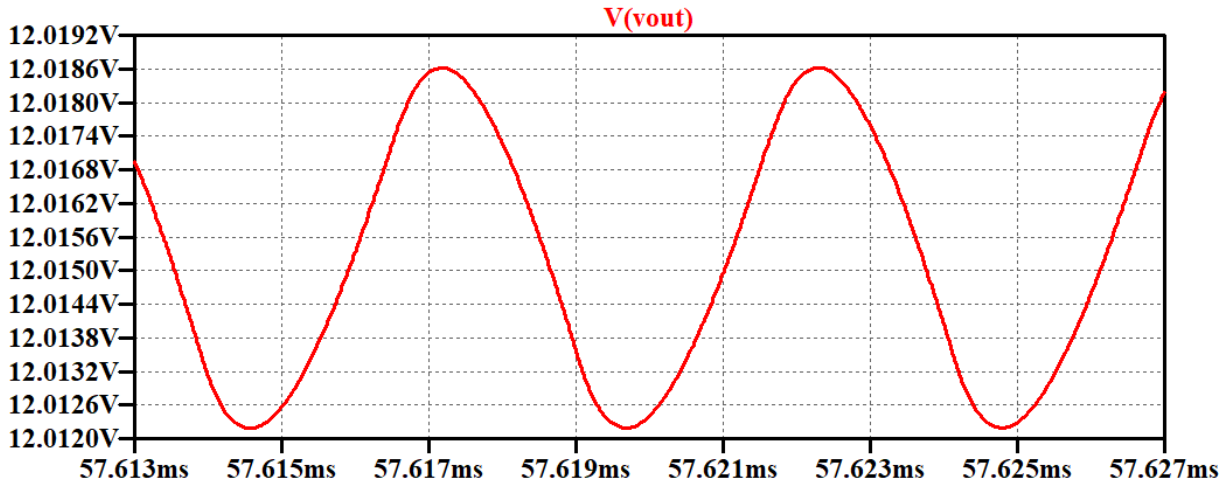


Figure 26. Output voltage ripple when input voltage is 400V

Inductor current waveform in the steady state can be seen in Figure 27.

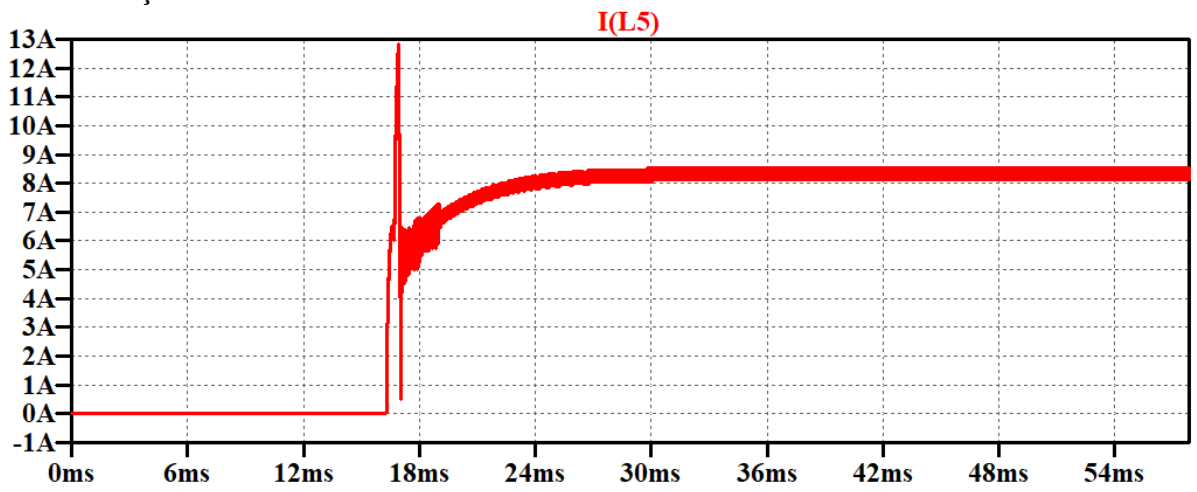


Figure 27. Inductor current waveform in the steady state when input voltage is 400V

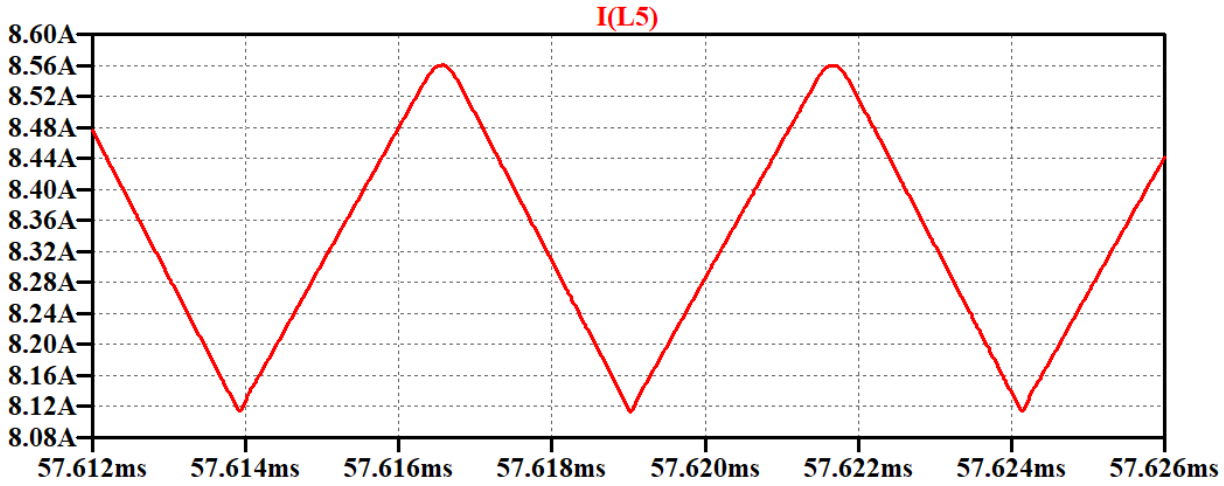


Figure 28. Inductor current ripple when input voltage is 400V

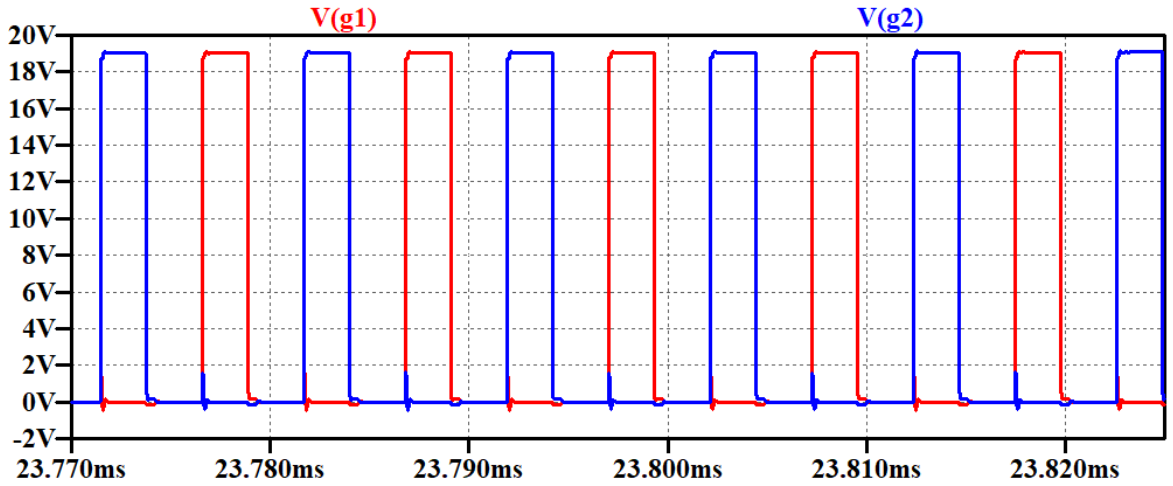


Figure 29. MOSFETs' gate signals when input voltage is 400V

From no load to full load the output voltage waveform can be seen in Figure 30.

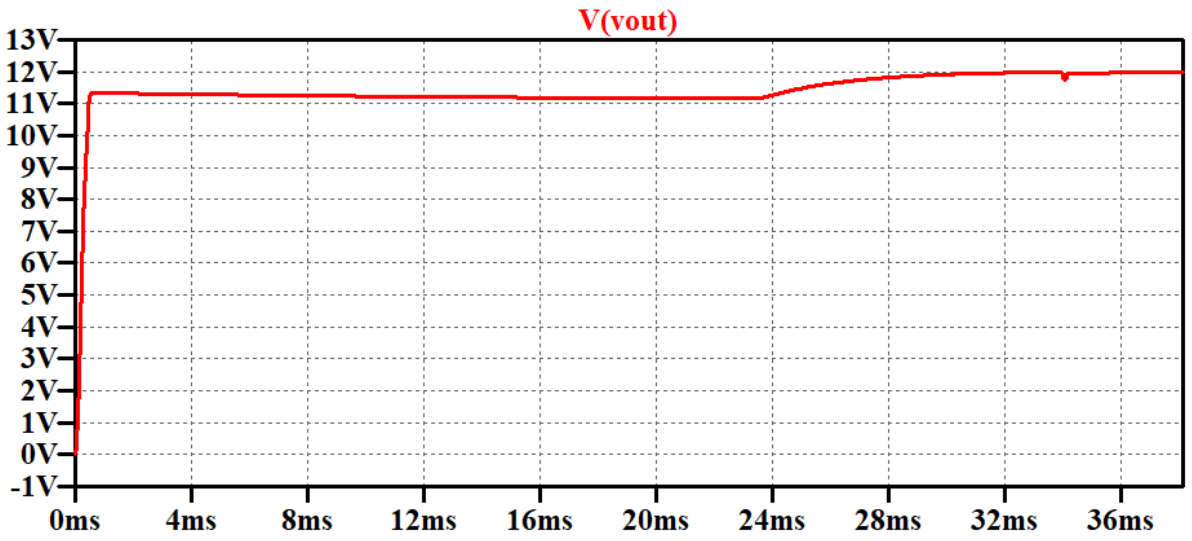


Figure 30. No load to full load stability performance when input voltage is 400V

In order to check the stability, we can analyze the compensator pin current. In desired situations, we should expect to see very little current. As a result, we measure almost no current in that leg. It means that the stability is satisfied.

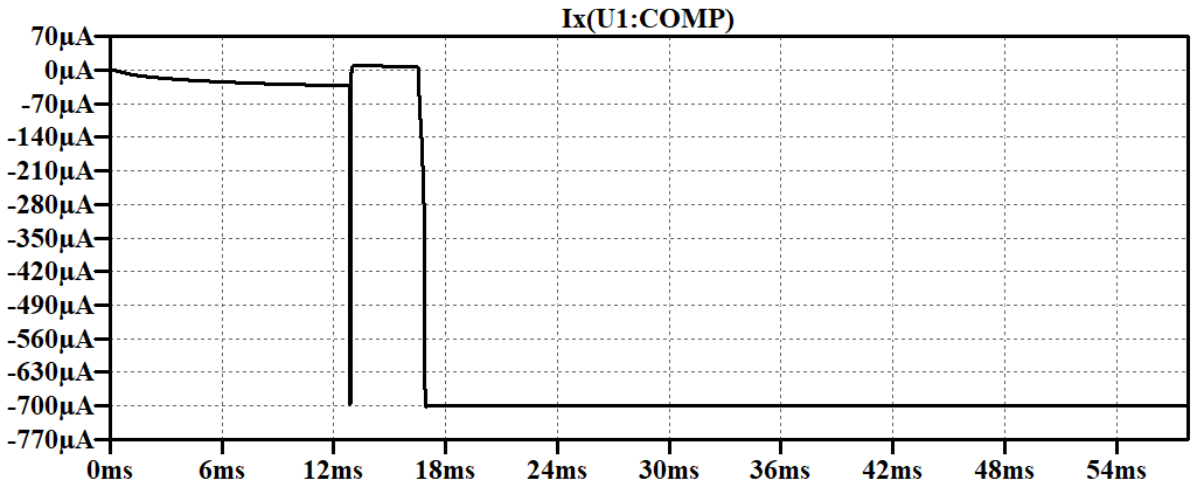


Figure 31. IC's COMP leg current

The line regulation when input voltage changes from 220 V to 400 V can be calculated from the above results as:

$$Line_{reg} = \left(\frac{V_{out}^{220V} - V_{out}^{400V}}{V_{out}^{220V}}\right) * 100 = \frac{12.02 - 12.0014}{12.02} * 100 = 0.155\%$$

8. Printed Circuit Board (PCB) Design

The designed board is drawn on the Altium Designer tool. First, the screenshot of the schematic design can be seen in Figure 25. The original output documentation will be attached at the end of this document.

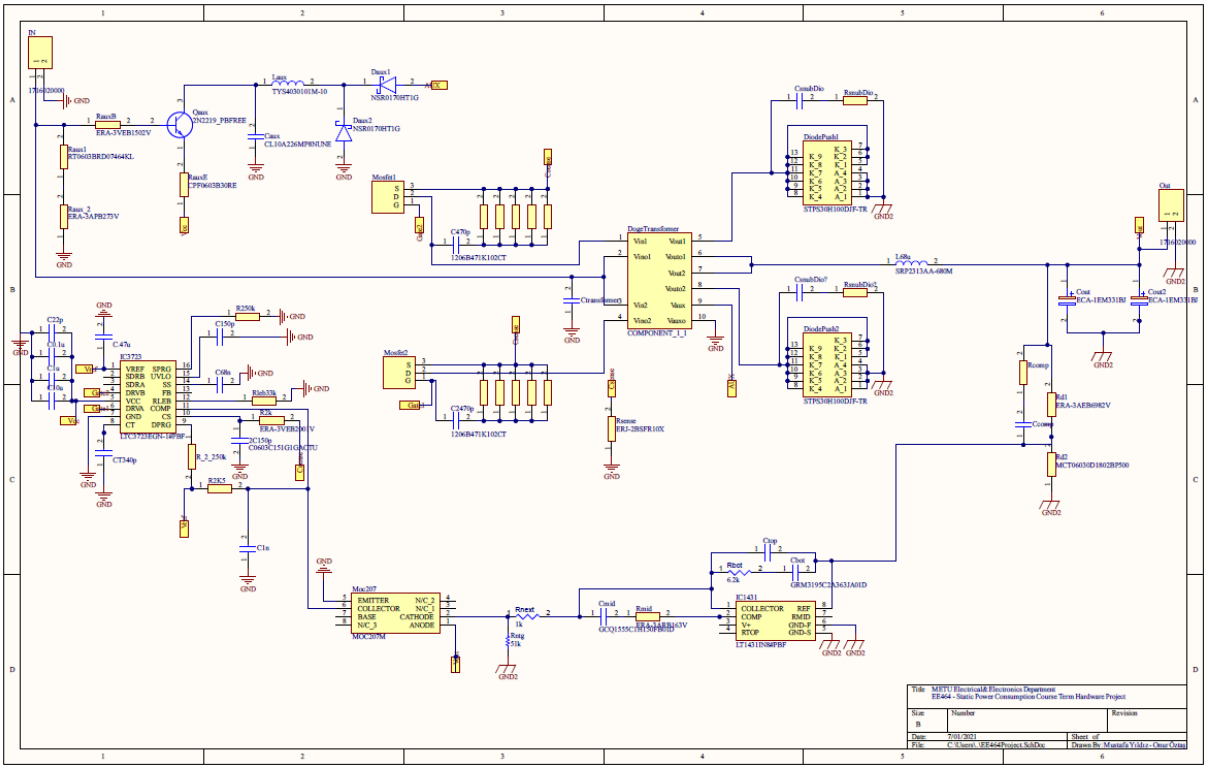


Figure 32. Schematic design of the project

After completing the schematic design, at first the schematic connections are checked whether there is a missing net or duplicated component name or not. After that, the routings are controlled. After deciding that everything is correct and as desired, then the layout drawing stage is started.

Before layout drawing, the critical parameters are set. They are the clearances and the width of the routings. For the minimum clearance criteria, the IPC2221 [1] standards are taken as reference. In that document, minimum clearance for 301-500V application is stated as 0.25mm. This value is set in the Altium rules section. For the width of the nets the current that passes through that wire is considered. For logical signals carrying wires minimum width is preferred, and for the higher current carrying wires maximum width is preferred. For minimum width 0.25mm, and for maximum width 2.5mm nets are used. For connections, usually polygon planes are used. They ease the current transmission, decrease the EMI/EMC effect, which may be created through the wires. Therefore, polygon planes are very critical in the power boards.

For the PCB, 2-layer board is used. The components are placed in the top layer. Whereas, the bottom layer is used for the grounds and input signals in a large polygon plane. The aim on this application is that the ground signals in the top layer is connected with a via connection to the

bottom layer. That will increase the signal transmission, also decrease the wire connection which is preferred. Overall, a PCB design with 67x86 mm size board is designed. The necessary outputs can be seen in the below figures.

The layout representation of the components can be seen in Figure 26.

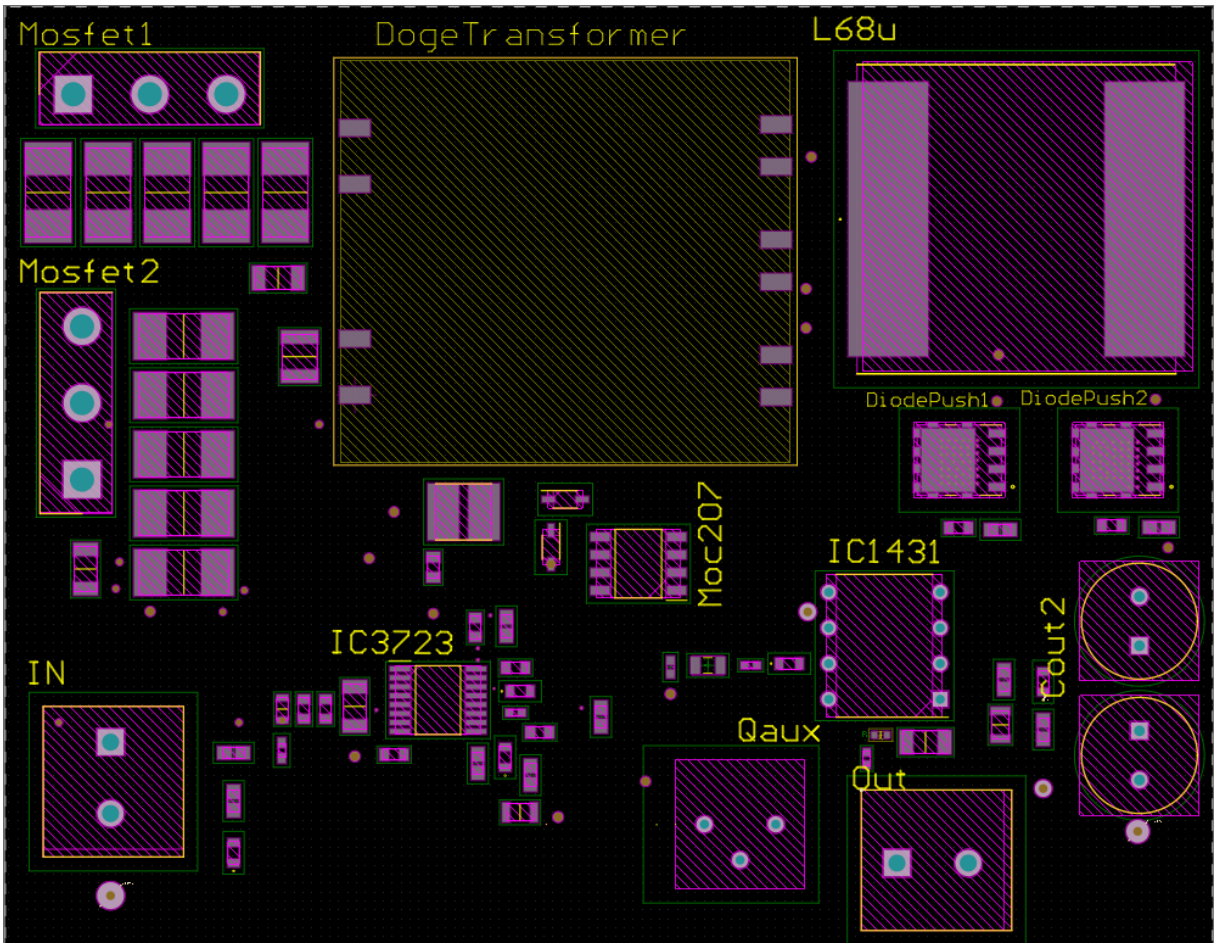


Figure 33. The layout representation of the components

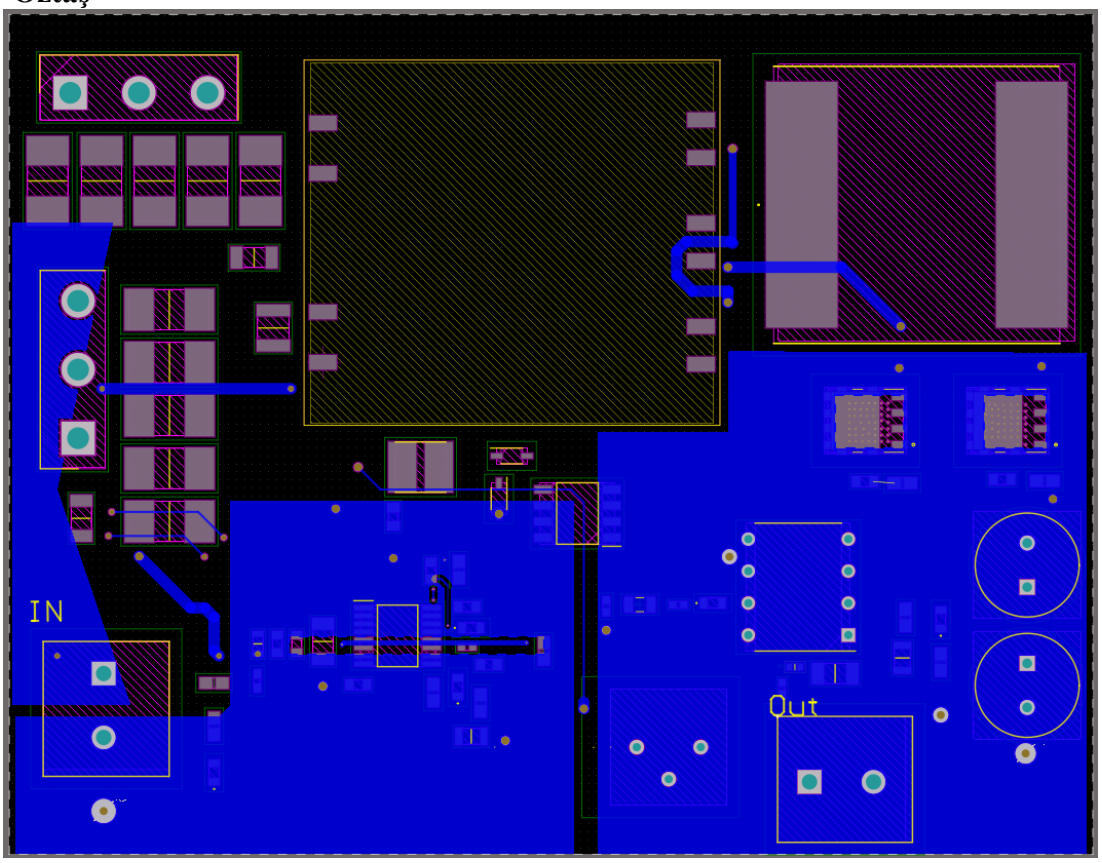


Figure 34. The bottom layer representation of the board

In this figure, the bottom layer can be seen. There are mainly three polygone plane, and some nets for the top layer components. The one with ‘IN’ representation can be seen is for the input voltage. The near one is the primary ground, and the right one is for the secondary ground. The connections with the top layer is completed by using the vias between these two layers.

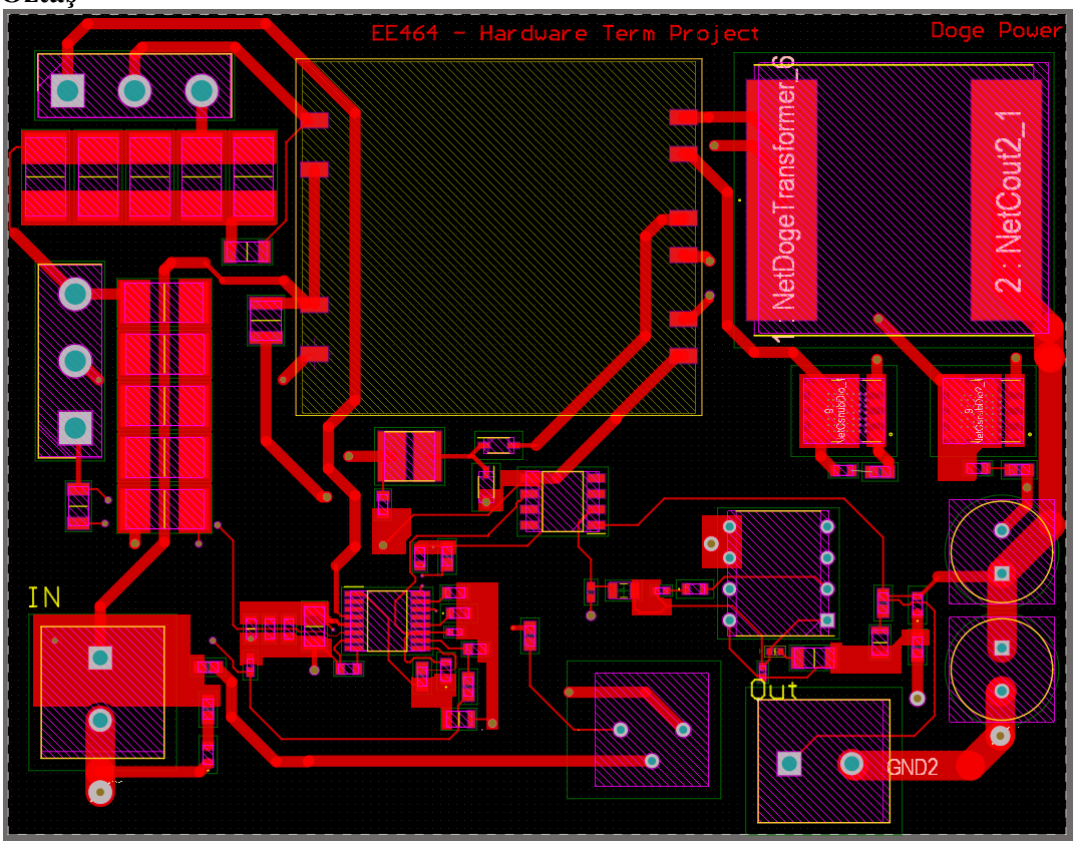


Figure 35. Top layer net representation

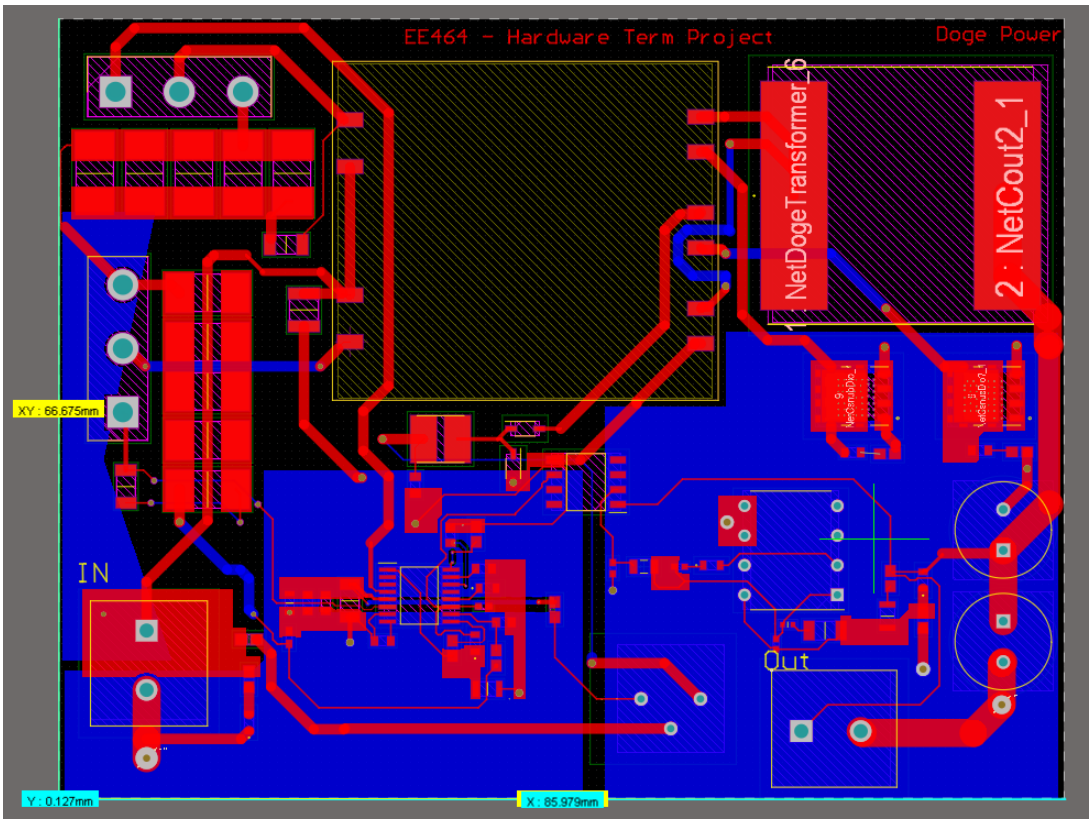


Figure 36. Overall PCB layout representation with board size is shown

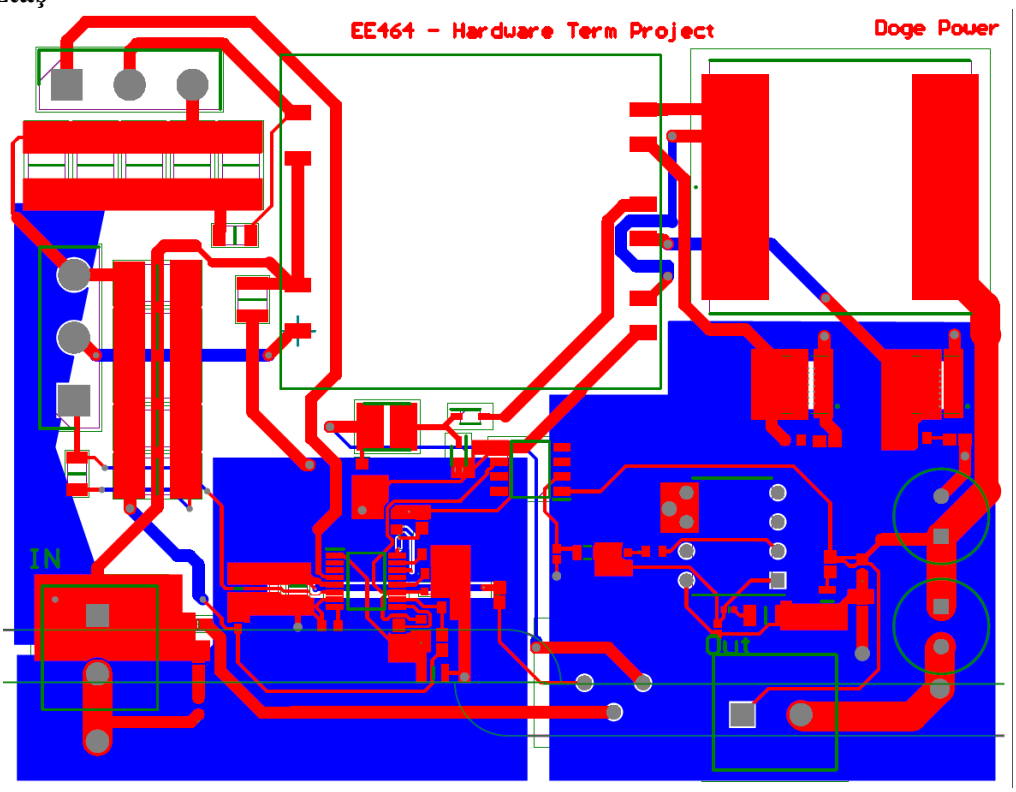


Figure 37. Altium smart pdf layout output for the design

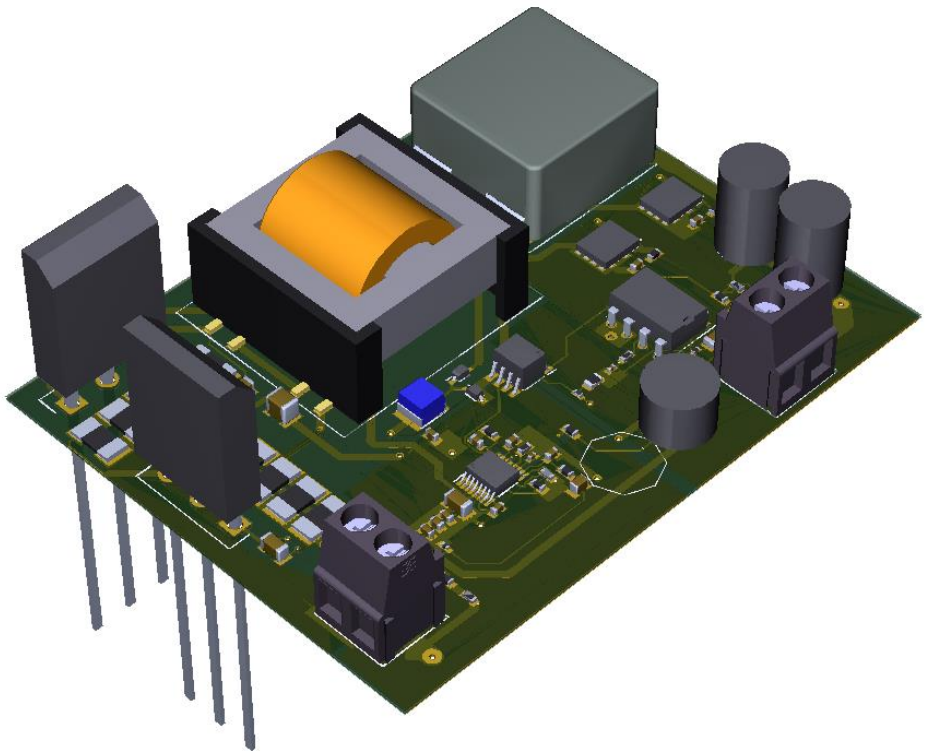


Figure 38. 3D view of the designed board.

The legs of the MOSFET's are seen as a long form. They are modified during the box design.

9. Coverage Box Design

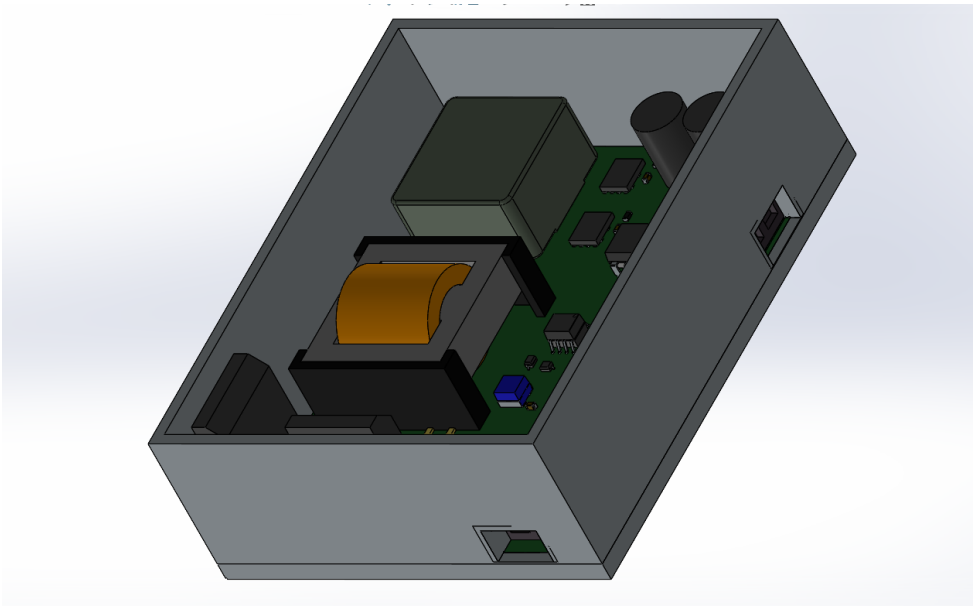


Figure 39. 3D Model of the Entire System

Figure 40. Input Enterance of the Converter

The converter needed a box which can provide insulation from outside and act like a heatsink, so we used metal material. The resulted 3D view of the box is seen in Figure 32. There is a cover that is fitting at the top, it is not shown in Figure 32 due to clear representation of inside. Figure 33 shows the input enterance of the converter, cover can be opened for cable adjustment with screwdrivers.

10. Cost Analysis

The overall project cost can be seen in Table 2. Table 2 indicates the BOM of the project taken from the Mouser Electronics. Additionally, the PCB cost is included for 1000 pieces. As a result, the project's cost is $38.264.

Table 1. Cost Analysis of the Project

SHOPPING BASKET				
This is not an invoice				
01-Jul-21 04:19:43				
	Mouser No	**Order Qty.**	**Price (USD)**	**Ext.: (USD)**
1	80-C0603C151G1GACTU	1000	$0.273	$273.00
2	581-06031C104K4Z2A	1000	$0.062	$62.00
3	581-04025C102J	1000	$0.013	$13.00
4	810-C1608X5R1H105K	1000	$0.055	$55.00
5	187-CL31A106MBHNNNE	1000	$0.082	$82.00
6	581-06035A220J	1000	$0.014	$14.00
7	710-885012206070	1000	$0.023	$23.00
8	187-CL10C151JB8NNNC	1000	$0.013	$13.00
9	791-1206B471K102CT	1000	$0.058	$58.00
10	810-CGA4J1X8L1H47412	1000	$0.205	$205.00
11	187-CL10A226MP8NUNE	1000	$0.038	$38.00
12	81-GRM3195C2A363JA1D	1000	$0.196	$196.00
13	81-GRM21B5C2J222FWAL	1000	$0.158	$158.00
14	81-GCQ1555C1H150FB1D	1000	$0.159	$159.00
15	667-ECA-1EM331BJ	1000	$0.094	$94.00
16	81-GRM1885C2A201JA1D	1000	$0.035	$35.00
17	81-GRM1885C2A361JA1D	1000	$0.039	$39.00
18	80-C0402C121K8RACTU	1000	$0.038	$38.00
19	80-C1210C104KBRAUTO	1000	$0.132	$132.00
20	863-NSR0170HT1G	1000	$0.043	$43.00
21	511-STPS30H100DJF-TR	1000	$0.468	$468.00
22	584-LT1431IN8#PBF	1000	$2.77	$2,770.00
23	584-C3723EGN-1TRPBF	2500	$6.43	$16,075.00
24	470-1716020000	2000	$0.372	$744.00
25	652-SRP2313AA-680M	1000	$4.28	$4,280.00
26	875-TYS4030101M-10	1000	$0.163	$163.00
27	512-MOC207M	1000	$0.288	$288.00
28	511-STW11NK100Z	2000	$4.06	$8,120.00
29	610-2N2219-PB	1000	$1.21	$1,210.00
30	667-ERA-3VEB2001V	1000	$0.15	$150.00
31	667-ERA-3AED2491V	1000	$0.032	$32.00
32	594-MCT06030C2493FP5	1000	$0.018	$18.00
33	603-RT0603BRD07464KL	1000	$0.05	$50.00
34	667-ERA-3APB273V	1000	$0.181	$181.00
35	667-ERA-3VEB1502V	1000	$0.15	$150.00
36	279-CPF0603B30RE	1000	$0.101	$101.00
37	603-RC0402JR-13390KL	1000	$0.004	$4.00
38	279-CPF0603B3K32E	1000	$0.105	$105.00
39	667-ERA-3AEB6982V	1000	$0.039	$39.00
40	594-MCT06030D1802BP5	1000	$0.181	$181.00
41	667-ERA-3AED333V	1000	$0.032	$32.00

	Mouser No	Order Qty.	Price (USD)	Ext.: (USD)
42	667-ERA-3ARB163V	1000	$0.201	$201.00
43	594-MCT06030C1001FP5	1000	$0.023	$23.00
44	754-RR0816P-513D	1000	$0.017	$17.00
45	667-ERJ-2BSFR10X	1000	$0.111	$111.00
46	603-RC0603FR-1022RL	1000	$0.005	$5.00
47	279-CRGH2512F221R	1000	$0.194	$194.00
48	0R42513EC	2000	2.500	$5000
49	PCB Cost	1000	$0.822	$822
By submitting your order you agreeto these ter			**Merchandise:**	$43,264.00
Prices are reflected at the date and time show			**Delivery Charge:**	$0.00
			Back-order Delivery:	$0.00

Figure 41.2 Layer PCB cost

Conclusion

The aim of this project is to obtain 100W 12V DC output from a variable DC voltage source. In order to obtain required DC-DC converter first a suitable topology is selected. According to the evaluations described above, push pull topology is preferred. After selecting topology, the power transformer analysis is conducted. While proceeding with the calculations a suitable inductance, turns ratio etc. value ranges are determined, and then by using a PExprt power transformer design application a primary and secondary inductance values are found by entering the found transformer values.

After finding transformer values, the system is performed in open loop. It gives 12V at 100W power in suitable pulse duty cycles. Next, selected integrated circuits are entered into the simulation, and system is run over closed loop design. At this stage, a compensator circuit is designed. For the system specifications, Type 3 compensator circuit is sufficient for system stability.

Next, filtering for the EMI effects is completed by designing snubber circuits. The power ratings of the snubber components are decreased by suitable number paralleling application. After completing the simulation step, a component selection is done, and a BOM is prepared.

As a final step, the schematic of the design is drawn over Altium Designer tool. For the designed components a schematic, footprint and 3D models are created. After completing schematic, layout part is started. A 2-layer PCB is designed. In the design process, polygon planes are used as far as possible. The reason for that, they will ease the current flowing, reduces the EMI/EMC problems. Components are placed in the top plane. Some of the wires are drawn on the bottom plane by connecting with vias. In the pads of the diodes, several vias are created, and they will be connected to the box of the design.

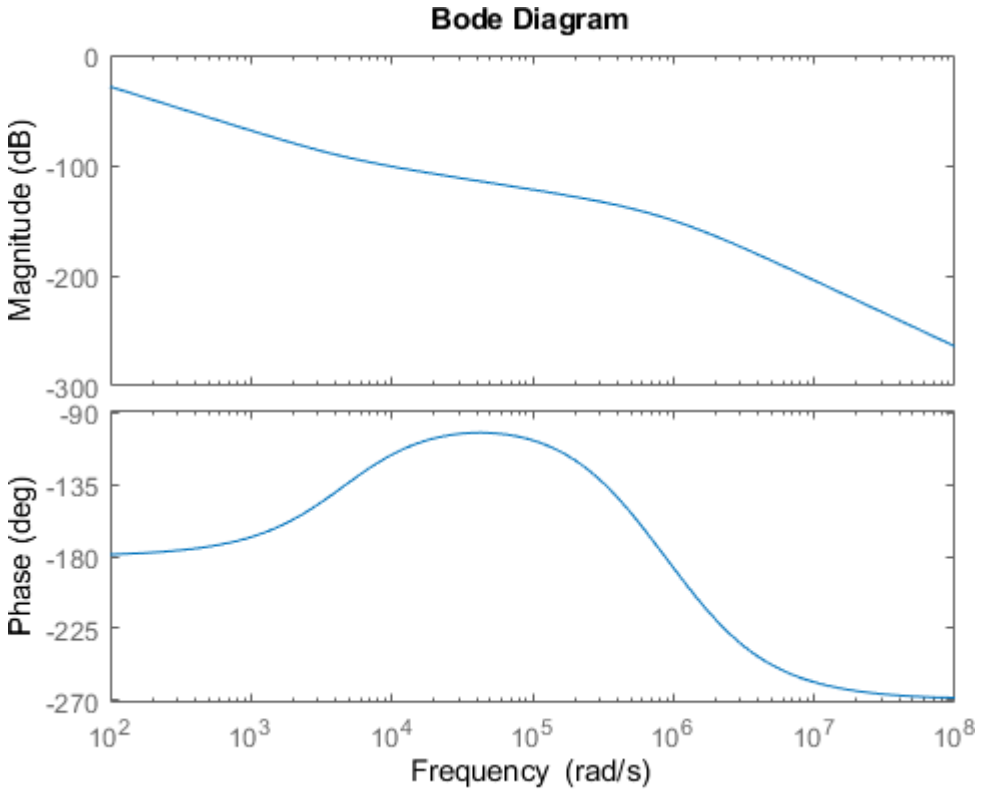
As a result, in this project an isolated variable input constant output DC-DC switched mode power supply design is conducted with very small ripple ratings and strong stability performances. Overall cost for this project almost 43$ levels.

References

[1] http://www-eng.lbl.gov/~shuman/NEXT/CURRENT_DESIGN/TP/MATERIALS/IPC-2221A(L).pdf

Appendix A – Compensation Circuit Design

```
%Doge Power Compensator Design File

L = 80e-6;                              %Output Inductance
C = 330e-6;                             %Output Capacitance
ESR = 56e-3;                            %Capacitor ESR value
F_lc = 1/(2*pi*sqrt(L*C));              %Filter frequency
F_esr = 1/(2*pi*ESR*C);                 %ESR frequency
Fsw = 100e3;                            %Switching frequency
Fzero = Fsw/10;                         %Center frequency

Vref = 2.5;                             %Driver reference voltage
Vout = 12;                              %Output voltage
Vosc = 2.35;                            %Peak-to-Peak
 oscillator amplitude voltage
Vin = 300;                              %Minimum input voltage

%Type 3 Compensator pole and zero frequencies
Fz2 = F_lc;                             %Second zero frequency
Fz1 = 0.75*F_lc;                        %First zero frequency
Fp2 = F_esr*10;                        %Second pole frequency
%Fp3 = Fsw/2;                           %Third pole frequency
Fp3 = Fsw*2.25;                         %Third pole frequency


%Type 3 Compansator Parameters
Cf3 = 2.2e-9;                           %Cf3 is selected then rest
 is calculated from it
Rf3 = 1/(2*pi*Cf3*Fp2);                 %Voltage division
compensator Rf1 = 1/(2*pi*Cf3*Fz2)-Rf3;   %Voltage division top
resistor Rf2 = (Rf1*Vref)/(Vout-Vref);%Voltage division bottom
 resistor
Rc1 =
(2*pi*Fzero*L*C*Vosc)/(Vin*Cf3); Cc1
= 1/(2*pi*Rc1*Fz1);
Cc2 = 1/(2*pi*Rc1*Fp3);


%Type 3 Compensator Transfer
Function s = tf('s');
H = tf([(Rc1*Cc1+Rc1*Cc1*Cf3*(Rf1+Rf3)) (1+Cf3*(Rf1+Rf3))],
[(Cc2*Rc1*Cf3*Rf3*Cc1*Rf1) (Cc1*Rf1*Rc1*Cc2+Cc1*Rf1*Rf3*Cf3)
(Cc1*Rf1)
 0 0]);
bode(H)
   ;
```



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Appendix B – Circuit Parameter Decision Table

Inputs	
Vin_max	400
Vin_min	220
D center	0,3
L	0,000047
C	0,000047
fs	100000
L	0,0001

If you use these fs will be your output

If you use these L*C and C will be your output

Outputs	
N1/N2	16
D_max	0,436363636
D_min	0,24
L*C*fs*fs	0,099431818
fs	6709,108765
L*C	9,94318E-12
C	9,94318E-08