The theory behind external DDR3 initialization on the Beaglebone Black

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Introduction

Before proceeding into the details of configuring and initializing the external DDR3 SDRAM on the Beaglebone Black, the theory behind how DDR3 operates, what it entails, and how it is set up generally and specifically with the AM335x processor will first be elaborated. This will provide the opportunity to gain a better understanding of the relationship between the DDR3 memory with the rest of the system.

SDRAM Composition and Operation

DDR3 SDRAM is an abbreviation for the third generation of double data rate synchronous dynamic random-access memory. Breaking down the abbreviation, DRAM is RAM, or random access memory, that is composed of mainly capacitors and transistors. One capacitor and one transistor is all that is needed to store one bit. On the contrary, SRAM can use up to four to six transistors to store one bit. As a result, DRAM can achieve higher densities at a reduced cost compared to SRAM.

How a capacitor in conjunction with a transistor encode a bit is that if a capacitor stores a charge then the value of the bit is 1, otherwise it is 0. DRAM is dynamic in the sense that the capacitors have to be refreshed periodically as the charge stored in the capacitors slowly discharge, or leak, over time.

Unlike DRAM where operations are asynchronous, SDRAM operates on a clock. There are mainly two forms of SDRAMs and those are “single data rate” and “double data rate”. Single data rate SDRAMs can only perform operations at one edge of a clock signal. The “double data rate” term in the abbreviation refers to the fact that data can be transferred at both edges of a clock that is fed into the the DDR3 memory. This effectively doubles the data throughput compared to other conventional memories that transfer data at only one edge of a clock signal (single data rate SDRAMs).

All SDRAMs provide the same set of control signals and bank selection and addressing schemes. There are only a subset of differences introduced in successive generations of SDRAMs.

The control signals that can be found in all SDRAMs are as follows:

SDRAM Control Signals		
Control Signal	**Name**	**Description**
CKE	Clock Enable	This signal is active-high. When not asserted, no commands are interpreted and all other control lines have no effect. It takes one clock cycle for the Clock Enable control signal to take effect, in particular everytime its state is changed.
/CS	Chip Select	The Chip Select control signal is active-low. When not asserted, the SDRAM ignores all inputs with the exception of CKE. The SDRAM will act as if an NOP command was received.
DQM	Data Mask	The Data Mask (DQM) control signal is active-high. When asserted, data I/O is suppressed. As a result, data that is presented to the SDRAM on the data I/O lines are not written during a Write command. In respect to a Read command, if DQM is asserted two cycles before a read cycle, the read data is not outputted
/RAS	Row Address Strobe	Despite the term "Stobe" in the name of the /RAS control signal, this is not a strobe line. The name was inherited by its corresponding control signal in asynchronous DRAMs. This control signal is simply a command bit. Along with /CAS and /WE, this selects one of 8 commands.
/CAS	Column Address Strobe	Just as with /RAS, /CAS also dictates the value of the corresponding command bit. Along with /RAS and /WE, this selects one of 8 commands.
/WE	Write Enable	Along with /RAS and /CAS, this selects one of 8 commands. This generally distinguishes the command from either a a command pertaining to a read or pertaining to a write.

Figure 1. SDRAM Control Signals

SDRAM devices are divided into 2, 4, or 8 independent internal memory banks. To address one of the internal memory banks, up to three bank address inputs (i.e. BA0, BA1, and BA2) are used to select which bank that a particular command should be applied to.

The remaining control inputs are the address inputs that select which row and which column should be addressed within a memory bank.

DDR3 SDRAM on the Beaglebone Black

The latest revision of the Beaglebone Black, which is the one that I have and will be using for this project when porting uMon, is Revision C. The board is integrated with a 512MB DDR3L SDRAM. As specified in the BBB SRM Section 5.3.1, there are two different 512MB DDR3L part numbers and those are the MT41K256M16HA-125 from Micron and the D2516EC4BXGGB from Kingston. On the board that I will be using, it has the 512MB DDR3L from Kingston where the datasheet can be found here.

Some of the specifications of the DDR3L SDRAM is that it has a desity of 4Gbits or 512MB which is divided into 8 banks. Each bank consists of 32M 16-bit words. The page size, which is also known as the number of bytes within a row, is 2KB. Within a single bank, given that there are 64MB within the bank, the number of rows is 64MB / 2KB = 32768 rows. As a result the number of bits required for the row address is 15 bits (A0 to A14). Given that there are 2KB in each row and that the word width is 16-bits, the number of columns in each row is 2KB / 2 bytes (the word width) = 1024 columns. Therefore, the number of bits required for the column address is 10 bits (A0 to A9).

Additional specifications of the DDR3L SDRAM is that it has both sequential and interleaving bursts with burst lengths of 8 and 4 with the Burst Chop (BC) command. Furthermore, both the /CAS latencies for reading and writing are programmable.

DDR3 Reset and Initialization

A specific sequence of steps need to be taken when initialzing DDR3 SDRAM in order to configure the memory properly for use. In the JEDEC DDR3 SDRAM Standard Section 3.3.1, the reset and initialization procedure for DDR3 is concisely enumerated.

In the context of powering up with no prior power supplied to the system (i.e. cold start), the

power-up and initialization sequence is as follows:

1. After applying power, `/RESET` is recommended to be maintained below $0.2 \times V_{DD}$. `/RESET` must be asserted for a minimum of $200\mu s$.
2. Once /RESET is de-asserted, the system must wait for $500\mu s$ until `CKE` becomes active, i.e. “high”. During this time, the DRAM will start the internal state initialization which will be done independently of external clocks.
3. The clock lines `CK` and `/CK`, where the latter clock signal is the inverse of the former, must be started and stabilized for at least $10ns$ or about $5t_{CK}$ before `CKE` goes active. Once `CKE` is “high” after reset, `CKE` needs to be maintained in the “high” state until the initialization sequence is finished. This includes the expiration of t_{DLLK} and t_{ZQinit}.
4. As long as `/RESET` is asserted, the DDR3 SDRAM keeps its on-die termination (`ODT`) in the high-impedance state. ODT is still in the high-impedance state after `/RESET` is de-asserted until `CKE` is “high”. When `CKE` is “high”, the `ODT` input signal may be statically held at either “low” or “high”. If `RTT_NOM` is to be enbled in `MR1`, the `ODT` input signal must be statically held “low”. In all other cases, the `ODT` input signal remains static until the initialization sequence is finished and t_{DLLK} and t_{ZQinit} expire.
5. Once `CKE` is high, the system must wait a minimum of “Reset `CKE` Exit” time, t_{XPR}, before issuing the first `MRS` command to load mode register.
   $t_{XPR} = max(t_{XS}; 5 \times t_{CK})$
6. Issue an `MRS` command to load `MR2` with all application settings. To do this, the bank address bit(s) `BA0` and `BA2` must be “low”, and `BA1` must be “high”.
7. Issue an `MRS` command to load `MR3` with all application settings. To do this, the bank address bit(s) `BA2` must be “low”, and `BA0` and `BA1` must be “high”.
8. Issue an `MRS` command to load `MR1` with all application settings and `DLL` enabled. To do this, the address bit `A0` must be “low”, the bank address bit(s) `BA1` and `BA2` must be “low” and `BA0` must be “high”.
9. Issue an `MRS` command to load `MR0` with all application settings and `DLL reset`. To do this, the address bit `A8` must be “high” and all bank address bits must be “low”.
10. Issue a `ZQCL` command to start ZQ calibration.
11. Wait for both t_{DLLK} and t_{ZQinit} to complete.
12. The DDR3 SDRAM is now ready for normal operation.

DDR3 Mode Registers

DDR3 SDRAMs can be configured based on the application that it is used for. DDR3 provides the capability to configure the various functions, features, and modes which must

be programmed via the Mode Register Set (`MRS`) command. The default values contained within the Mode Registers are not defined and as a result the registers must be initialized and/or re-initialized after power-up and/or reset for proper operation. Additionally, the contents of the Mode Registers can be altered during normal operation with the `MRS` command.

The time between two `MRS` commands, which is also the time required for a write operation to a mode register to complete, is specified by the mode register set command cycle time, t_{MRD}.

AM335x Interface to DDR3 SDRAM

According to the AM335x TRM Section 7.3, the memory subsystem that is used to interface with the DDR3 memory is the EMIF subsystem. The features are specified in detail in Section 7.3.1.1. Some of the notable features are its 16-bit data path to external SDRAM memory, support for DDR3 interface, 1GB of memory addressability, programmable bank/row/column addressing schemes, programmable CAS latencies, programmable page size, programmable burst lengths, and more.

The signals associated with EMIF include a maximum width of 16 bits for the data bus, a maximum width of 16 bits for the address bus with an additional 3 bits for bank selection, differential clock lines, row and column address strobes (RAS and CAS respectively), write enable, data strobe and data mask, chip select, clock enable, and on-die termination.

An illustration of the control signals and the direction of the signals can be found in Figure 7-202 Section 7.3.3.1, and is shown below.

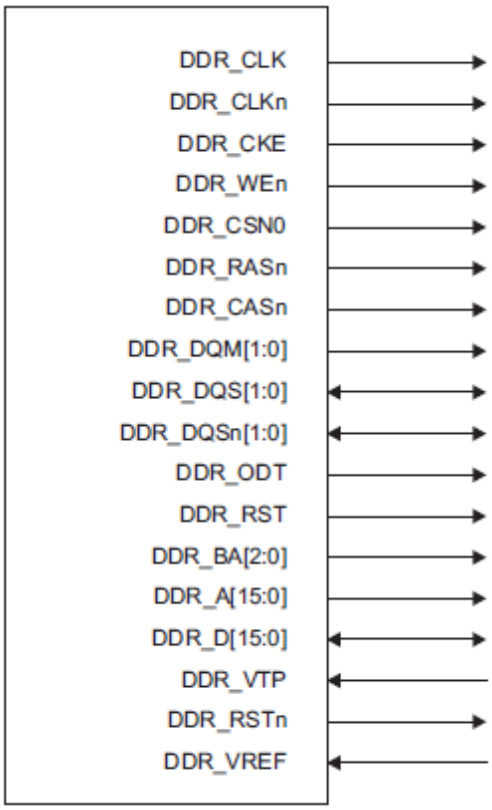

Figure 2. DDR2/3/mDDR Memory Controller Signals

DDR Clock

In order for the DDR memory to operate properly that the EMIF subsystem is interfaced with, the clocks going into the memory must be configured beforehand as specified in Section 7.3.3.2. This clock is derived directly from the DDR PLL's VCO output and is explained in more detail in Section 8.1. With the type of DDR memory that exists on the Beaglebone Black, the maximum frequency that the memory can operate in is 400 MHz as indicated in the features of the AM335x Processors datasheet as well as the BBB SRM, Section 5.3.1 "512 MB DDR3L".

Initializing the DDR3 on the Beaglebone Black

Fortunately, TI has provided an extensive amount of documentation on how to properly configure the DDR3 memory with the AM335x processor found on the Beaglebone Black. To get the DDR3 properly configured, there are three separate components that must be set up. These involve initializing the clocks going into the DDR memory and the clocks involved

in the DDR transactions between the processor and the DDR memory, the EMIF subsystem that determine the characteristics of the DDR, and the DDR PHY regsiters that tune the timing characteristics of all aspects that are involved with the interface.

TI has created a wiki that provides an insight on how to configure the EMIF subsystem and the DDR PHY timing charateristcss. In this wiki, all the information required to set up the AM335x to interface with DDR3 are contained within.

As for the clocks, the major clock subsystem that must be configured properly is the DDR PLL which must be set to provide 400 MHz which is required to drive the DDR3 on the Beaglebone Black. More information about this can be found in the AM335x TRM, Section 8 “ Power, Reset, and Clock Management (PRCM)”.

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This is Jarielle Catbagan's personal website for all things robotics, computers, technology, and science.