GLS,BLOCKING VS NON BLOCKING AND SYNTHESIS SIMULATION MISMATCH

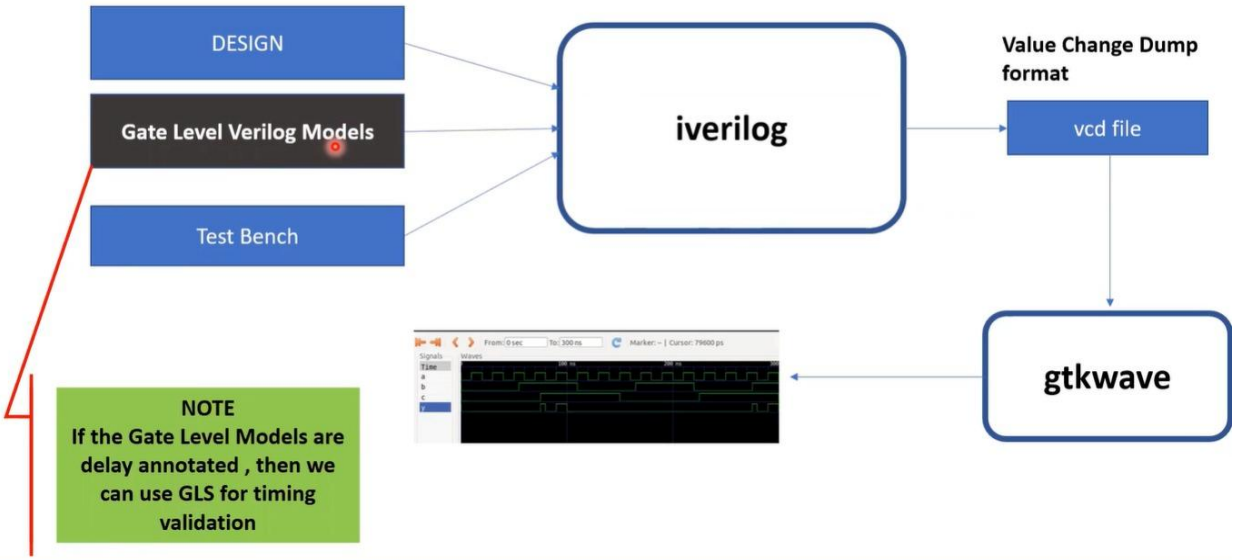
What is GLS

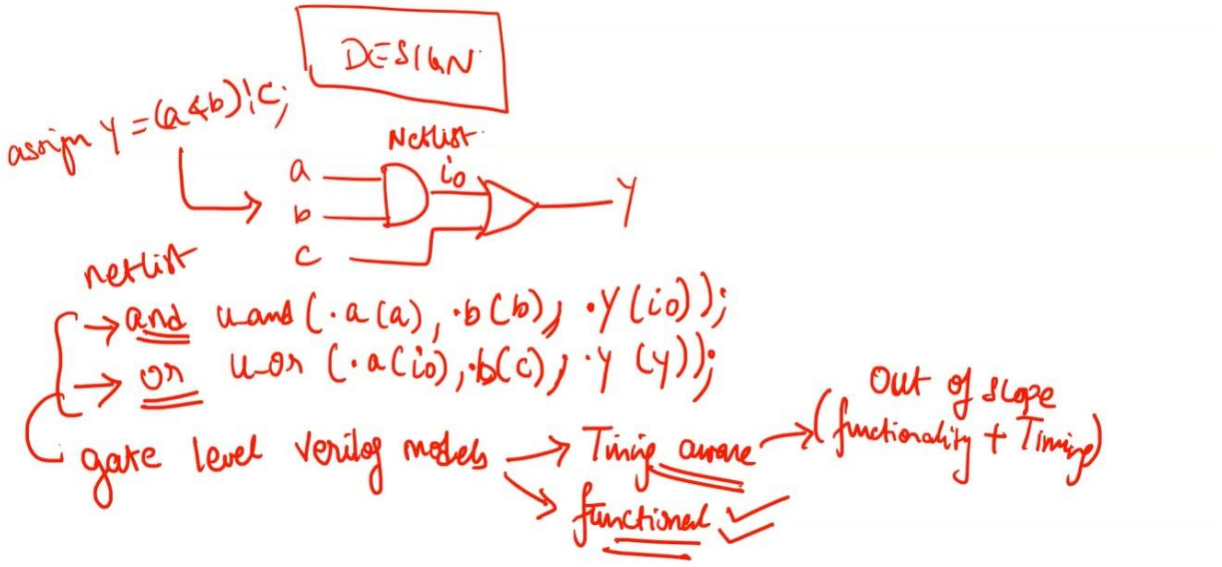
- Running the test bench with Netlist as Design Under Test
- Netlist is logically same as RTL Code.
  - Same Test Bench will align with the Design .

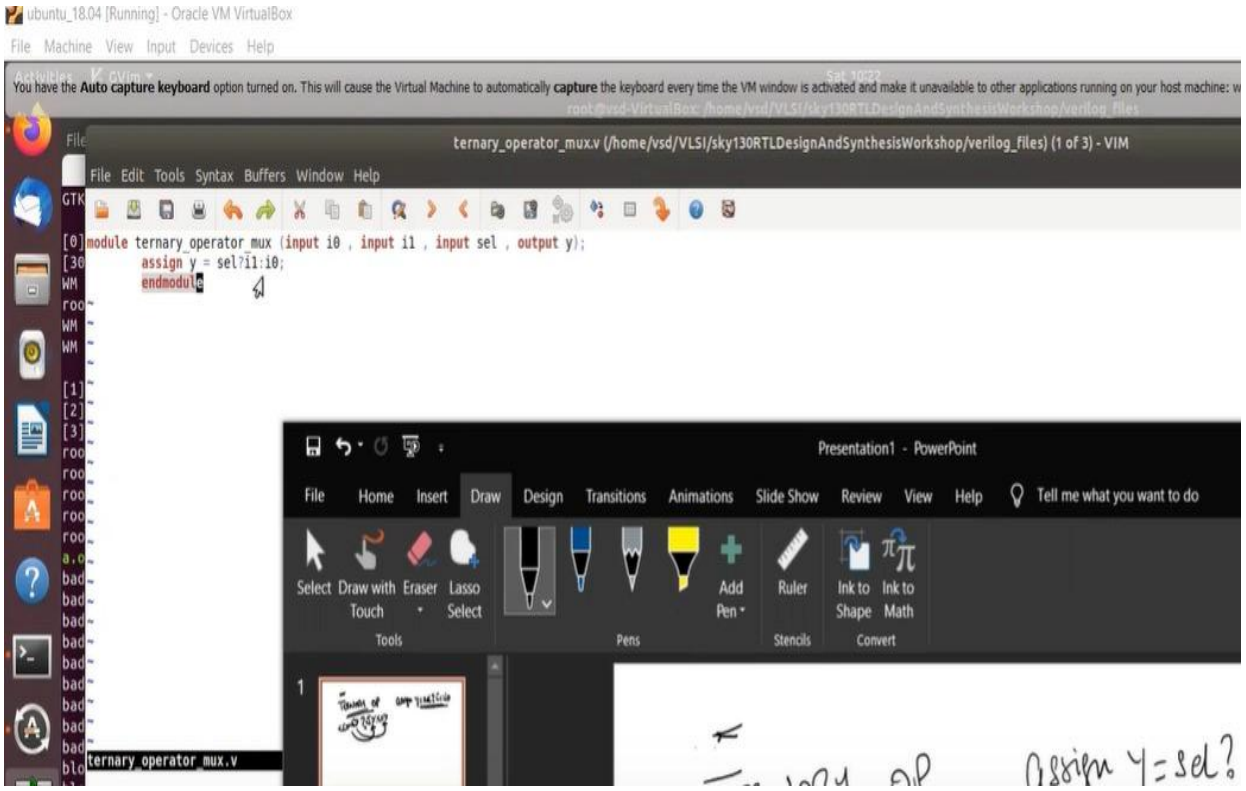
Why GLS

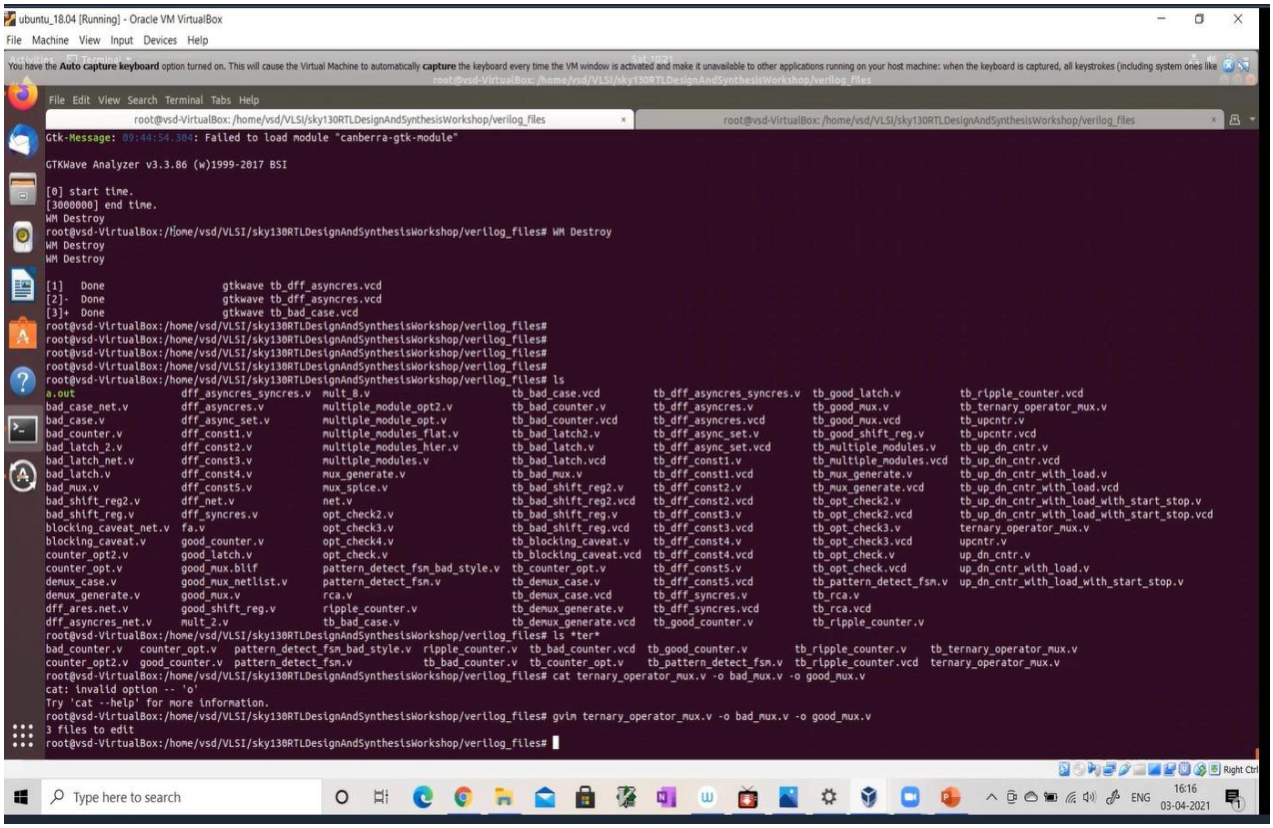
- Verify the logical correctness of design after synthesis
- Ensuring the timing of the design is met.
  - For this GLS needs to be run with delay annotation. (outside the scope of this discussion).

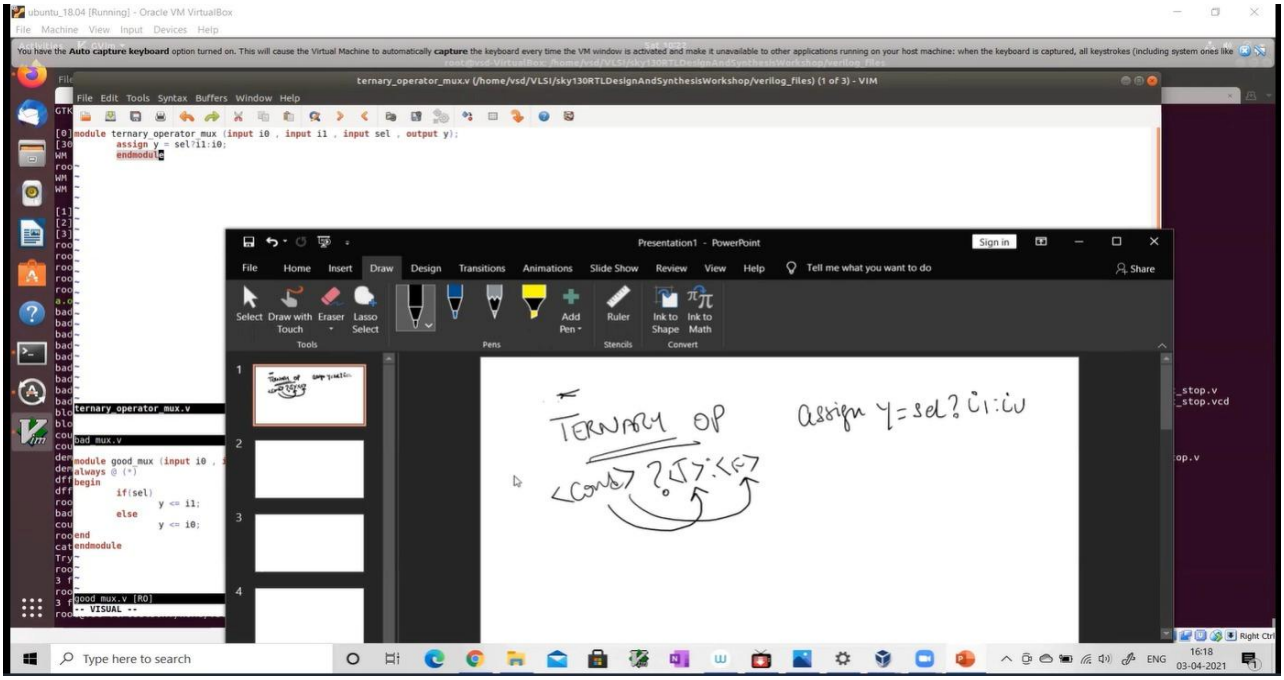
GLS using IVERILOG




DESIGN
assign y = (a & b) | c;
Netlist
io
a
b
c
y
netlist
and u_and (.a(a), .b(b), .y(io));
or u_or (.a(io), .b(c), .y(y));
gate level verilog models
Timing aware
functional
Out of slope
(functionality + Timing)


ubuntu_18.04 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
You have the Auto capture keyboard option turned on. This will cause the Virtual Machine to automatically capture the keyboard every time the VM window is activated and make it unavailable to other applications running on your host machine:
ternary_operator_mux.v (/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files) (1 of 3) - VIM
File Edit Tools Syntax Buffers Window Help
module ternary_operator_mux (input i0 , input i1 , input sel , output y);
assign y = sel?i1:i0;
endmodule
Presentation1 - PowerPoint
File Home Insert Draw Design Transitions Animations Slide Show Review View Help
Tell me what you want to do
Select
Draw with Touch
Eraser
Lasso Select
Add Pen
Ruler
Ink to Shape
Ink to Math
Tools
Pens
Stencils
Convert
ternary_operator_mux.v
assign y = sel?


ubuntu_18.04 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
You have the Auto capture keyboard option turned on. This will cause the Virtual Machine to automatically capture the keyboard every time the VM window is activated and make it unavailable to other applications running on your host machine: when the keyboard is captured, all keystrokes (including system ones like
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
File Edit View Search Terminal Tabs Help
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
Gtk-Message: 09:44:54.304: Failed to load module "canberra-gtk-module"
GTKWave Analyzer v3.3.86 (w)1999-2017 BSI
[0] start time.
[3000000] end time.
WM Destroy
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# WM Destroy
WM Destroy
WM Destroy
[1] Done gtkwave tb_dff_asyncres.vcd
[2]- Done gtkwave tb_dff_asyncres.vcd
[3]+ Done gtkwave tb_bad_case.vcd
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# ls
a.out dff_asyncres_syncres.v mult_8.v tb_bad_case.vcd tb_dff_asyncres_syncres.v tb_good_latch.v tb_ripple_counter.vcd
bad_case_net.v dff_asyncres.v multiple_module_opt2.v tb_bad_counter.v tb_dff_asyncres.v tb_good_mux.v tb_ternary_operator_mux.v
bad_case.v dff_async_set.v multiple_module_opt.v tb_bad_counter.vcd tb_dff_asyncres.vcd tb_good_mux.vcd tb_upcntr.v
bad_counter.v dff_const1.v multiple_modules_flat.v tb_bad_latch2.v tb_dff_async_set.v tb_good_shift_reg.v tb_upcntr.vcd
bad_latch_2.v dff_const2.v multiple_modules_hier.v tb_bad_latch.v tb_dff_async_set.vcd tb_multiple_modules.v tb_up_dn_cntr.v
bad_latch_net.v dff_const3.v multiple_modules.v tb_bad_latch.vcd tb_dff_const1.v tb_multiple_modules.vcd tb_up_dn_cntr.vcd
bad_latch.v dff_const4.v mux_generate.v tb_bad_mux.v tb_dff_const1.vcd tb_mux_generate.v tb_up_dn_cntr_with_load.v
bad_mux.v dff_const5.v mux_spice.v tb_bad_shift_reg2.v tb_dff_const2.v tb_mux_generate.vcd tb_up_dn_cntr_with_load.vcd
bad_shift_reg2.v dff_net.v net.v tb_bad_shift_reg2.vcd tb_dff_const2.vcd tb_opt_check2.v tb_up_dn_cntr_with_load_with_start_stop.v
bad_shift_reg.v dff_syncres.v opt_check2.v tb_bad_shift_reg.v tb_dff_const3.v tb_opt_check2.vcd tb_up_dn_cntr_with_load_with_start_stop.vcd
blocking_caveat_net.v fa.v opt_check3.v tb_bad_shift_reg.vcd tb_dff_const3.vcd tb_opt_check3.v ternary_operator_mux.v
blocking_caveat.v good_counter.v opt_check4.v tb_blocking_caveat.v tb_dff_const4.v tb_opt_check3.vcd upcntr.v
counter_opt2.v good_latch.v opt_check.v tb_blocking_caveat.vcd tb_dff_const4.vcd tb_opt_check.v up_dn_cntr.v
counter_opt.v good_mux.blif pattern_detect_fsm_bad_style.v tb_counter_opt.v tb_dff_const5.v tb_opt_check.vcd up_dn_cntr_with_load.v
demux_case.v good_mux_netlist.v pattern_detect_fsm.v tb_demux_case.v tb_dff_const5.vcd tb_pattern_detect_fsm.v up_dn_cntr_with_load_with_start_stop.v
demux_generate.v good_mux.v rca.v tb_demux_case.vcd tb_dff_syncres.v tb_rca.v
dff_ares.net.v good_shift_reg.v ripple_counter.v tb_demux_generate.v tb_dff_syncres.vcd tb_rca.vcd
dff_asyncres_net.v mult_2.v tb_bad_case.v tb_demux_generate.vcd tb_good_counter.v tb_ripple_counter.v
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# ls *ter*
bad_counter.v counter_opt.v pattern_detect_fsm_bad_style.v ripple_counter.v tb_bad_counter.vcd tb_good_counter.v tb_ripple_counter.v tb_ternary_operator_mux.v
counter_opt2.v good_counter.v pattern_detect_fsm.v tb_bad_counter.v tb_counter_opt.v tb_pattern_detect_fsm.v tb_ripple_counter.vcd ternary_operator_mux.v
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# cat ternary_operator_mux.v -o bad_mux.v -o good_mux.v
cat: invalid option -- 'o'
Try 'cat --help' for more information.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# gvim ternary_operator_mux.v -o bad_mux.v -o good_mux.v
3 files to edit
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#
Right Ctrl
Type here to search
ENG
16:16
03-04-2021


ubuntu_18.04 [Running] - Oracle VM VirtualBox
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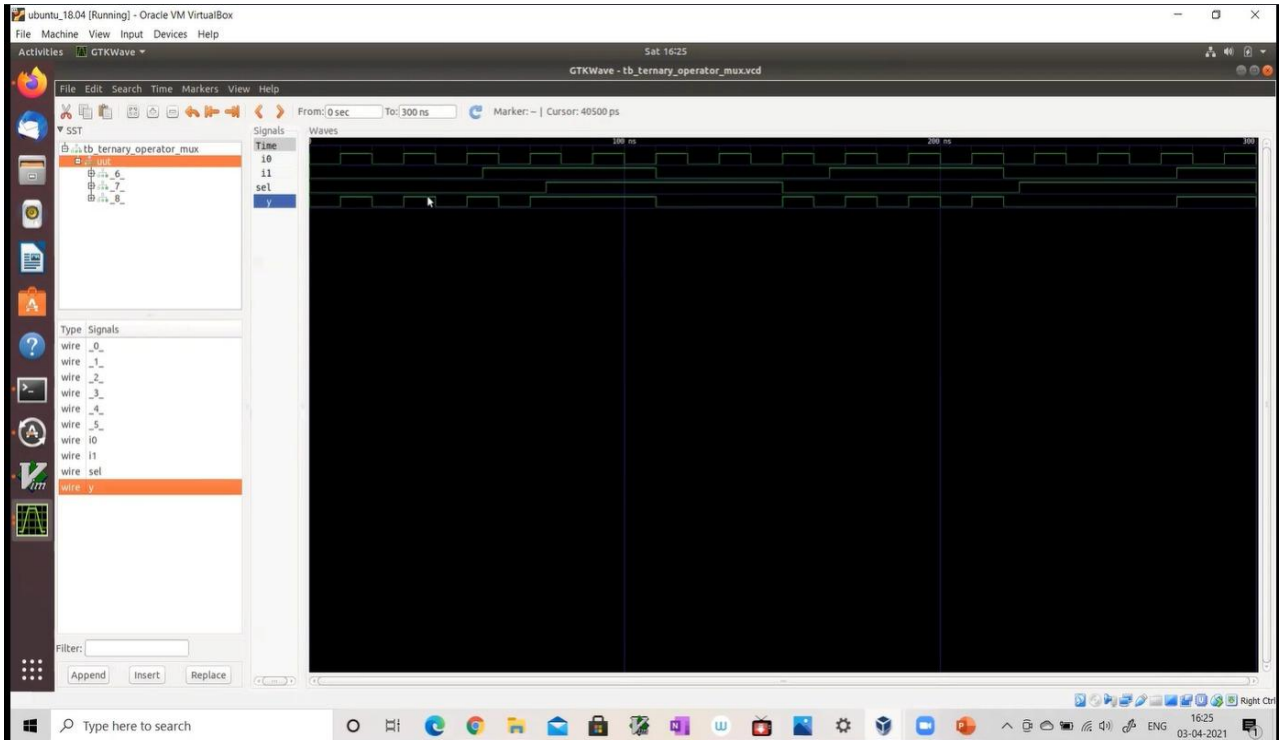
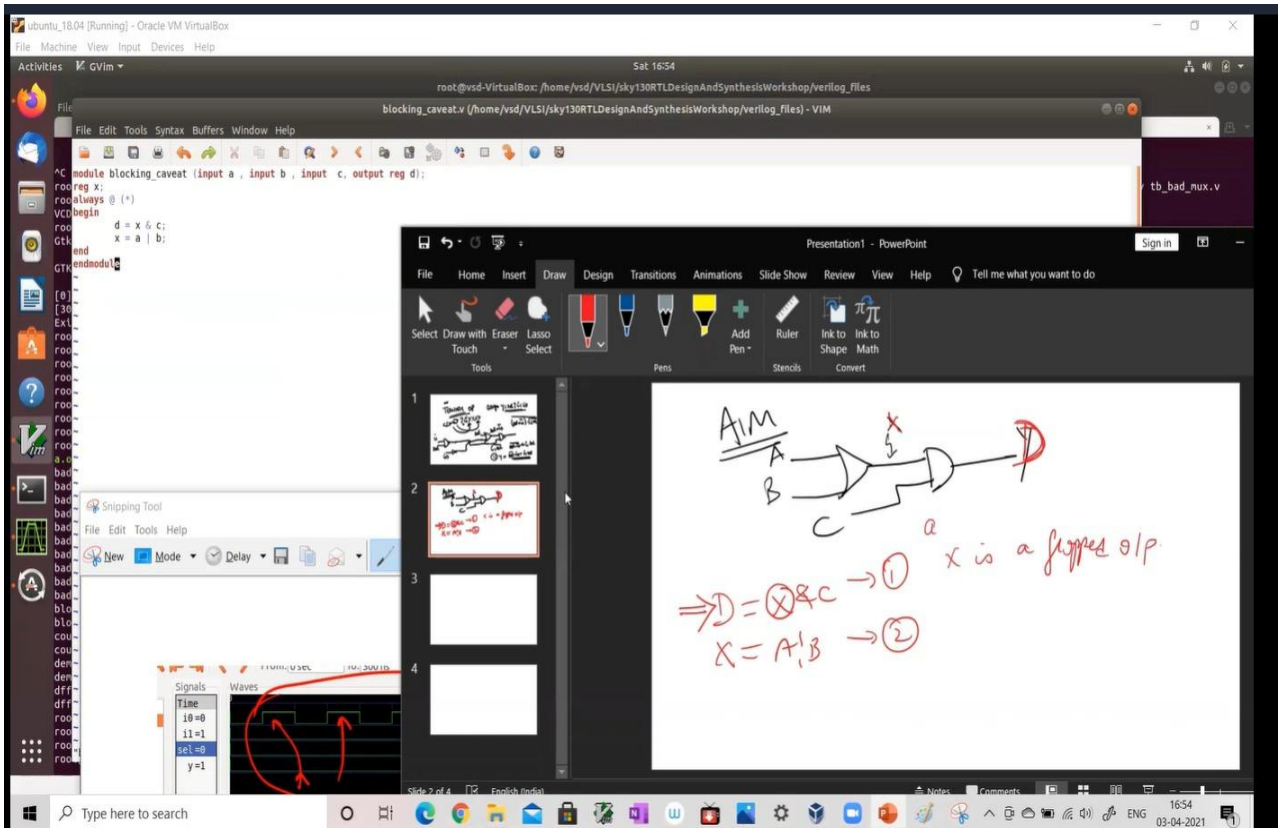
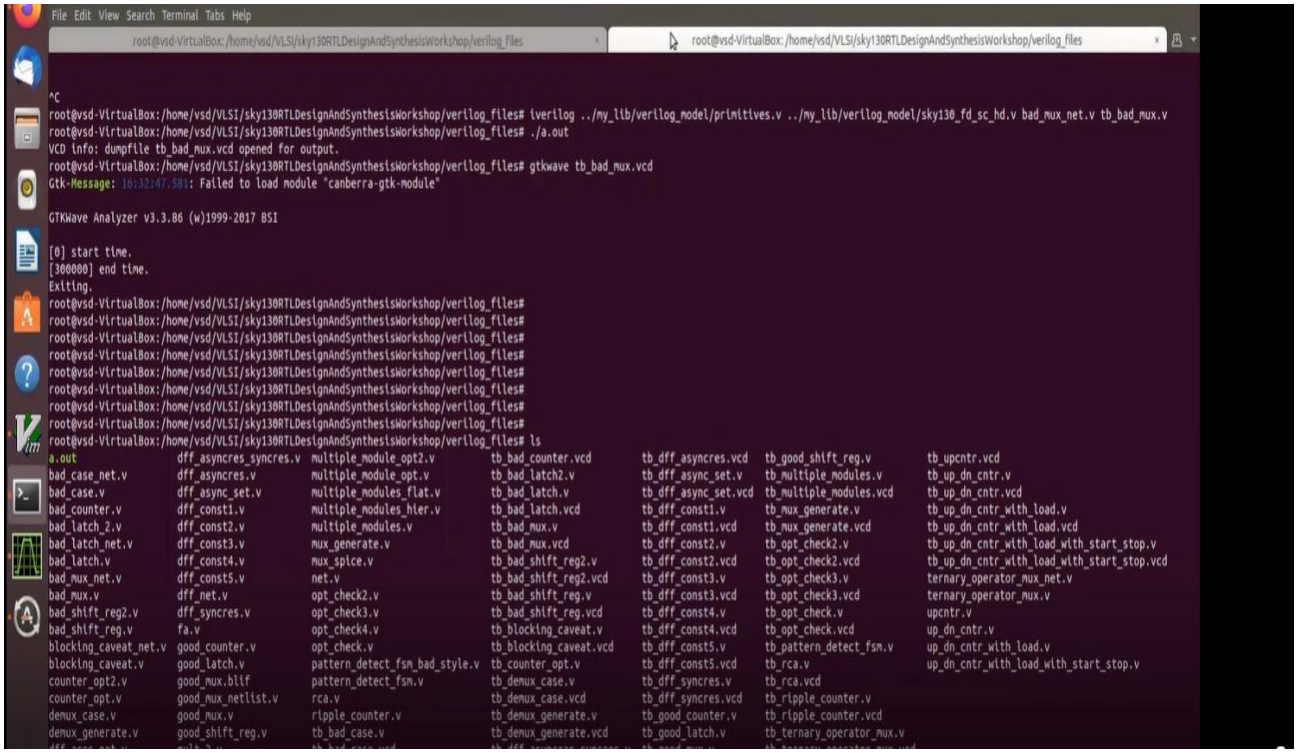
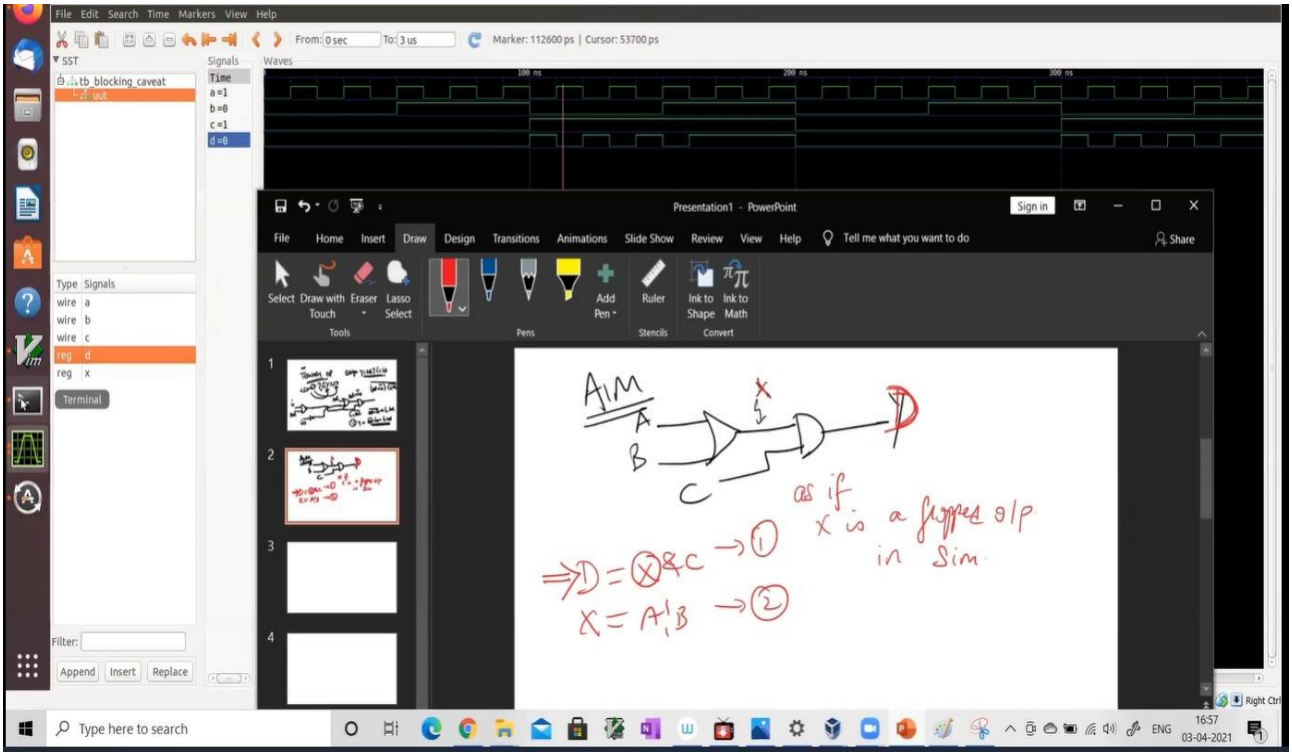
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
ternary_operator_mux.v (/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files) (1 of 3) - VIM
File Edit Tools Syntax Buffers Window Help
module ternary_operator_mux (input i0 , input i1 , input sel , output y);
assign y = sel?i1:i0;
endmodule
ternary_operator_mux.v
bad_mux.v
module good_mux (input i0 ,
always @ (*)
begin
if(sel)
y <= i1;
else
y <= i0;
end
endmodule
good_mux.v [RO]
-- VISUAL --
Presentation1 - PowerPoint
Sign in
File Home Insert Draw Design Transitions Animations Slide Show Review View Help
Tell me what you want to do
Share
Select
Draw with Touch
Eraser
Lasso Select
Add Pen
Ruler
Ink to Shape
Ink to Math
Tools
Pens
Stencils
Convert
TERNARY OP
assign y=sel?i1:i0
Right Ctrl
Type here to search
ENG
16:18
03-04-2021


ubuntu_18.04 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
Activities
GTKWave
Sat 16:25
GTKWave - tb_ternary_operator_mux.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 300 ns
Marker: -- | Cursor: 40500 ps
SST
tb_ternary_operator_mux
Signals
Time
i0
i1
sel
y
Waves
Type Signals
wire _0_
wire _1_
wire _2_
wire _3_
wire _4_
wire _5_
wire i0
wire i1
wire sel
wire y
Filter:
Append
Insert
Replace
Type here to search
ENG
16:25
03-04-2021


ubuntu_18.04 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
Activities
GVim
Sat 16:54
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
blocking_caveat.v (/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files) - VIM
File Edit Tools Syntax Buffers Window Help
module blocking_caveat (input a , input b , input c, output reg d);
reg x;
always @ (*)
begin
d = x & c;
x = a | b;
end
endmodule
tb_bad_mux.v
Presentation1 - PowerPoint
Sign in
File Home Insert Draw Design Transitions Animations Slide Show Review View Help
Tell me what you want to do
Select
Draw with Touch
Eraser
Lasso Select
Add Pen
Ruler
Ink to Shape
Ink to Math
Tools
Pens
Stencils
Convert
Snipping Tool
File Edit Tools Help
New
Mode
Delay
Signals
Waves
Time
i0 =0
i1 =1
sel =0
y =1
AIM
A
B
C
D
X
a
x is a flipped o/p
D = X&C → (1)
X = A'B → (2)
Type here to search
ENG
16:54
03-04-2021


File Edit View Search Terminal Tabs Help
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
^C
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog ../my_lib/verilog_model/primitives.v ../my_lib/verilog_model/sky130_fd_sc_hd.v bad_mux_net.v tb_bad_mux.v
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_bad_mux.vcd opened for output.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# gtkwave tb_bad_mux.vcd
Gtk-Message: 16:32:47.581: Failed to load module "canberra-gtk-module"
GTKWave Analyzer v3.3.86 (w)1999-2017 BSI
[0] start time.
[300000] end time.
Exiting.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# ls
a.out
bad_case_net.v
bad_case.v
bad_counter.v
bad_latch_2.v
bad_latch_net.v
bad_latch.v
bad_mux_net.v
bad_mux.v
bad_shift_reg2.v
bad_shift_reg.v
blocking_caveat_net.v
blocking_caveat.v
counter_opt2.v
counter_opt.v
demux_case.v
demux_generate.v
dff_asyncres_syncres.v
dff_asyncres.v
dff_async_set.v
dff_const1.v
dff_const2.v
dff_const3.v
dff_const4.v
dff_const5.v
dff_net.v
dff_syncres.v
fa.v
good_counter.v
good_latch.v
good_mux.blif
good_mux_netlist.v
good_mux.v
good_shift_reg.v
multiple_module_opt2.v
multiple_module_opt.v
multiple_modules_flat.v
multiple_modules_hier.v
multiple_modules.v
mux_generate.v
mux_spice.v
net.v
opt_check2.v
opt_check3.v
opt_check4.v
opt_check.v
pattern_detect_fsm_bad_style.v
pattern_detect_fsm.v
rca.v
ripple_counter.v
tb_bad_case.v
tb_bad_counter.vcd
tb_bad_latch2.v
tb_bad_latch.v
tb_bad_latch.vcd
tb_bad_mux.v
tb_bad_mux.vcd
tb_bad_shift_reg2.v
tb_bad_shift_reg2.vcd
tb_bad_shift_reg.v
tb_bad_shift_reg.vcd
tb_blocking_caveat.v
tb_blocking_caveat.vcd
tb_counter_opt.v
tb_demux_case.v
tb_demux_case.vcd
tb_demux_generate.v
tb_demux_generate.vcd
tb_dff_asyncres.vcd
tb_dff_async_set.v
tb_dff_async_set.vcd
tb_dff_const1.v
tb_dff_const1.vcd
tb_dff_const2.v
tb_dff_const2.vcd
tb_dff_const3.v
tb_dff_const3.vcd
tb_dff_const4.v
tb_dff_const4.vcd
tb_dff_const5.v
tb_dff_const5.vcd
tb_dff_syncres.v
tb_dff_syncres.vcd
tb_good_counter.v
tb_good_latch.v
tb_good_shift_reg.v
tb_multiple_modules.v
tb_multiple_modules.vcd
tb_mux_generate.v
tb_mux_generate.vcd
tb_opt_check2.v
tb_opt_check2.vcd
tb_opt_check3.v
tb_opt_check3.vcd
tb_opt_check.v
tb_opt_check.vcd
tb_pattern_detect_fsm.v
tb_rca.v
tb_rca.vcd
tb_ripple_counter.v
tb_ripple_counter.vcd
tb_ternary_operator_mux.v
tb_upcntr.vcd
tb_up_dn_cntr.v
tb_up_dn_cntr.vcd
tb_up_dn_cntr_with_load.v
tb_up_dn_cntr_with_load.vcd
tb_up_dn_cntr_with_load_with_start_stop.v
tb_up_dn_cntr_with_load_with_start_stop.vcd
ternary_operator_mux_net.v
ternary_operator_mux.v
upcntr.v
up_dn_cntr.v
up_dn_cntr_with_load.v
up_dn_cntr_with_load_with_start_stop.v


File Edit Search Time Markers View Help
From: 0 sec
To: 3 us
Marker: 112600 ps | Cursor: 53700 ps
SST
tb_blocking_caveat
uut
Signals
Time
a=1
b=0
c=1
d=0
Waves
Type Signals
wire a
wire b
wire c
reg d
reg x
Terminal
Filter:
Append
Insert
Replace
Presentation1 - PowerPoint
Sign in
File
Home
Insert
Draw
Design
Transitions
Animations
Slide Show
Review
View
Help
Tell me what you want to do
Share
Select
Draw with Touch
Eraser
Lasso Select
Add Pen
Ruler
Ink to Shape
Ink to Math
Tools
Pens
Stencils
Convert
AIM
A
B
C
X
D
as if x is a flopped o/p in Sim
D = X & C → (1)
X = A ! B → (2)
Type here to search
ENG
16:57
03-04-2021