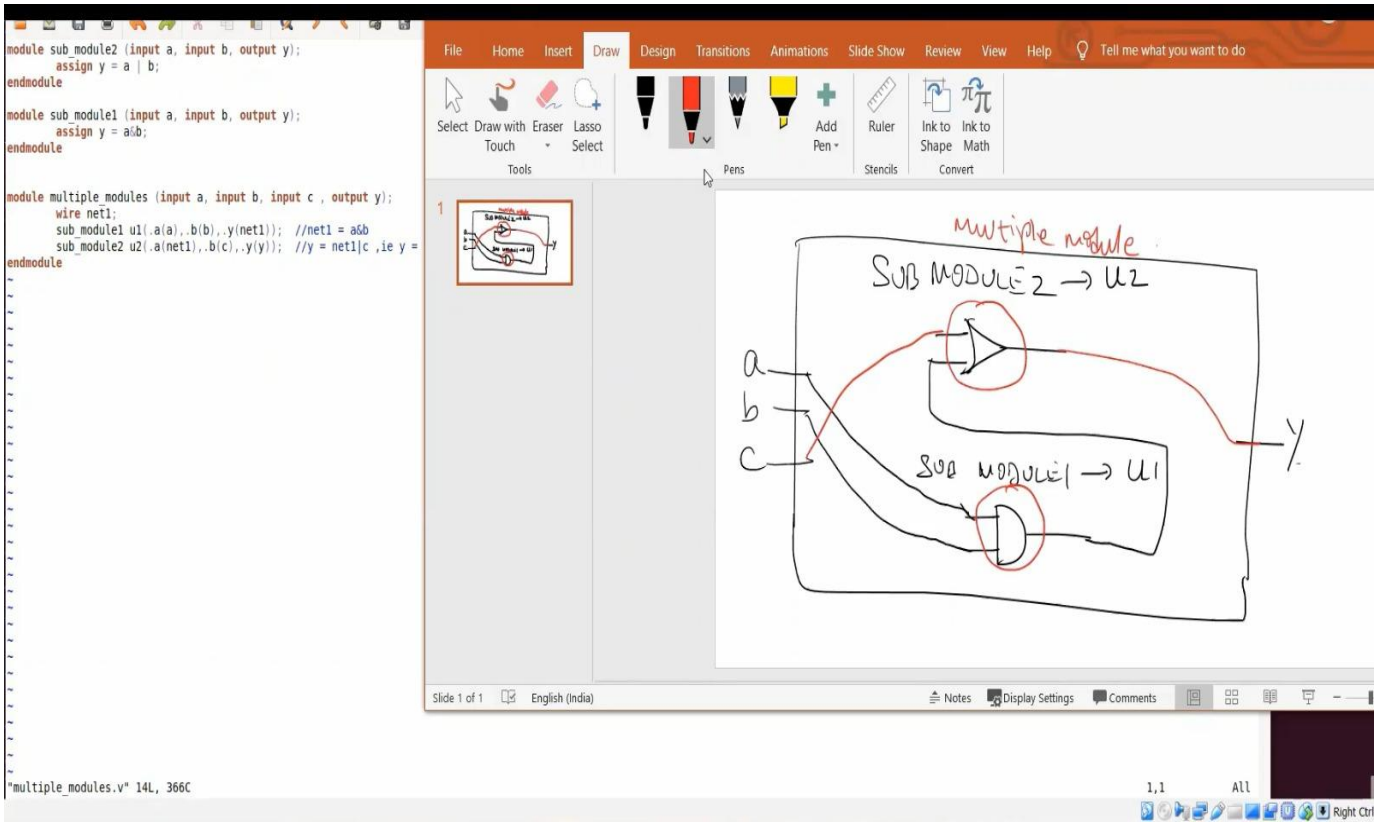
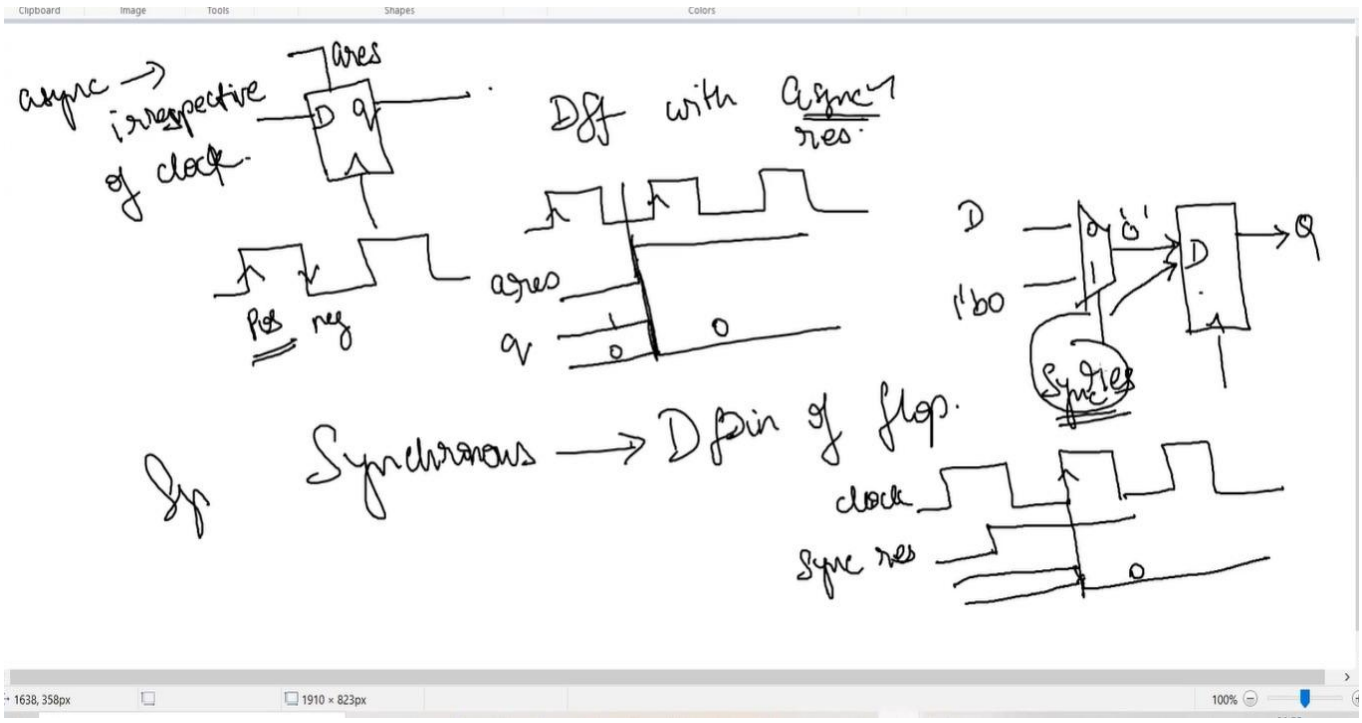
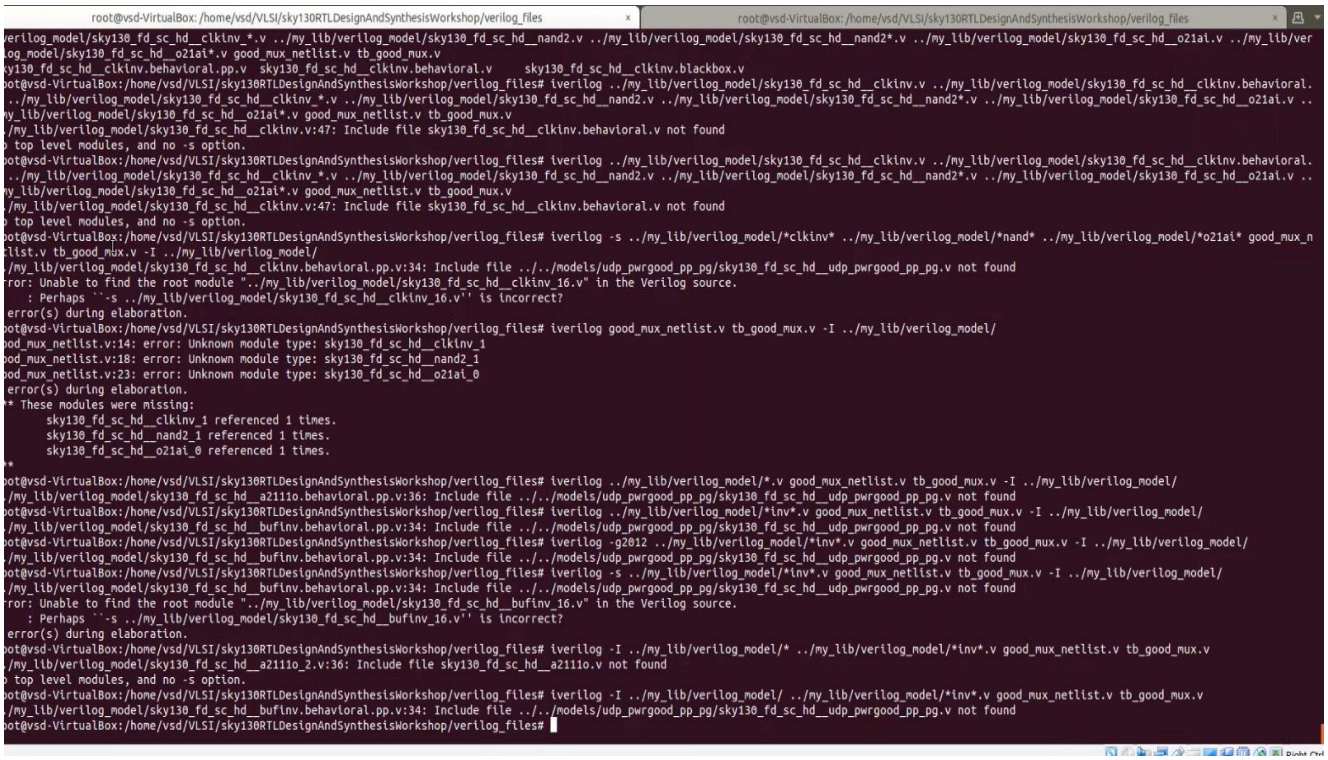
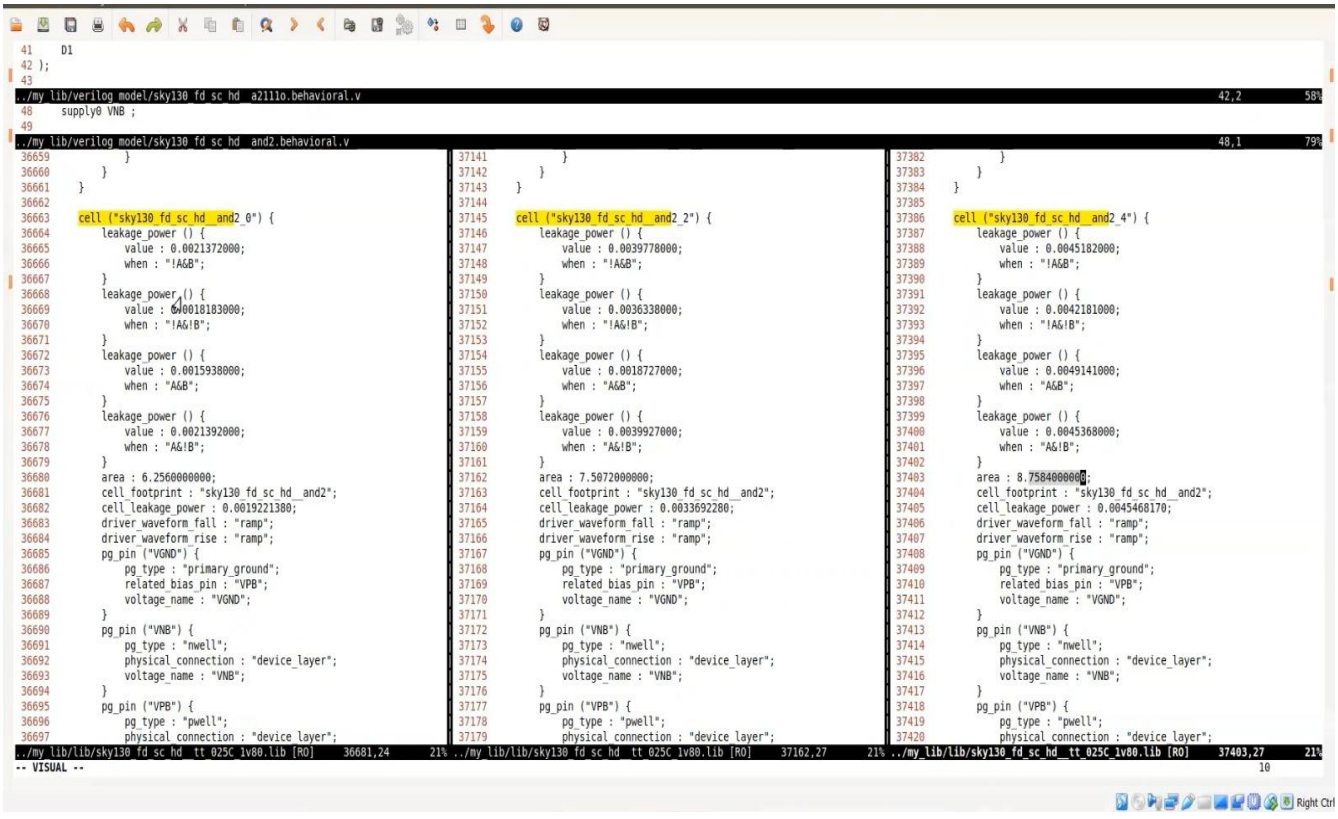
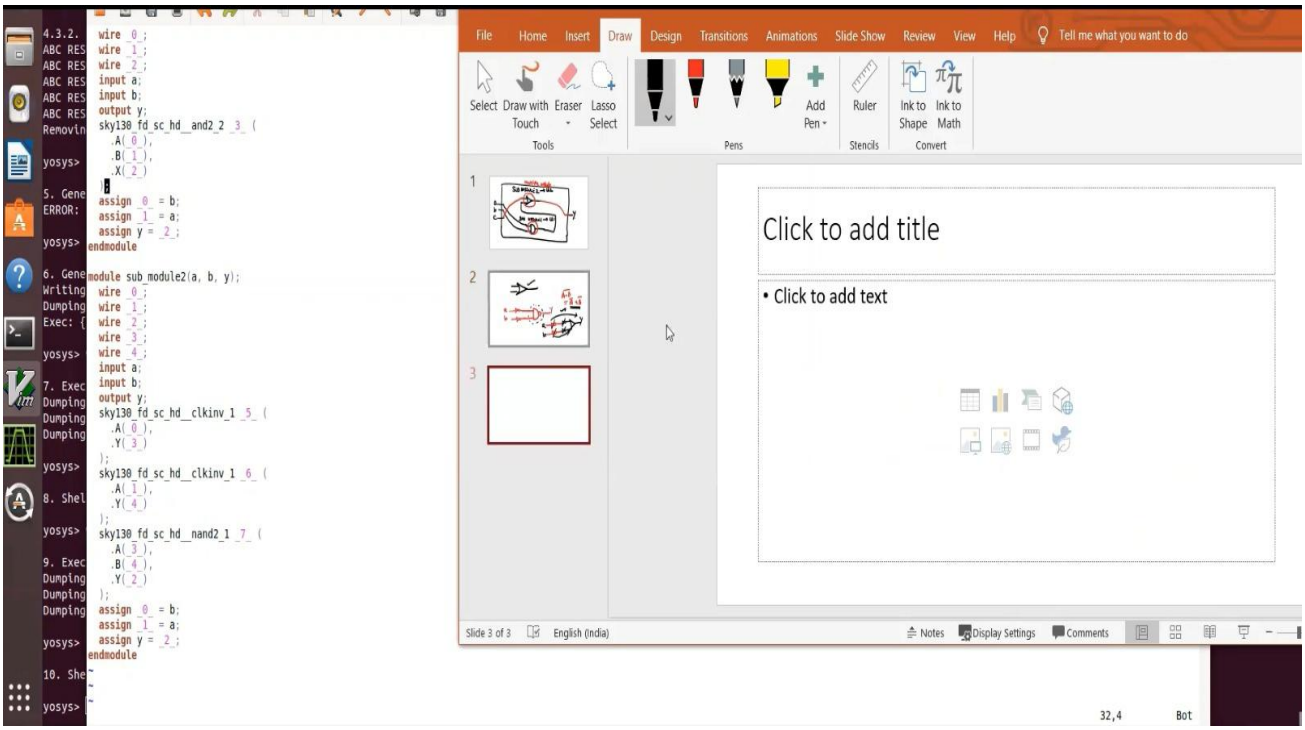
TIMING LIBS, HEIRACHICAL VS FLAT SYNTHESIS AND EFFICIENT FLOP CODING STYLES

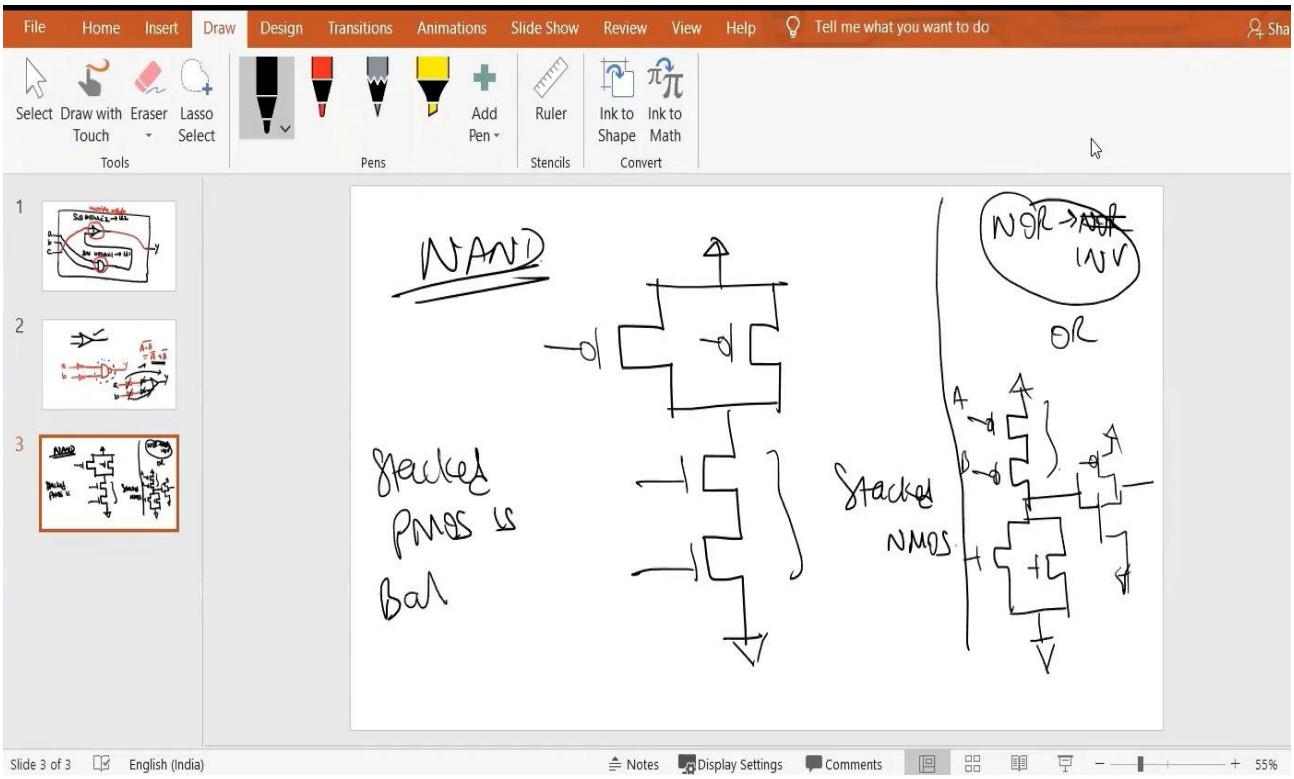


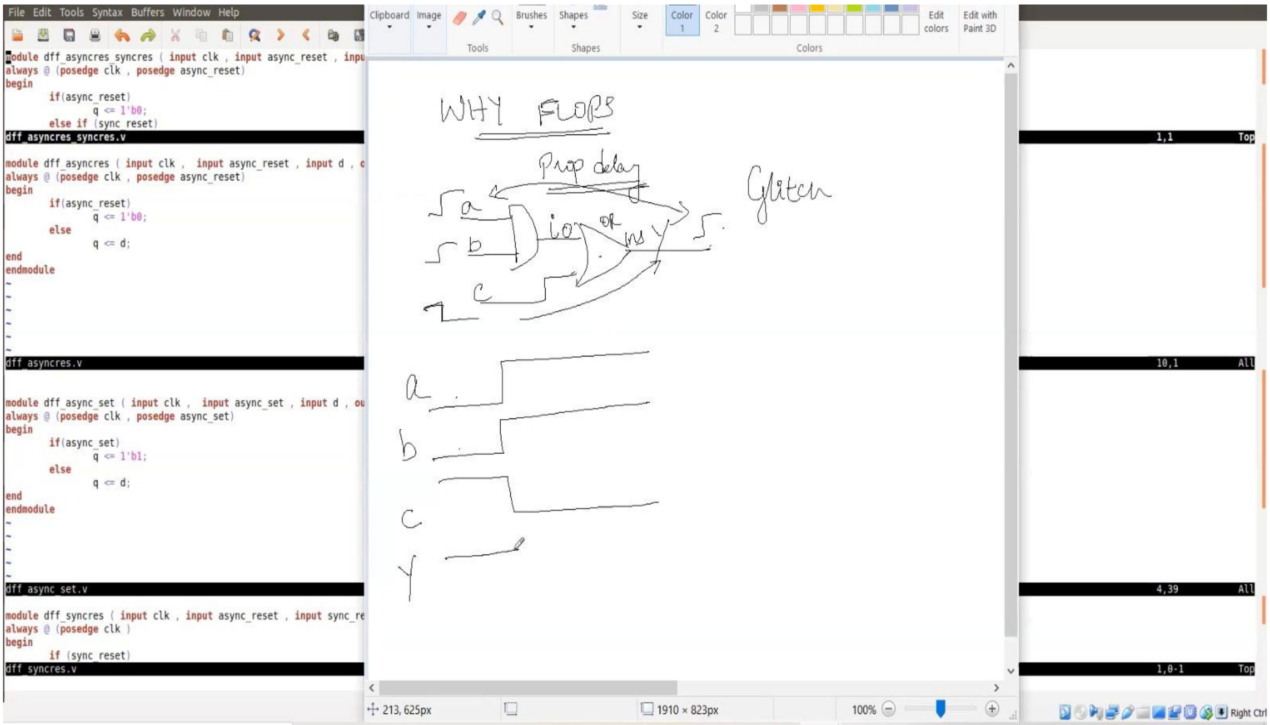


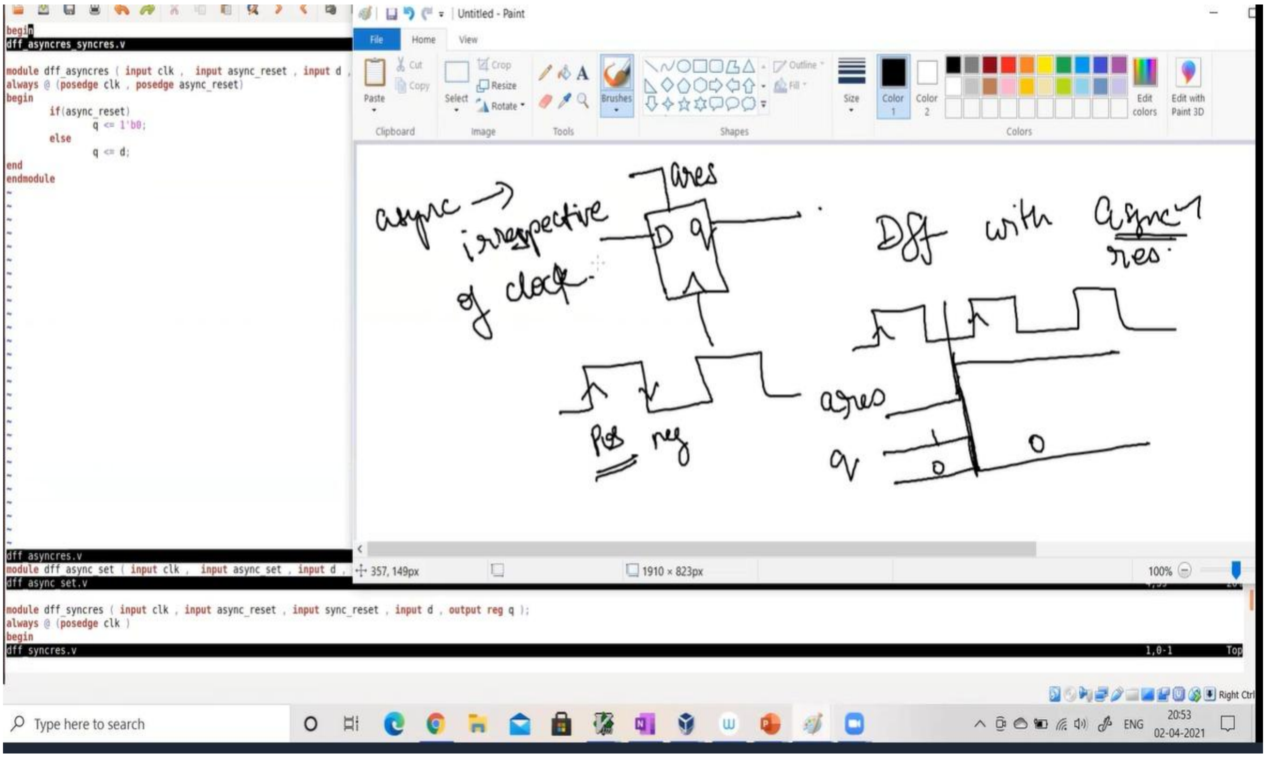

root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
root@vsd-VirtualBox: /home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog ../my_lib/verilog_model/sky130_fd_sc_hd__clkinv.v ../my_lib/verilog_model/sky130_fd_sc_hd__clkinv.behavioral.
../my_lib/verilog_model/sky130_fd_sc_hd__clkinv_*.v ../my_lib/verilog_model/sky130_fd_sc_hd__nand2.v ../my_lib/verilog_model/sky130_fd_sc_hd__nand2*.v ../my_lib/verilog_model/sky130_fd_sc_hd__o21ai.v ..
my_lib/verilog_model/sky130_fd_sc_hd__o21ai*.v good_mux_netlist.v tb_good_mux.v
../my_lib/verilog_model/sky130_fd_sc_hd__clkinv.v:47: Include file sky130_fd_sc_hd__clkinv.behavioral.v not found
0 top level modules, and no -s option.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog -s ../my_lib/verilog_model/*clkinv* ../my_lib/verilog_model/*nand* ../my_lib/verilog_model/*o21ai* good_mux_n
etlist.v tb_good_mux.v -I ../my_lib/verilog_model/
../my_lib/verilog_model/sky130_fd_sc_hd__clkinv.behavioral.pp.v:34: Include file ../../models/udp_pwrgood_pp_pg/sky130_fd_sc_hd__udp_pwrgood_pp_pg.v not found
Error: Unable to find the root module "../my_lib/verilog_model/sky130_fd_sc_hd__clkinv_16.v" in the Verilog source.
: Perhaps ``-s ../my_lib/verilog_model/sky130_fd_sc_hd__clkinv_16.v'' is incorrect?
1 error(s) during elaboration.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog good_mux_netlist.v tb_good_mux.v -I ../my_lib/verilog_model/
good_mux_netlist.v:14: error: Unknown module type: sky130_fd_sc_hd__clkinv_1
good_mux_netlist.v:18: error: Unknown module type: sky130_fd_sc_hd__nand2_1
good_mux_netlist.v:23: error: Unknown module type: sky130_fd_sc_hd__o21ai_0
3 error(s) during elaboration.
** These modules were missing:
sky130_fd_sc_hd__clkinv_1 referenced 1 times.
sky130_fd_sc_hd__nand2_1 referenced 1 times.
sky130_fd_sc_hd__o21ai_0 referenced 1 times.
**
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog ../my_lib/verilog_model/*.v good_mux_netlist.v tb_good_mux.v -I ../my_lib/verilog_model/
../my_lib/verilog_model/sky130_fd_sc_hd__a2111o.behavioral.pp.v:36: Include file ../../models/udp_pwrgood_pp_pg/sky130_fd_sc_hd__udp_pwrgood_pp_pg.v not found
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog ../my_lib/verilog_model/*inv*.v good_mux_netlist.v tb_good_mux.v -I ../my_lib/verilog_model/
../my_lib/verilog_model/sky130_fd_sc_hd__bufinv.behavioral.pp.v:34: Include file ../../models/udp_pwrgood_pp_pg/sky130_fd_sc_hd__udp_pwrgood_pp_pg.v not found
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog -g2012 ../my_lib/verilog_model/*inv*.v good_mux_netlist.v tb_good_mux.v -I ../my_lib/verilog_model/
../my_lib/verilog_model/sky130_fd_sc_hd__bufinv.behavioral.pp.v:34: Include file ../../models/udp_pwrgood_pp_pg/sky130_fd_sc_hd__udp_pwrgood_pp_pg.v not found
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog -s ../my_lib/verilog_model/*inv*.v good_mux_netlist.v tb_good_mux.v -I ../my_lib/verilog_model/
../my_lib/verilog_model/sky130_fd_sc_hd__bufinv.behavioral.pp.v:34: Include file ../../models/udp_pwrgood_pp_pg/sky130_fd_sc_hd__udp_pwrgood_pp_pg.v not found
Error: Unable to find the root module "../my_lib/verilog_model/sky130_fd_sc_hd__bufinv_16.v" in the Verilog source.
: Perhaps ``-s ../my_lib/verilog_model/sky130_fd_sc_hd__bufinv_16.v'' is incorrect?
1 error(s) during elaboration.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog -I ../my_lib/verilog_model/* ../my_lib/verilog_model/*inv*.v good_mux_netlist.v tb_good_mux.v
../my_lib/verilog_model/sky130_fd_sc_hd__a2111o_2.v:36: Include file sky130_fd_sc_hd__a2111o.v not found
0 top level modules, and no -s option.
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog -I ../my_lib/verilog_model/ ../my_lib/verilog_model/*inv*.v good_mux_netlist.v tb_good_mux.v
../my_lib/verilog_model/sky130_fd_sc_hd__bufinv.behavioral.pp.v:34: Include file ../../models/udp_pwrgood_pp_pg/sky130_fd_sc_hd__udp_pwrgood_pp_pg.v not found
root@vsd-VirtualBox:/home/vsd/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files#


../my_lib/verilog_model/sky130_fd_sc_hd__a2111o.behavioral.v
../my_lib/verilog_model/sky130_fd_sc_hd__and2.behavioral.v
cell ("sky130_fd_sc_hd__and2_0") {
cell ("sky130_fd_sc_hd__and2_2") {
cell ("sky130_fd_sc_hd__and2_4") {
../my_lib/lib/sky130_fd_sc_hd__tt_025C_1v80.lib [RO]
-- VISUAL --


wire _0_;
wire _1_;
wire _2_;
input a;
input b;
output y;
sky130_fd_sc_hd__and2_2 _3_ (
.A(_0_),
.B(_1_),
.X(_2_)
);
assign _0_ = b;
assign _1_ = a;
assign y = _2_;
endmodule
module sub_module2(a, b, y);
wire _0_;
wire _1_;
wire _2_;
wire _3_;
wire _4_;
input a;
input b;
output y;
sky130_fd_sc_hd__clkinv_1 _5_ (
.A(_0_),
.Y(_3_)
);
sky130_fd_sc_hd__clkinv_1 _6_ (
.A(_1_),
.Y(_4_)
);
sky130_fd_sc_hd__nand2_1 _7_ (
.A(_3_),
.B(_4_),
.Y(_2_)
);
assign _0_ = b;
assign _1_ = a;
assign y = _2_;
endmodule
File Home Insert Draw Design Transitions Animations Slide Show Review View Help
Tell me what you want to do
Select
Draw with Touch
Eraser
Lasso Select
Tools
Add Pen
Pens
Ruler
Stencils
Ink to Shape
Ink to Math
Convert
Click to add title
• Click to add text
Slide 3 of 3
English (India)
Notes
Display Settings
Comments
32,4
Bot


File Home Insert Draw Design Transitions Animations Slide Show Review View Help
Tell me what you want to do
Select
Draw with Touch
Eraser
Lasso Select
Tools
Add Pen
Pens
Ruler
Stencils
Ink to Shape
Ink to Math
Convert
NAND
Stacked PMOS is Bad
NOR → INV
OR
Stacked NMOS
Slide 3 of 3
English (India)
Notes
Display Settings
Comments
55%


File Edit Tools Syntax Buffers Window Help
module dff_asyncres_syncres (input clk , input async_reset ,
always @ (posedge clk , posedge async_reset)
begin
if(async_reset)
q <= 1'b0;
else if (sync_reset)
dff_asyncres_syncres.v
module dff_asyncres (input clk , input async_reset , input d ,
always @ (posedge clk , posedge async_reset)
begin
if(async_reset)
q <= 1'b0;
else
q <= d;
end
endmodule
dff_asyncres.v
module dff_async_set (input clk , input async_set , input d ,
always @ (posedge clk , posedge async_set)
begin
if(async_set)
q <= 1'b1;
else
q <= d;
end
endmodule
dff_async_set.v
module dff_syncres (input clk , input async_reset , input sync_re
always @ (posedge clk)
begin
if (sync_reset)
dff_syncres.v
WHY FLOPS
Prop delay
Glitch
a
b
c
y
1910 × 823px
100%


Untitled - Paint
begin
dff_asyncres_syncres.v
module dff_asyncres (input clk , input async_reset , input d ,
always @ (posedge clk , posedge async_reset)
begin
if(async_reset)
q <= 1'b0;
else
q <= d;
end
endmodule
dff_asyncres.v
module dff_async_set (input clk , input async_set , input d ,
dff_async_set.v
module dff_syncres (input clk , input async_reset , input sync_reset , input d , output reg q);
always @ (posedge clk)
begin
dff_syncres.v
async → irrespective of clock.
ares
D q
Pos neg
Dff with async res.
ares
q
0
1910 × 823px
Type here to search
20:53
02-04-2021