Design of 1-bit Full Adder using CMOS

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***Abstract*—A full adder is a combinational circuit that forms the arithmetic sum of three bits, that is, two single-bit binary values with a carry input. In this work, 1-bit full adder is to be realized using conventional CMOS design style due to its robustness and scalability at low supply voltages. The transistor-level design of 1-bit full adder consisting of 28 MOSFET transistors is implemented in 28nm CMOS technology using Synopsys Custom Compiler Platform.**

Keywords—full adder, CMOS, 28nm technology

I. CIRCUIT DETAILS

Arithmetic operations are used extensively in most VLSI applications, such as digital signal processing, image and video processing, and microprocessors. The most widely utilised operations include addition, subtraction, multiplication, and multiply and accumulate (MAC). All of these modules are built around the 1-bit full-adder cell.

A full adder is a circuit that creates two outputs, a sum and a carry, by adding two single-bit binary values with a carry input [1]. The truth table of the full adder taken from [2] is listed in Fig. 1. The sum and carry_out signals of the full adder are defined as the following two combinational Boolean functions of the three input variables A, B and C.

$$\text{sum} = A \text{ exor } B \text{ exor } C \quad (1)$$

$$\text{carry\_out} = AB + AC + BC \quad (2)$$

Instead of realizing the two functions separately, the sum output is generated using the carry out signal. As a result of this implementation, the circuit complexity will be reduced, and chip space will be saved.

INPUT			OUTPUT	
A	B	C	carry_out	sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig. 1. Truth table of full-adder.

Fig. 2 shows the transistor-level design of the CMOS 1-bit full adder circuit. The circuit is realized in conventional CMOS design style using a total of 28 MOSFET transistors consisting of 14 NMOS and 14 PMOS transistors. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes [4]. The circuit is to be implemented in 28nm CMOS technology using Synopsys Custom Compiler. Fig 3 shows the testbench circuit created for simulation. The input and output voltage waveforms of the 1-bit CMOS full adder obtained from simulation using PrimeWave are shown Fig. 3.

II. CIRCUIT DESIGN

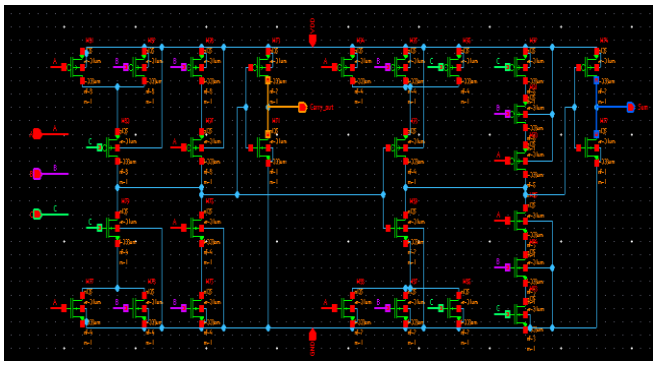

Fig. 2. Transistor level schematic of 1-bit full-adder using CMOS.

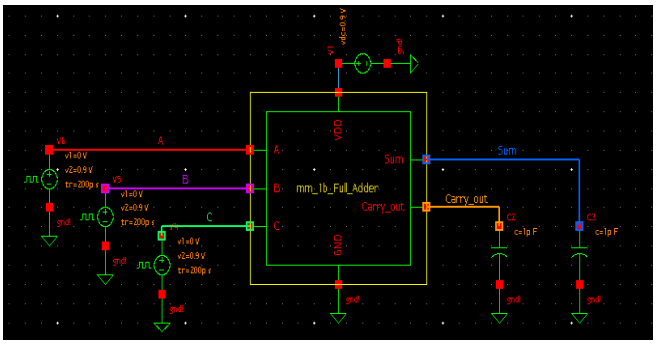

Fig. 3. Testbench circuit for simulatio

III. RESULTANT WAVEFORM

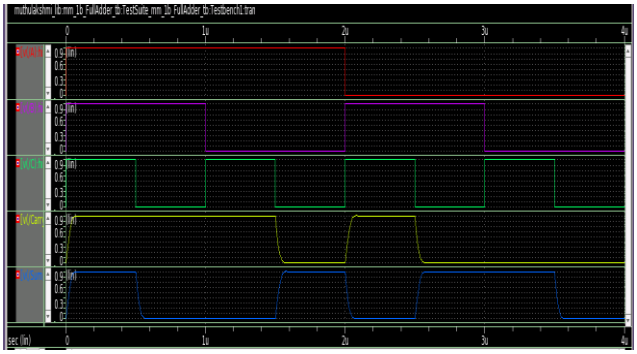

Fig. 4. Input and output waveforms of CMOS 1-bit full-adder circuit.

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