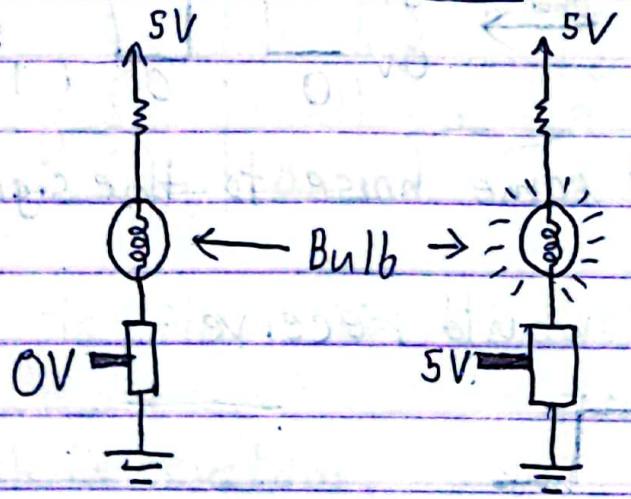
Transistors:

* They are 3 terminal devices, (Input, Output and Control).
* The I-V characteristics of this device can be changed by using the control terminal.
* 2 types of Transistors:

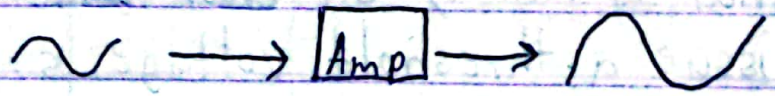
① BJT - Bipolar Junction Transistor
② MOSFET - Metal Oxide Semi-conductor Field Effect Transistor

Application of Transistors:

① Switch:



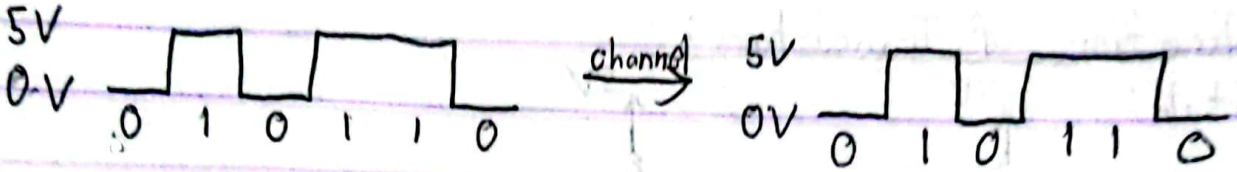
② Logic gates: AND, OR, NOT, NAND, NOR

③ Amplifiers: 

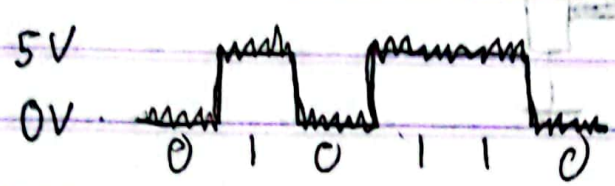
* Binary → 2 states
  x, y
  0 (False) 1 (True)

Voltage	Current	Diode State	Resistance
1 → 5V, 0V	1 → 6mA	1 → ON	1 → low res
0 → 0V, 3.3V	0 → 3mA	0 → OFF	0 → high "

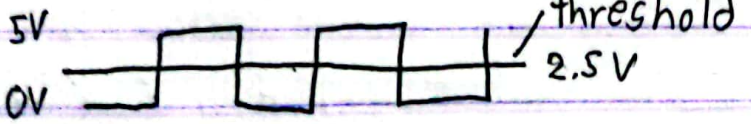
* Sender → 010110



- The channel may add some noise to the signal being sent.
- Therefore the receiver would receive:-



- ∴ Having just 2 levels of signal would cause problem as the received signal is nearly at 0V or 5V level.
- To solve this issue a threshold voltage is considered



- If at a point the voltage is above the threshold voltage it will be considered 5V and vice versa.

  $V_{received}$ (Vr) $< 2.5 \Rightarrow 0, 0V$

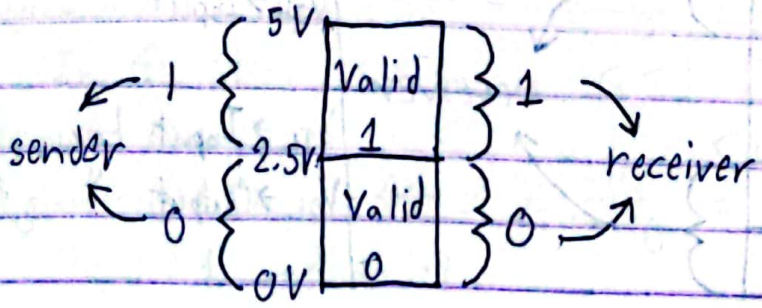
  $(Vr) > 2.5 \Rightarrow 1, 5V$

Static Discipline:

* Specification for digital devices
* Requires devices to adhere to common representation **Valid → Valid**

Send '0' —noise→ receive '0'
" '1' —noise→ " '1'

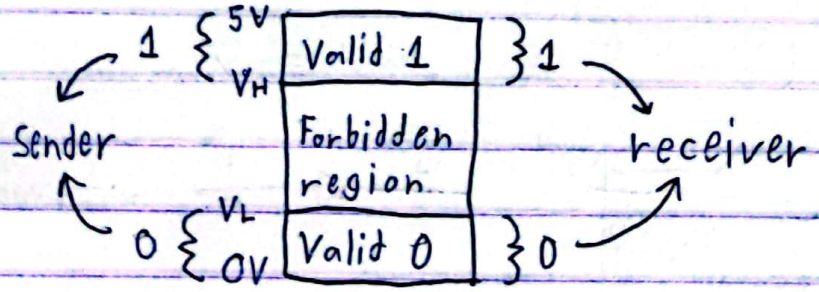
① naive approach → single threshold



$V_{Threshold}\ (V_T) = 2.5V$
$V < 2.5 = 0$
$V > 2.5 = 1$

- Problem is when $V_r = 2.5\ V$

② 2 Threshold system:



V_H → high voltage threshold
V_L → Low voltage threshold
$V_L \leq V \leq V_H$ → invalid
$V < V_L = 0$
$V > V_H = 1$

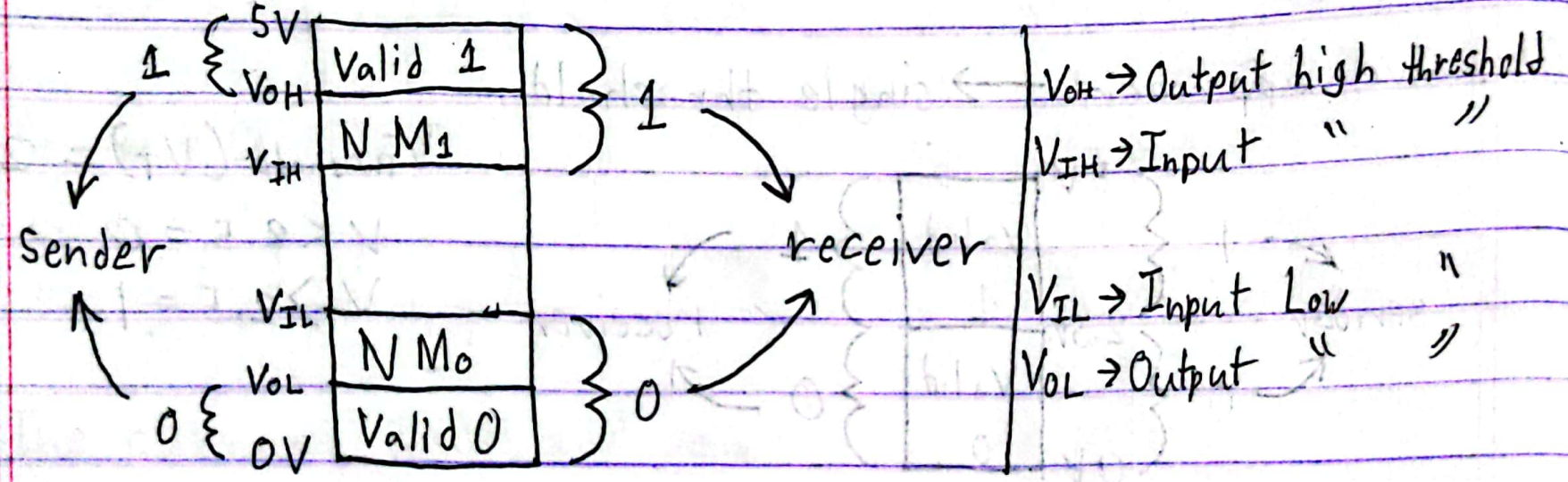
- Example:

Logic 0: $0V \leq V \leq 2V$
" 1: $3V \leq V \leq 5V$

* Problem here is there is no margin for noise. So even if transmitted signal is valid received signal can become invalid.

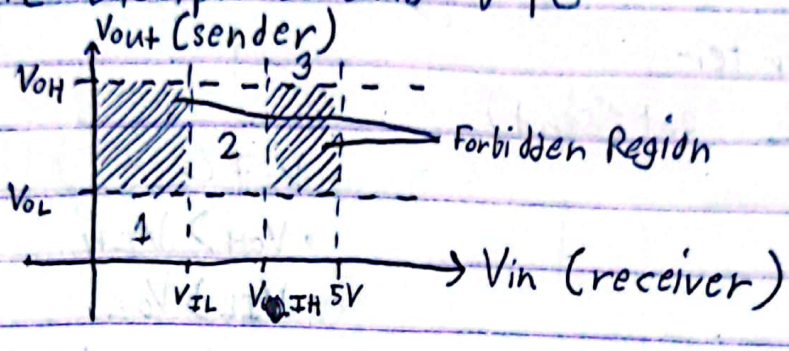
③ Tighter restriction on sender (4 threshold levels):

Sender (Output (O))	Reciver (Input (I))
Logic 0 : [0V, 0.5 V] → V_{OL}	Logical 0 : [0V, 2V] → V_{IL}
" 1 = [4.5V, 5V]	" 1 : [3V, 5V]
↓ V_{OH}	↓ V_{IH}



* $V_{OH} > V_{IH}$ and $V_{IL} > V_{OL}$
* Noise Margin for Logical 1 (NM_1) = $V_{OH} - V_{IH}$
* " " " " 0 (NM_0) = $V_{IL} - V_{OL}$

Static Discipline and VTC



Restrictions:

Logic 0 : $V_{OL} < V_{IL}$

" 1 : $V_{OH} > V_{IH}$

$V_{OL} = V_{IL} - \Delta_1 \quad -①$

$V_{OH} = V_{IH} + \Delta_2$

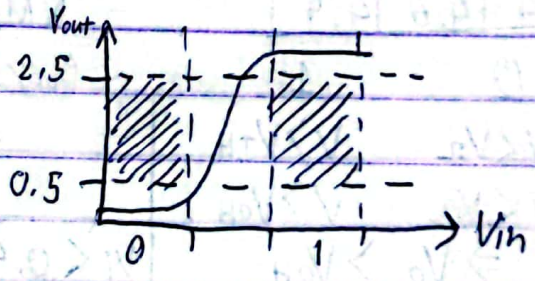
- Region - ① : Slope $= \frac{\Delta y}{\Delta x} = \frac{V_{OL} - 0}{V_{IL} - 0} = \frac{V_{IL} - \Delta_1}{V_{IL}} = \frac{V_{IL}}{V_{IL}} - \frac{\Delta_1}{V_{IL}} = 1 - \Delta_1'$

  ∴ In ①, Slope, $S < 1$ or $G < 1$ [Gain, $G = \frac{out}{In}$]
- Region - ② : Slope, $S < 1$ and $G < 1$.
- Region - ③ : Slope $= \frac{\Delta y}{\Delta x} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} = 1 + \Delta_3'$

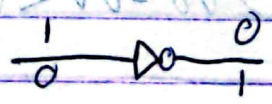
  ∴ Slope > 1 and $G > 1$

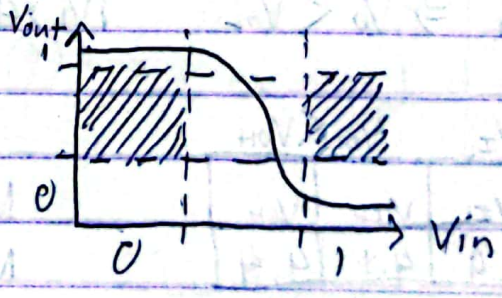
* Examples:

① Buffer



② inverter



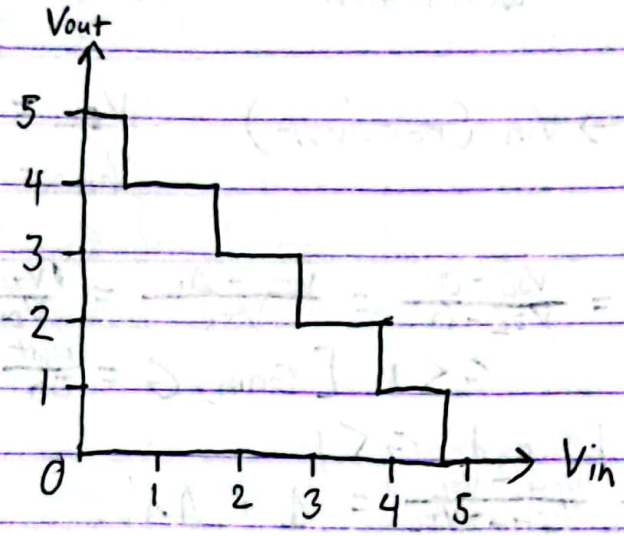


* Since the slope changes these devices are non-linear.

* Example:

● Not Gate / Inverter

In (Receive) 0/1 ▷o 1/0 out (send)



VTC
- $V_{OH} > V_{IH}$
- $V_{IL} > V_{OL}$
- Valid input ⇒ Valid Output

① $V_{OL} < V_{IL}$ $V_{IH} < V_{OH}$

V_{OL}	V_{IL}	V_{IH}	V_{OH}
0.1	0.4	4.6	4.9

$NM_0 = V_{IL} - V_{OL} = 0.3$

$NM_1 = V_{OH} - V_{IH} = 0.3$

Obey's static discipline = Yes

0	1
input $V < V_{IL}$	$V > V_{IH}$
output $V < V_{OL}$	$V > V_{OH}$
$V_i < V_{IL} \Rightarrow V_o > V_{OH}$	$V_i < 0.4 \Rightarrow V_o = 5V > V_{OH}$
$V_i > V_{IH} \Rightarrow V_o < V_{OL}$	$V_i > 4.6 \Rightarrow V_o = 0V < V_{OL}$

② $V_{OL} < V_{IL}$ $V_{IH} < V_{OH}$

V_{OL}	V_{IL}	V_{IH}	V_{OH}
0.6	0.9	4.1	4.4

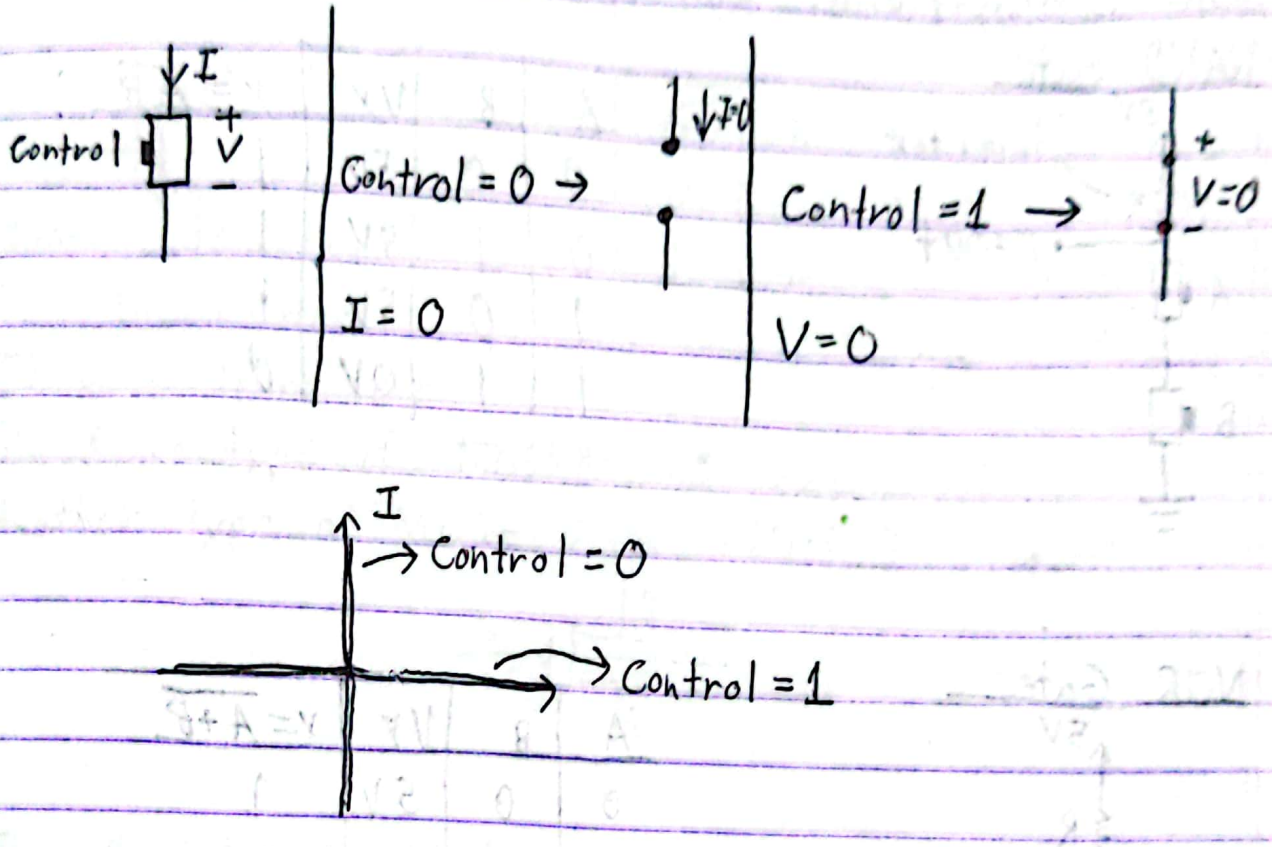
$NM_0 = 0.3V$

$NM_1 = 0.3V$

Obey' static discipline = No

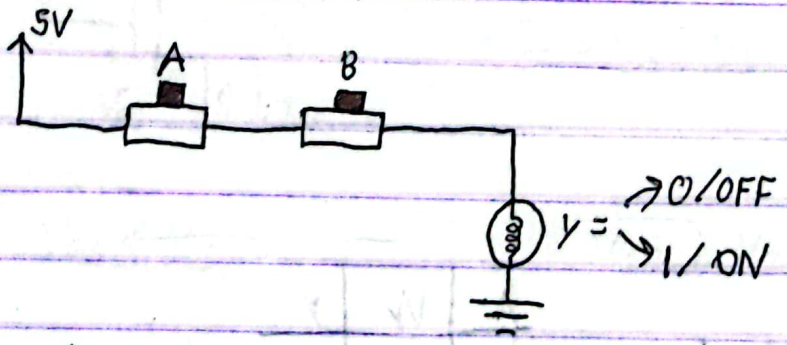
$V_i < V_{IL} \Rightarrow V_o > V_{OH}$	$V_o \geq 4V \; ! < 4.4V$ X
$V_i > V_{IH} \Rightarrow V_o < V_{OL}$	X

SWITCHES:



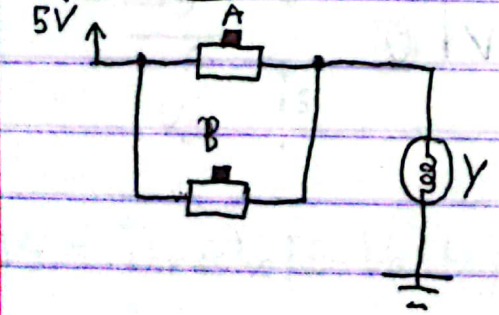
Steering Logic gates using switch:

① AND Gate:



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

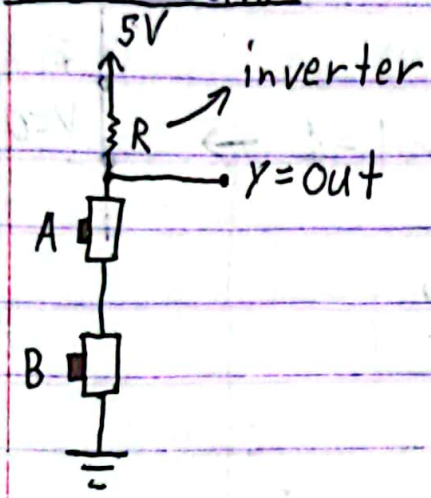
② OR Gate:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

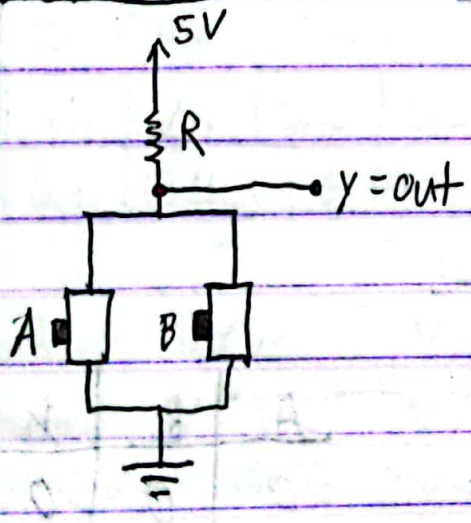
Semi Combinational Logic gates:

① NAND Gate:



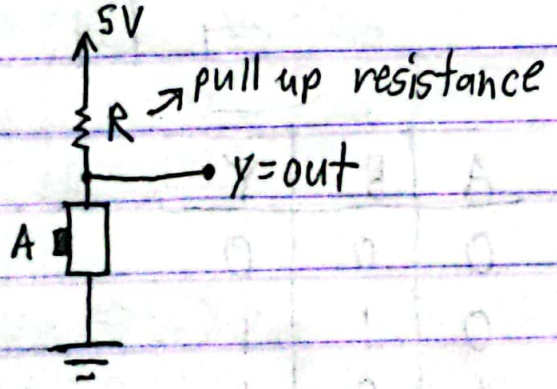
A	B	Vy	$y = \overline{AB}$
0	0	5V	1
0	1	5V	1
1	0	5V	1
1	1	0V	0

② NOR Gate:



A	B	Vy	$y = \overline{A+B}$
0	0	5V	1
0	1	0V	0
1	0	0V	0
1	1	0V	0

③ NOT Gate:



A	Vy	y
0	5V	1
1	0V	0