Experiment number: 03

Name of the experiment : Parity generator and checker

Group number : 03

Group members names and Ids:

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Name of the Experiment: Parity Generator and Checker

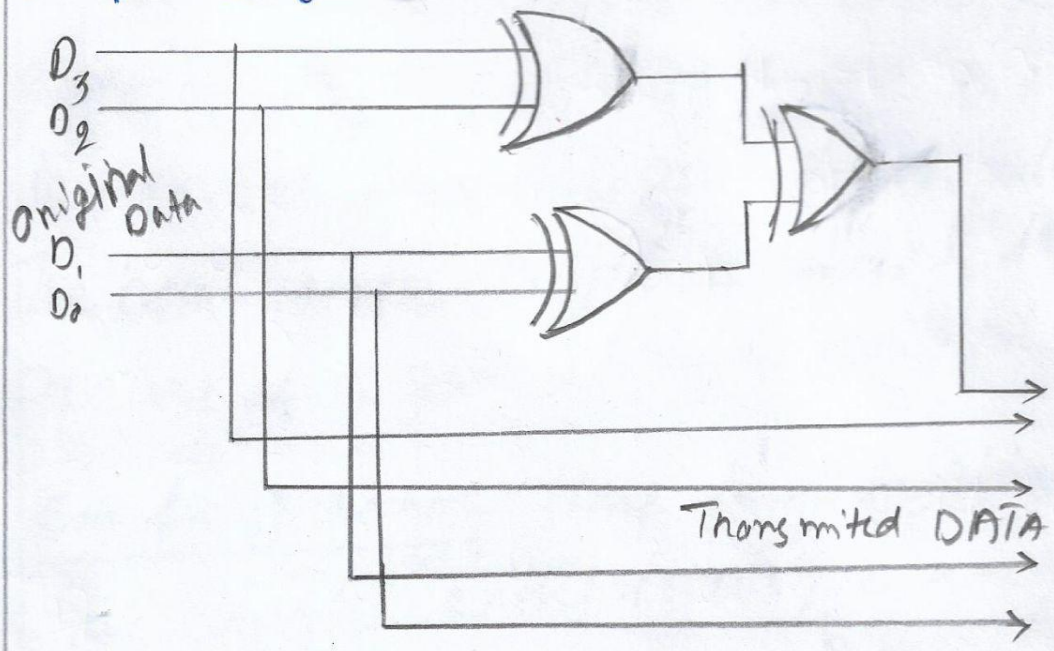
Objective: To design and impliment an even parity generator and Even parity checker using XOR gate (IC-7486)

Required components and Equiments:

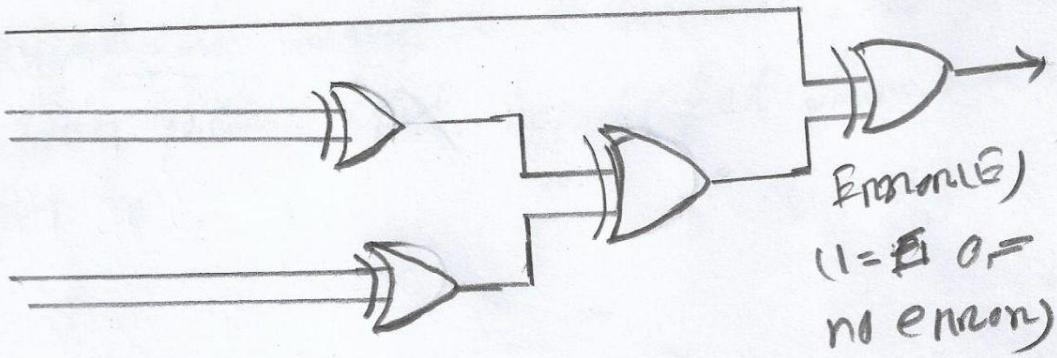
- NT-200 portable Analog / Digital Labroratry
- 7400 x3
- Logicstates
- wire
- x-OR gate
- Logic probe

Experimental setup:

Even parity generation:



Even parity checker:



Generator: We have taken 4 logic states. denoted as D_0, D_1, D_2, D_3. Than D_0 & D_1 is connected to a x-OR gate and D_1 & D_3 is connected to another gate x-OR gate. The bouth of the output is connected to another x-OR gate which is parity bit.

Even parity checker: Here four logic states, have connected with to unique x-OR gate D_0, D_1, D_2, D_3 one those. The two output is connected to another x-OR gate there parts and initial input there are get E

Results in Truth table Form:

From Even parity Generation.

D_3	D_2	D_1	D_0	Parity	Transmit DATA
0	1	1	1	1	10111
1	0	0	1	0	01001
0	0	0	0	0	00000
0	1	0	0	1	10110

1011

$D_0 \oplus D_1 = D_0\hat{}D_1' + D_1 D_0 = 0+0 = 0$

$D_2 \oplus D_3 = D_2 + D_3' + D_3' D_2 = 1+1 = 0$

$\therefore 0 \oplus 1 = 1$

01001

$D_0 \oplus D_1 = D_0' D_1 + D_1 D_0 = 0+1 = 1$

$D_2 \oplus D_3 = D_2' D_3 + D_3' D_2 = 0+1 = 1$

$\therefore 1 \oplus 1 = 0$

00000

$D_0 \oplus D_1 = 0 + 1 = 0$

$D_2 \oplus D_3 = 0 + 0 = 0$

$\therefore 0 \oplus 0 = 0$

10100

$D_0 \oplus D_1 = 0 + 1 = 1$

$D_2 \oplus D_3 = 0 + 0 = 0$

$\therefore 1 \oplus 0 = 1$

Parity checker:

P	D_3	D_2	D_1	D_0	Generated Parity	Error	Output
0	1	0	1	0	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	0	1	1
1	0	0	0	0	0	1	1

Discussion: From the parity checker, we can notice that the calculation is correct because the calculated of generated parity and given parity the error and the output from the circuit is similar. From this experiment, we can learn parity bit generation using logic gates and implement.

■ Determine the parity checker's output for each of the following sets of data from the transmitter

P	D_3	D_2	D_1	D_0	Error
0	1	0	1	0 → 0	0
1	1	1	1	0 → 1	0
1	1	1	1	1 → 1	1
1	0	0	0	0 1	1

Report:

The report should cover the followings

1. Name of the Experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup (You must draw the diagrams)
5. Results in Tabulated form.
6. Discussions (Explanation of the results)

Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment # 3

Parity Generator and Checker

Objective:

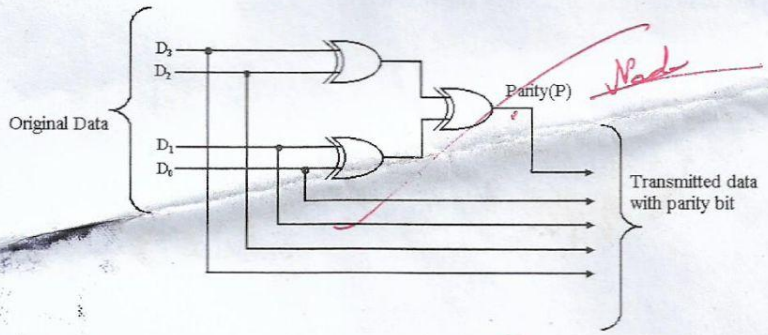
- To design and implement an Even parity Generator and Even parity checker using XOR gates) (IC-7486).

Required Components and Equipments

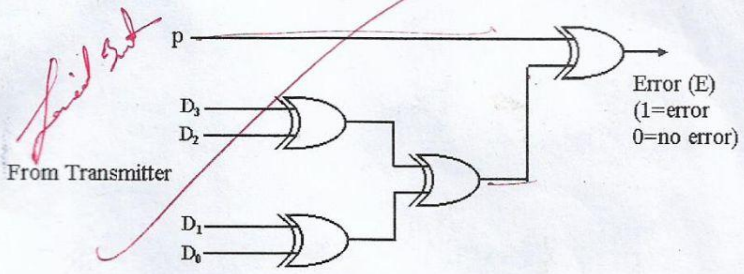
1. AT-700 Portable Analog/Digital Laboratory
2. 7400×3

Diagram of Circuit:

Even Parity generator



Even Parity Checker



Procedure:

- Construct the Circuit of Figure 1, on the breadboard of AT-700.
- Remember each IC's pin 14 connected to "+5V" position of DC Power Supply of AT-700, and pin 7 connected to "GND" position.
- Connect the inputs to Data switches and outputs to any position of LED Display.
- Determine the parity generator's output for each of the following sets of input data, $D_3D_2D_1D_0$; (a) 0111; (b) 1001; (c) 0000; (d) 0100