RK1108 Hardware Design Introduction

Sep., 2016

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Agenda

- RK1108 Power Design Introduction
- RK1108 GPIO Introduction
- RK1108 Storage Design Introduction
- RK1108 Function Module Design Introduction
- Q&A

RK1108 Power Design Introduction

Power Design

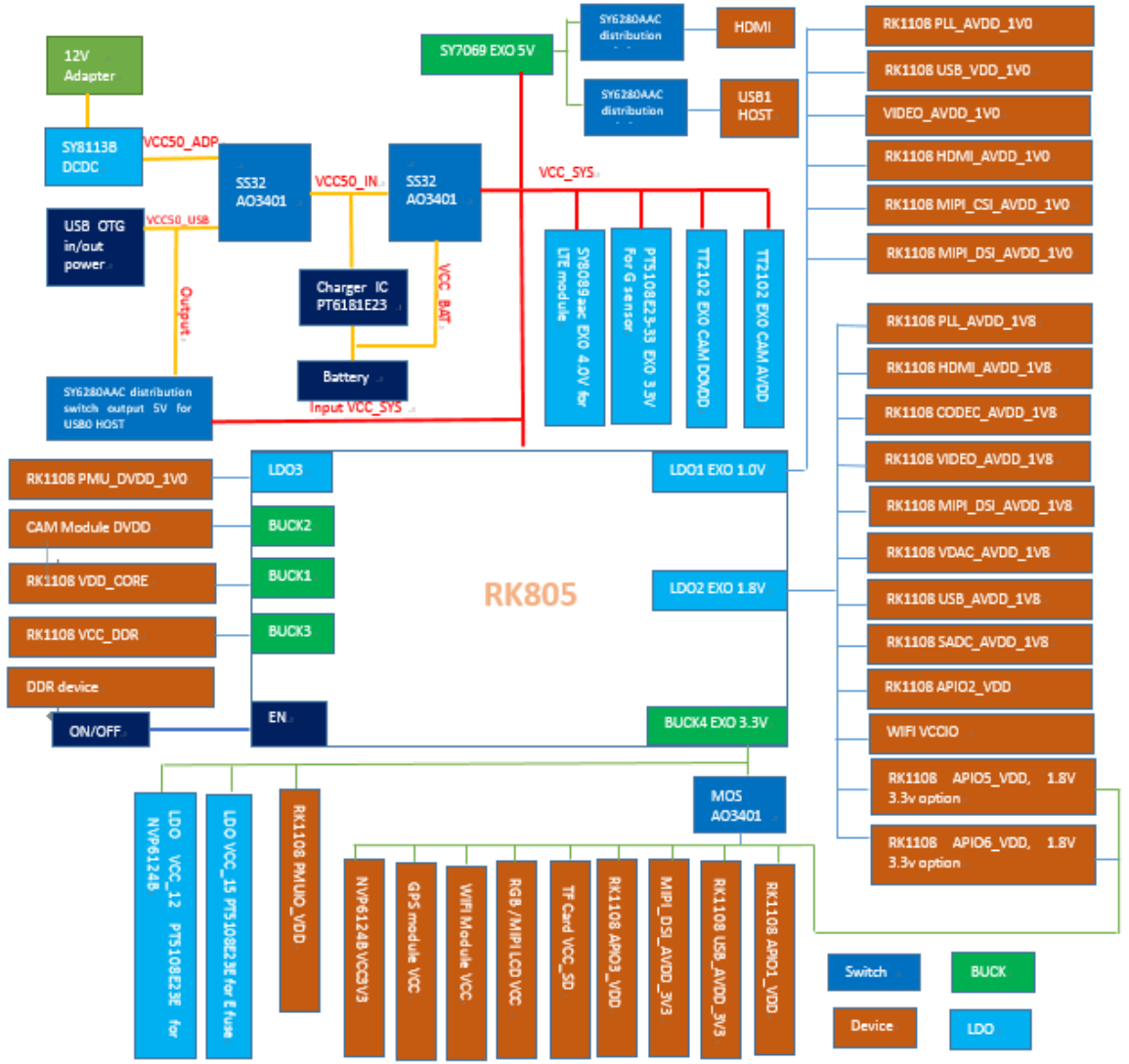
➢ Power Tree

1. 3 kinds of power supply： Adapter 12V, USB OTG 5V , Battery Input
2. PMIC RK805-2 is used, to power supply system as well as other modules such as WIFI, GPS , LCDC and CAM DVDD
3. CAM DOVDD, AVDD is power supplied by 2 LDO

Note: Above RK805+2 LDO can meet above function power requirement

4. HDMI/USB HOST need to use 1 current-limited IC. If system is only supplied by battery, 1 5V BOST is needed as well.
5. G sensor collision power on , need to use 1 LDO to power supply
6. 4 in 1 video function NVP6124B, need to use 1 LDO to power supply

Note: Point 4 to Point 6 add LDO or DCDC, customer can determine whether to use according to his product definition.



Power Design

- PMIC RK805-2

1. In BOM, RK805-2 must to be used

- RK1108 Power Domain

1. APIO1,2,3,5,6，PMUIO，PMUIO must be 3.3V，other power domain IO is compatible 1.8V and 3.3V
2. In RK1108 chip design, function modules not in use can’t be floating.

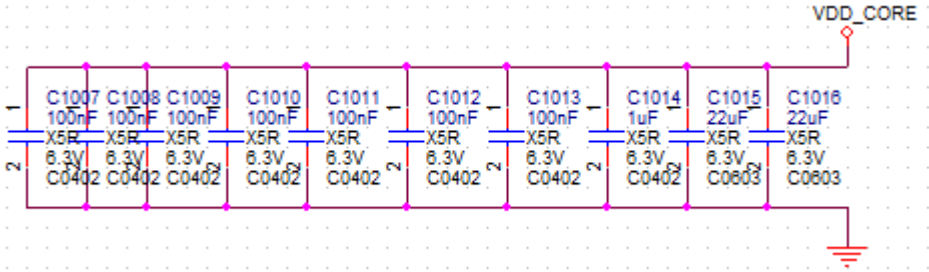
RK805-2 上电时序 V1.0 20160824					
输入	通道	供电能力	RK1108	默认电压	上电时序
VCC1	CH1	2A@0.7-1.5V	VDD_CORE	1.0V	2
VCC2	CH2	2A@0.7-1.5V	DVDD_CAM	1.0V	OFF
VCC3	CH3	1A@1-1.5V	VCC_DDR	FB=0.8V	3
VCC4	CH4	1A@1.8-3.6V	VCC_IO	3.3V	5
VCC5	LDO1	300mA	VDD_10	1.0V	1
VCC5	LDO2	300mA	VCC_18	1.8V	4
VCC6	LDO3	100mA	VDD1V0_PMU	1.0V	1

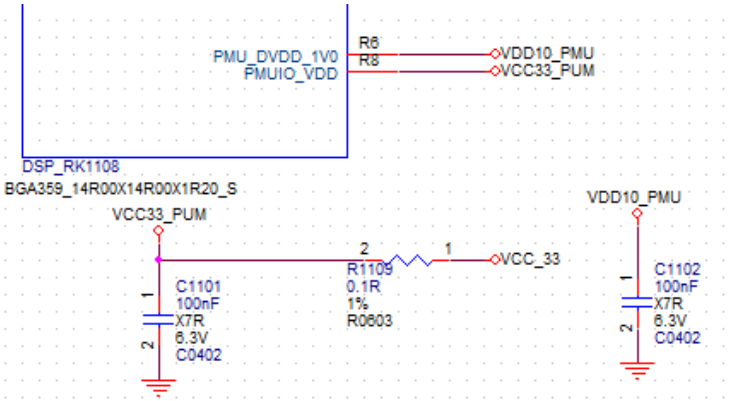
Power Design

➢Power Capacitance Location

1. Big capacitance of VDD_CORE should be placed to reverse side of CPU (or close to) .

2. Please place 100nF coupling capacitance close to chip pin.

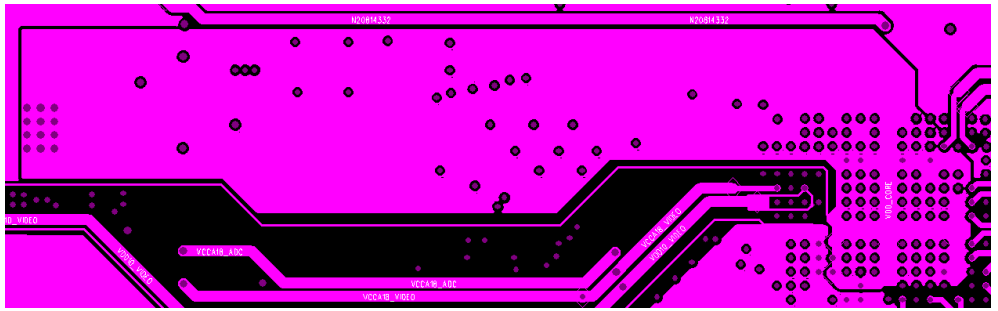




➢ Power Layout

1. A large area of power copper between PMIC power output and CPU power pin can enhance the capacity of current and reduce the loss of trace resistance.

2. Place more enough vias in the power trace layer change node, to enhance the capacity of current, and reduce the loss of trace resistance.

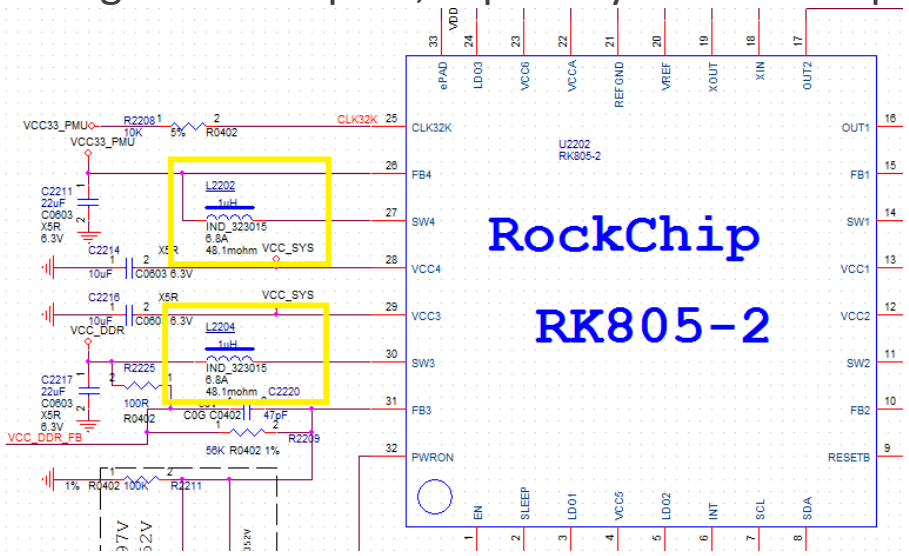


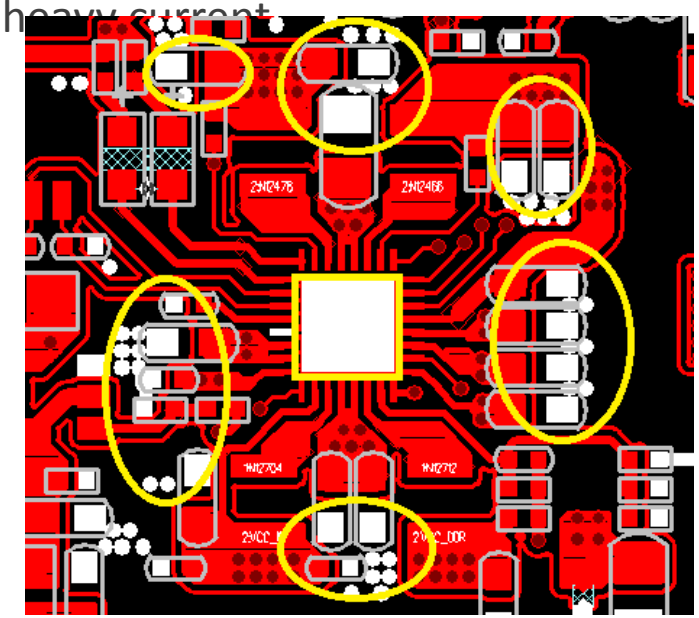
Power Design

- RK805-2 Notes

1. RK805-2 BUCK1,2,3,4 power inductors should be 0.47uH~1uH. Keep enough space between power inductors, or high voltage caused by mutual inductances may damage chip.

2. All input and output capacitors should be placed close to RK805-2. Keep enough GND vias to ensure signal return path, especially for those capacitors with heavy current.

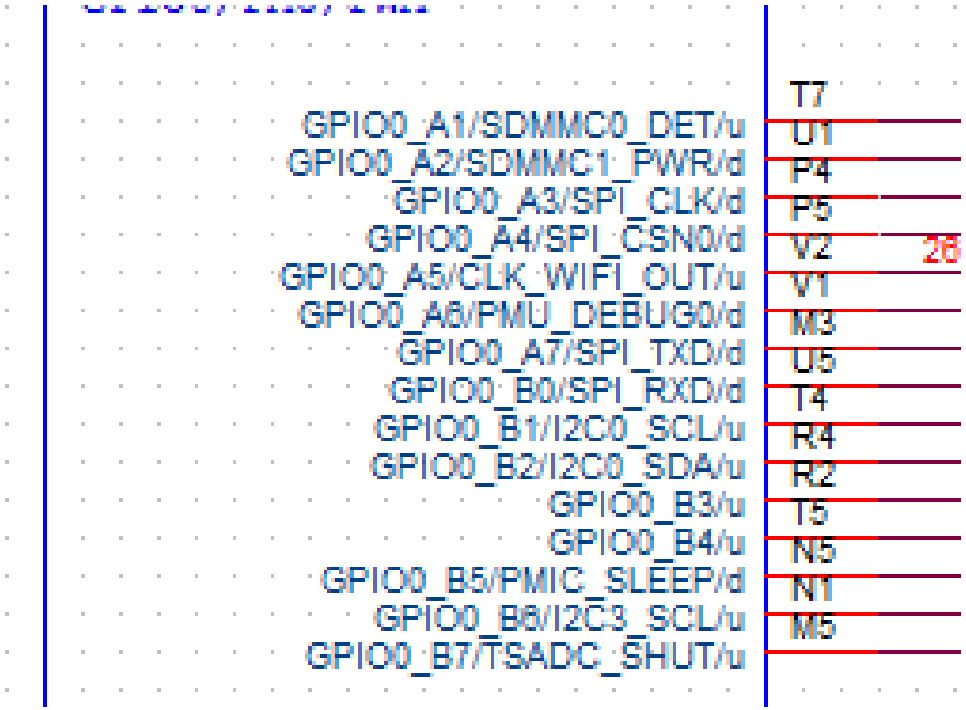




RK1108 GPIO Introduction

GPIO Notes

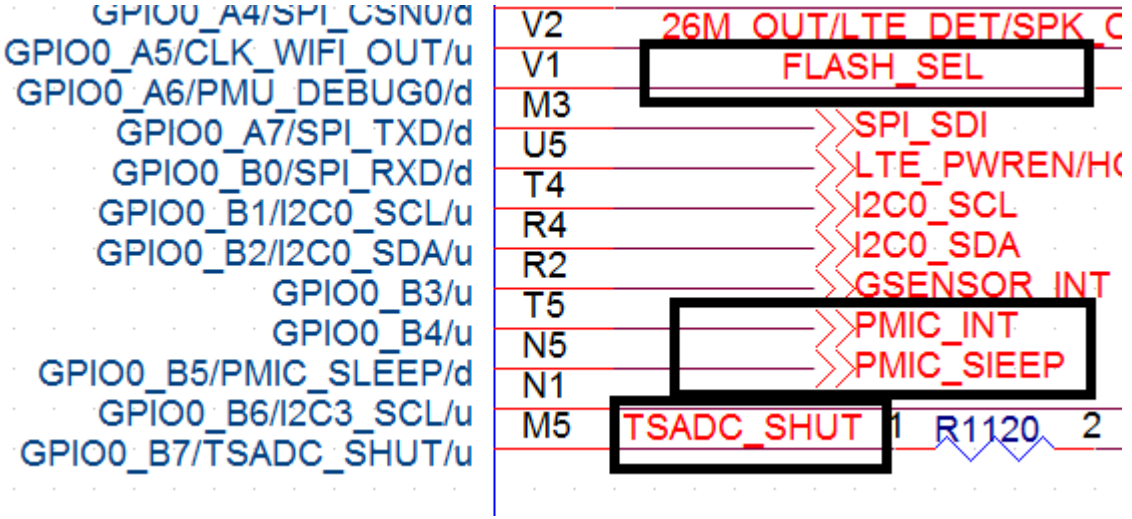
- Please strictly follow GPIO configured in datasheet if possible.
- In product design, if GPIO defined by RK need to be changed, please make sure IO level and GPIO up and down features must be matched, or it may cause function abnormal.
- RK1108 GPIO up and down level can be configured or closed after power on, packaging remarked with "_d" in diagram is internal down after power on as default, remarked with "_u" is internal up. Any modification, please refer to datasheet released by RK



GPIO Notes

- PMUIO Power Domain IO

1. PMU power domain is always supplied, even when standby
2. FLASH_SEL, TSADC_SHUT, PMIC_INT and PMIC_SLEEP connection must follow reference design, can't be changed.
3. If HDMI function is used, please take I2C4。
4. If IO is used, make sure this power domain IO is 3.3V.

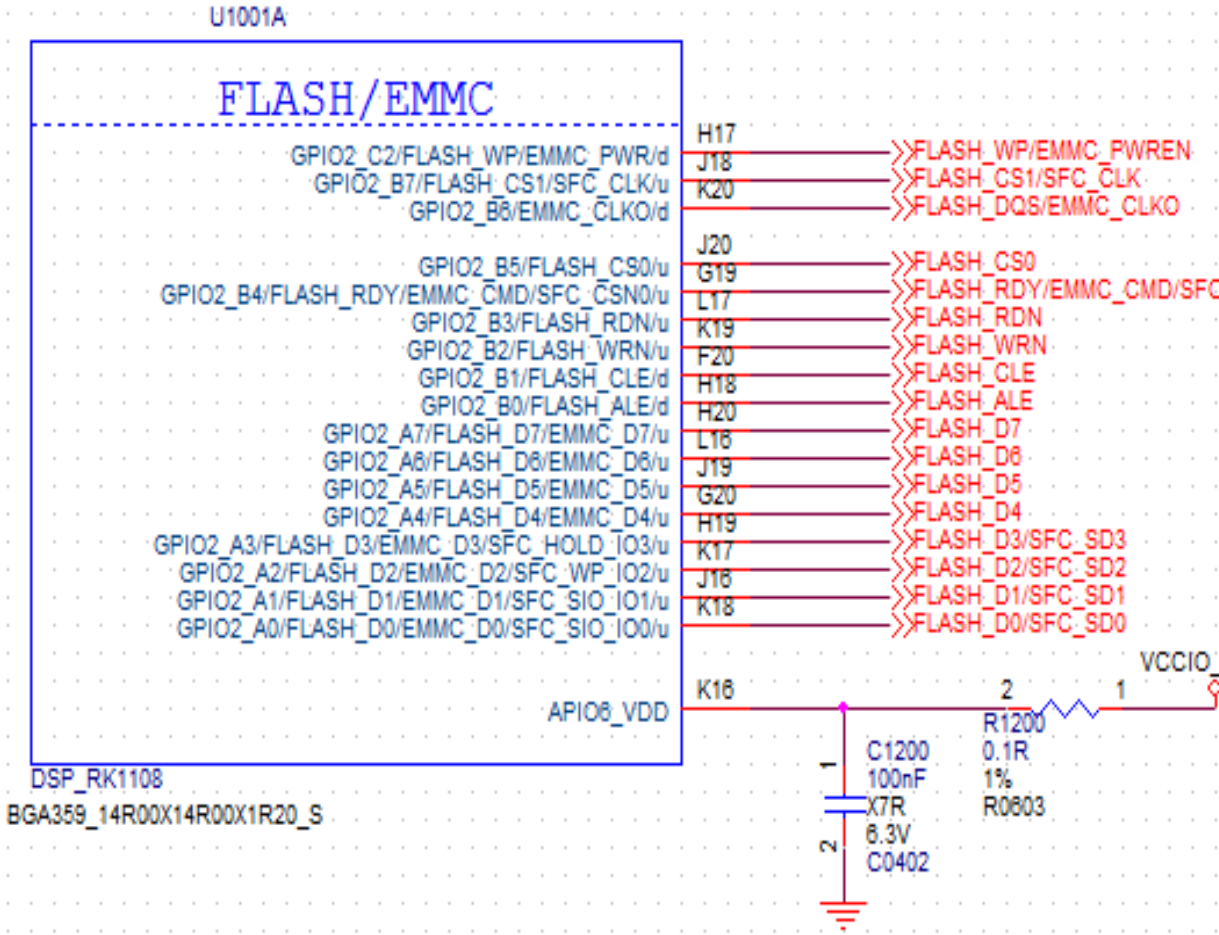


RK1108 Storage Design

FLASH/EMMC

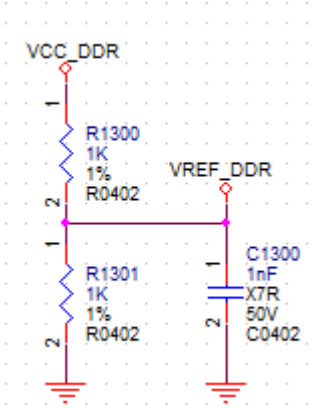
- Support SPI NOR /NANDflash,EMMC
- Power domain belongs to APIO6, which can support 3.3V and 1.8V
- Flash firmware update uses flash_D0; EMMC firmware update uses FLASH_DQS
- Routing：

1. Flash routing should be away from high-speed signals.
2. Flash data trace can't go through adjacent layers, which copper plane is with large ripple wave and current signal such as VCC_SYS .



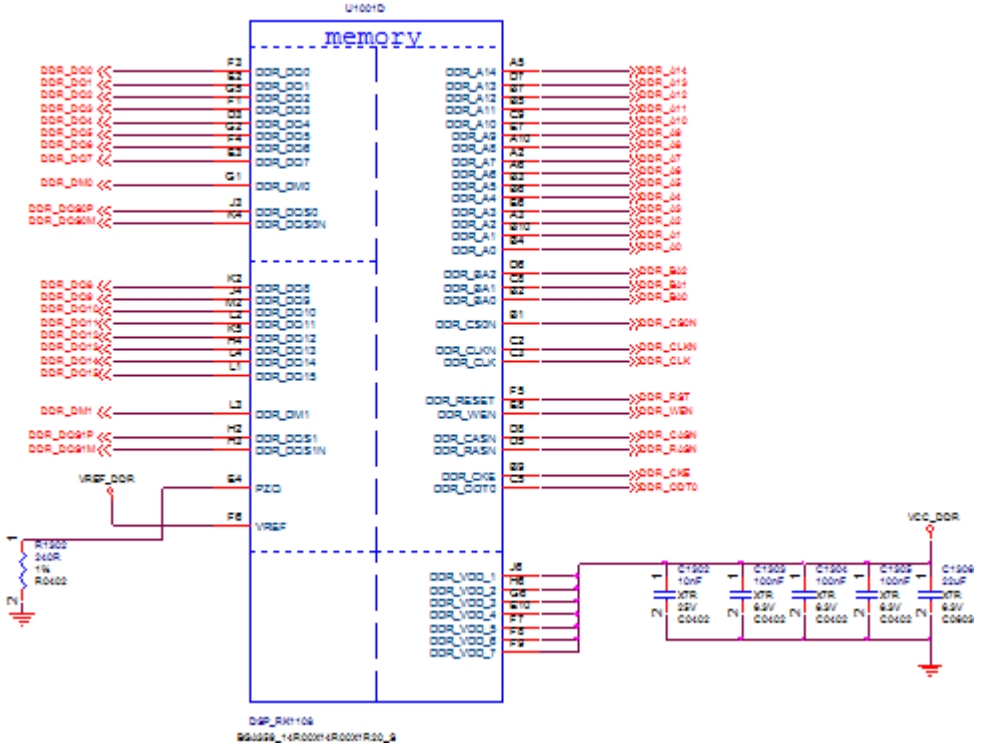
DDR Controler&DRAM

- DDR supports 1X16bit
- Divider resistance value of VREF_VDD reference power supply should be sure 1% accuracy, two divider resistance should be 1k.



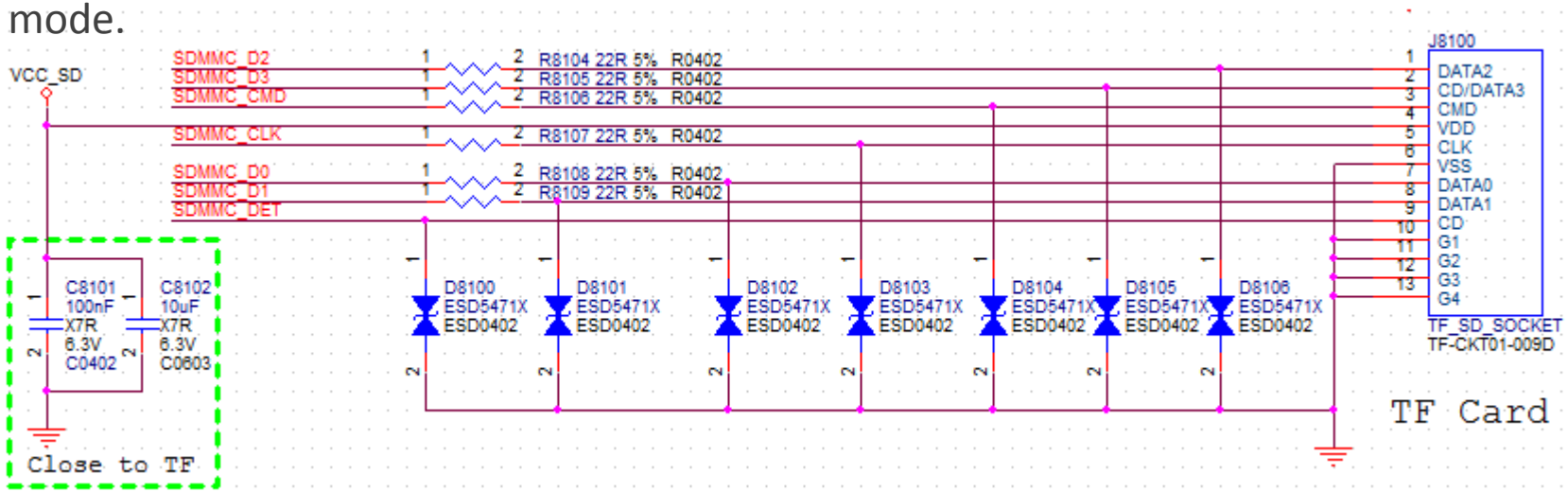
- Routing Space
- Routing trace should be equal-leng… deign guideline for more details.

Note：Suggest to follow demo board routing if product layout permits.



TF Card

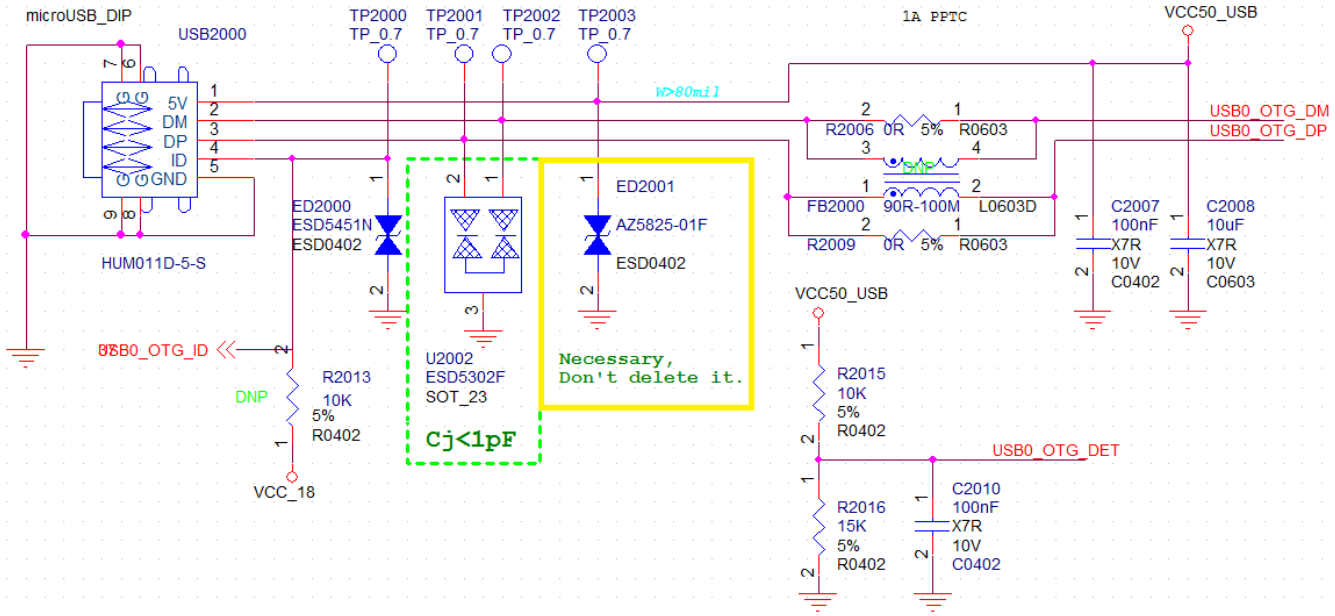
- Support SD3.0
- If SD 3.0 need to be supported, SD card IO should be compatible with 3.3V and 1.8V.
- Note: All SD data traces are required to be routed by ground, the same for CLK, which should be routed respectively.
- The trace length of the same group signals should be limited within 400mil, or it will restrain frequency on high-speed mode.



RK1108 Function Module Design Introduction

USB

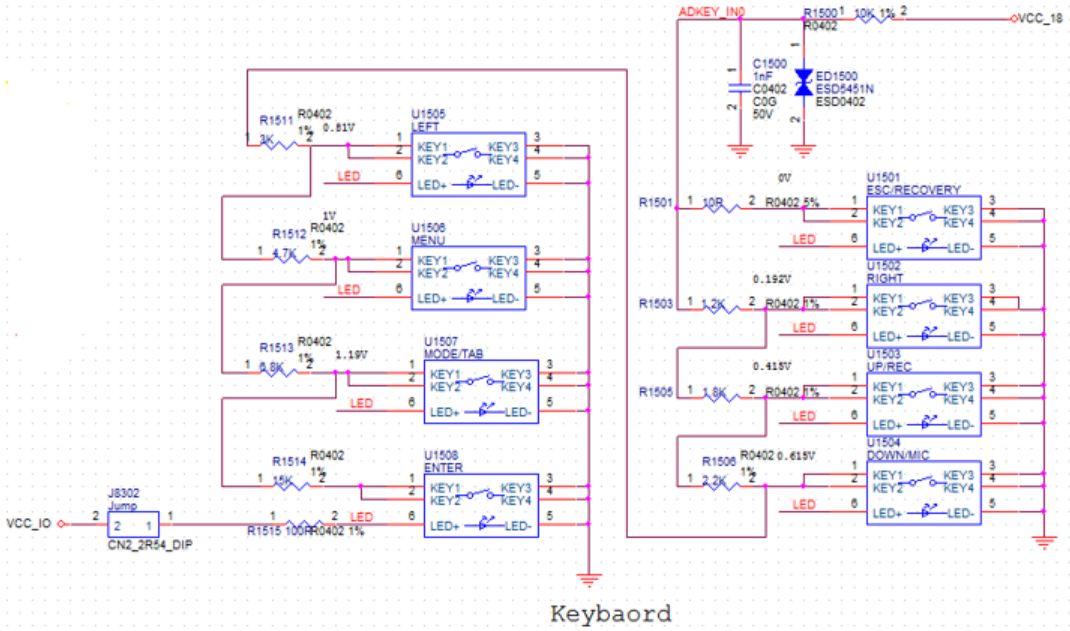
- RK1108 has two sets of USB interfaces, USB OTG and USB HOST, USB2.0 protocol.
- USB_ID pull-up is 1.8V.
- Low junction capacitance (less than 1pF) ESD protective components should be used for USB differential signals.
- ED2001 is necessary, it can't be deleted
- To reduce EMI, suggest to reserve common mode chokes on signal traces. The usage of resistor or common mode choke depends on the actual situation in debugging.



SARADC&KEY

- SARADC sampling range is 0-1.8 V, sampling accuracy is 10 bit
- Key voltage difference of any two keys is suggested to be greater than 200 mv.
- Key PCB Layout Notes As Follow：

1. Place ESD protective component close to key for electrostatic protection;
2. Place key shake elimination capacitor close to chip;
3. ADKEY_IN trace and other signal traces should be isolated by GND, to avoid key value misjudgment caused by crosstalk between traces.



DVP Interface&Camera

- DVP interface power domain is APIO5_VDD, which can support 1.8 V and 3.3 V. CAM I2C pull-up voltage should match with APIO5.

- DVP SOC Camera Sensor Using Tips：

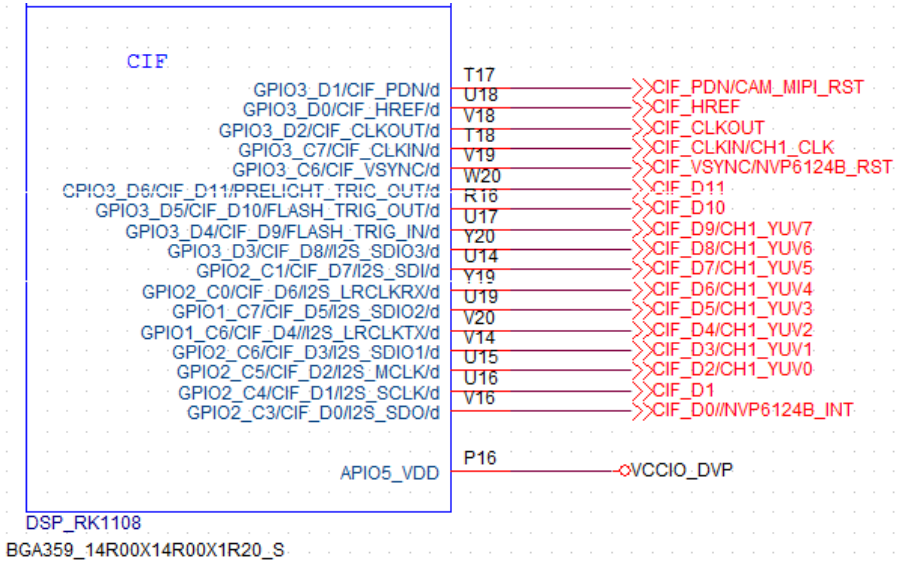
1. Sensor output YUV data bit0-bit7 and RK1108 DVP interface bit2-bit9 should be corresponding connected;

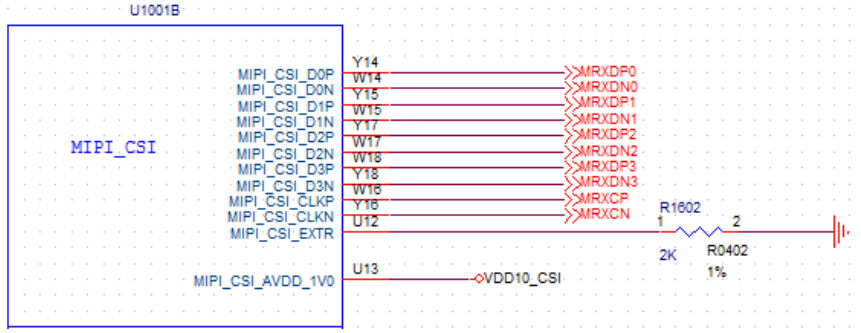
- MIPI DSI is 4lane
- Can satisfy front and back camera requirement.

- Routing：

1. MIPI trace should be as short as possible, for independence control, protected by GND, and reduce vias between layers.
2. DVP Sensor signal trace is CIF_D2-D9, suggested to be protected by GND in group.

Note: Suggest to check RK Camera Sensor certification list before use.

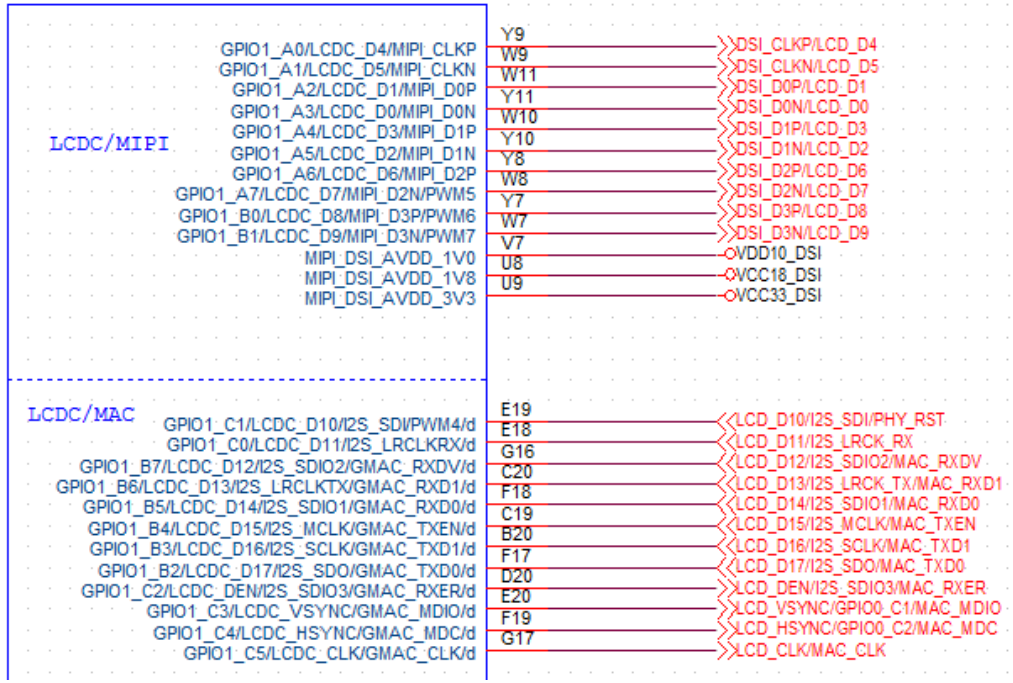


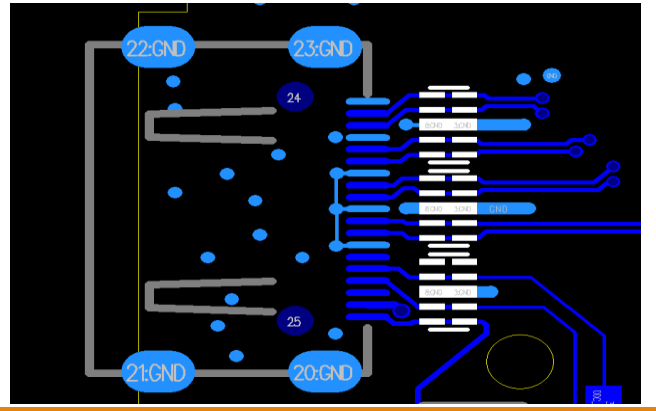


Display Interface

- RK1108 support multiple video outputs such as Parallel/serial RGB, MIPI and HDMI.
- MIPI DSI and RGB IO is reused, so these two kinds of screen can't be used at the same time.
- HDMI High-speed differential signal is very sensitive to parasitic capacitor, thus low junction capacitor compliant to relevant specification should be selected as ESD protective component（Cj<=0.4pF）
- Routing：

1. Signal connector should be placed close to chip, to shorten trace length
2. MIPI, HDMI signal trace impedance is Z=100ohm±10%；
3. Place ESD component close to HDMI socket

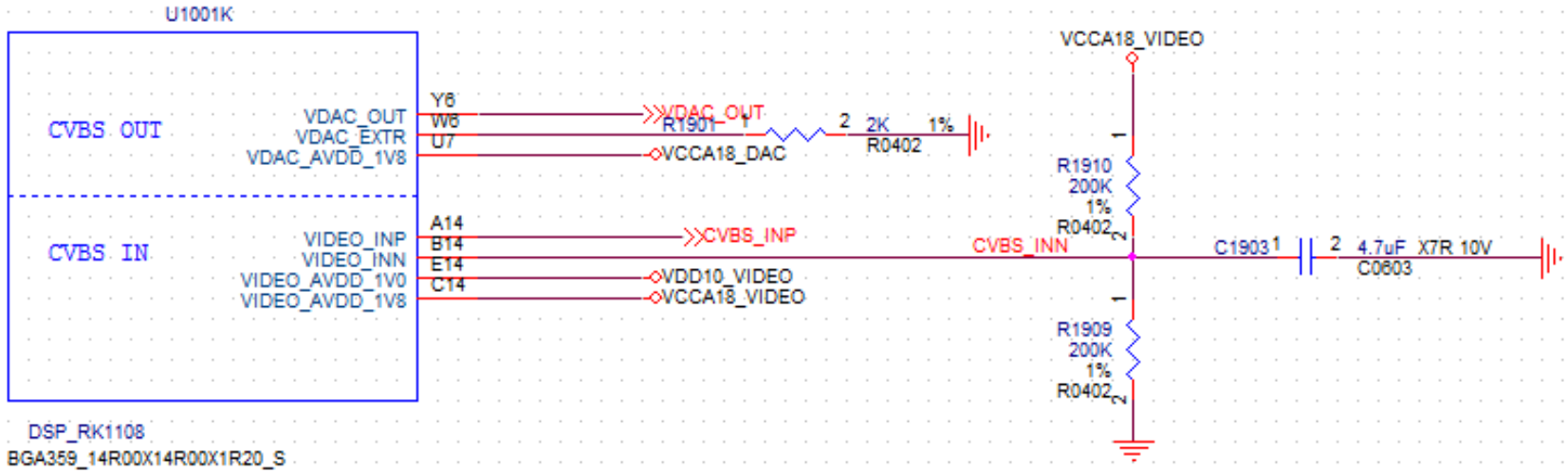




CVBS IN/CVBS OUT

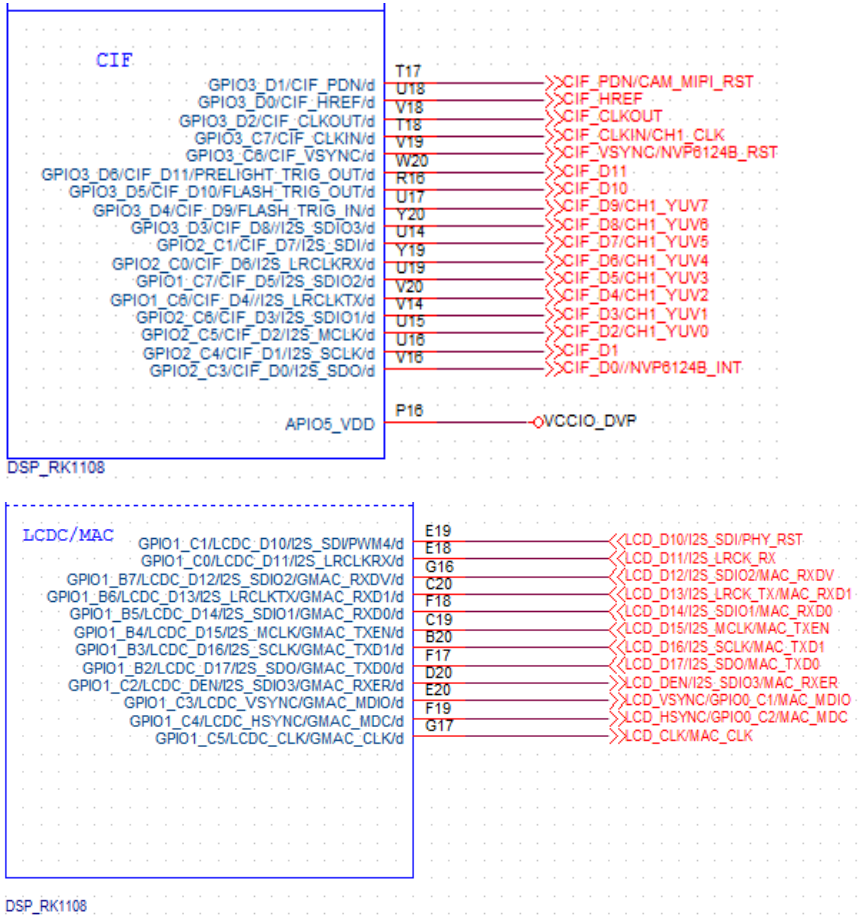
- CVBS OUT reference resistance accuracy is 1%.
- CVBS INN need 0.9V offset voltage.
- Routing：

1. CVBS signal need to be surrounded by GND (including peer layers and adjacent layers) to avoid output distortion and noise, also need to be separated from other digital signals. Output signal trace width is suggested to be above 15mils.



Audio Codec

- RK1108 has built-in CODEC, MIC supports single-ended and differential input (specification selected electret MIC), COEDC output is line out mode, it doesn't support the headphones, need external amplifier speaker .
- RK1108 has I2S interface from two power domain, APIO1 and APIO5, which is reused with DVP interface, LCDC interface and MAC interface. Consider to choose any one of the interfaces in actual product design.
- Support MIC array, I2C pull-up level is used for MIC array, should match with I2S APIO.



Audio Codec

- Routing：

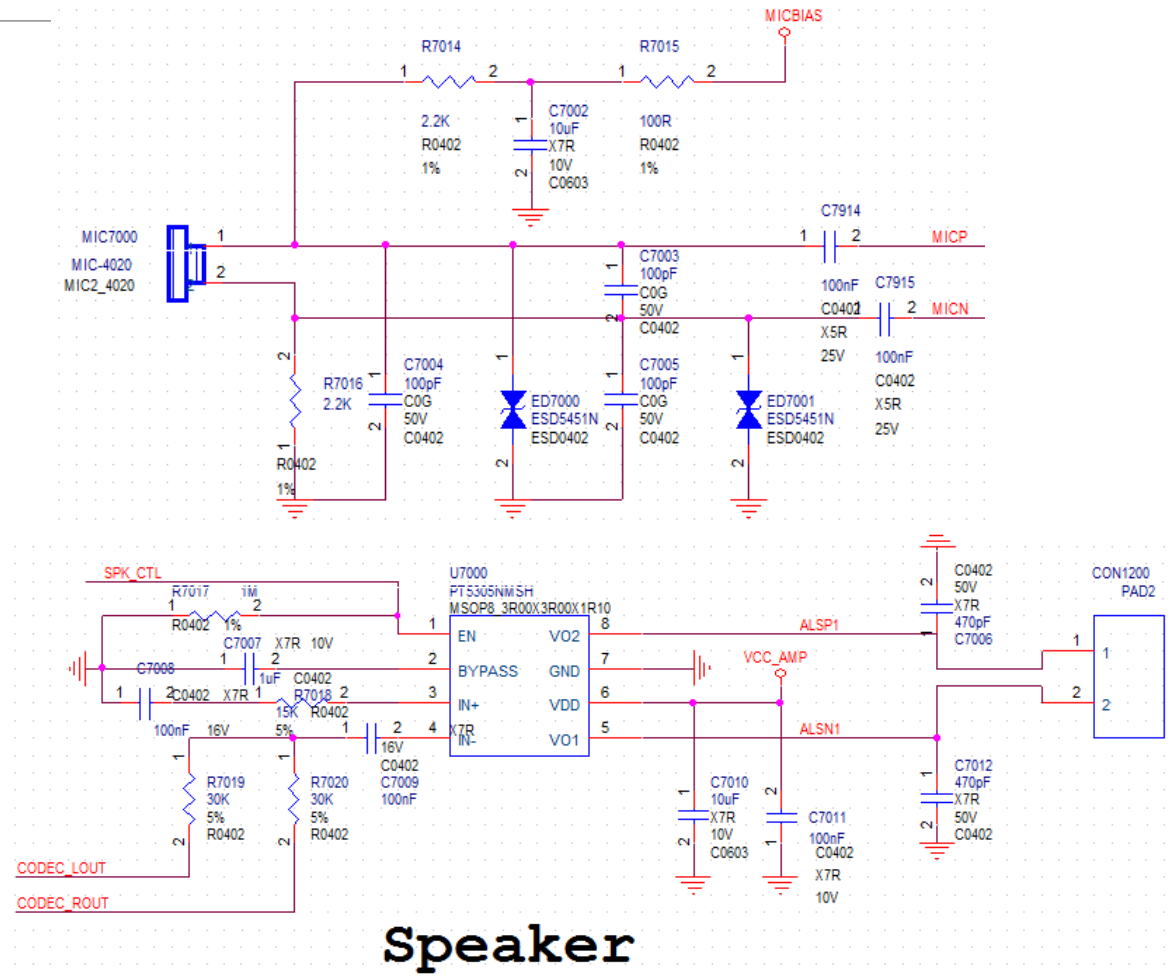
1. Trace width of all Codec power supply is requested to be above 15mils， SPK power trace width should be above 30mils

2. Each analog signals input/output from Codec need to be surrounded by GND also separated from other digital signals, to avoid output distortion and noise.

3. MIC input signal is sensitive, MIC coupling capacitor should be placed close to Codec, to avoid noise.

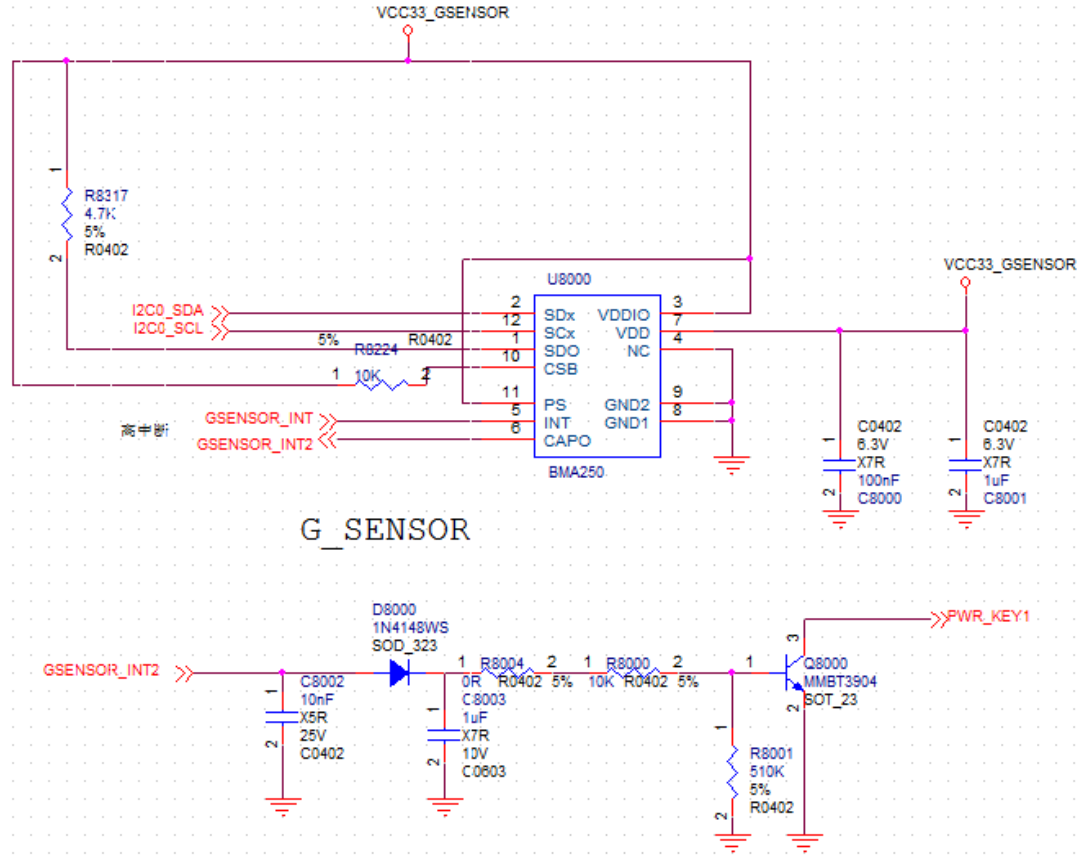
4. Codec should be placed close to headphone jack, trace length is the shorter the better.

5. Trace length from amplifier to speaker should be as short as possible, with wider width, less corner. Suggest differential routing, trace width is above 20mils, trace spaces is below 10mils to avoid noise.



G Sensor

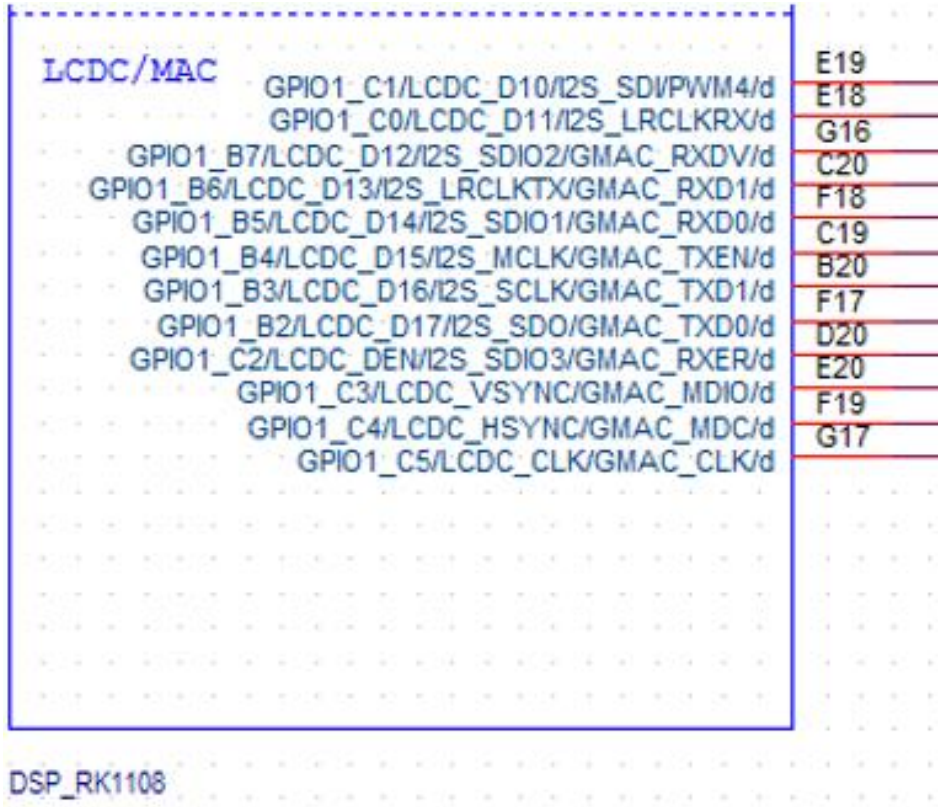
- G sensor collision power on
- Make sure I2C pull-up level should match with G sensor IO.
- Take care of G sensor direction, suggest to place the first pin on the upper left corner of product front view



MAC

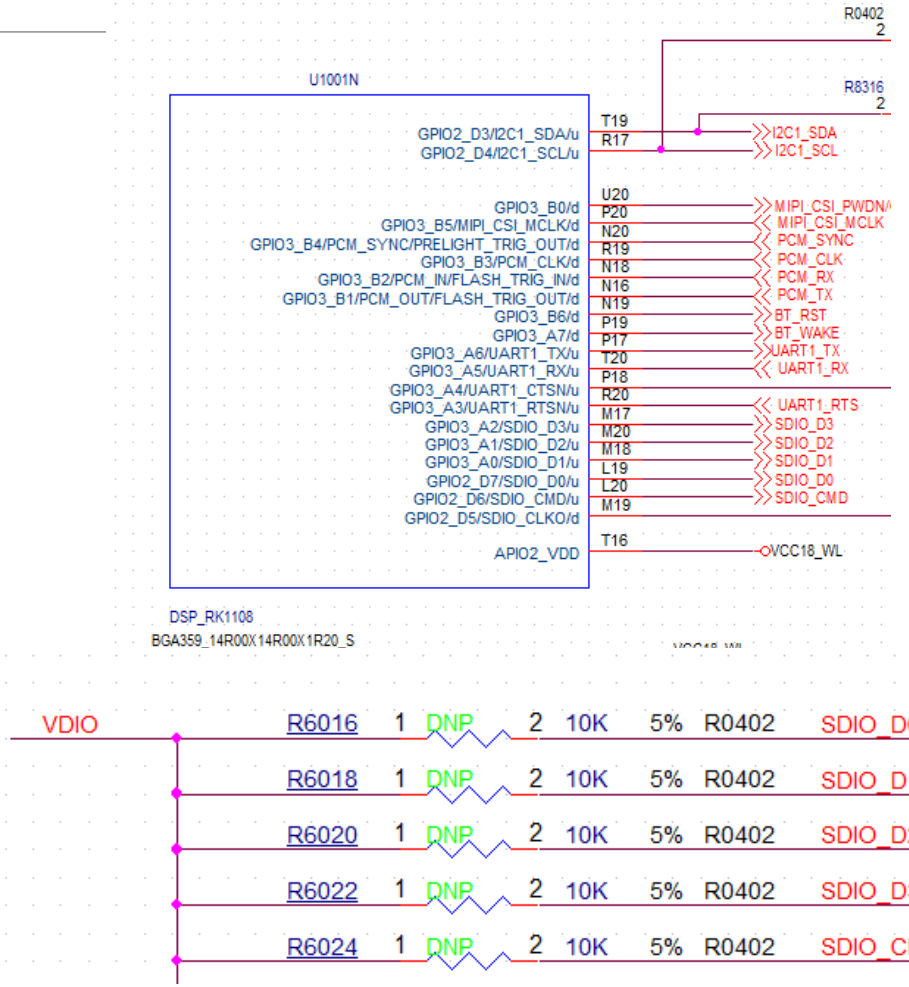
- RK1108 support RMII mode MB Ethernet connection.
- Compatible with IEEE802.3, support 10/100M data rate.
- Belongs to APIO1 power domain, MAC and I2S, LCDC is reused.
- To pass EMI test, MAC output differential trace need consider Common mode choke. (Common mode choke is 90-120ohm).
- Suggest to use RJ45 jack with metal shield.
- Routing:

1. PHY must be placed close to RK1108, the EMI will be less, that means RMII trace is the shorter, EMI will be less.
2. Better to place RJ45 is close to PHY.
3. MAC_CLK should be packed to ground, have a complete reference plane.



WIFI&BT

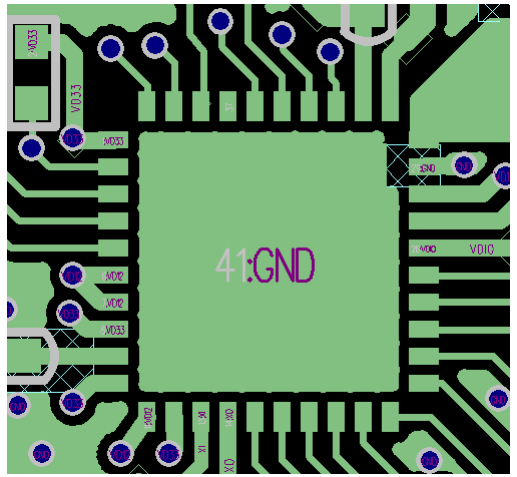
- RK1108 SDIO support 3.0 protocol
- WIFI RTL clock is output from RK805-2, notice level match.
- WIF need choose ESR less than 60ohm, crystal frequency offset error is 20ppm .
- Reserve SDIO pull-up resistor to improve SDIO driver capability.

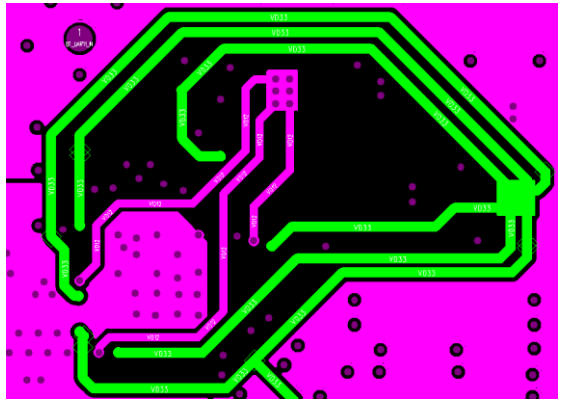


WIFI&BT

Routing:

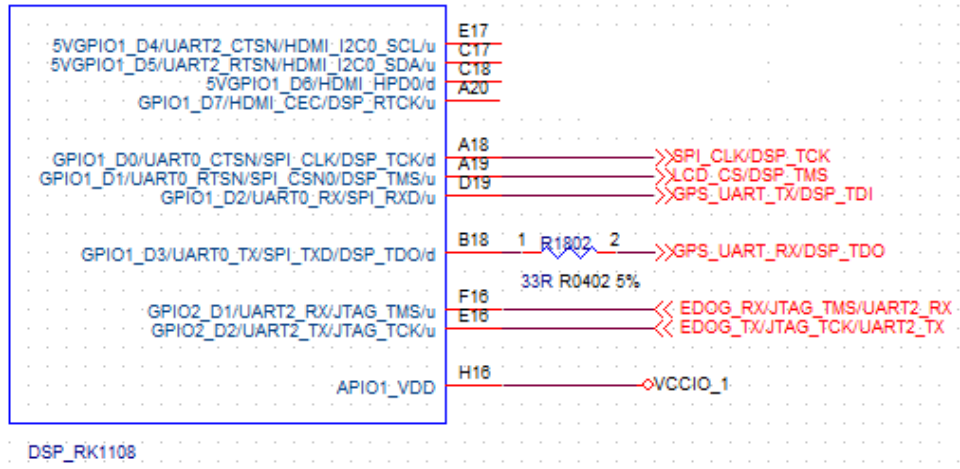
- Place WIFI module far away from high-speed components like DDR.
- SDIO, CLK trace should be in parallel and protected by GND, and avoid to be close to power and high-speed signals.
- Trace length is controlled in 12.4inch, error in group is within 400mil.
- Keep complete plane under crystal, and make sure enough vias to GND for crystal pin
- Keep complete plane on the first layer under Wifi module/chip
- Power routing is around IC crystal, don’t go through it
- Antenna and micro-strip trace width impedance is Z=50±10ohm , RF trace reference plane is complete.
- Antenna should match, don't twist with battery speaker wire in assembly, and don’t go through FPC and DDR area;

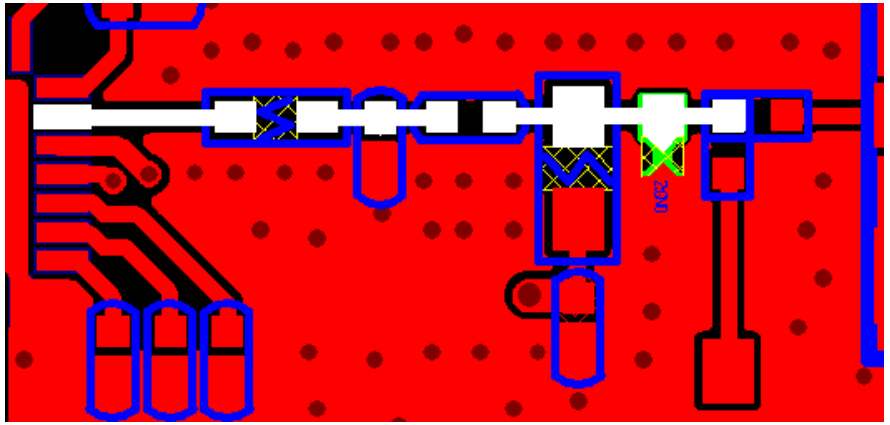




GPS

- UART0 and GPS module is used for communication.
- GPS is sensitive component, easy to have magnetic interference, so any inappropriate structure in space or layout can affect the GPS performance, such as speakers, batteries, metal, buttons, connectors, LCD and touch FPC cables and all kinds of long jumper wire. In structure , GPS antenna should be placed as far as possible to battery, speakers, connectors, LCD and Camera seat, and try to put the GPS antenna on EMI and noise floor smallest corner on PCB.
- For products with GPS, the device adopts plastic case as far as possible, and don't use aluminum alloy shell, or GPS signal will be completely shielded and unable to work.
- For aluminum alloy frame, ensure that antenna is more than 7 mm away from box .If aluminum alloy shell must be adopted, antenna window should be more than 3*3 cm, and ensure good GND connection.
- To guarantee GPS performance , shield and conductive foam, conductive cloth is necessary .
- GPS internal layout, make sure relevant components of RF circuits should be put as compact as possible, namely LNA, SAW Filter, matching circuit such as antenna feed to RF_IN path should be put compact to reduce interference.





Q&A

Thanks!