Muya Chang

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Education

(Expect: 2020) | (1st Major) **Ph.D Candidate** in **Electrical & Computer Engineering** | Advisor: Arijit Raychowdhury
Current | **Georgia Institute of Technology**, Atlanta, GA, USA | Gpa: 4.00/4.00
Aug 2016 | Current Status: Passed Proposal Exam in Fall 2019 | Detailed list of courses

(Expect: 2020) | (2nd Major) **M.S Student** in **Computer Science** (Dual Degree)
Current | **Georgia Institute of Technology**, Atlanta, GA, USA | Gpa: 4.00/4.00
Jan 2019 | Specialization: **Computing Systems** | Detailed list of courses

May 2014 | Exchange student in **Electrical & Computer Engineering**
Jan 2014 | **University of Illinois at Urbana-Champaign**, Champaign, IL, USA | Gpa: 3.79/4.00

Jul 2014 | Bachelor of Science Degree in **Electronic Engineering** | Advisor: Bo-Cheng Charles Lai
Sep 2010 | **National Chiao Tung University**, Hsinchu City, Taiwan | Gpa: 3.90/4.00
Thesis: "Hardware Exploration on GPGPU"

Computer Skills

Digital Design	System Verilog, Verilog, VHDL, HSPICE, Synopsys Design Compiler, Cadence Virtuoso
Physical Design	Cadence Encounter/Innovus, Mentor Graphics Calibre
Hardware Design	Xilinx FPGA&Vivado, Arduino, Raspberry Pi, EAGLE
Scripting Language	Perl, TCL, Skill, Regular Expression
Serial Language	C++/C, Python
API & Framework	CUDA, OpenCL, OpenGL, OpenMP, POSIX Threads
Software	Matlab, Mathematica, Keyshot
Systems	Linux environment
Revision Control	Git, Rational ClearCase

Work Experience

Current | Server Administrator at Integrated Circuits & Systems Research Lab (ICSRL), GaTech
Nov 2017 | - Install, configure, administer, and optimize ICSRL servers
- Maintain all PDK, IPs, and Tape out flow

Current | Researcher at Integrated Circuits & Systems Research Lab (ICSRL), GaTech
Aug 2016 | Thesis: "Hardware Dynamical System for Solving Optimization Problems"

Aug 2019 | Interim Engineering Intern at Qualcomm Inc., Raleigh, NC
May 2019 | *CR&D Team*
- Develop near-memory computing by optimizing SRAM sub-array based on target DNN workloads for ML accelerators.

Jan 2018 | Vice President of Taiwan Student Association of GaTech, USA
Aug 2017 | - Held several events

Aug 2017 | Marketing Engineer at M2COMM Inc., Taiwan
Sep 2015 | *Business Team*
- Company website hosting (Front-End & Back-End)

Sep 2014 Sep 2013	Intern at M2COMM Inc., Taiwan *Production Team & Hardware Team (2 terms)* - Team leader for building mass production auto test station
Aug 2012 Sep 2011	Vice President of Student Organization of NCTU Dept. EE, Taiwan - Fund raised up to $4000 for the department

Awards

May 2019	Taiwan Government Scholarship to Study Abroad (GSSA)
May 2019	Qualcomm Innovation Fellowship Award
May 2019	Chih Foundation Graduate Student Research Publication Award
Apr 2019	ECE Graduate TA Excellence Award (GaTech)
Jan 2014	Exchange Program Scholarship to University of Illinois at Urbana-Champaign (NCTU)
Jun 2011	Calculus Award (Top 20/1166) (NCTU)
Jan 2011	Calculus Award (Top 20/1202) (NCTU)
Sep 2010	Merit Scholarships in the department of Electrics & Engineering (NCTU)

Publications

1. **Optimo: A 65nm 279gops/w 16b programmable spatial-array-processor with on-chip network for solving distributed optimizations via the alternating direction method of multipliers**
   M. Chang, L. Lin, J. Romberg, and A. Raychowdhury
   IEEE JSSC, 2019.

2. **A 65nm 8-3b 1.0-0.36v 9.1-1.1tops/w hybrid digital-mixed-signal computing platform for accelerating swarm robotics**
   N. Cao, M. Chang, and A. Raychowdhury
   IEEE JSSC, 2019.

3. **A ferrofet based in-memory processor for solving distributed and iterative optimizations via least-squares method**
   I. Yoon, M. Chang, A. Raychowdhury et al.
   IEEE JXCDC, 2019.

4. **Efficient signal reconstruction via distributed least square optimization on a systolic fpga architecture**
   M. Chang, S. Gangopadhyay, T. Hamam, J. Romberg, and A. Raychowdhury
   IEEE ICASSP, 2019.

5. **65nm 49core processor array with hierarchical multicast on chip network for solving distributed optimizations**
   M. Chang, L. Lin, J. Romberg, and A. Raychowdhury
   IEEE CICC, 2019.

6. **14.1 a 65nm 1.1-to-9.1tops/w hybrid-digital-mixed signal computing platform for accelerating model-based and model-free swarm robotics**
   N. Cao, M. Chang, and A. Raychowdhury
   IEEE ISSCC, 2019.

7. **A fefet based processing-in-memory architecture for solving distributed least-square optimizations**
   I. Yoon, M. Chang, A. Raychowdhury et al.
   76th DRC, 2018.

Projects

Spring 2019	Implementation of Dynamo: Amazon's Highly Available Key-value Store - Distributed key-value store - Focus on scalability, availability, and resilience to temporary node failures	|Language: C/C++

Spring 2019 | Implementation of LRVM: Lightweight recoverable virtual memory |Language: C

Spring 2019 | Inter-process Communication Services |Language: C
- Synchronous/Asynchronous service calls support
- Quality of Service support

Spring 2019 | Implementation of Xen Credit-based schedulers |Language: C
- Multi-Processor support
- Local runqueue

Spring 2019 | Variation-Aware SWAP-based BidiRectional heuristic search algorithm (SABRE) |Language: Python
- Environment: IBM Q Melbourne (14 qubits)
- Metrics: Effective improvement in PST and compile time

Fall 2018 | Chip-Multiprocessor Memory System Emulator with OoO Pipeline & Precise Exceptions |Language: C/C++
- Multi-core & Multi-level cache emulator with DRAM based main memory

Spring 2018 | Post-Dominator (PDOM) algorithm for branch divergence in GPUs |Language: C/C++
- Implemented with mini-harp parallel processor
- Thread Block Compaction (TBC) supported

Spring 2018 | Sobel Operator based Image Edge Detection on FPGA |Language: Verilog
- Extracted pixels from an image and convolved with sobel kernel for edge detection

Fall 2017 | 512x512 Pixels Mandelbrot Set Display using OpenGL & CUDA |Language: C/C++
- Use CUDA & OpenGL API to compute and display a visual image of the *Mandelbrot Set*

Spring 2017 | 45nm 1.81GHz 6T SRAM Array Design with Bubble Razor and SSCFF @ Vdd=1V |Tool: Cadence Virtuoso
- Front-End design : Bubble Razor, SSCFF, and full-system design

Fall 2016 | High Speed and Low Power 45nm 1.9GHz 6T SRAM Array @ Vdd=1V |Tool: Cadence Virtuoso
- Front-End design : SRAM peripherals, SRAM cell, Sense Amplifier, and Full-System Design
- Back-End design : Full-System layout with clean DRC & LVS & PEX

Fall 2016 | A Low Power Noise Cancelling Wideband Direct Down-Conversion Receiver @ Vdd=1.2V |Tool: Agilent ADS
- Target : IEEE 802.11 a/g WLAN standard with 2 frequency bands of 2.4GHz and 5GHz
- LNA Architecture : Differential common gate LNA with noise-cancelling
- Mixer Architecture : Gilbert mixer

Spring 2014 | 180nm Unity gain buffer circuit @ Vdd=1.8V |Tool: Cadence Virtuoso
- Closed loop bandwidth: 132.7MHz
- Output swing: 509.33mV
- DC loop gain: 72.6dB
- Loop phase margin: 65.51°
- LF PSRR: -94.67dB
- Power consumption: 1.8mW

Spring 2014 | Stencil computation in MPI parallel ways |Language: C/C++ & OpenMP
- Implement a five-point stencil computation with Jacobi style

Spring 2014 | Real-Time Speech-Driven Facial Animation |Language: Matlab

- Given a set of audio and image features, train a mapping between the two.
- Generate a set of test images given a set of audio features.

Fall 2013 | High Performance Single-View Conversion on Heterogeneous Throughput Processors | Language: C/C++ & CUDA

Fall 2013 | Multivariate density estimation by Bayesian Sequential Partitioning | Language: C/C++ & OpenCL

Spring 2013 | Region Query Problem | Language: C/C++

- # of polygons contained by a given (rectangular) window area
- # of polygons interacting with a given window area
- # of polygons interacting with given window
- # of polygons whose areas are less than a given number
- % of the given window area that is covered by polygons

Spring 2012 | Gate-Level Logic Waveform Evaluator | Language: C/C++

- Generate the waveform from the gate-level logic and the corresponding pattern

Fall 2011 | Timing analysis of circuits | Language: C/C++

- Analyze the timing of the given circuit using topological sort with propagation delay

Course List

ECE Ph.D. Program at GaTech, Atlanta

Course #	Course	Instructor	Term	Grade
ECE 6130	Advanced VLSI Systems	Saibal Mukhopadhyay	Fall 2016	A
ECE 6420	Wireless IC Design	Hua Wang	Fall 2016	A
ECE 8903	Special Problems	Arijit Raychowdhury	Fall 2016	A
ECE 6122	Advanced Programming Techniques	George F Riley	Spring 2017	A
ECE 8893	Digital Systems at Nanometer Nodes	Saibal Mukhopadhyay	Spring 2017	A
ECE 8843	Mathematical Foundations of Machine Learning	Justin Keith Romberg	Fall 2017	A
ECE 6133	Physical Design Automation-VLSI	Sung Kyu Lim	Spring 2018	A
ECE 8813	Advanced Digital Design with Verilog	Timothy J Brothers	Spring 2018	A
ECE 8823	GPU Architecture	Sudhakar Yalamanchili	Spring 2018	A
ECE 6500	Fourier Tech & Signal Analysis	David Citrin	Spring 2019	A
ECE 8853	Intro to Quantum Systems	Moinuddin K. Qureshi	Spring 2019	A
			Gpa	**4.00/4.00**

CS M.S Program at GaTech, Atlanta

Course #	Course	Instructor	Term	Grade
CS 6290	High Perform Computer Architecture	Moinuddin K. Qureshi	Fall 2018	A
CS 6505	Computability & Algorithms	Santosh Vempala	Fall 2018	A
CS 6210	Advanced Operating Systems	Ada Gavrilovska	Spring 2019	A
CS 6220	Big Data System & Analytics	Ling Liu	Fall 2019	-
CSE 6230	High Perf Parallel Computing	Tobin Gregory Isaac	Fall 2019	-
CSE 6242	Data & Visual Analytics	Duenhorng Chau	Fall 2019	-
			Gpa	**4.00/4.00**