Latest Mobile Phone Processors & Their Features

CSE216: Microprocessor Interfacing & Assembly Language
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Introduction

01

Today, we're examining something extraordinary.

02

These processors aren't just components - they're architectural marvels that represent the pinnacle of semiconductor engineering.

03

We'll explore how modern SoCs implement advanced microprocessor concepts directly relevant to our interfacing studies.

The Leading Mobile Processors

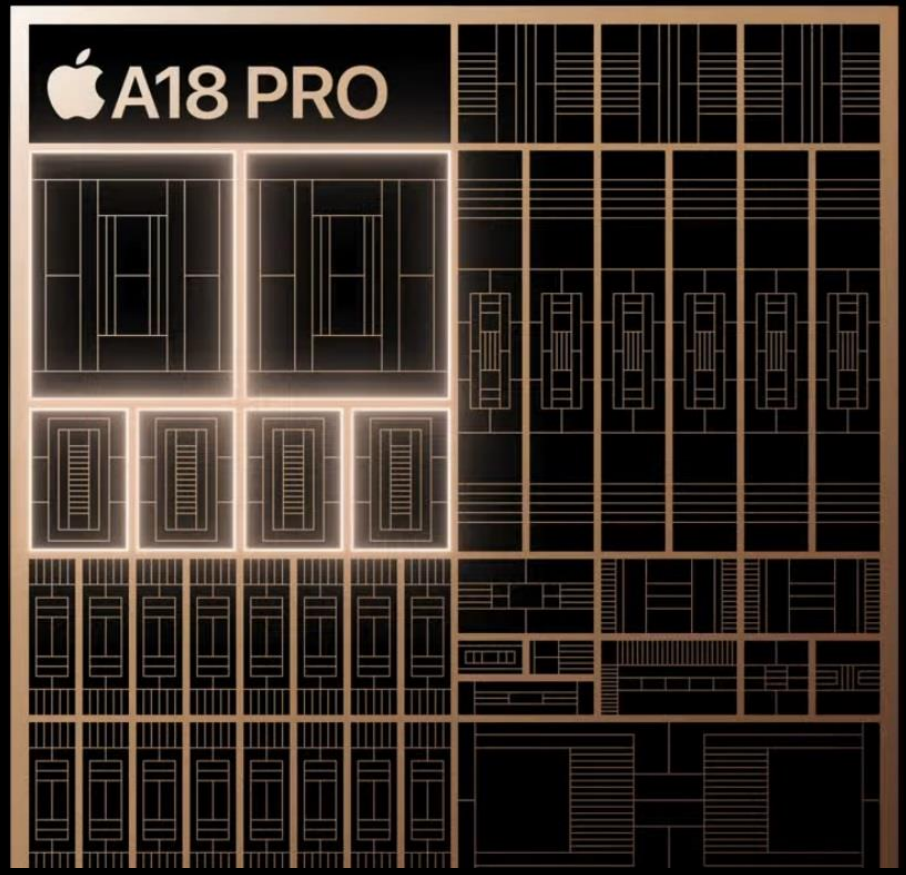
These four chips define the cutting edge of mobile computing:

- Apple A18 Pro
- Qualcomm Snapdragon 8 Elite
- MediaTek Dimensity 9400+
- Samsung Exynos 2400

Apple A18 Pro

The A18 Pro showcases heterogeneous core design principles:

- **3nm TSMC process**
- **CPU architecture:** Asymmetric big.LITTLE implementation
  - 2 performance cores (ARMv9.2-A) @ 4.05 GHz with dedicated instruction decoders
  - 4 efficiency cores @ 2.42 GHz with shared decoder logic
- **16MB L2 cache**
- **Neural Engine:** 16-core matrix multiplication accelerator delivering 35 TOPS
- **ISA extensions:** Advanced SIMD, AMX (Apple Matrix Extensions)



Qualcomm Snapdragon 8 Elite

The Snapdragon architecture employs advanced interconnect topology:

- **3nm TSMC process**
- **CPU implementation**
  - Performance Cores: 2×4.32 GHz Oryon (Phoenix L)
  - Efficiency Cores: 6×3.53 GHz Oryon (Phoenix M)
- **System-level cache:** 12MB L3
- **NPU integration:** Hexagon processor with tensor accelerator units
- **ISA extensions:** ARM v9.2-A

MediaTek Dimensity 9400+

The Dimensity 9400+ demonstrates sophisticated core clustering:

- **3nm TSMC process**
- **CPU microarchitecture:**
  - 1×Cortex-X925 @ 3.63 GHz with 2MB L2 cache
  - 3×Cortex-X4 cores with shared 6MB L2 cache
  - 4×Cortex-A720 cores with 4MB L3 cache interconnect
- **Memory subsystem:** LPDDR5X controller with 10667 Mbps throughput
- **APU design:** 8th-gen AI processor with 80% faster language model inference
- **Instruction set optimizations:** ARM v9.2-A with custom extensions

Samsung Exynos 2400

The Exynos demonstrates sophisticated power management architecture:

- **4nm Samsung LPP+ process** - In-house fabrication
- **CPU core layout:** Deca-core configuration with adaptive clock domains
  - 1×Cortex-X4 @ 3.2 GHz (prime core)
  - 2×Cortex-A720 @ 2.9 GHz (performance cluster)
  - 3×Cortex-A720 @ 2.6 GHz (balanced cluster)
  - 4×Cortex-A520 @ 1.95 GHz (efficiency cluster)
- **Thermal management:** Dynamic voltage/frequency scaling with per-core granularity
- **GPU implementation:** AMD RDNA 3-based Xclipse 940 with ray tracing hardware
- **NPU design:** 17K MAC neural engine with specialized matrix operations

Architectural Comparisons

Processor	ISA	Node	Peak CPU	Cache Architecture
Apple A18 Pro	ARMv9.2-A	3nm	4.20 Ghz	16MB unified L2
Snapdragon 8 Elite	ARMv9.2-A	3nm	4.32 Ghz	12MB L3
Dimensity 9400+	ARMv9.2-A	3nm	3.63 Ghz	12MB distributed
Exynos 2400	ARMv9-A	4nm	3.20 Ghz	8MB L3

Key Trends

Process node advancement: Race to 3nm and beyond

AI acceleration: Specialized NPUs in all flagship chips

Graphics convergence: Ray tracing across all platforms

Performance-efficiency balance: Heterogeneous cores

Q&A

Thank you for your attention!

Thank You!