CIRCULARITY

CYLINDRICITY

PROFILE OF ANY LINE

PROJECTED TOLERANCE ZONE

## 1. GENERAL:

a. THIS PCB SHALL BE MANUFACTURED IN
ACCORDANCE WITH SIERRA WIRELESS RIGIG PCB
GENERAL SPECIFICATION (DOCUMMENT #4112171).
INTERPRET DRAWINGS AS PER IPC-2222. INTERPRET
DIMENSIONS AS PER ASME Y14.5 WORKMANSHIP
TO COMPLY WITH IPC-6012 CLASS 2, AND
INSPECTED AS PER IPC-600. PCB BOW AND TWIST
TO BE 0.75% MAX. IN CASE OF DISCREPAENCY IN
THE REQUIREMENTS SPECS, THESE NOTES SHALL
TAKE PRECIDENCE. IN CASE OF DISCREPANCY IN THE
DATA, THE GERBERS SHALL TAKE PRECEDENCE. THE
EXTRACTED GERBERS MUST MATCH THE IPC-D-356-A
NETLIST PROVIDED. NOTIFY SIERRA WIRELESS IF
THEY DO NOT MATCH.

### 2. MATERIAL:

a. THE MATERIAL CHOSEN IS TU-747HF ALONG WITH THE STACKUP SHOWN ON PAGE 2. NO DEVIATIONS TO THE STACKUP UNLESS APPROVED BY SIERRA WIRELESS IN ADVANCE. LAMINATE AND PREPREG MATERIAL TO BE LOW COST, CAPABLE OF Pb FREE SOLDERING WITH >= 3X HEAT CYCLES, AND BE HALOGEN FREE. MATERIAL SHALL HAVE Tg >= 150C, AND PASS T-260/T-288 TESTING. MATERIAL SHALL HAVE A FLAMMABILITY RATING OF UL94V-0 OR BETTER.

### 3. DRILLING AND PLATING:

a. HOLE SIZES LISTED IN DRILL CHARTS ARE FINISHED HOLE SIZES. ALL HOLES LOCATED WITHIN 0.15mm TRUE POSITION DIAMETER. ALL PLATED HOLES SURROUNDED BY LANDS SHALL HAVE NO BREAKOUT. VENDOR OK TO TEARDROP TRACE—JUNCTION IN ORDER TO AVOID BREAKOUT. REMOVE NON FUNCTIONAL PADS ON INTERNAL LAYERS. PLATING IN PTH BARREL SHALL BE ACCORDING TO IPC—6012 CLASS 2. THIS BOARD USES SOLID COPPER FILLED VIAS FOR L1—L2 & L5—L6.

#### 4. SURFACE FINISH:

a. APPLY LPI SOLDERMASK PER IPC-SM-840 CLASS T TO BOTH SIDES OF THE BOARD OVER BARE COPPER. COLOR RED SOLDERMASK REQUIRED BETWEEN ALL CONDUCTIVE SURFACES. SOLDERMASK IS NOT ALLOWED ON SOLDERABLE SURFACES. VENDOR IS ALLOWED TO MODIFY OPENINGS IF NEEDED. THE SURFACE FINISH SHALL BE ENIG. WITH MINIMUM 2uIN GOLD OVER 100-300 uIN NICKEL. SILKSCREEN IS NOT ALLOWED ON SOLDERABLE SURFACES. VENDOR ALLOWED TO CLIP SILKSCREEN LAYER AGAINST SOLDERMASK OPENINGS IF NEEDED. COLOR WHITE. REMOVE ALL BURRS AND SHARP EDGES.

# 5. TEST REQUIREMENTS:

a. ALL BOARDS SHALL BE 100% ELECTRICALY TESTED AS DEFINED BY IPC-9252 AND MARKED WITH STAMP WHEN THEY HAVE PASSED.
THIS IS A CONTROLLED IMPEDANCE DESIGN AS DEFINED IN THE STACKUP DETAIL IN THIS DOCUMENT.

# 6. TRACEABILITY:

a. BOARD SUPPLIER SHALL BE UL RECOGNIZED, AND SHALL LOCATE MANUFACTURING TRACEABILITY, CONTRY OF ORIGIN, AND UL RECOGNIZED MARKINGS ON THE BACK AS SHOWN, USING A PERMANENT, NON-CONDUCTIVE EPOXY INK. PCBS ARE TO BE CLEAN AND FREE OF ALL FOREIGN MATERIALS AND PACKAGED FOR MOISTURE SENSITIVE PART LEVELS PER EIA JEDEC STANDARD JESD22-A112.

Drill Schedule - Thru

Hole Symbol	Hole Size	Count	Plated	Tolerance			
⊞	0.25000	2920	YES	+/- 0.07600			
Φ	0.40000	8	YES	+/- 0.07600			
В	0.55000	16	YES	+/- 0.07600			
Ө	0.60000	8	YES	+/- 0.08000			
Ш	0.65000	16	YES	+/- 0.07600			
Ф	0.83000	16	YES	+/- 0.07600			
	0.90000	24	YES	+/- 0.08000			
	1.01000	8	YES	+/- 0.13000			
	1.20000	152	YES	+/- 0.07600			
	1.30000	12	YES	+/- 0.07600			
⊗	3.00000	8	YES	+/- 0.12500			
0	3.50000	16	YES	+/- 0.15000			
•	1.40000	4	NO	+/- 0.05000			
⊗	1.50000	8	NO	+/- 0.08000			
Ф	1.55000	8	NO	+/- 0.12500			
×	4.00000	4	NO	+/- 0.05000			

0.25000

Drill Schedule (Physical Range 5 - 6)

0.10000

Hole Symbol | Hole Size | Count

4836

6496

YES

Plated

YES

+/- 0.07600

Tolerance

+/- 0.07600

TOP VIEW

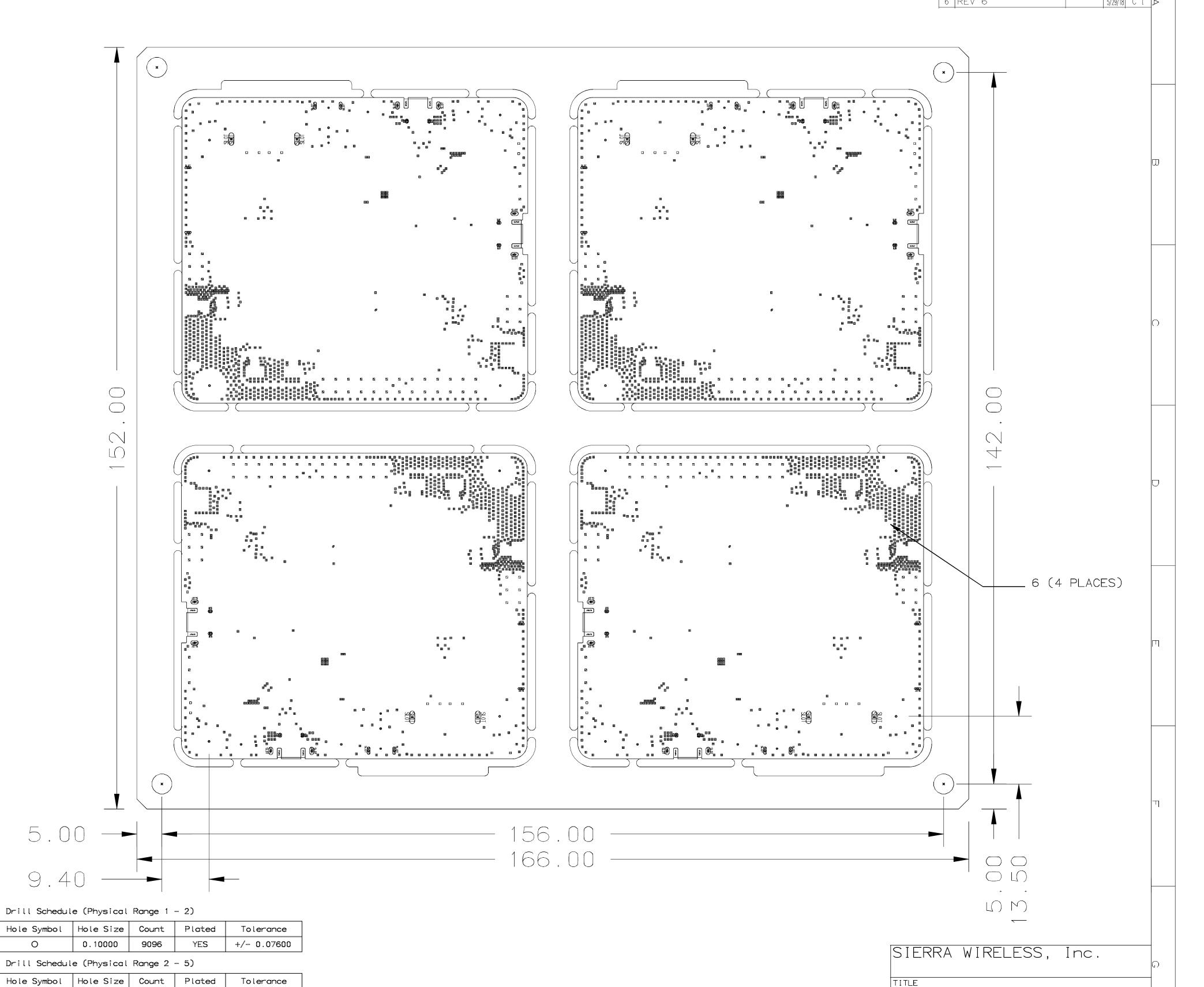
REVISION RECORD	ECO NUMBER	DATE	DRAWN
INITIAL RELEASE		10/13/16	MBS
REV 2		2/2/17	MBS
REV 3		3/25/17	MBS
REV 4		4/9/17	MBS
REV 5		6/26/17	MBS
REV 6		5/20/19	ΩI

FABRICATION DRAWING,

MangOH Red

SHEET 1 of 2

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6L 1+4+1 stackup of board thickness		1.6 mm +/-10%	Thicknes s(mil)	Thicknes s(mm)		
				Solder mask	1	0.0254
L1				copper foil + plated	1.6	0.0406
				Prepreg 1080x1	2.8	0.0711
L2				copper foil + plated	1.3	0.0330
				Prepreg 1080x2	6.2	0.1575
L3	DTH	DODLI		copper foil 0.5 oz	0.6	0.0152
	PTH PTH 2-5	CORE		CORE	35	0.8890
L4		2-3		copper foil 0.5 oz	0.6	0.0152
				Prepreg 1080x2	6.2	0.1575
L5				copper foil + plated	1.3	0.0330
				Prepreg 1080x1	2.8	0.0711
L6				copper foil + plated	1.6	0.0406
				Solder mask	1	0.0254
•			_	Total:	62	1.5748

layer	Reference layer	Туре	Impedance control(+/- 10%)	Customer Impedance trace width/space(mil)	Customer Impedance trace width/space(mm)	Impedance trace width/space(mil)	Impedance trace width/space(mm)	Evaluated Impedanc e (ohm)
L1	L2	Differential	90ohm	5.0/12.0	0.127 / 0.3048			
L1	L3	Single	50ohm	19.5	0.4950			
L2	L1/L3	Single	50ohm	3.2	0.0810	3.20		49.2
L2	L1/L3	Differential	90ohm	3.7/9.3	0.094 / 0.236	3.7/9.3		90
L4	L3/L5	Single	50ohm	8.3	0.211			
L4	L3/L5	Differential	90ohm	11/22	0.28/0.56			
L5	L4/L6	Single	50ohm	3.2	0.0810	3.20		49.2
L5	L4/L6	Differential	90ohm	3.7/9.3	0.094 / 0.236	3.7/9.3		90
L6	L4	Single	50ohm	19.5	0.4950			

#### Notes:

All dielectric layer thickness are estimated based on inner layer copper remain ratio 70% Mid Tg and Halogen Free material and propose to use TU-747HF