



UNIVERZITET U NOVOM SADU
FAKULTET TEHNIČKIH NAUKA
KATEDRA ZA ELEKTRONIKU



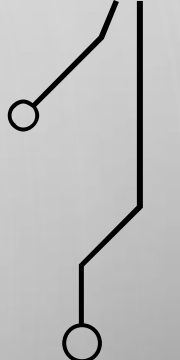
HARDVERSKA IMPLEMENTACIJA AKCELERATORA ZA ISPRAVLJANJE SADRŽAJA SLIKA NA ZYBO RAZVOJNOJ PLOČI

U Novom Sadu,
28. oktobra 2022.

Srđan Babić EE 53/2014



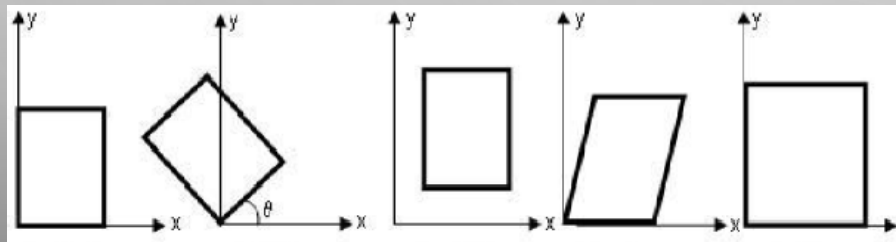
MOTIVACIJA

- Unapređenje postojećeg jezgra
 - Standardni format slike
 - Programabilnost
 - Frekvencija rada
 - Pretprocesiranje slike za rad klasifikatora cifara
 - Rukopis može biti zakrivljen
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ALGORITAM

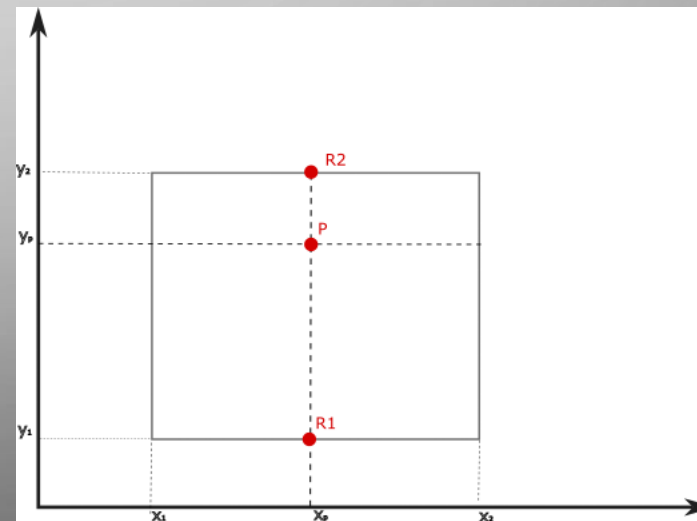
- Afina transformacija

- $$\begin{bmatrix} x_p \\ y_p \end{bmatrix} = \begin{bmatrix} 1 & skew & -0.5 * img_dim * skew \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} x \\ y \\ 1 \end{bmatrix}$$



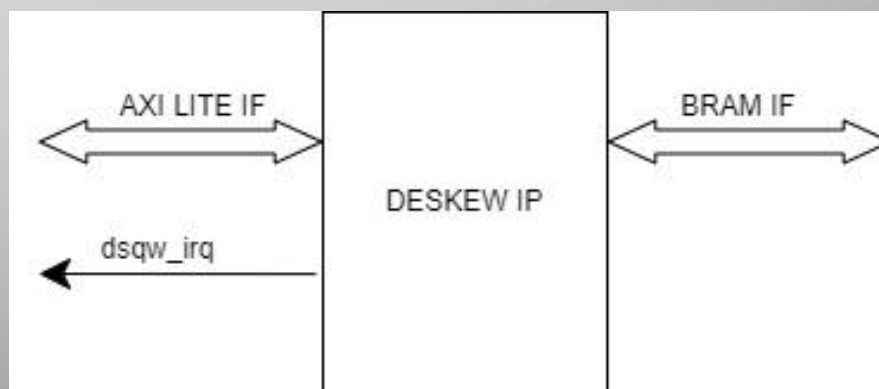
- Interpolacija

- $$P = R2 + ((y_p - y1) / (y2 - y1)) * (R1 - R2)$$



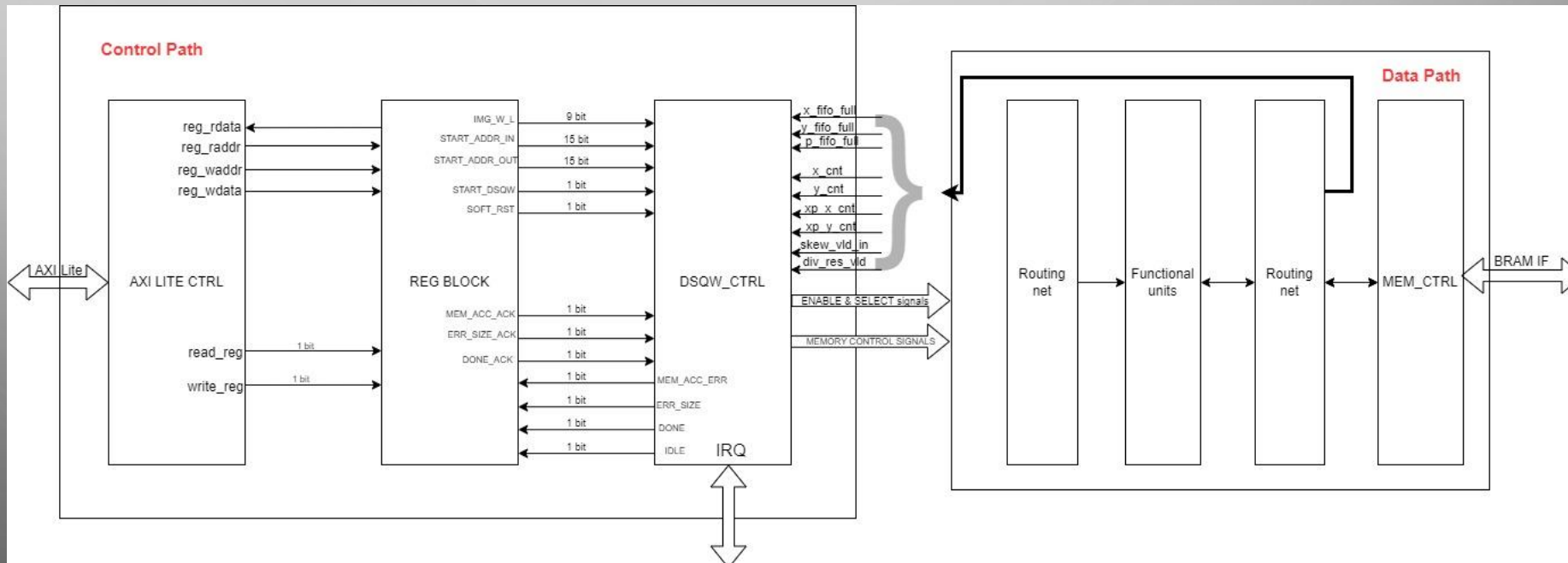
PROJEKTOVANJE MIKROARHITEKTURE

- Interfejsi jezgra
 - AXI LITE
 - BRAM
 - Linija prekida



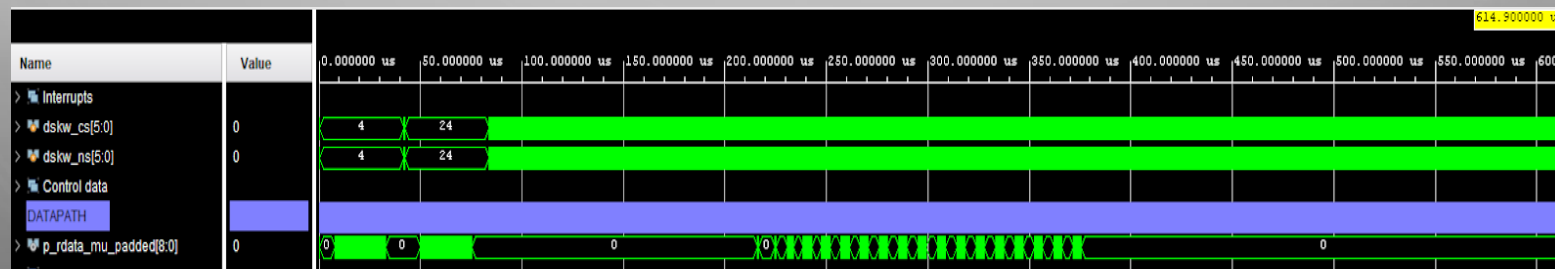
PROJEKTOVANJE MIKROARHITEKTURE

- RTL metodologija
- Partitionisanje na nivou IP-ja

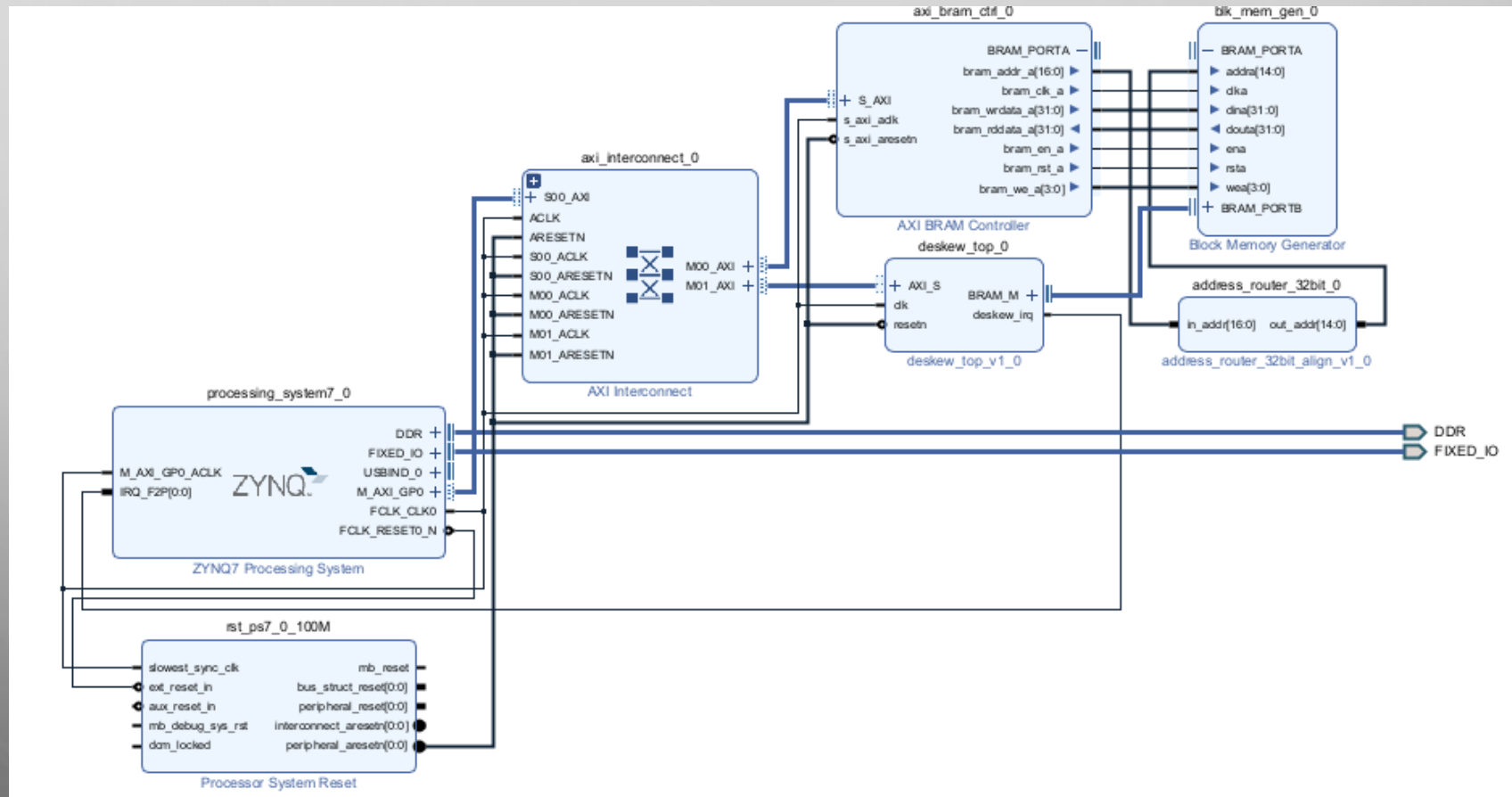


BIHEVIORALNA SIMULACIJA - PERFORMANSE

- Provera funkcionalnosti
- Provera protoka
 - Za sliku 64 x 64 piksela predviđeno 19254
 - Postignuto (bez učitavanja slike) 61490

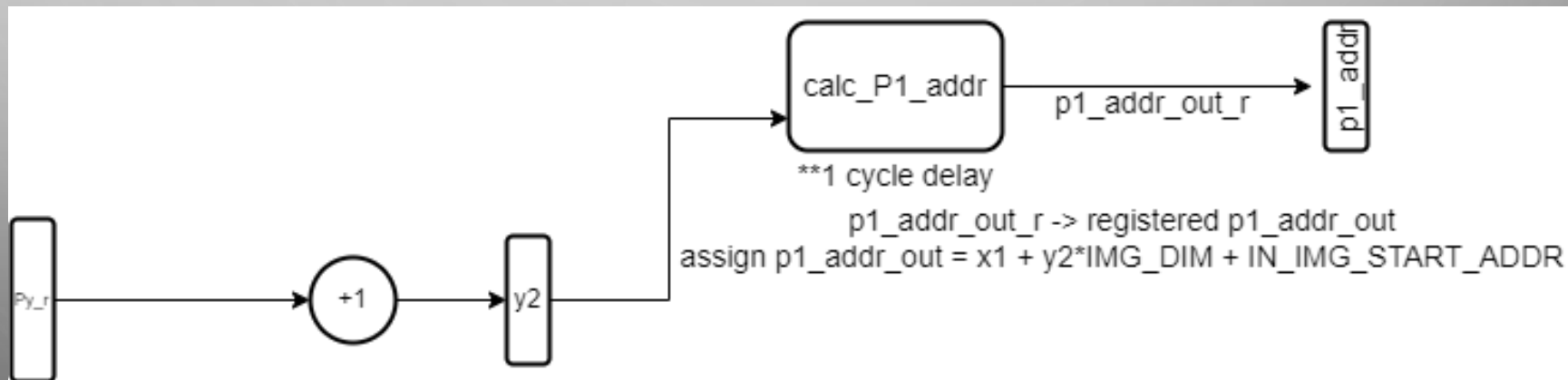


INTEGRACIJA JEZGRA I PROJEKTOVANJE SISTEMA



VREMENSKA ANALIZA

- Postignuta frekvencija rada 100MHz
 - Procenjena 94.25MHz
- Kritična putanja zbog neoptimizovane kaskadne veze množača i sabirača



RAZVOJ SOFTVERA

- Unapred parsirana slika
 - Niz osmobitnih neoznačenih brojeva
- Učitavanje u memoriju
- Programiranje IP-ja
- Čekanje na prekid
 - Implementirana servisna rutina
- Čitanje izlazne slike

```
int main()
{
    int Status; //IRQ Init fucntion status
    u32 img_array_length;
    u32 in_img_ptr;
    u32 out_img_ptr;
    u32 img_dim;

    DSQW_INTERRUPTS_CLEARED = 0;

    init_platform();

    /* INITIALIZE SYSTEM INTERRUPTS*/
    Status = InitDeskewIrq(XPAR_PS7_SCUGIC_0_DEVICE_ID);
    if (Status != XST_SUCCESS)
    {
        xil_printf("IRQ INIT FAILED. Status : %0d\n", Status);
        return Status;
    }

    /*CONFIGURE IMAGE PARAMETERS*/
    img_array_length = 65536;
    img_dim = 256;
    in_img_ptr = 0x00000000;
    out_img_ptr = 0x00010000;

    /*LOAD IMAGE TO MEMORY*/
    load_input_image(in_img_ptr, img_array_length);

    /*Kick-off the Deskewer*/
    ProgramDeskewIp(in_img_ptr, out_img_ptr, img_dim);

    xil_printf("Deskew Programmed!\n");

    /*Wait for the interrupt*/
    while(DSQW_INTERRUPTS_CLEARED != 1)
    {
        sleep(10);
    }

    DSQW_INTERRUPTS_CLEARED = 0;

    xil_printf("Interrupt acknowledged!\n");

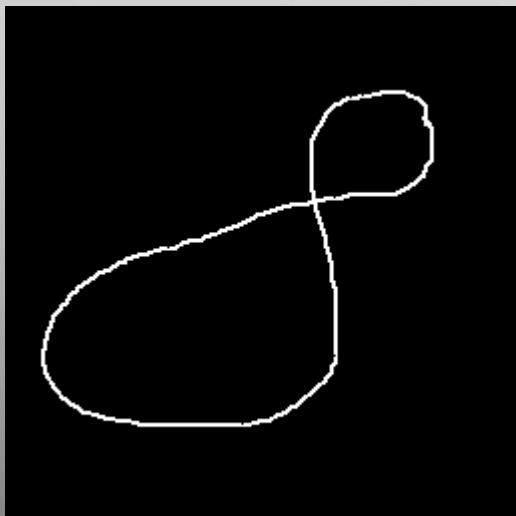
    /*READ OUTPUT IMAGE FROM MEMORY*/
    read_output_image(out_img_ptr, img_array_length);

    /*Format the rest of the print*/
    xil_printf("\n\n");

    /*LOAD IMAGE TO MEMORY*/
    print("Deskew done\n\r");
    cleanup_platform();
    return 0;
}
```

REZULTAT OBRADJE SLIKE

- Ulazna slika

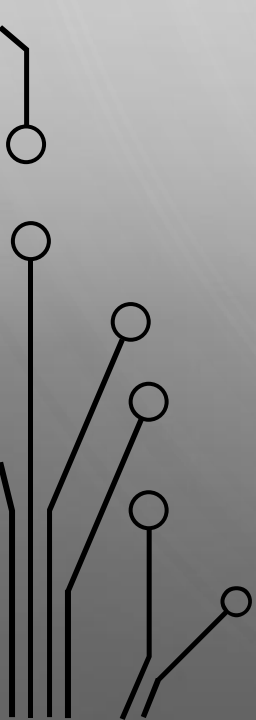
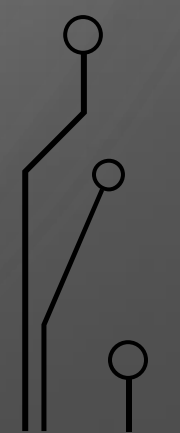


- Izlazna slika





MOGUĆA UNAPREĐENJA

- Slika crnih cifara na beloј pozadini
 - Korisnička aplikacija za dinamičko slanje slika
 - Brže učitavanje slike koristeći DMA
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The background features a light gray gradient with faint, concentric circular lines. In the four corners, there are decorative black line art elements resembling electronic circuit traces or a stylized tree structure, with small circles at the end of the lines.

Hvala na pažnji!