DD LAB5

一、地點：工學501A

二、準備時間：4/27 1924-1932

三、DEMO時間：4/27 1932-1940

四、評分方式

    1. 利用 testbench於命令提示字元中顯示生日(20%)
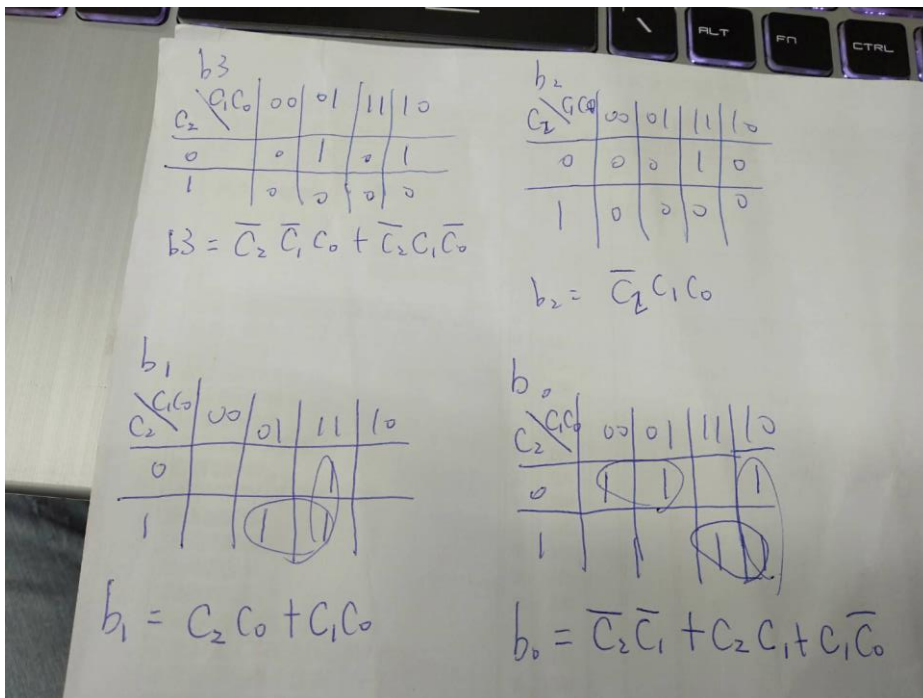
        (1)路徑 C:\Users\User\Desktop\CO\2019_COLAB2\iverilog\bin開啟cmd

        (2)$iverilog -o test tb_lab5.v

        (3)$vvp test

        (4)化簡過程

Cnt 2	Cnt 1	Cnt 0	birth_num3	birth_num2	birth_num1	birth_num0	Num
0	0	0	0	0	0	1	1
0	0	1	1	0	0	1	9
0	1	0	1	0	0	1	9
0	1	1	0	1	1	0	6
1	0	0	0	0	0	0	0
1	0	1	0	0	1	0	2
1	1	0	0	0	0	1	1
1	1	1	0	0	1	1	3

化簡成SOP

birth_num[3] = (!cnt[2] & !cnt[1] & cnt[0]) | (!cnt[2] & cnt[1] & !cnt[0])

birth_num[2] = (!cnt[2] & cnt[1] & cnt[0])

birth_num[1] = (cnt[2] & cnt[0]) | (cnt[1] & cnt[0])

birth_num[0] = (!cnt[2] & !cnt[1]) | (cnt[2] & cnt[1]) | (cnt[1] & !cnt[0])

(5)結果

```
C:\Users\User\Desktop\C0\2019_COLAB2\iverilog\bin>vvp test
VCD info: dumpfile lab5.fsdb opened for output.
           250005   cnt = 1, ,birth =   9, output = 0010000
           500005   cnt = 2, ,birth =   9, output = 0010000
           750005   cnt = 3, ,birth =   6, output = 0000010
          1000005   cnt = 4, ,birth =   0, output = 1000000
          1250005   cnt = 5, ,birth =   2, output = 0100100
          1500005   cnt = 6, ,birth =   1, output = 1111001
          1750005   cnt = 7, ,birth =   3, output = 0110000
          2000005   cnt = 0, ,birth =   1, output = 1111001
          2250005   cnt = 1, ,birth =   9, output = 0010000
          2500005   cnt = 2, ,birth =   9, output = 0010000
          2750005   cnt = 3, ,birth =   6, output = 0000010
          3000005   cnt = 4, ,birth =   0, output = 1000000
          3250005   cnt = 5, ,birth =   2, output = 0100100
          3500005   cnt = 6, ,birth =   1, output = 1111001
          3750005   cnt = 7, ,birth =   3, output = 0110000
          4000005   cnt = 0, ,birth =   1, output = 1111001
          4250005   cnt = 1, ,birth =   9, output = 0010000
          4500005   cnt = 2, ,birth =   9, output = 0010000
          4750005   cnt = 3, ,birth =   6, output = 0000010
          5000005   cnt = 4, ,birth =   0, output = 1000000
```

2. 以sw14為開關，為0時最右邊的七段顯示器會依序顯示0~7，為1時則會依序顯示出自己的生
日　(60%)
　　　(1)須帶身分證
　　　(2)Sw 15為rst　用Sw14 on 顯示生日八碼　Sw14 off顯示0-7
　　　(3)Case版本設計：偵測到sw14 on　(mod)就把cnt0-7對應到19960213，
　　　　　　　　　　　　　　　若sw14 off (!mod)就把cnt0-7對應01234567

```verilog
always@(posedge clk) begin
    if ( mod ) begin
        case(cnt)
            3'b000:seg_number = 4'd1;
            3'b001:seg_number = 4'd9;
            3'b010:seg_number = 4'd9;
            3'b011:seg_number = 4'd6;
            3'b100:seg_number = 4'd0;
            3'b101:seg_number = 4'd2;
            3'b110:seg_number = 4'd1;
            3'b111:seg_number = 4'd3;
        endcase
    end
    else begin
        case(cnt)
            3'b000:seg_number = 4'd0;
            3'b001:seg_number = 4'd1;
            3'b010:seg_number = 4'd2;
            3'b011:seg_number = 4'd3;
            3'b100:seg_number = 4'd4;
            3'b101:seg_number = 4'd5;
            3'b110:seg_number = 4'd6;
            3'b111:seg_number = 4'd7;
        endcase
    end
```

(4)Gate版本設計：偵測到sw14 on　(mod)就把算好的birth num給seg_number
　　　　　　　　　若sw14 off (!mod)就把cnt0-7對應01234567

```verilog
/////**YOUR_DESIGN**/////
//**CODE_CONVERTER** 19960213//
assign    birth_num[3] = (!cnt[2] & !cnt[1] & cnt[0]) | ( !cnt[2] & cnt[1] & !cnt[0] );
assign    birth_num[2] = (!cnt[2] & cnt[1] & cnt[0] );
assign    birth_num[1] = (cnt[2] & cnt[0]) | (cnt[1] & cnt[0]);
assign    birth_num[0] = (!cnt[2] & !cnt[1]) | (cnt[2] & cnt[1]) | (cnt[1] & !cnt[0]);

always@(posedge clk) begin
    if ( mod ) begin
    //**BCD_to_7SEG
        seg_number = birth_num;
    end

    else begin
        case(cnt)
            3'b000:seg_number = 4'd0;
            3'b001:seg_number = 4'd1;
            3'b010:seg_number = 4'd2;
            3'b011:seg_number = 4'd3;
            3'b100:seg_number = 4'd4;
            3'b101:seg_number = 4'd5;
            3'b110:seg_number = 4'd6;
            3'b111:seg_number = 4'd7;
        endcase
    end
end
```

3.於回饋單上描述比較兩種方法在開發版上合成的差異　（20%）
　　(1)使用case的方法是流程控制結構並非像用邏輯閘一直計算去實現，相對硬體需求上會更
　　加有效率跟省力，並且代碼更易讀
4.問題
　　(1)回饋單的填寫20%是事後給嗎？　因為都是之後才寫回饋單
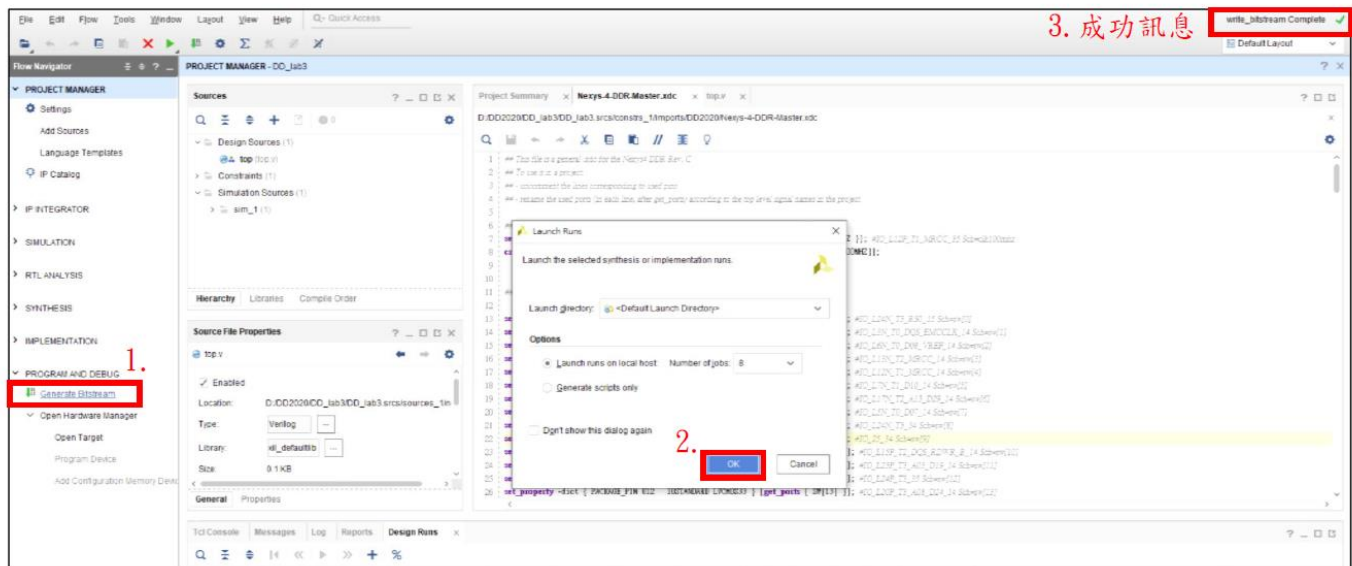　　(2)case和邏輯閘設計兩種方法都需要做嗎？　還是可以做一種就好？
　　(3)用sw14當作開關的意思是說用sw15 當作rst　sw14當作mod去切換0~7或是生日8碼嗎？

5.附錄：燒錄方法說明

■ 專案完成後要將電路燒錄至FPGA上
　□ 左方欄位選擇Generate Bitstream > OK > 等待右上角跳出成功訊息

■ Open Target > Auto Connect > Program Device > Program
　(燒錄完後同學們可以確認switches是否能控制LED明滅)