```
1   module moor_with_default (input clk, rst, j, output w);
2       reg [2:0] ns, ps;
3
4       always @(ps,j) begin
5           ns = 3'b000;
6           case(ps)
7               3'b000: ns = j ? 3'b001 : 3'b000;
8               3'b001: ns = j ? 3'b001 : 3'b010;
9               3'b010: ns = j ? 3'b011 : 3'b000;
10              3'b011: ns = j ? 3'b100 : 3'b010;
11              3'b100: ns = j ? 3'b001 : 3'b010;
12              default: ns = 3'b000;
13          endcase
14      end
15
16      assign w = (ps == 3'b100) ? 1'b1 : 1'b0;
17
18      always @(posedge clk, posedge rst) begin
19          if (rst)
20              ps <= 3'b000;
21          else
22              ps <= ns;
23      end
24  endmodule
```

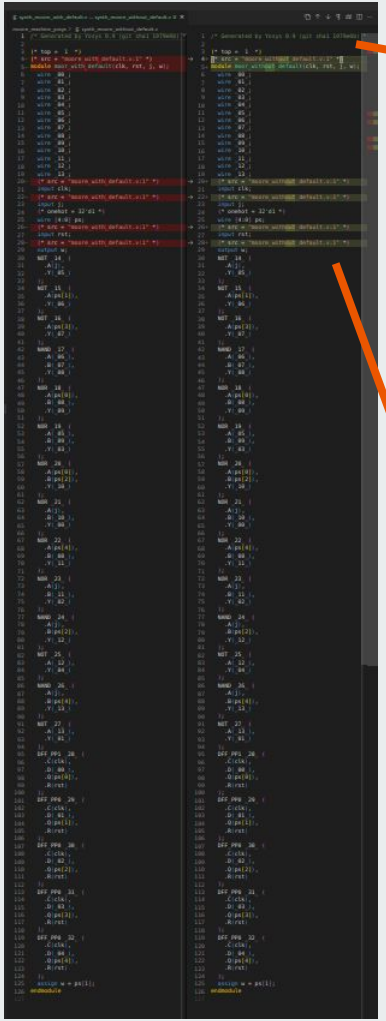
```
591   === moor_with_default ===
592
593       Number of wires:                 16
594       Number of wire bits:             20
595       Number of public wires:           5
596       Number of public wire bits:       9
597       Number of memories:               0
598       Number of memory bits:            0
599       Number of processes:              0
600       Number of cells:                 16
601         $_ANDNOT_                       1
602         $_AND_                          2
603         $_AOI3_                         2
604         $_DFF_PP0_                      4
605         $_DFF_PP1_                      1
606         $_NOR_                          3
607         $_NOT_                          3
```

```
1   module moor_without_default (input clk, rst, j, output w);
2       reg [2:0] ns, ps;
3
4       always @(ps,j) begin
5           ns = 3'b000;
6           case(ps)
7               3'b000: ns = j ? 3'b001 : 3'b000;
8               3'b001: ns = j ? 3'b001 : 3'b010;
9               3'b010: ns = j ? 3'b011 : 3'b000;
10              3'b011: ns = j ? 3'b100 : 3'b010;
11              3'b100: ns = j ? 3'b001 : 3'b010;
12          endcase
13      end
14
15      assign w = (ps == 3'b100) ? 1'b1 : 1'b0;
16
17      always @(posedge clk, posedge rst) begin
18          if (rst)
19              ps <= 3'b000;
20          else
21              ps <= ns;
22      end
23  endmodule
```

```
591   === moor_without_default ===
592
593       Number of wires:                 16
594       Number of wire bits:             20
595       Number of public wires:           5
596       Number of public wire bits:       9
597       Number of memories:               0
598       Number of memory bits:            0
599       Number of processes:              0
600       Number of cells:                 16
601         $_ANDNOT_                       1
602         $_AND_                          2
603         $_AOI3_                         2
604         $_DFF_PP0_                      4
605         $_DFF_PP1_                      1
606         $_NOR_                          3
607         $_NOT_                          3
```

```
=== moor_without_default ===

16
20
5
9
0
0
0
16
1
2
2
4
1
3
3
```

```
=== moor_with_default ===

   Number of wires:                 16
   Number of wire bits:             20
   Number of public wires:           5
   Number of public wire bits:       9
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 16
     $_ANDNOT_                       1
     $_AND_                          2
     $_AOI3_                         2
     $_DFF_PP0_                      4
     $_DFF_PP1_                      1
     $_NOR_                          3
     $_NOT_                          3
```



synth_moore_with_default.v ↔ synth_moore_without_default.v U

moore_machine_yosys > synth_moore_without_default.v

```
1  /* Generated by Yosys 0.9 (git sha1 1979e0b) *
2
3  (* top =  1  *)
4- (* src = "moore_with_default.v:1" *)
5- module moor_with_default(clk, rst, j, w);
6    wire _00_;
7    wire _01_;
8    wire _02_;
9    wire _03_;
10   wire _04_;
11   wire _05_;
12   wire _06_;
13   wire _07_;
14   wire _08_;
15   wire _09_;
16   wire _10_;
17   wire _11_;
18   wire _12_;
19   wire _13_;
20-  (* src = "moore_with_default.v:1" *)
21   input clk;
22-  (* src = "moore_with_default.v:1" *)
23   input j;
24   (* onehot = 32'd1 *)
25   wire [4:0] ps;
26-  (* src = "moore_with_default.v:1" *)
27   input rst;
28-  (* src = "moore_with_default.v:1" *)
29   output w;
30   NOT _14_ (
31     .A(j),
32     .Y(_05_)
33   );
```

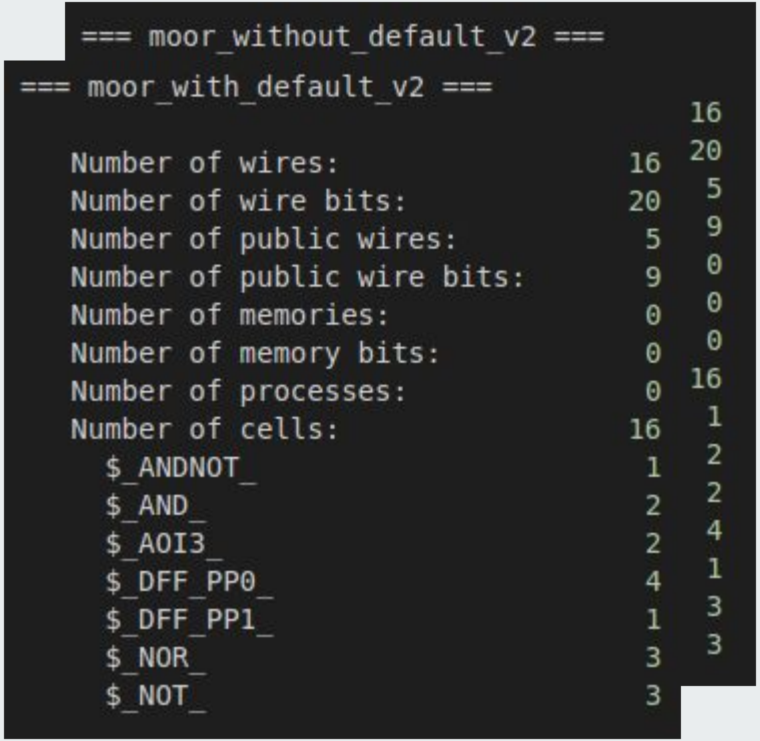
```
1  /* Generated by Yosys 0.9 (git sha1 1979e0b) *
2
3  (* top =  1  *)
4+ (* src = "moore_without_default.v:1" *)
5+ module moor_without_default(clk, rst, j, w);
6    wire _00_;
7    wire _01_;
8    wire _02_;
9    wire _03_;
10   wire _04_;
11   wire _05_;
12   wire _06_;
13   wire _07_;
14   wire _08_;
15   wire _09_;
16   wire _10_;
17   wire _11_;
18   wire _12_;
19   wire _13_;
20+  (* src = "moore_without_default.v:1" *)
21   input clk;
22+  (* src = "moore_without_default.v:1" *)
23   input j;
24   (* onehot = 32'd1 *)
25   wire [4:0] ps;
26+  (* src = "moore_without_default.v:1" *)
27   input rst;
28+  (* src = "moore_without_default.v:1" *)
29   output w;
30   NOT _14_ (
31     .A(j),
32     .Y(_05_)
33   );
```

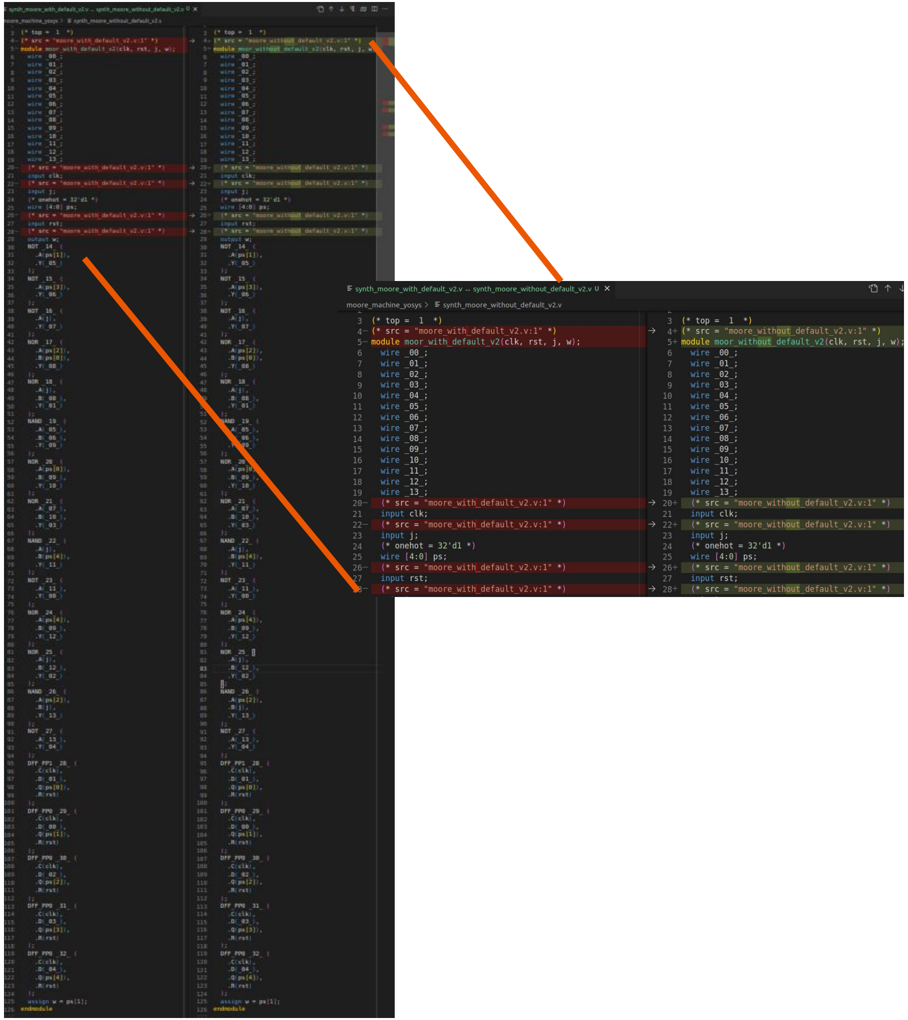
```
1   module moor_with_default_v2 (input clk, rst, j, output w);
2       reg [2:0] ns, ps;
3
4       always @(ps,j) begin
5           ns = 3'b100;
6           case(ps)
7               3'b100: ns = j ? 3'b101 : 3'b100;
8               3'b101: ns = j ? 3'b101 : 3'b110;
9               3'b110: ns = j ? 3'b111 : 3'b100;
10              3'b111: ns = j ? 3'b000 : 3'b110;
11              3'b000: ns = j ? 3'b101 : 3'b110;
12              default: ns = 3'b100;
13          endcase
14      end
15
16      assign w = (ps == 3'b000) ? 1'b1 : 1'b0;
17
18      always @(posedge clk, posedge rst) begin
19          if (rst)
20              ps <= 3'b100;
21          else
22              ps <= ns;
23      end
24  endmodule
```

```
=== moor_with_default_v2 ===

   Number of wires:                 16
   Number of wire bits:             20
   Number of public wires:           5
   Number of public wire bits:       9
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 16
     $_ANDNOT_                       1
     $_AND_                          2
     $_AOI3_                         2
     $_DFF_PP0_                      4
     $_DFF_PP1_                      1
     $_NOR_                          3
     $_NOT_                          3
```

```
1  module moor_without_default_v2 (input clk, rst, j, output w);
2      reg [2:0] ns, ps;
3
4      always @(ps,j) begin
5          ns = 3'b100;
6          case(ps)
7              3'b100: ns = j ? 3'b101 : 3'b100;
8              3'b101: ns = j ? 3'b101 : 3'b110;
9              3'b110: ns = j ? 3'b111 : 3'b100;
10             3'b111: ns = j ? 3'b000 : 3'b110;
11             3'b000: ns = j ? 3'b101 : 3'b110;
12         endcase
13     end
14
15     assign w = (ps == 3'b000) ? 1'b1 : 1'b0;
16
17     always @(posedge clk, posedge rst) begin
18         if (rst)
19             ps <= 3'b100;
20         else
21             ps <= ns;
22     end
23 endmodule
```

```
=== moor_without_default_v2 ===

   Number of wires:                 16
   Number of wire bits:             20
   Number of public wires:           5
   Number of public wire bits:       9
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 16
     $_ANDNOT_                       1
     $_AND_                          2
     $_AOI3_                         2
     $_DFF_PP0_                      4
     $_DFF_PP1_                      1
     $_NOR_                          3
     $_NOT_                          3
```


=== moor_without_default_v2 ===
16
20
5
9
0
0
0
16
1
2
2
4
1
3
3
=== moor_with_default_v2 ===
Number of wires: 16
Number of wire bits: 20
Number of public wires: 5
Number of public wire bits: 9
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 16
$_ANDNOT_ 1
$_AND_ 2
$_AOI3_ 2
$_DFF_PP0_ 4
$_DFF_PP1_ 1
$_NOR_ 3
$_NOT_ 3


synth_moore_with_default_v2.v ↔ synth_moore_without_default_v2.v U
moore_machine_yosys > synth_moore_without_default_v2.v
(* top = 1 *)
(* src = "moore_with_default_v2.v:1" *)
module moor_with_default_v2(clk, rst, j, w);
(* src = "moore_without_default_v2.v:1" *)
module moor_without_default_v2(clk, rst, j, w);
input clk;
input j;
(* onehot = 32'd1 *)
wire [4:0] ps;
input rst;