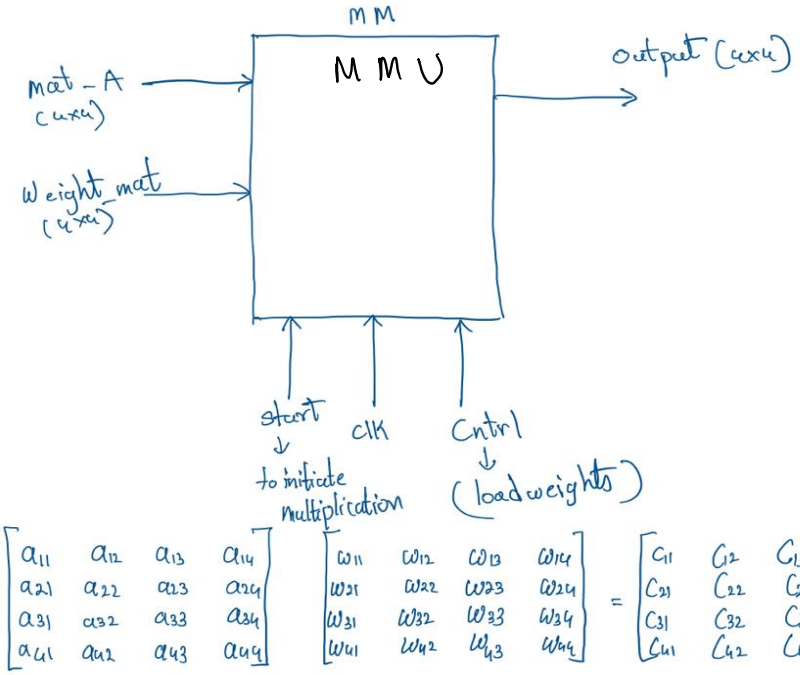
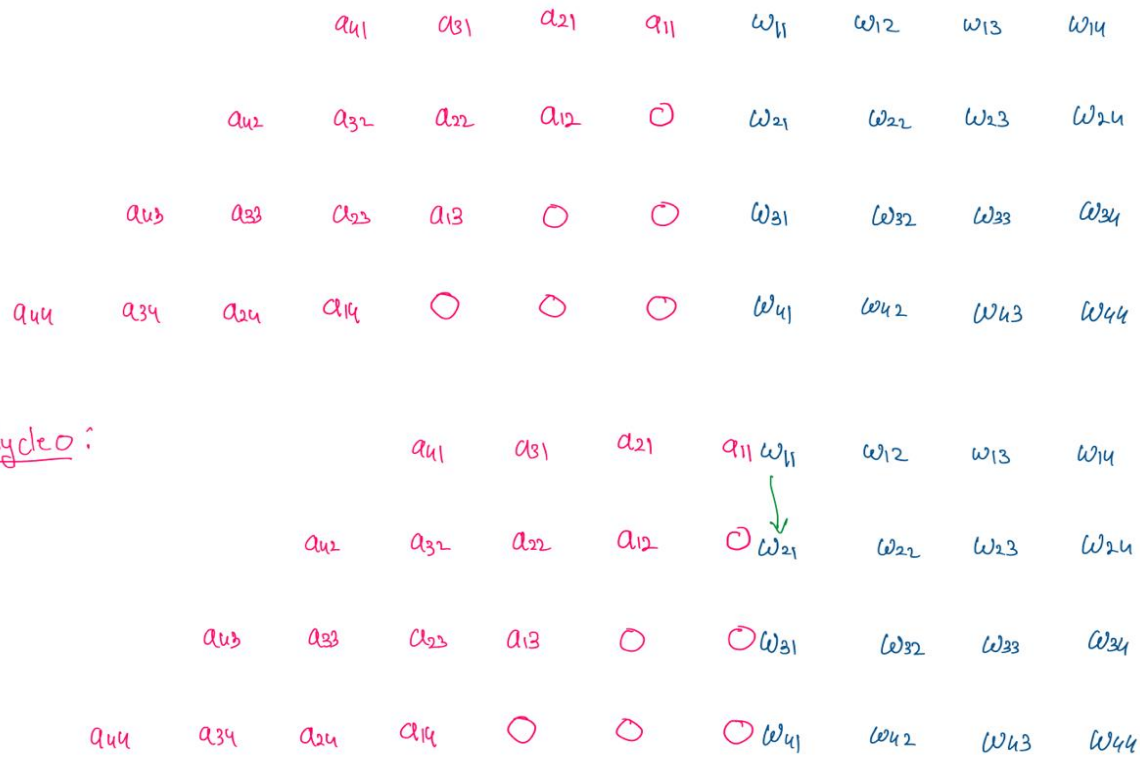
4x4 weight stationary Systolic Array Matrix Multiplication:



$$\begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{bmatrix} \begin{bmatrix} w_{11} & w_{12} & w_{13} & w_{14} \\ w_{21} & w_{22} & w_{23} & w_{24} \\ w_{31} & w_{32} & w_{33} & w_{34} \\ w_{41} & w_{42} & w_{43} & w_{44} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C_{34} \\ C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}$$



Homework-2

Cycle-0 :

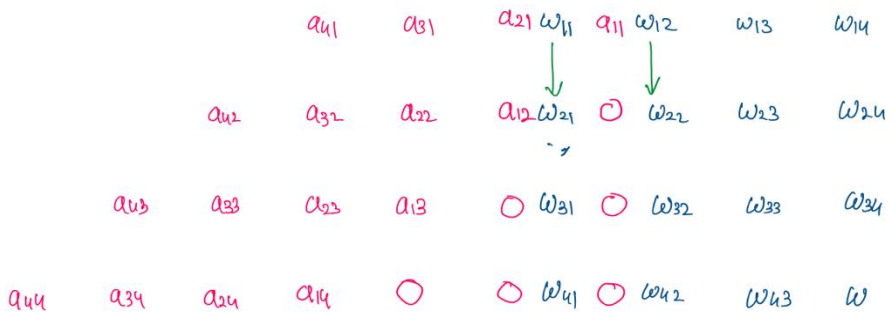
$C_{11} = a_{11} w_{11}$

$C_{21} = 0$

$C_{31} = 0$

$C_{41} = 0$

Cycle 1:



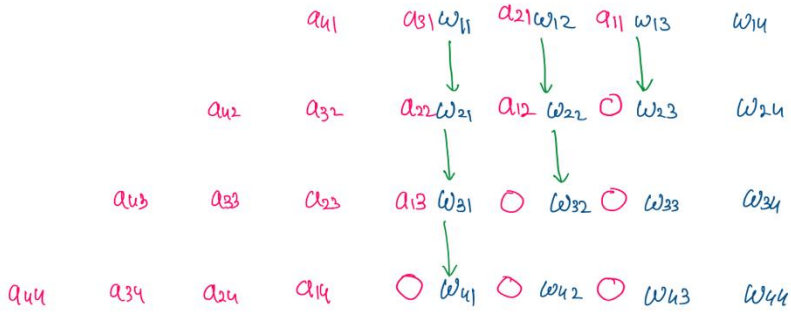
cycle-1 :

$C_{11} = a_{11} w_{11} + a_{12} w_{21}$

$C_{12} = a_{11} w_{12}$

$C_{21} = a_{21} w_{11}$

cycle - 2 :



Cycle -2 :

$C_{11} = a_{11} w_{11} + a_{12} w_{21} + a_{13} w_{31}$

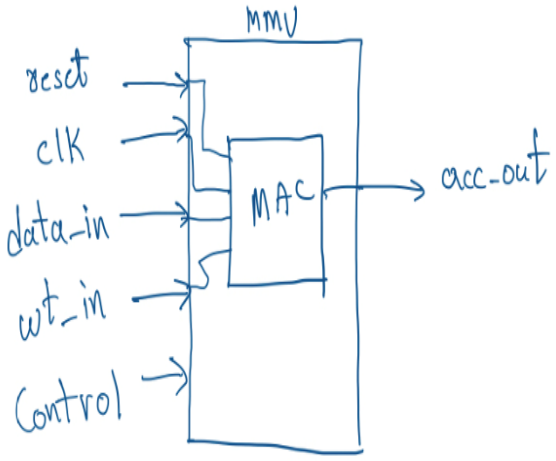
$C_{12} = a_{11} w_{12} + a_{12} w_{22}$

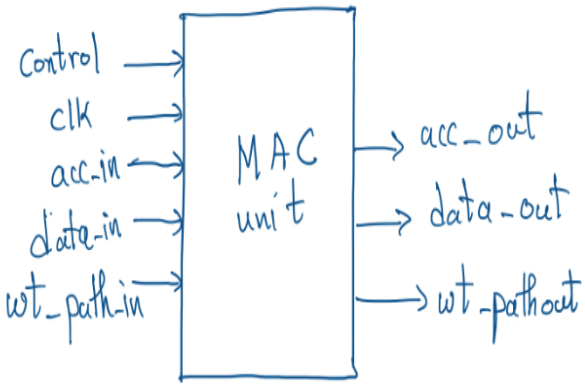
$C_{21} = a_{21} w_{11} + a_{22} w_{21}$

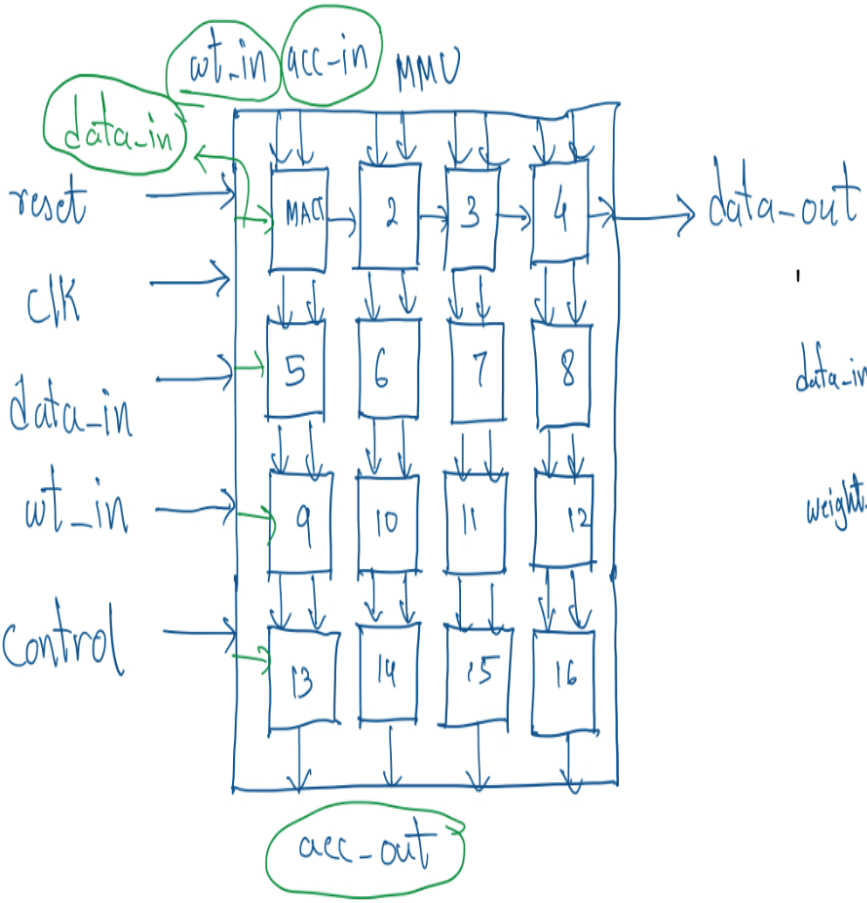
$C_{22} = a_{21} w_{12} +$

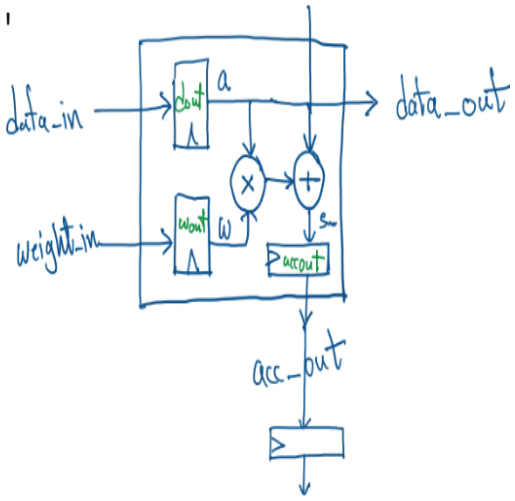
$C_{13} = a_{11} w_{13} +$

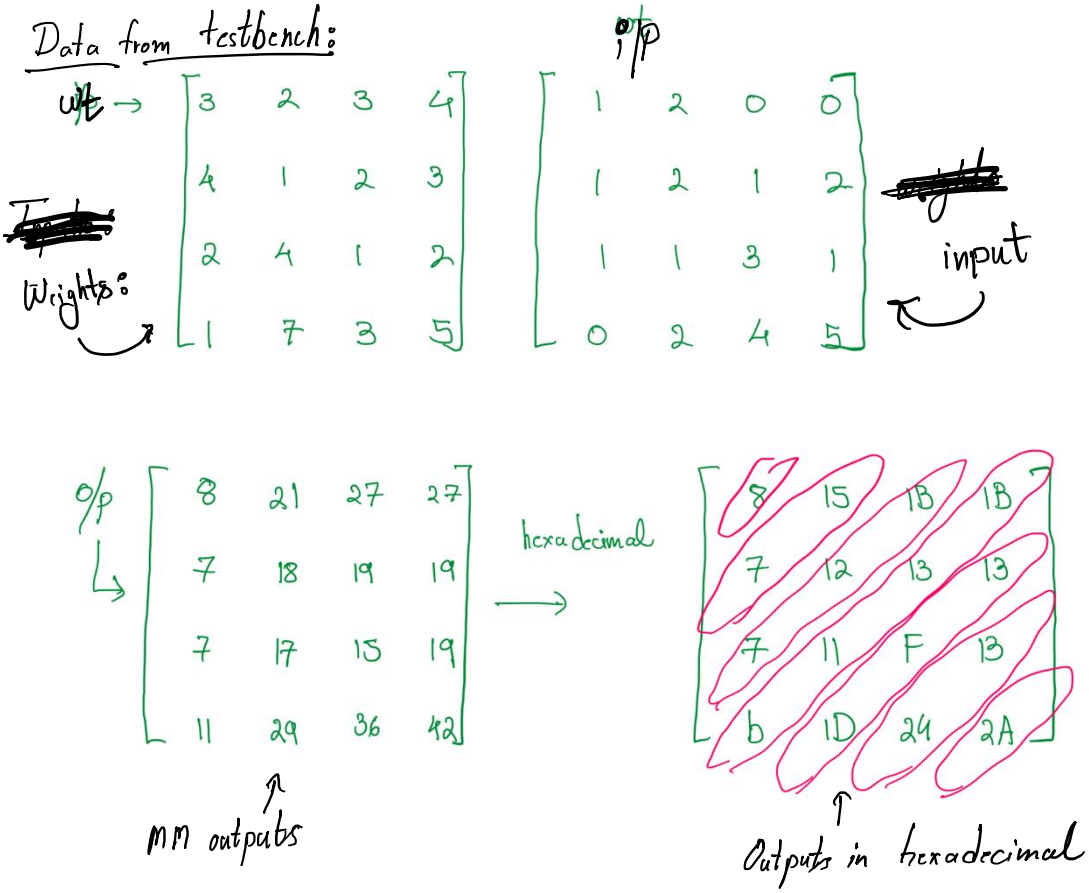
$C_{31} = a_{31} w_{11} +$


MMU
reset
clk
data_in
wt_in
Control
MAC
acc_out


Control
clk
acc_in
data_in
wt_path_in
MAC
unit
acc_out
data_out
wt_pathout


wt_in
acc_in
MMU
data_in
reset
clk
data_in
wt_in
Control
MAC
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
data_out
acc_out

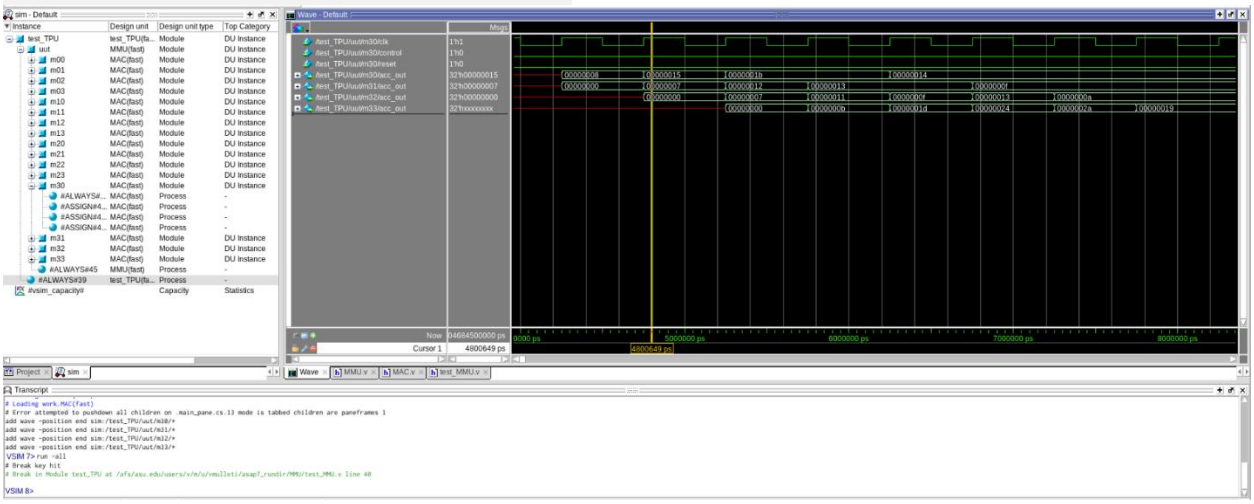

data_in
din
a
data_out
weight_in
wout
w
x
+
sum
accout
acc_out



The MMU (Matrix Multiplication Unit) module is the top-level module that represents a systolic array for matrix multiplication. It takes several inputs, processes them through multiple MAC (Multiply-Accumulate) units arranged in a 2D array, and produces an output accumulator result.

The MAC (Multiply-Accumulate) module represents a single multiply-accumulate unit. It takes inputs, multiplies data with weight, accumulates the results, and produces output data and accumulation. Overall, the MMU module orchestrates the interaction between multiple MAC modules, arranging them in a systolic array fashion to perform matrix multiplication. The MAC module represents a single multiply-accumulate operation, with control for weight loading and accumulator reset. The design as a whole is intended for matrix multiplication operations in a systolic array configuration.

Screenshots of RTL simulation results:



DC synthesis report on timing, power, and area:

```
clock clk (rise edge)                                  500.00     500.00
clock network delay (ideal)                              0.00     500.00
clock uncertainty                                       -0.01     499.99
m01_acc_out_reg_14_/CLK (DFFHQNx1_ASAP7_75t_R)           0.00     499.99 r
library setup time                                     -16.13     483.86
data required time                                                483.86
--------------------------------------------------------------------------
data required time                                                483.86
data arrival time                                                -483.02
--------------------------------------------------------------------------
slack (MET)                                                         0.84
```

```
Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_22b_AO_RVT_TT_170906
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ps
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------------------
                                   Switch   Int      Leak     Total
Hierarchy                          Power    Power    Power    Power    %
--------------------------------------------------------------------------------
MMU                                   0.464    1.263 5.13e+05    1.728 100.0
1
```

From the above power data we can observe about both dynamic and leakage power, Dynamic power units measure the power consumed during active, dynamic operations, while leakage power units measure the power consumed when the circuit is idle. A balance between minimizing both dynamic and leakage power is essential for achieving energy-efficient and high-performance integrated circuits. From the timing report, there is a slack of 0.84 and most of the time got utilized perfectly.

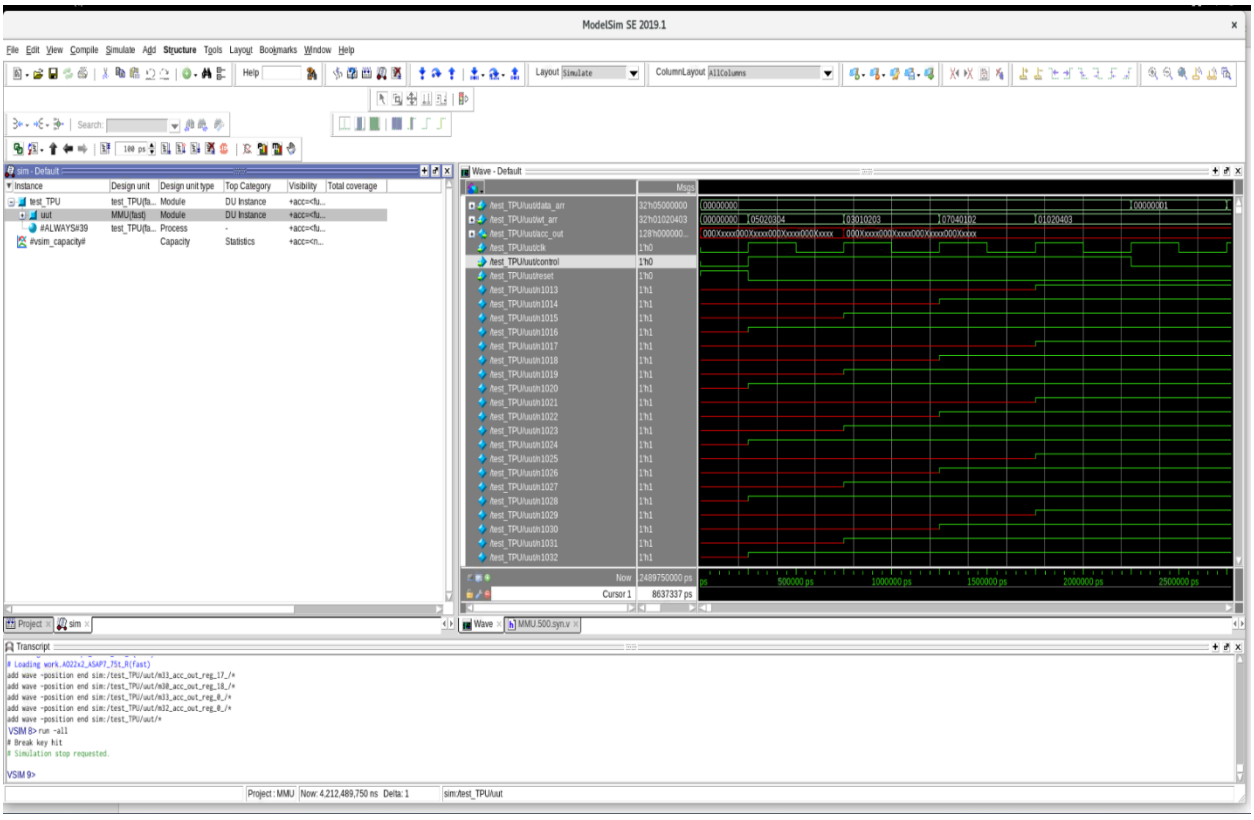
```
Number of ports:                          195
Number of nets:                          7023
Number of cells:                         6251
Number of combinational cells:           5671
Number of sequential cells:               580
Number of macros/black boxes:               0
Number of buf/inv:                       1339
Number of references:                      40

Combinational area:               6961.774980
Buf/Inv area:                      948.049932
Noncombinational area:            2706.047897
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  9667.822877
Total area:                 undefined
```

From the above report the "Total cell area" is a significant metric in the area report, representing the sum of areas occupied by cells within the chip design. In this case, the total cell area is approximately 9667.82 square units. This metric provides a fundamental measurement of the chip's physical footprint and is essential for estimating chip manufacturing costs, power consumption, and overall performance

Post-synthesis gate level simulation results:



The above fig describes the accumulator outputs of (30,31,32,33 elements) post generating the netlist after doing synthesis and simulating it with the main testbench where we get the outputs diagonally in hexadecimal radix form.

Homework-2