Vijay Rajan Machingauth

Engineering Manager Technical

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English, Tamil, Malayalam, Hindi

BACKGROUND

ABOUT

Building & leading high-velocity teams focused on delivering complex products, experience managing cross-geo teams, server SoC power management, firmware validation, arch/micro arch debug in pre/post-si env, ARM and X86 architectures, CAD tools development for microprocessors/graphics, C, C++, python, perl & ruby, emulation bring up/debug/collateral development

WORK EXPERIENCE

Senior Engineering Manager Technical, IPG, Intel Corporation , Intel Corporation

Nov, 2015 - Present

Lead the server power management firmware validation and the Intel server manageability IP development teams - reponsible for delivery of zero-defect power management FW for all Intel server products & Intel server manageability IP. Also lead the power-management IP emulation strategy

Senior Chief Engineer, Validation Architect , Samsung India Software Operations, Bangalore

Jul, 2014 - Sep, 2015 1 year 2 months

Senior Chief Engineer and Validation Architect responsible for validation strategy for Exynos mobile SoCs. simulation, emulation, multi-IP validation & multi-processor validation strategies

Technical Lead, Post-Silicon Validation, Intel Technology India Pvt Ltd

May, 2012 - Jun, 2014 2 years 1 month

Lead a team focused on Xeon power management post-silicon validation. Driving test content development, execution and debug. Responsibilities include content and execution planning, failure debug for internal and externally reported issues.

- Lead power management post-si validation of Jaketown, Ivytown and Broadwell Server

Technical Lead, Post-Silicon Debug and Debug tools, Intel Technology India Pvt Ltd

Jul, 2010 - Jun, 2014 3 years 11 months

Lead a team developing post-silicon debug tools. These tools are used for the post-si system debug of Intel multi-core Xeon Microprocessors. validation of power management features and manual debug of failures.

Technical Lead, SV tools, Intel Technology India Pvt Ltd

Jul, 2008 - Jul, 2010 2 years

Lead a team to develop post-si tools that increased debug productivity and improved TTM.

Senior CAD Engineer , Intel Technology India Pvt Ltd

Oct, 2003 - Nov, 2008 5 years 1 month

Validation tools - architectural/micro-architectural pre-silicon validation tools, developing simulation/emulation solutions.

SKILLS

Hardware Architecture & Design

Microprocessors | Debug | Firmware Design & Validation | CAD Automation | RTL Design & Validation | Architecture | SystemVerilog | Post-Si Validation | SoC Power Management | Emulation | Simulation

Software/Programming Languages

C | C++ | Python | Perl | Ruby | X86/IA32 | General Assembly Language Programming | Debug

Leadership

Mentoring | Building & Leading High-Velocity Teams | Project Management

EDUCATION

Computer Engineering & Math Minor, MS, University of Minnesota

Sep, 2001 - May, 2003

Computer Architecture | Advanced Computer Architecture | VLSI Design I & II | Design Automation I | Advanced Algorithms & Data Structures | Computer Networks

Electrical and Electronics Engg, B.E., Sri Venkateswara College of Engg, Chennai

Jun, 1997 - May, 2001

AWARDS

IAA at Intel Intel Corportation

Awarded on: May 31, 2005

Intel Achievement Award (IAA) for RTL simulator development and deployment.