VIJAY RAJAN MACHINGAUTH

ENGINEERING DIRECTOR, INTEL CORPORATION

ABOUT

CAMPBELL, CALIFORNIA, CA 95008

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HARDWARE ARCHITECTURE & DESIGN

MICROPROCESSORS
DEBUG
FIRMWARE DESIGN & VALIDATION
CAD AUTOMATION
RTL DESIGN & VALIDATION
ARCHITECTURE
SYSTEMVERILOG
POST-SI VALIDATION
SOC POWER MANAGEMENT
EMULATION
SIMULATION

SOFTWARE/PROGRAMMING LANGUAGES

C
C++
PYTHON
PERL
RUBY
X86/IA32
GENERAL ASSEMBLY LANGUAGE PROGRAMMING
DEBUG

LEADERSHIP

MENTORING
BUILDING & LEADING HIGH-VELOCITY TEAMS
PROJECT MANAGEMENT

LANGUAGES

ENGLISH, TAMIL, MALAYALAM, HINDI

SUMMARY

Building & leading high-velocity teams focused on solving complex engineering problems, managing cross-geo teams, SoC power management, firmware validation, arch/micro arch debug in pre/post-si env, ARM and X86 architectures, CAD tools development for microprocessors/graphics, emulation bring up/debug/collateral development, Arch simulation & modeling, Virtual Platforms, C, C++, python, perl & ruby

EXPERIENCE

INTEL CORPORATION
07/2021 - PRESENT

ENGINEERING DIRECTOR, SOFTWARE & ADVANCED TECHNOLOGY GROUP

Lead the client power management virtual platform and the Simulation Architecture teams - responsible for delivering virtual platforms for Intel's client products with power management capabilities, R&D of advanced simulation capabilities. Hands-on role setting the technical direction & strategy, design, modeling, development, platform debug and deployment.

INTEL CORPORATION
11/2015 - 06/2021

SENIOR ENGINEERING MANAGER TECHNICAL, IPG

Led the server power management IP and firmware validation and the Intel server manageability IP development teams - delivering power management and manageability IPs and FW for all Intel server products.

- Icelake Server, Snowridge, Icelake-D, Sapphire Rapids, Intel 4 Server Products

SAMSUNG INDIA SOFTWARE OPERATIONS, BANGALORE
07/2014 - 09/2015

SENIOR CHIEF ENGINEER, VALIDATION ARCHITECT

Senior Chief Engineer and Validation Architect responsible for validation strategy for Exynos mobile SoCs. simulation, emulation, multi-IP & multi-processor validation strategies

INTEL TECHNOLOGY INDIA PVT LTD
05/2012 - 06/2014

TECHNICAL LEAD, POST-SILICON VALIDATION

Led a team focused on Xeon power management post-silicon validation on Jaketown, Ivytown and Broadwell server. Driving test content development, execution and debug. Responsibilities include content and execution planning, failure debug for internal and externally reported issues.

INTEL TECHNOLOGY INDIA PVT LTD
07/2010 - 06/2014

TECHNICAL LEAD, POST-SILICON DEBUG AND DEBUG TOOLS

Led a team developing post-silicon debug tools. These tools are used for the post-si system debug of Intel multi-core Xeon Microprocessors. Validation of power management features and manual debug of failures.

INTEL TECHNOLOGY INDIA PVT LTD
07/2008 - 07/2010

TECHNICAL LEAD, SV TOOLS

Led a team to develop post-si tools that increased debug productivity and improved TTM.

INTEL TECHNOLOGY INDIA PVT LTD
10/2003 - 11/2008

SENIOR CAD ENGINEER

Validation tools - architectural/micro-architectural pre-silicon validation tools, developing simulation/emulation solutions.

EDUCATION

UNIVERSITY OF MINNESOTA
09/2001 - 05/2003

MS COMPUTER ENGINEERING & MATH (MINOR)

SRI VENKATESWARA COLLEGE OF ENGG, CHENNAI
06/1997 - 05/2001

B.E. ELECTRICAL AND ELECTRONICS ENGG

AWARDS

INTEL ACHIEVEMENT AWARD

INTEL CORPORTATION

Intel Achievement Award (IAA) for RTL simulator development and deployment.