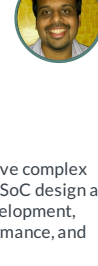


# VIJAY RAJAN MACHINGAUTH

ENGINEERING DIRECTOR, INTEL CORPORATION



## ABOUT

SANFIELL, CALIFORNIA, CA  
95058  
VIJAY.RAJAN@INTEL.COM  
9408-707-4235

## HARDWARE ARCHITECTURE & DESIGN

MICROPROCESSORS  
DESIGN  
FIRMWARE DESIGN &  
VALIDATION  
CAD AUTOMATION  
RTL DESIGN & VALIDATION  
ARCHITECTURE  
SYSTEM VERLOG  
POST-SYNTHESIS  
SOC POWER MANAGEMENT  
EMULATION  
SIMULATION

## SOFTWARE/PROGRAM MING LANGUAGES

C  
C++  
PYTHON  
PERL  
RUBY  
X86/IA32  
GENERAL ASSEMBLY LANGUAGE  
PROGRAMMING  
VERILOG

## LEADERSHIP

MENTORING  
BUILDING LEADING-HIGH-  
VELOCITY TEAMS  
PROJECT MANAGEMENT

## LANGUAGES

ENGLISH, TAMIL, MALAYALAM,  
HINDI

## SUMMARY

Dynamic Technical Leader: Building high-velocity, cross-geta teams to solve complex engineering challenges in system power management (PM), firmware (Firmware), design and validation across X86 and ARM Architectures. Expertise in CAD tools development, emulation, virtual platforms, and architectural modeling for power, performance, and thermal projections.

## EXPERIENCE

### INTEL CORPORATION<sup>1,2</sup> SOFTWARE & ADVANCED TECHNOLOGY GROUP ENGINEERING DIRECTOR

Lead the client power management (PM) virtual platform (VP) and the Simulation Architecture teams, responsible for delivering virtual platforms for Intel's client products with PM capabilities, R&D of advanced simulation capabilities. Hands-on role setting the technical direction, strategy, design, modeling, development, platform debug and deployment.

- At Intel at Intel, the team delivered several critical platform PM flows on a VP with full software stack that include OS, FW and drivers. Transforming several foundational simulation and modeling capabilities to code generation focusing on efficiency and quality. Team-driving software development practices and training.

### INTEL CORPORATION<sup>1,2</sup> SENIOR ENGINEERING MANAGER TECHNICAL (PG)

Lead the server PM/firmware validation and the Intel server manageability (IP) development teams, delivering PM and manageability (IP) and FW for all Intel server products.

- Delivered manageability IP and PM FW for Intelake Server, Snowridge, Intelake-D, Sapphire Rapids, Intel 3 and 4 Server Products.
- Instrumental in driving significant improvements in IP and FW quality keeping pace with increasing complexity and scope gain-over-gain.

### SAMSUNG INDIA SOFTWARE OPERATIONS, BANGALORE<sup>1,2</sup>

Senior Chief Engineer and Validation Architect responsible for validation strategy for Exynos mobile SoC. Simulation, emulation, multi-IP & multi-processor validation strategy.

- Built IP and sub-system validation strategy for PM and memory. Lead the collaboration with industry EDA partners including Cadence, Synopsys and Mentor delivering verification strategies via Peripac, Integrity and

### INTEL TECHNOLOGY INDIA PVT LTD<sup>1,2</sup> TECHNICAL LEAD, POST-SILICON VALIDATION

Lead a team focused on Xeon PM post-silicon validation on Lakotown, Wynton and Braswell server. Driving test content development, execution and debug.

- Responsibilities include content and execution planning, failure debug for internal and customer reported issues.

### INTEL TECHNOLOGY INDIA PVT LTD<sup>1,2</sup> TECHNICAL LEAD, POST-SILICON DEBUG AND DEBUG TOOLS

Lead a team developing post-silicon debug tools. These tools are used for the post-silicon debug of Intel multi-core Xeon Microprocessors. Validation of PM features and manual debug of failures.

- Lead the team to deliver a SM (Server) based SI-to-Model failure reproduction flow for the first time on a Server product - Xeon.

### INTEL TECHNOLOGY INDIA PVT LTD<sup>1,2</sup> TECHNICAL LEAD, SV TOOLS

Lead a team to develop post-silicon tools that increased debug productivity and improved TTM.

- Built several innovative debug tools and solution that directly impacted TTM for several client and server products - 25% improvement in debug productivity on SandyBridge family of Intel server products.

### INTEL TECHNOLOGY INDIA PVT LTD<sup>1,2</sup> SENIOR CAD ENGINEER

Validation team - architect and micro-architectural pre-silicon validation tools, developing simulation/emulation solutions.

- Individually lead the development and support of simulation tools and models for server development team in Bangalore development center.

## EDUCATION

UNIVERSITY OF MINNESOTA 09/2001 - 07/2003  
MS COMPUTER ENGINEERING & MATH (MINOR)

SRI VENKATESWARA COLLEGE OF ENGG, CHENNAI 06/1997 - 05/2001  
B. ELECTRICAL & ELECTRONICS ENGINEERING

## AWARDS

### INTEL ACHIEVEMENT AWARD

INTEL CORPORATION  
Intel Achievement Award (IAA) for RTL simulator development and deployment.