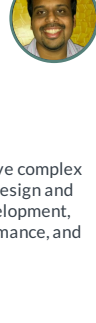


VIJAY RAJAN MACHINGAUTH

ENGINEERING DIRECTOR, INTEL CORPORATION



ABOUT

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HARDWARE ARCHITECTURE & DESIGN

MICROPROCESSORS
DESIGN
FIRMSWARE DESIGN & VALIDATION
CAD AUTOMATION
RTL DESIGN & VALIDATION
ARCHITECTURE
SYSTEM VERLOG
POST-SILICON
SOC POWER MANAGEMENT
EMULATION
SIMULATION

SOFTWARE/PROGRAMMING LANGUAGES

C
C++
PYTHON
PERL
RUBY
X86/IA32
GENERAL ASSEMBLY LANGUAGE
PROGRAMMING
DEBUG
LEADERSHIP
BUILDING LEADING-HIGH-VELOCITY TEAMS
PROJECT MANAGEMENT
LANGUAGES
ENGLISH, TAMIL, MALAYALAM, HINDI

SUMMARY

Dynamic Technical Leader: Building high-velocity, cross-gene teams to solve complex engineering challenges in server power management. Firmware/PSiC design and validation across X86 and ARM Architectures. Expertise in CAD tools development, emulation, virtual platforms, and architectural modeling for power, performance, and thermal projections.

EXPERIENCE

INTEL CORPORATION¹² ENGINEERING DIRECTOR, SOFTWARE & ADVANCED TECHNOLOGY GROUP

Lead the client power management virtual platform and the Simulation Architecture teams, responsible for delivering virtual platforms for Intel's client products with power management capabilities. R&D of advanced simulation capabilities. Hands-on role setting the technical direction & strategy, design, modeling, development, platform debug and deployment.

- First at Intel the team delivered several critical platform power management flows on a virtual platform with the full software stack including OS, FW and drivers. Transferring several foundational simulation and modeling capabilities like code generation focusing on efficiency and quality. Team-driving software development projects and testing.

INTEL CORPORATION¹² SENIOR ENGINEERING MANAGER TECHNICAL, I/O

11/2015 - 09/2021

Lead the server power management IP and firmware validation and the Intel server manageability IP development teams - delivering power management and manageability IPs and FW for all Intel server products.

- Delivered manageability IP and power management FW for Intel's Server, Knowledge Institute, 5, Supply, Rapids, Intel 3 and 4 Server Products
- Instrumental in driving significant improvements in IP and FW quality keeping pace with increasing complexity and scope given over-gen

SAMSUNG INDIA SOFTWARE OPERATIONS, BANGALORE¹²

SENIOR CHIEF ENGINEER, VALIDATION ARCHITECT 07/2014 - 09/2015

Senior Chief Engineer and Validation Architect responsible for validation strategy for Intel's multi-core Xeon-M processors. Validation of power management strategies

- Built IP and sub-system validation strategy for power management and memory. Lead the collaboration with industry EDA partners including Cadence, Synopsys and Mentor delivering verification strategies eg. Perseus, Jazpergold

INTEL TECHNOLOGY INDIA PVT LTD¹² TECHNICAL LEAD, POST-SILICON VALIDATION

05/2012 - 06/2014

Lead a team focused on Xeon power management post-silicon validation on Jaketown, Jazpergold and Broadwell Server. Driving test content development, execution and debug. Responsibilities include content and execution planning, failure debug for internal and external customers.

- Established Server power management Post-silicon Expertise in the Bangalore development center and delivered several product launches, meeting and beating expectations.

INTEL TECHNOLOGY INDIA PVT LTD¹² TECHNICAL LEAD, POST-SILICON DEBUG AND DEBUG TOOLS

07/2010 - 06/2014

Lead a team developing post-silicon debug tools. These tools are used for the post-silicon debug of Intel multi-core Xeon-M processors. Validation of power management features and manual debug of failures.

- Lead the team delivering a Jazpergold based 5th Intel Model failure reproduction flow for the first time on a Server product - Jazpergold

INTEL TECHNOLOGY INDIA PVT LTD¹² TECHNICAL LEAD, SVT TOOLS

07/2008 - 07/2010

Lead a team to develop post-silicon tools that increased debug productivity and improved TTM.

- Built several innovative debug tools and solution that directly impacted TTM for several client and server products - 25% improvement in debug productivity on SandBridge family of client-server products

INTEL TECHNOLOGY INDIA PVT LTD¹² SENIOR CAD ENGINEER

03/2003 - 11/2008

Validation tools - architectural silicon architectural pre-silicon validation tools, developing simulation/emulation solutions.

- Individually lead the development and support of simulation tools and models for Server development team in Bangalore development center

EDUCATION

UNIVERSITY OF MINNESOTA 09/2001 - 05/2003

M.S. COMPUTER ENGINEERING & MATH (MINOR)

SRIVENKATESWARA COLLEGE OF ENGG, CHENNAI 06/1997 - 05/2001

B.E. ELECTRICAL AND ELECTRONICS ENGG

AWARDS

INTEL ACHIEVEMENT AWARD

Intel Achievement Award (IAA) for RTL simulator development and deployment.