Vijay Rajan Machingauth

Engineering Manager Technical

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English, Tamil, Malayalam, Hindi

BACKGROUND

ABOUT

Building & Leading high-velocity teams focused on delivering Complex Products, Experience managing cross-geo teams, Server SoC Power Management, Firmware Validation, Arch/Micro arch debug in Pre/Post Si Env, ARM and X86 architectures, CAD tools development for Microprocessors/Graphics, C, C++, Python, Perl & Ruby, Emulation bring up/debug/collateral development

WORK EXPERIENCE

Senior Engineering Manager Technical, IPG, Intel Corporation, Intel Corporation
Nov, 2015 - Present

Lead the Server Power Management Firmware Validation and the Intel Server Manageability IP Development Teams - Reponsible for delivery of Zero-Defect Power Management FW for all Intel Server Products & Intel Server Manageability IP. Also Lead the Power-Management IP Emulation Strategy

Senior Chief Engineer, Validation Architect, Samsung India Software Operations, Bangalore
Jul, 2014 - Sep, 2015   1 year 2 months

Senior Chief Engineer and Validation Architect responsible for Validation Strategy for Exynos Mobile SoCs. Simulation, Emulation, Multi-IP Validation & Multi-Processor Validation Strategies

Technical Lead, Post-Silicon Validation, Intel Technology India Pvt Ltd
May, 2012 - Jun, 2014   2 years 1 month

Lead a team focused on Xeon Power Management Post-Silicon Validation. Driving test content development, execution and debug. Responsibilities include content and execution planning, failure debug for internal and externally reported issues.

- Lead Power Management Post-Si Validation of Jaketown, Ivytown and Broadwell Server

Technical Lead, Post-Silicon Debug and Debug tools, Intel Technology India Pvt Ltd
Jul, 2010 - Jun, 2014   3 years 11 months

Lead a team developing Post-Silicon Debug Tools. These tools are used for the Post-Si System Debug of Intel Multi-Core Xeon Microprocessors. Validation of Power-Management features and manual debug of failures.

Technical Lead, SV tools, Intel Technology India Pvt Ltd

Jul, 2008 - Jul, 2010 🕐 2 years

Lead a team to develop Post-Si tools that increased debug productivity and improved TTM.

Senior CAD Engineer, Intel Technology India Pvt Ltd

Oct, 2003 - Nov, 2008 🕐 5 years 1 month

Validation tools - Architectural/Micro-Architectural pre-silicon validation tools, Developing simulation/emulation solutions.

🛠 SKILLS

Hardware Architecture & Design

Microprocessors   Debug   Firmware Design & Validation   CAD Automation   RTL Design & Validation   Architecture

SystemVerilog   Post-Si Validation   SoC Power Management   Emulation   Simulation

Software/Programming Languages

C   C++   Python   Perl   Ruby   X86/IA32   General Assembly Language Programming   Debug

Leadership

Mentoring   Building & Leading High-Velocity Teams   Project Management

🎓 EDUCATION

Computer Engineering & Math Minor, MS, University of Minnesota

Sep, 2001 - May, 2003

Computer Architecture   Advanced Computer Architecture   VLSI Design I & II   Design Automation I

Advanced Algorithms & Data Structures   Computer Networks

Electrical and Electronics Engg, B.E., Sri Venkateswara College of Engg, Chennai

Jun, 1997 - May, 2001

🏆 AWARDS

IAA at Intel Intel Corportation

Awarded on: May 31, 2005

Intel Achievement Award (IAA) for RTL simulator development and deployment.