VIJAY RAJAN MACHINGAUTH

ENGINEERING DIRECTOR, INTEL CORPORATION

ABOUT

CAMPBELL, CALIFORNIA, CA 95008

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(408)-797-4215

HARDWARE ARCHITECTURE & DESIGN

- MICROPROCESSORS
- DEBUG
- FIRMWARE DESIGN & VALIDATION
- CAD AUTOMATION
- RTL DESIGN & VALIDATION
- ARCHITECTURE
- SYSTEMVERILOG
- POST-SI VALIDATION
- SOC POWER MANAGEMENT
- EMULATION
- SIMULATION

SOFTWARE/PROGRAMMING LANGUAGES

- C
- C++
- PYTHON
- PERL
- RUBY
- X86/IA32
- GENERAL ASSEMBLY LANGUAGE PROGRAMMING
- DEBUG

LEADERSHIP

- MENTORING
- BUILDING & LEADING HIGH-VELOCITY TEAMS
- PROJECT MANAGEMENT

LANGUAGES

ENGLISH, TAMIL, MALAYALAM, HINDI

SUMMARY

Dynamic Technical Leader: Building high-velocity, cross-geo teams to solve complex engineering challenges in system power management (PM), firmware/IP/SoC design and validation across X86 and ARM Architectures. Expertise in CAD tools development, emulation, virtual platforms, and architectural modeling for power, performance, and thermal projections.

EXPERIENCE

INTEL CORPORATION

07/2021 - PRESENT

ENGINEERING DIRECTOR, SOFTWARE & ADVANCED TECHNOLOGY GROUP

Lead the client power management (PM) virtual platform (VP) and the Simulation Architecture teams - responsible for delivering virtual platforms for Intel's client products with PM capabilities, R&D of advanced simulation capabilities. Hands-on role setting the technical direction & strategy, design, modeling, development, platform debug and deployment.

- A first at Intel, the team delivered several critical platform PM flows on a VP with full software stack that inclues OS, FW and drivers. Transforming several foundational simulation and modeling capabilities like code generation focusing on efficiency and quality. Team driving software development practices and training

INTEL CORPORATION

11/2015 - 06/2021

SENIOR ENGINEERING MANAGER TECHNICAL, IPG

Led the server PM IP/firmware validation and the Intel server manageability IP development teams - delivering PM and manageability IPs and FW for all Intel server products.

- Delivered manageability IP and PM FW for Icelake Server, Snowridge, Icelake-D, Sapphire Rapids, Intel 3 and 4 Server Products
- Instrumental in driving significant improvements in IP and FW quality keeping pace with increasing complexity and scope gen-over-gen

SAMSUNG INDIA SOFTWARE OPERATIONS, BANGALORE

07/2014 - 09/2015

SENIOR CHIEF ENGINEER, VALIDATION ARCHITECT

Senior Chief Engineer and Validation Architect responsible for validation strategy for Exynos mobile SoCs. Simulation, emulation, multi-IP & multi-processor validation strategies

- Built IP and sub-system validation strategy for PM and memory. Lead the collaboration with industry EDA partners including Cadence, Synopsys and Mentor delivering verification strategies eg Perspec, Jaspergold

INTEL TECHNOLOGY INDIA PVT LTD

05/2012 - 06/2014

TECHNICAL LEAD, POST-SILICON VALIDATION

Led a team focused on Xeon PM post-silicon validation on Jaketown, Ivytown and Broadwell server. Driving test content development, execution and debug. Responsibilities include content and execution planning, failure debug for internal and customer reported issues.

- Established Server PM Post-si expertise in the Bangalore development center and delivered several product launches, meeting and beating expectations

INTEL TECHNOLOGY INDIA PVT LTD

07/2010 - 06/2014

TECHNICAL LEAD, POST-SILICON DEBUG AND DEBUG TOOLS

Led a team developing post-silicon debug tools. These tools are used for the post-si system debug of Intel multi-core Xeon Microprocessors. Validation of PM features and manual debug of failures.

- Lead the team to deliver a SMI (interrupt) based Si-to-Model failure reproduction flow for the first time on a Server product - Ivytown

INTEL TECHNOLOGY INDIA PVT LTD

07/2008 - 07/2010

TECHNICAL LEAD, SV TOOLS

Led a team to develop post-si tools that increased debug productivity and improved TTM.

- Built several innovative debug tools and solution that directly impacted TTM for several client and server products - 25% improvement in debug productivity on SandyBridge family of client/server products

INTEL TECHNOLOGY INDIA PVT LTD

10/2003 - 11/2008

SENIOR CAD ENGINEER

Validation tools - architectural/micro-architectural pre-silicon validation tools, developing simulation/emulation solutions.

- Individually lead the development and support of simulation tools and models for Server development team in Bangalore development center

EDUCATION

UNIVERSITY OF MINNESOTA

09/2001 - 05/2003

MS COMPUTER ENGINEERING & MATH (MINOR)

SRI VENKATESWARA COLLEGE OF ENGG, CHENNAI

06/1997 - 05/2001

B.E. ELECTRICAL AND ELECTRONICS ENGG

AWARDS

INTEL ACHIEVEMENT AWARD

INTEL CORPORTATION

Intel Achievement Award (IAA) for RTL simulator development and deployment.