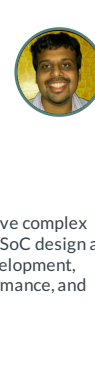


VIJAY RAJAN MACHINGAUTH

ENGINEERING DIRECTOR, INTEL CORPORATION



ABOUT

SANBRIEL, CALIFORNIA, CA
1008
 VIJAY.RAJAN@INTEL.COM
 909-797-4231

HARDWARE ARCHITECTURE & DESIGN

MICROPROCESSORS
DEBUG
FIRMWARE DESIGN & VALIDATION
CAD AUTOMATION
ARCHITECTURE
RTL DESIGN & VALIDATION
SYSTEM VERIFICATION
SOC POWER MANAGEMENT
EMULATION

SOFTWARE PROGRAMMING LANGUAGES

C++
PYTHON
PERL
X86/IA32
GENERAL ASSEMBLY LANGUAGE
PROGRAMMING
DEBUG

LEADERSHIP

MENTORING
BUILDING LEADING-HIGH-VELOCITY TEAMS
PROJECT MANAGEMENT

LANGUAGES

ENGLISH, TAMIL, MALAYALAM, HINDI

SUMMARY

Dynamic Technical Leader: Building high-velocity, cross-gen teams to solve complex engineering challenges in system-on-chip management (SOC), firmware (FW), SOC design and validation across X86 and ARM Architectures. Expertise in CAD tool development, emulation, virtual platforms, and architectural modeling for power, performance, and thermal projections.

EXPERIENCE

INTEL CORPORATION 07/2021 - PRESENT
ENGINEERING DIRECTOR, SOFTWARE & ADVANCED TECHNOLOGY GROUP

Lead the client power management (PM) virtual platform (VP) and the simulation Architecture teams - responsible for delivering virtual platforms for Intel's client products with PM capabilities. R&D of advanced simulation capabilities. Hands-on role setting the technical direction's strategy, design, modeling, development, platform debug and deployment.

- As a part of Intel's team, delivered several virtual platforms (PM) across a VP with full software stack that includes OS, FW and drivers. Transforming several foundational simulation and modeling capabilities like code generation focusing on efficiency and quality. Team driving software development practices and training

INTEL CORPORATION 11/2015 - 06/2021
SENIOR ENGINEERING MANAGER, TECHNICAL OPS

Lead the server PM (P) firmware validation and the Intel server manageability (P) development teams - delivering PM and manageability (P) and FW for all Intel server products.

- Delivered manageability (P) and PM FW for Intel's Server, ServerEdge, Intel Xeon, Sapphire Rapids, Intel Xeon and Server Products
- Instrumental in driving significant improvements in IP and FW quality keeping pace with increasing complexity and scope gen-over-gen

SAMSUNG INDIA SOFTWARE OPERATIONS, BANGALORE 07/2014 - 09/2015
SENIOR CHIEF ENGINEER, VALIDATION ARCHITECT

Senior Chief Engineer and Validation Architect responsible for validation strategy for Exynos mobile SoC's simulation, emulation, multi-IP & multi-processor validation strategies

- Built IP and sub-system validation strategy for PM and memory. Lead the collaboration with industry EDA partners including Cadence, Synopsys and Mentor delivering verification strategies to Perseus, Exynos

INTEL TECHNOLOGY INDIA PVT LTD 05/2012 - 06/2014
TECHNICAL LEAD, POST-SILICON VALIDATION

Lead a team focused on Xeon PM post-silicon validation on Intel's Xeon, Xeon and Broadwell server. Driving test content development, execution and debug. Responsibilities include content and execution planning, failure debug for internal and customer reported issues

- Established Server PM Post-silicon expertise in the Bangalore development center and delivered several product launches, meeting and beating expectations

INTEL TECHNOLOGY INDIA PVT LTD 07/2010 - 06/2014
TECHNICAL LEAD, POST-SILICON DEBUG AND DEBUG TOOLS

Lead a team developing post-silicon debug tools. These tools are used for the post-silicon debug of Intel multi-core Xeon Microprocessors. Validation of power management features and manual debug of failures.

- Lead the team to deliver a PM based SI-to-Model failure reproduction flow for the first time on a Server product - Xeon

INTEL TECHNOLOGY INDIA PVT LTD 07/2008 - 07/2010
TECHNICAL LEAD, SV TOOLS

Lead a team to develop post-silicon tools that increased debug productivity and improved TTM.

- Built several innovative debug tools and solution that directly impacted TTM for several client and server products - 25% improvement in debug productivity on Intel's Xeon family of client/server products

INTEL TECHNOLOGY INDIA PVT LTD 03/2003 - 11/2008
SENIOR CAD ENGINEER

Validation tools - architecture, system architectural pre-silicon validation tools, developing simulation/emulation solutions.

- Individually lead the development and support of simulation tools and models for Server development team in Bangalore development center

EDUCATION

UNIVERSITY OF MINNESOTA 09/2001 - 05/2003
M.Sc. IN ELECTRICAL AND ELECTRONIC ENGINEERING (M.ASINOR)

SRI VENKATESWARA COLLEGE OF ENG. CHENNAI 06/1997 - 05/2001
B.E. IN ELECTRICAL AND ELECTRONIC ENGINEERING

AWARDS

INTEL ACHIEVEMENT AWARD
INTEL CORPORATION
Intel Achievement Award (IAA) for RTL, simulator development and deployment.