

CprE 381 – Computer Organization and Assembly-Level Programming

Lab-03 Report

Student Name Mason Walls

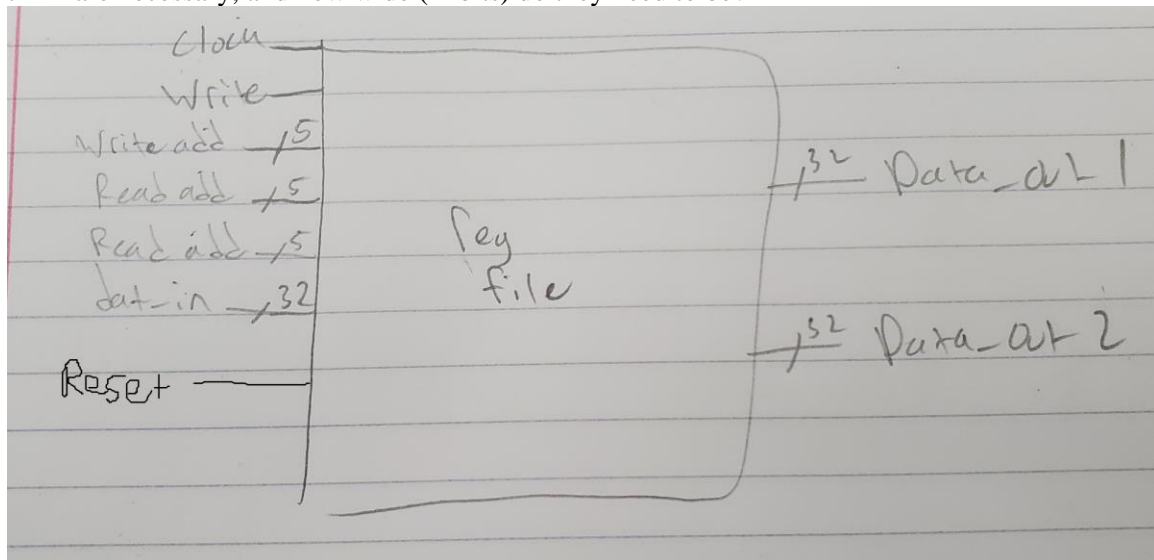
Section / Lab Time Section 6 / 4:10pm to 6:00 pm

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-03 instructions for the context of the following questions.

- [Prelab] At the end of Chapter 5, answer question 5. At the end of Chapter 7, answer exercise 2.
- [Prelab] In your Lab #3 report PDF, provide the Canvas group name for your project team, and a listing of its members. On a scale of 1-10, how comfortable with VHDL does each team member currently feel?

Sect-06.Group-04. I am at about a 7 with VHDL, and my partner is at a 6

- [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?



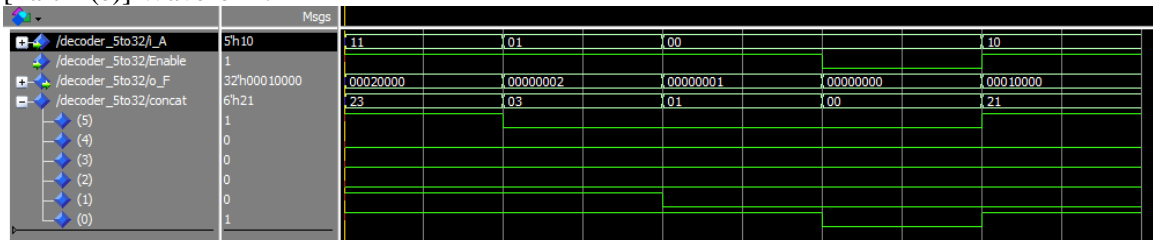
- [Part 1 (c)] Waveform.

	Msgs	
/tb_reg/s_CLK	No Data-	
/tb_reg/s_RST	No Data-	
/tb_reg/s_WE	No Data-	
/tb_reg/s_D	No Data-	FFFFFFFF 00000000 ABCDEF12 12345678 1F2E3D4C
/tb_reg/s_Q	No Data-	00000000 00000000 00000000 12345678

- [Part 1 (d)] What type of decoder would be required by the MIPS register file and why?

A 5 to 32 decoder is required because we need 32 different 1 bit high outputs. 5 bits can go from 0 to 31.

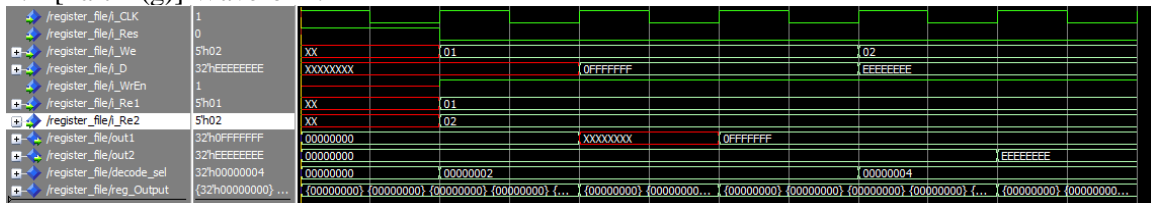
f. [Part 1 (e)] Waveform.



g. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

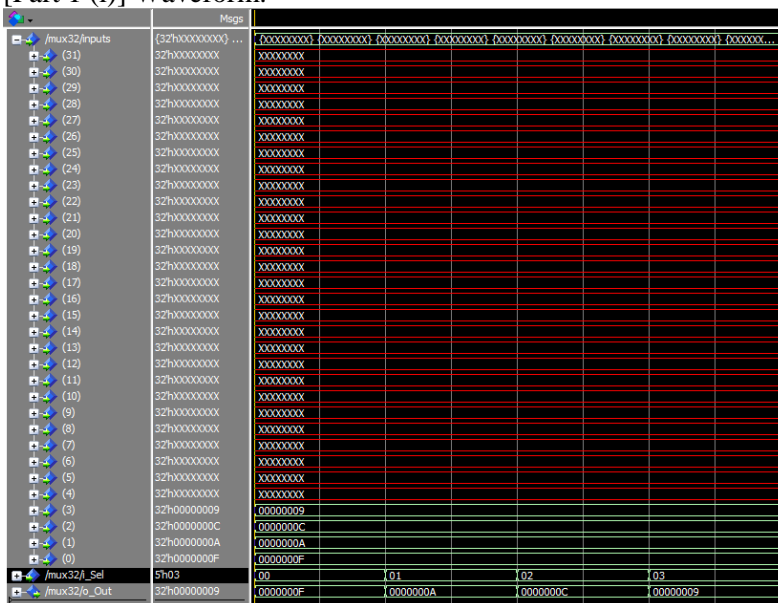
What I did for the multiplexor was use a new type, that allowed me to make an array of 32 32bit items, then select these items using a 5 bit input. This greatly simplified the task of creating and using a 32 to 1 multiplexor

h. [Part 1 (g)] Waveform.



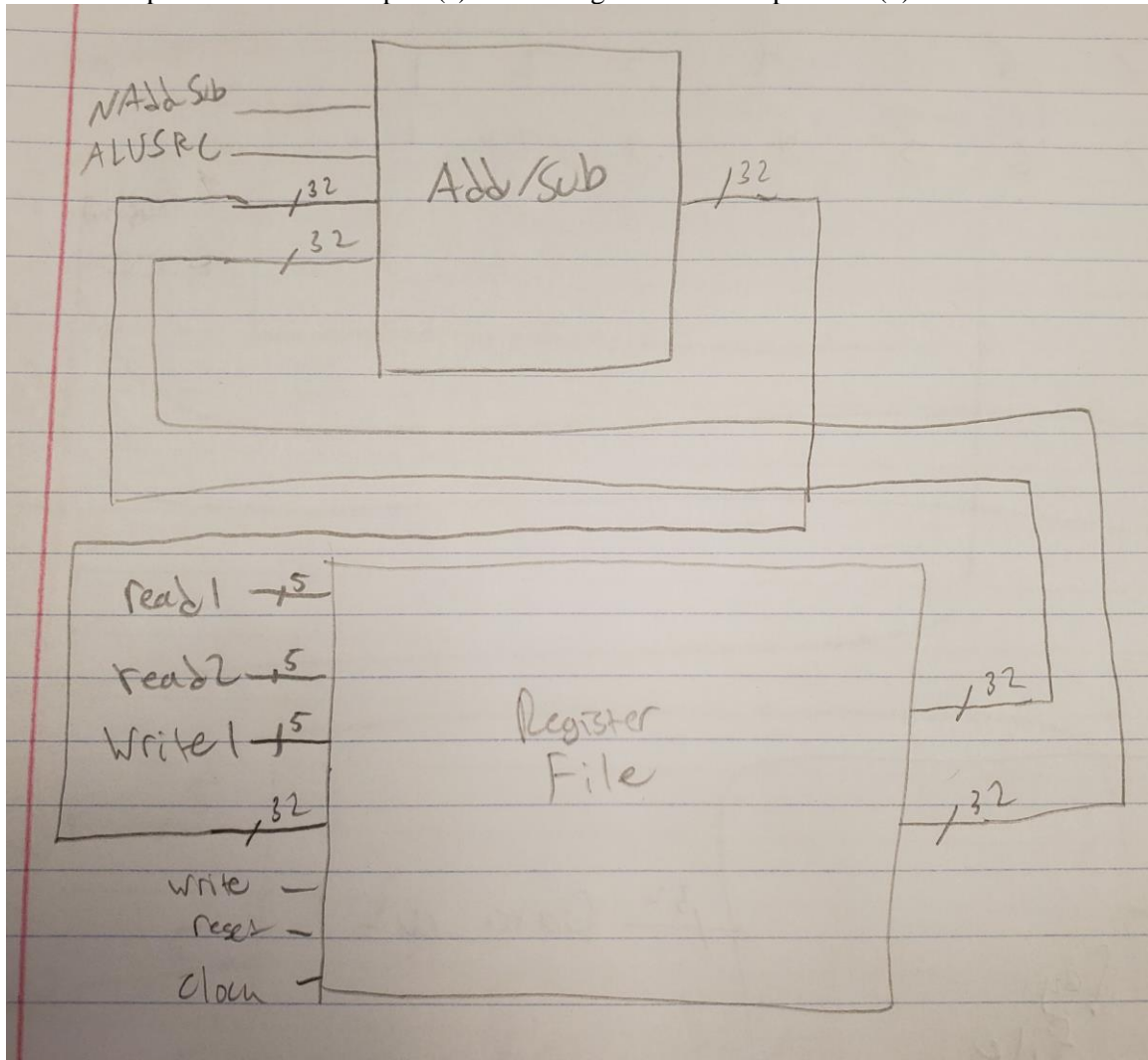
i. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).

j. [Part 1 (i)] Waveform.

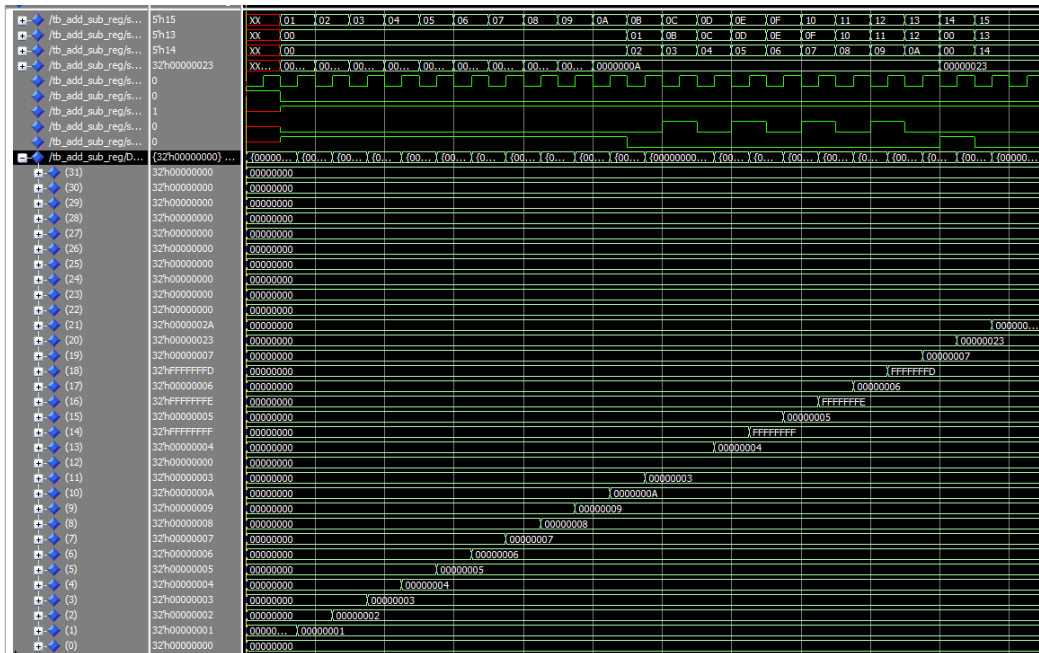


Didn't test every input because it would take forever.

- k. [Part 2 (b)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).



- l. [Part 2 (c)] Include in your report waveform screenshots that demonstrate your properly functioning design.



m. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	.5	.5
Pencil/paper design	.2	.5
VHDL design	1	2
Assembly coding	0	0
Simulation	.2	2
Debugging	.1	.5
Report writing	0	1
Other:	0	0
Total	2	6.5

ii. If you could change one thing about the lab experience, what would it be? Why?
I enjoyed this lab. Now that we've got more experience, I wouldn't change anything.

iii. What was the most interesting part of the lab?

How the processor we created has no outputs.