CprE 381 – Computer Organization and Assembly-Level Programming

Lab-04 Report

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Section / Lab Time Section 6, Thurs 4:10 to 6:00

Submit a typeset pdf version of this on Canvas by the due date. Refer to the highlighted language in the Lab-04 instructions for the context of the following questions.

a. [Prelab] Based on the waveforms, provide a description in your own words of how this component operates. This can be in the form of a textual description, flow chart, or state machine

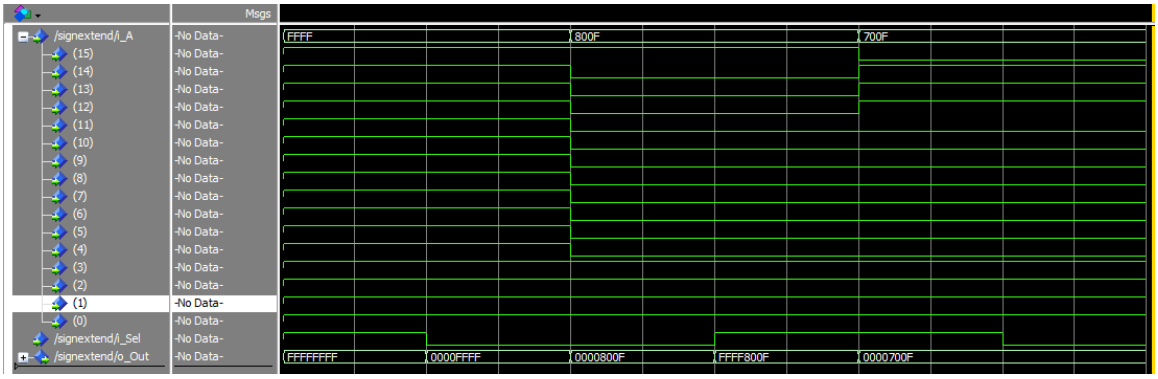
b. [Part 1 (a)] What are the MIPS instructions that require some value to be sign extended? What are the MIPS instructions that require some value to be zero extended?

Sign extended: sw, slti, sh
Zero extended: ori, andi

c. [Part 1 (b)] what are the different 16-bit to 32-bit "extender" components that would be required by a MIPS processor implementation?

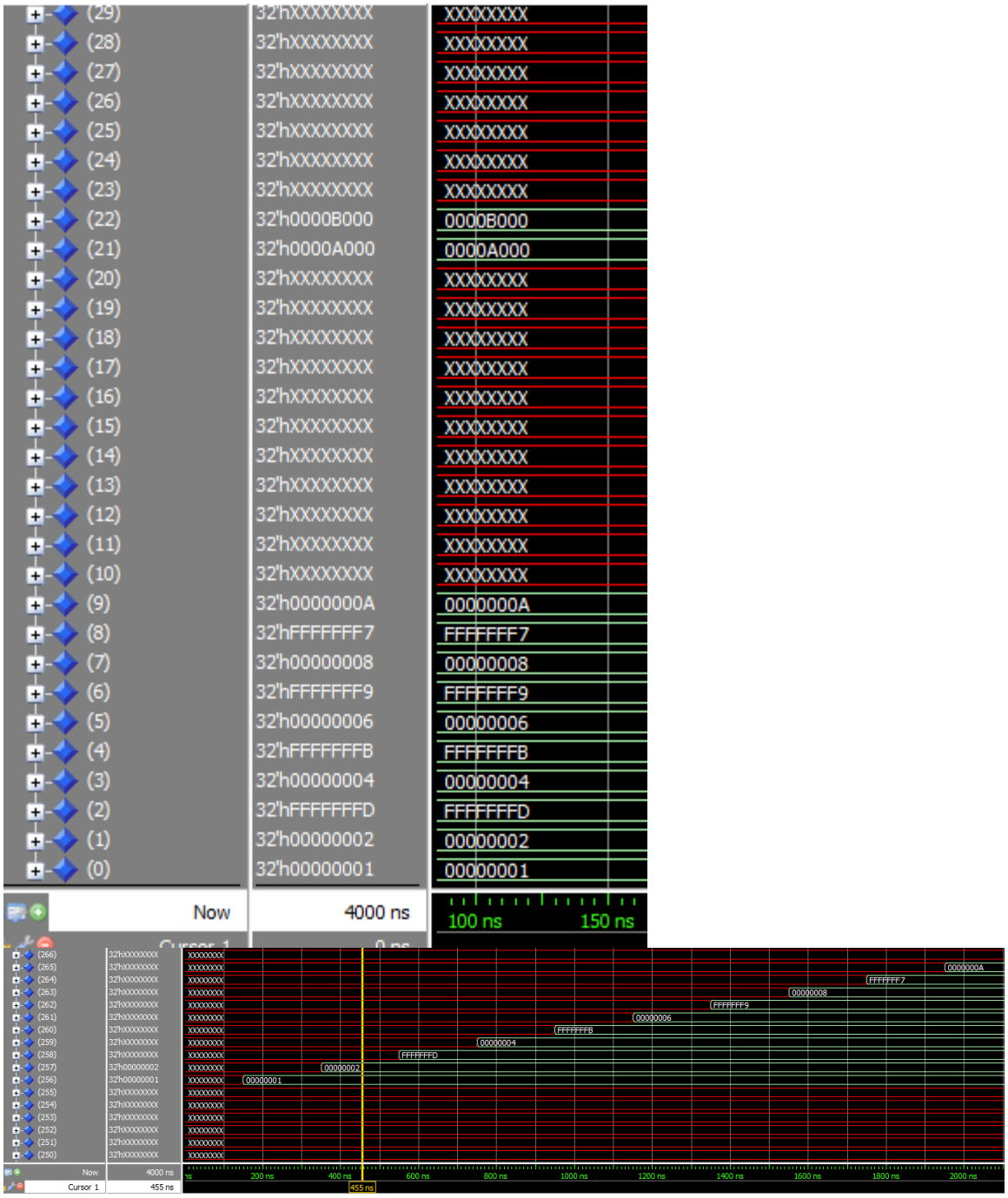
Zero extender and sign extender

d. [Part 1 (d)] Waveform.



e. [Part 2 (b)] Provide a 2-3 sentence description of each of the individual ports (both generic and regular).
Clk is the clock input which enables writing. Addr is the address that we are writing to, data is what is going to be stored, we is the write enable input. Q is the data output for reading.

f. [Part 2 (c)] Waveform.

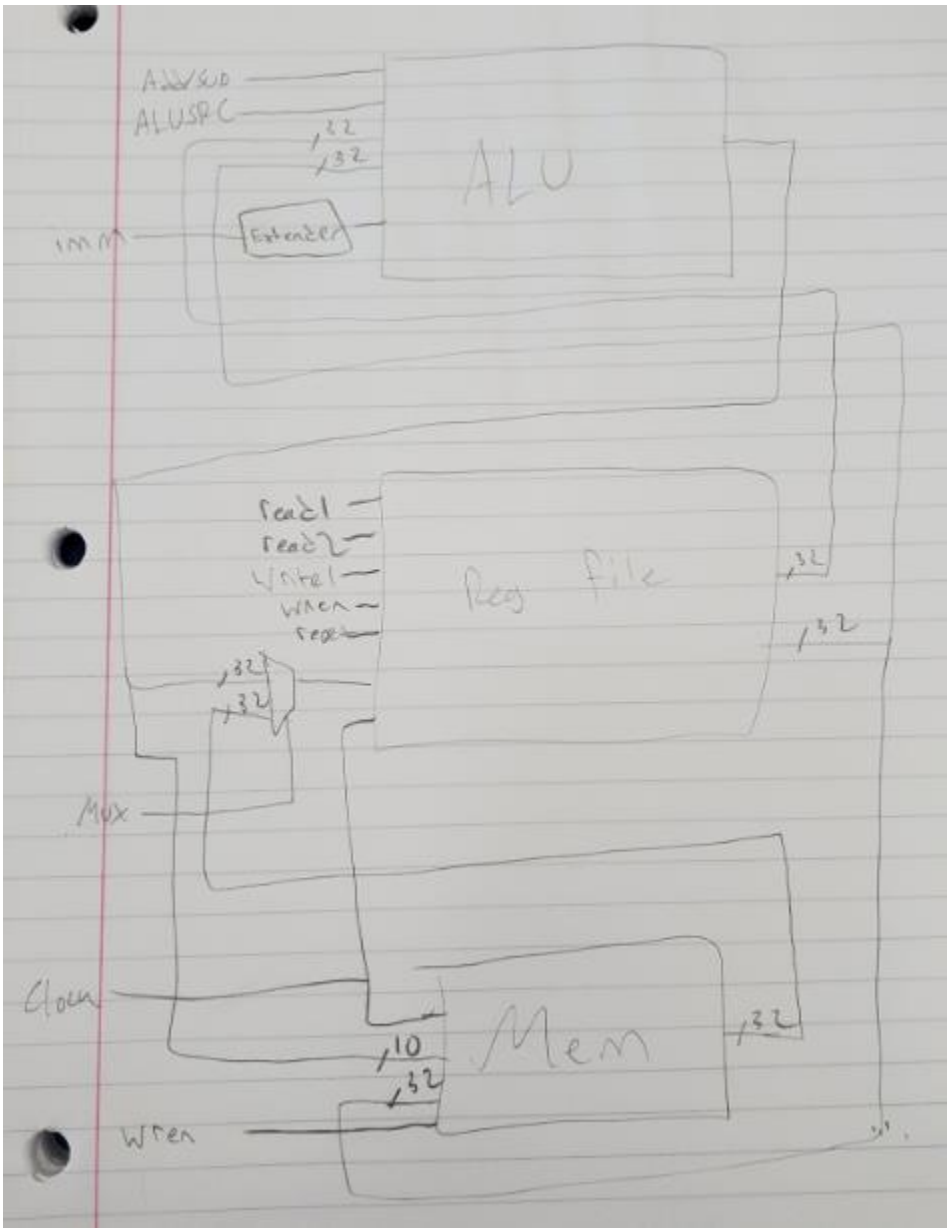

(29) 32'hXXXXXXXX XXXXXXXX
(28) 32'hXXXXXXXX XXXXXXXX
(27) 32'hXXXXXXXX XXXXXXXX
(26) 32'hXXXXXXXX XXXXXXXX
(25) 32'hXXXXXXXX XXXXXXXX
(24) 32'hXXXXXXXX XXXXXXXX
(23) 32'hXXXXXXXX XXXXXXXX
(22) 32'h0000B000 0000B000
(21) 32'h0000A000 0000A000
(20) 32'hXXXXXXXX XXXXXXXX
(19) 32'hXXXXXXXX XXXXXXXX
(18) 32'hXXXXXXXX XXXXXXXX
(17) 32'hXXXXXXXX XXXXXXXX
(16) 32'hXXXXXXXX XXXXXXXX
(15) 32'hXXXXXXXX XXXXXXXX
(14) 32'hXXXXXXXX XXXXXXXX
(13) 32'hXXXXXXXX XXXXXXXX
(12) 32'hXXXXXXXX XXXXXXXX
(11) 32'hXXXXXXXX XXXXXXXX
(10) 32'hXXXXXXXX XXXXXXXX
(9) 32'h0000000A 0000000A
(8) 32'hFFFFFFF7 FFFFFFF7
(7) 32'h00000008 00000008
(6) 32'hFFFFFFF9 FFFFFFF9
(5) 32'h00000006 00000006
(4) 32'hFFFFFFFB FFFFFFFB
(3) 32'h00000004 00000004
(2) 32'hFFFFFFFD FFFFFFFD
(1) 32'h00000002 00000002
(0) 32'h00000001 00000001
Now
4000 ns
100 ns
150 ns
Cursor 1
0 ns
Now
4000 ns
Cursor 1
455 ns
200 ns
400 ns
600 ns
800 ns
1000 ns
1200 ns
1400 ns
1600 ns
1800 ns
2000 ns

g. [Part 2 (d)] Briefly describe how the waveforms for this mem.vhd module differ from those that you analyzed as part of the pre-lab.
The wave form differs because we do not have a byte enable line. We also do not read and write at the same time so there is not as much overlap. Each cycle is done one after another

h. [Part 3 (a)] what control signals will need to be added to the simple processor from Lab #3? How do these control signals correspond to the ports on the mem.vhd component analyzed in problem 2)?

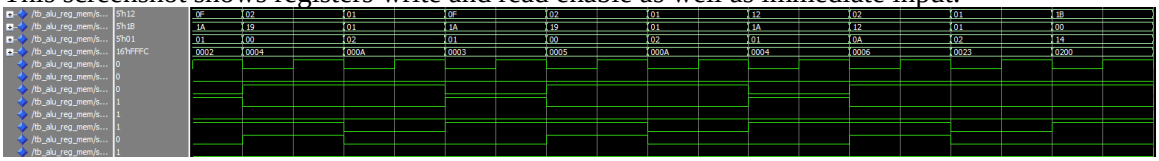
We will need to add a mux select for the alu and memory outputs being fed into register file's data port, as well as a sign/zero extend signal for the immediate value into the alu.

i. [Part 3 (b)] Draw a schematic of a simplified MIPS processor consisting only of the base components used in Lab #3, the extender component described in problem (1), and the data memory from problem (2).

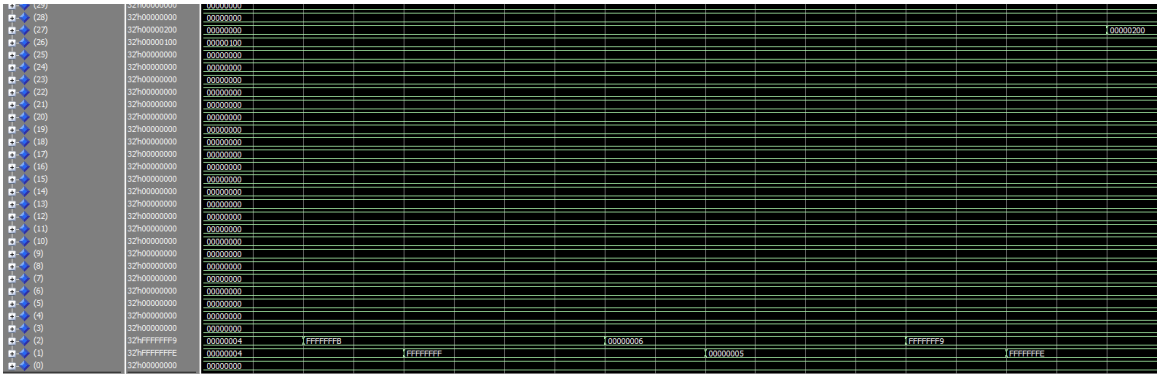


j. [Part 3 (c)] Waveform.

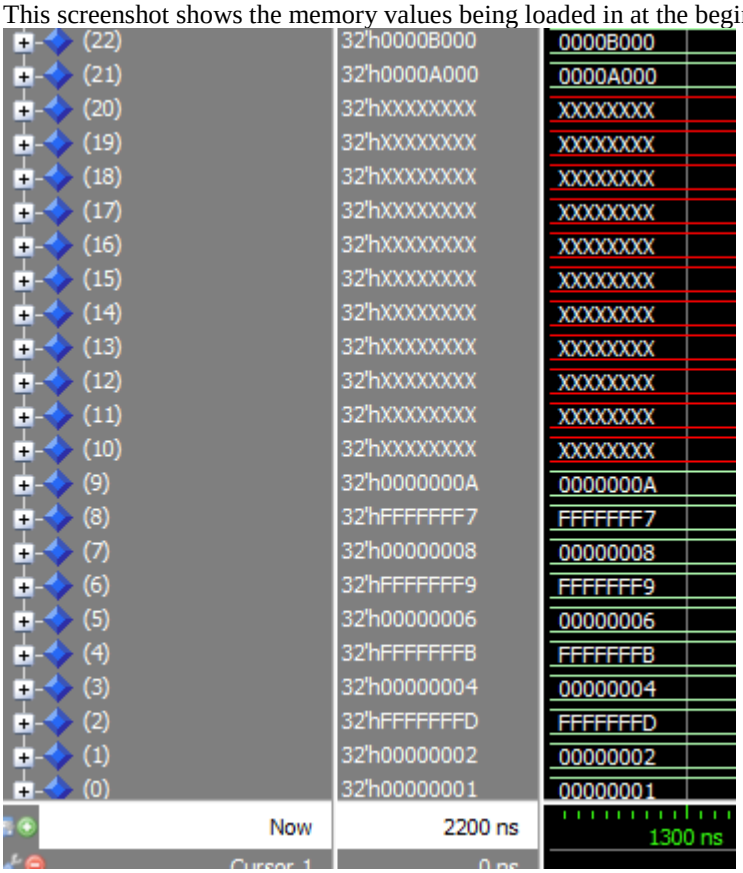
This screenshot shows registers write and read enable as well as immediate input.



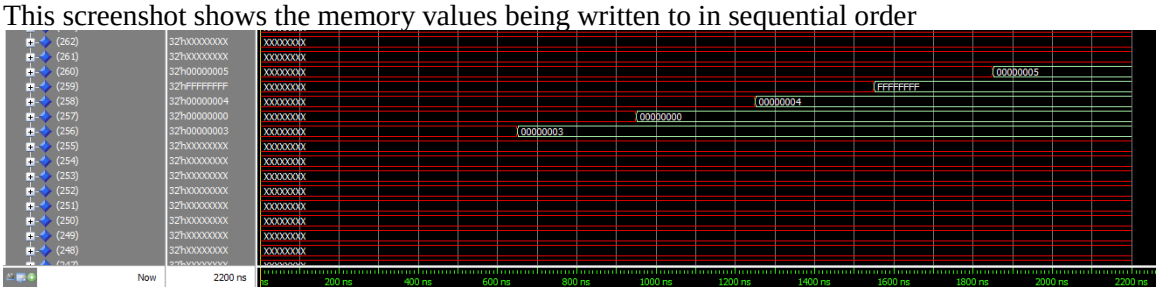
This screenshot shows the register values chaning as lw and add/addi are being called



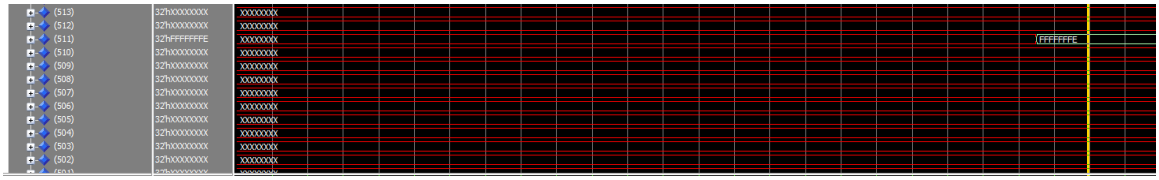
This screenshot shows the memory values being loaded in at the beginning



This screenshot shows the memory values being written to in sequential order



This screenshot shows the last sw call that stores into B[255]



k. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	.25	0
Pencil/paper design	1	.25
VHDL design	2	.25
Assembly coding	0	0
Simulation	.5	.25
Debugging	.25	.25
Report writing	0	.75
Other:	0	0
Total	4	1.75

ii. If you could change one thing about the lab experience, what would it be? Why?
Better explanation of how the alu, register file, and memory are supposed to mesh together. Had to ask a TA and it was still rather confusing at times

iii. What was the most interesting part of the lab?
Being able to mesh together all of the parts of lab and be able to store it into ram