# A New Low-Power, Low-area, Parallel Prefix Sklansky Adder with Reduced Inter-Stage Connections Complexity

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*Abstract*— In this paper a relation between graph energy and electrical energy or power consumption with graph nodes and edges for PPA structures is introduced. The Sklansky PPA is selected as the target PPA and its recursion steps limited. This reduced the internal nodes of the PPA. The reduction of nodes and edges and limiting the recursive stages to maximum 8 steps, resulted in proposed adder I and using special dot and semi-dot operators for graph nodes in proposed adder I led to proposed adder II. The number of transistors, total power and critical delay path of our proposed adder II are reduced about 31%, 29% and 7% versus Sklansky adder respectively. Finally the power-delay-product (PDP) of proposed PPA II comes with about 35% improvement compared with Sklansky adder.

***Keywords-component; Parallel prefix adder; Sklansky; Low-power; CMOS Circuits; physical power; graph energy***

## I. INTRODUCTION

The rapid growth rate of mobile and portable electronic devices shows higher demands on low-power and power-aware hardware designs. Adders are the most common units in broad scope of applications ranging from Arithmetic Logic Units (ALU), Digital Signal processors (DSP), Microprocessor, Digital communication sub units to mobile handsets and all portable and embedded devices. The propagation delay of an adder unit puts a major constraint on the minimum cycle time or maximum clock frequency.

The most known adders are Ripple Carry Adder (RCA), Conditional Sum Adder (CS), Carry Select Adder (CSA), Carry Look-Ahead (CLA), Carry Skip Adder, and Manchester Carry Chain (MCC). The parallel Prefix Adders (PPAs) are the target of most recent scientific investigations [1] [2]. PPAs have unified organizations in their structure and are superior over the other adder structures. They are in different structures, but most of their differences belong to their propagate tree structure. The Sklansky (SK) adder was introduced in 1960 which achieved the minimum logic depth in cost of large fan-out [3] [4]. The Kogge-Stone (KS) adder has the minimum logical depth of SK adder with the fan-out limited to maximum=2 where it is achieved in cost of computations nodes and interconnections complexity and increased power dissipation [5]. The Brent-Kung (BK) [6] adder in 1982 was proposed to resolve the drawbacks in KS adder [4]. It has $2N-2-\log_2 N$ merge carry blocks and has less complexity than KS adder. The logical depth is increased to $2\log_2 N-1$ that results in more delay and lower operational speed [4] [5]. The Han-Carlson adder is based on combination of KS and BK adders. In this adder, fan-out is decreased in cost of large logic depth [7]. Knowles presented a group of PPAs with minimum logic depth and higher fan-out [8]. The Ladner–Fischer is a general algorithm for PPA with higher logic depth than SK adder with reduced maximum fan-out in the critical delay path nodes [8].

The most common inspiration for from all above mentioned PPA structures is their regular and special graph structures. Due to our knowledge the graphs of PPA structures are not studied from the low-power viewpoint directly.

In this paper we study the relation of PPA graph nodes and connections or graph edges with graph energy in a meaningful manner. Furthermore, we applied our studies on graph theoretical energy to graph physical and electrical power and energy and show the direct relation between them. Finally using a trade-off between graph theoretical energy and logical-depth in SK adder we introduced a new PPA 8 level of recursive steps.

The structure of the reminder of this paper is organized in the following manner: In section 2 the basic theory of PPA is discussed. In section 3 the relation of graph theoretical energy and graph electrical power are studied. The proposed PPAs is presented in section 4. Section 5 is for circuit level (transistor-level) simulations and performance measures. Finally, section 6 concludes the paper.

## II. PARALLEL PREFIX ADDERS

PPAs are based on a tree structure to reduce the latency to $O(\log_2 n)$ where n is the number of bits [8]. The addition is performed in three stages. The first stage or pre-processing stage produces the Generate and Propagate signals of two input operands. In the second stage, two special operators of dot and semi-dot (●,○) produce the required signals. The two operators of dot and semi dot are defined according to (1) and (2) respectively [8].

$$(p_i,g_i)\bullet(p_{i-1},g_{i-1})=(p_i.p_{i-1},g_i+p_i.g_{i-1}) \quad (1)$$

$$(p_i,g_i)\circ(p_{i-1},g_{i-1})=(g_i+p_i.g_{i-1}) \quad (2)$$

In the PPAs, the dot operator produces group generate and group propagate signals. The semi-dot operator has the same functionality but it is used in the end nodes of each column and used to generate the group generate signals only. The third stage is called post processing which results the final bits by XOR of carry and propagate signals from previous stages.

## III. GRAPH THEORETICAL AND PHYSICAL POWER AND ENERGY OF PARALLEL PREFIX ADDERS

### A. Adjacency matrix of PPAs

In PPAs the major functional unit with dense orientation of calculations and logical functionalities to produce carry signal is middle stage. The complexity and function rich feature of this stage plays a major impact on power consumption in it. Therefore, in this section the middle stage is studied in more details from theoretical and physical graph power issues.

From graph theoretical aspects if in the PPA graph, each computational node is assumed as a node, and each connection between any two computational nodes is assigned as edge, then the adjacency matrix of the graph is a matrix of n*n where n is the total number of nodes. In adjacency matrix the ij-th element is nonzero if there is an edge between node i and node j otherwise it is zero.

The adjacency matrix for 4 and 8-bit KS adders are depicted in Fig. 1 and 2. As shown in Fig. 1, the 4-bit KS adder has 6 computational nodes in middle stage. Therefore, its adjacency matrix order is 6*6. The most of the elements in this matrix are zero. The 8-bit KS adder comes with more complex adjacency matrix and increased non-zero elements in it. This implies that adjacency matrix is a good candidate for PPA study for number of computational nodes, wiring tracks and estimated logic area. Furthermore the consecutive multiplication of adjacency matrix is a good candidate for logical depth evaluation.

### B. The graph energy and Physical Power of PPAs

In a graph G with n nodes and $\lambda_1,\lambda_2,\ldots,\lambda_n$ as the special values of its adjacency matrix, then the graph theoretical energy is according to relation 3 [9].

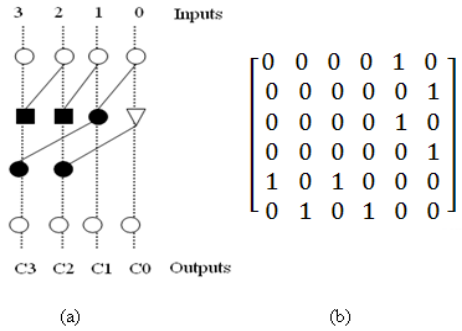


Fig. 1. (a) The structure of 4-bit KS adder, (b) The adjacency matrix of 4-bit KS adder

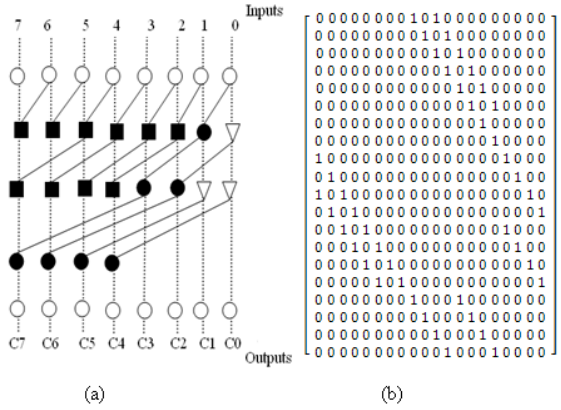


Fig. 2. (a) The structure of 8-bit KS adder, (b) The adjacency matrix of 8-bit KS adder

$$E = E(G) = \sum_{i=1}^{n} |\lambda_i| \quad (3)$$

The theoretical graph energy for main three PPA structures of BK, SK, and KS adders with 16-bit configuration is summarized in Table I. In the first scenario, at the calculations it is assumed that the power of individual nodes and the connections are not taken into account. For direct calculations, the dot and semi-dot nodes are assumed equivalent and all the present buffers are omitted except the buffer of $C_0$ in KS adder. The connections of other buffer are transferred to their previous nodes. To have a clear start point for our study, the physical power and propagation delay of the target adders are measured via HSPICE simulation. The results of simulations presented in Table I. It is obviously seen that there is a linear

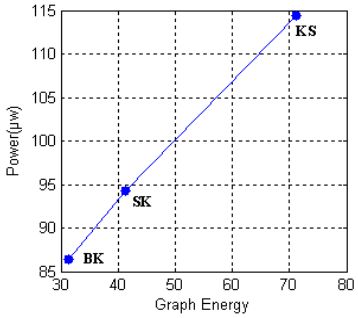


Fig. 3. The variation of Power versus graph energy for 16-bit adders

Table I. The graph energy and physical power of 16-bit PPAs

| Adder | Vertices | Edges | Graph Energy | Power (µw) | Delay (ns) |
|---|---|---|---|---|---|
| Brent- kung | 26 | 29 | 31.3913 | 86.36104 | 0.97 |
| Sklansky | 32 | 41 | 41.2863 | 94.3991 | 0.64 |
| Kogge-Stone | 50 | 68 | 71.0924 | 114.3645 | 0.62 |

Table II. The graph energy of various 32-bit adders

| Adder | Vertices | Edges | Graph Energy | Power (µw) | Logic depth |
|---|---|---|---|---|---|
| Reduced[8] | 54 | 62 | 65.3509 | 184.51 | 9 |
| Brent-kung | 57 | 67 | 69.9956 | 186.94 | 9 |
| Sklansky | 80 | 113 | 106.2993 | 246.94 | 5 |
| Kogge-Stone | 130 | 196 | 193.7620 | 291.44 | 5 |
| Propposed I | 65 | 82 | 81.0984 | 194.36 | 6 |

relation between the number of nodes/edges and graph energy in PPA graphs. The physical powers of the studied adders of Table I are illustrated in Fig. 3. As seen in this figure, the physical power is linearly related to graph theoretical energy.

Our main goal in this research is based on using from graph theoretical energy and its direct dependency to nodes and edges for study of high performance adders with modification on graph inner structure while preserving the functionality and correctness. We applied this idea on SK structure which has high power consuming, to change the number of inner nodes and edges. This approach does not alter the circuit functionality. It slightly increases the delay or degrades the speed but reasonably reduces the power which in overall reduces the PDP of the proposed adder.

## IV. THE STRUCTURE OF 32 BIT PROPOSED ADDER

### *A. Proposed adder I*

In the SK adder, the fan-out is linearly related to logic depth and increases with it. The logic depth increase in turn causes to more buffers insertion and degrades the speed and area penalty. On the other hand, the main factor for power consumption in this structure is MSB. In the main scope of adder applications like ALU, the most frequently changed bit is LSB not MSB. The former bit change rate is very in-frequent and there is no need for speed-up in this section. Therefore, it is possible to reduce the number of nodes and connections with fixed fan-out reduce the power and area of this unit reasonably.

Reducing the number of recursive steps in the middle stage of PPAs is one of technique to reduce nodes number and connections in this stage. The Fig. 4 part (a) illustrates the structure of presented adder in [8] with dot and semi-dot cells, the recursive steps in the middle stage of this adder were reduced to 4 that reduce the number of nodes and edges

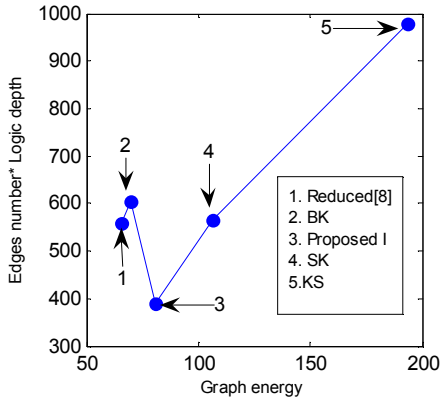


Fig. 5. The variations of logic depth * edges number versus graph energy

considerable. Its maximum fan out is 4 which causes large logic depth, hence degrades performance. Our proposed adder I is shown in Fig. 4 part b that it is achieved by reducing the recursive steps to 8. In our proposed design I a tradeoff between graph energy and logic depth is introduced which removes the problems of SK adder in terms of area and maximum fan-out.

Table 2 reports the graph energy and power consumption of 32-bit PPAs. The condition of buffers in this table is similar to Table 2. In this table the adder with maximum recursive steps 4 which is indicated as reduced [8] has minimum graph energy, nodes and edges number. However, this advantage comes in cost of logic depth. While, the graph energy of proposed adder I decreased 24% over the SK adder, its logic depth is increased one step only. As see in Table II increase in edges number results in more graph energy. The rate of increase is linear. Therefore the edges number of PPA adders is directly proportional with power dissipation and it can be used to compare of PPAs power. The variation in product of logic depth and edges number is illustrated in Fig. 5. It is seen that the minimum value is achieved for the proposed adder I. This resulted from in a tradeoff between logic depth and edges number.

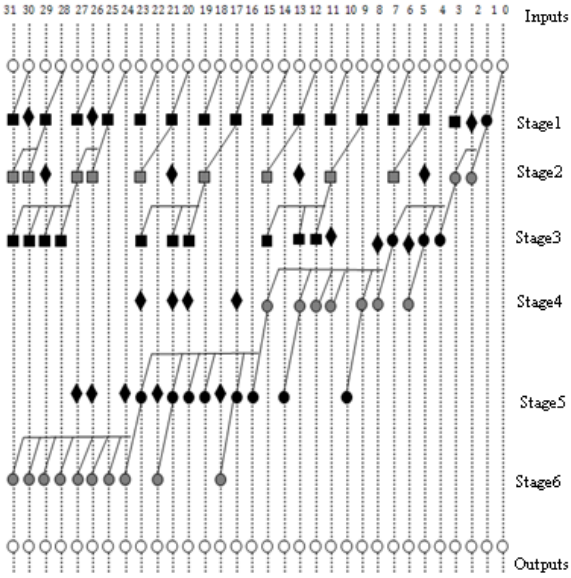


Fig. 6. The Structure of 32-bit proposed adder II

Table III. Characteristics of 32 bit PPAs

| Adder | Number of computation nodes | | Transistors count in intermediate Stage | Logic Depth |
|---|---|---|---|---|
| | Dot | Semi-Dot | | |
| Ramanathan | 23 | 31 | 688 | 9 |
| Kogge-Stone | 98 | 31 | 2136 | 5 |
| Sklansky | 49 | 31 | 1254 | 5 |
| Proposed II | 34 | 31 | 862 | 6 |

Table IV. Performance comparison of 32 PPAs using TSMC 180nm in $V_{DD}$=1.8v

| Adder | Delay (ns) | Average power (µw) | Power-Delay Product (x $10^{-15}$ Joules) | Maximum Frequency (GHz) |
|---|---|---|---|---|
| Ramanathan | 1.25 | 160.70 | 200.875 | 0.8 |
| Sklansky | 1.09 | 246.94 | 269.165 | 0.91 |
| Kogge-Stone | 0.92 | 291.44 | 268.130 | 1.08 |
| Proposed II | 1.01 | 173.34 | 175.164 | 0.99 |

### *B. proposed adder II*

In this section, we modify the structure of proposed adder I and suggest the proposed adder II. The graph of our proposed adder II is illustrated in Fig 6. This adder is implemented with calculation nodes (odd-dot, even-dot, odd-semi-dot and even-semi-dot) are based on [8]. Using the implemented nodes, the overlaps between sub-terms are reduced and the total performance is improved. In Fig. 6 the shown symbols of ■,■,●,● and ♦ cells are odd-dot, even-dot, odd-semi-dot, even-semi-dot and a pair inverter respectively. By using two cells for dot operator and two for semi-dot operator, a large number of inverters are eliminated. This results in decreased power dissipation significantly due to reduction of switching.

## V. SIMULATIONS

In this section the simulation scenario for the proposed adder II and reference PPA adders are presented. The target technology of simulation is CMOS 180nm. All the simulations are applied for test with at least 250 random vector inputs. The aspect ratio of the MOS transistors is selected as $(w/l)_p = 3(w/l)_n$. Threshold voltages during the simulation are $V_{thp} = 0.3944v$ and $V_{thn} = 0.3694v$ for PMOS and NMOS respectively. The detailed results of simulation are collected in Table III. As seen in this table, the graph constraint on the maximum level of recursive levels to only 8 levels reduced about 20% on the total number of computational nodes and number of transistors used in the final proposed design is also reduced about 31% in compared with SK adder. This improvement is achieved in the cost of one stage increase. The reduction of recursive steps caused to reduce the maximum fan-out, which in turn removes extra buffers of SK adder structure. The overall effect of these modifications reduces total area for target layout.

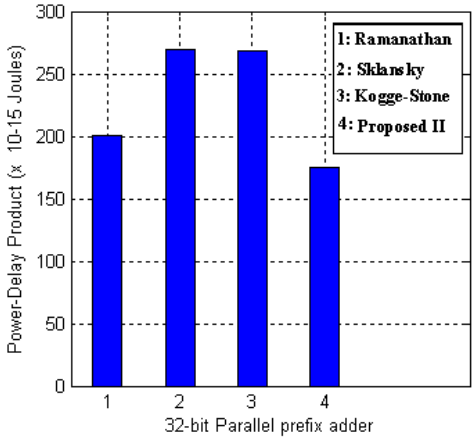


Fig. 7. The PDP variations of 32-bit PPAs

The simulation results on power, delay, power-delay-product and maximum operational frequency are presented in Table IV. The reduction of switching in the interior stages is the main responsible for total reduced power. The PDP variations for all three studied and our proposed PPA II are depicted in Fig. 7. The PDP of proposed PPA II comes with about 35% improvement versus SK adder. The total power of proposed adder II is increased about 8% versus Ramanathan [8] with even and odd cells, since the delay is reduced about 19%. Therefore, the total PDP is improved about 11%.

## VI. CONCLUSION

In this paper, it is shown that there is a direct relation between graph energy and electrical energy or power consumption with graph nodes and edges. In the Sklansky parallel prefix adder, the reduction of nodes and edges and limiting the recursive stages to maximum 8 steps from one side and using even and odd cells for graph nodes from the second side, resulted in a new PPA structure. The PDP of this proposed PPA comes with about 35% improvement versus Sklansky adder.

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