ECE555

Final Project Assignment

Due 6:00pm - Dec 13, 2011 – we will have a demo session at EH B555!

Objective: Design and layout a 32-bit parallel prefix adder while minimizing the product of area, delay, and dynamic power consumption.

Note:

- Use the cells that you design from CAD assignment 1 and 2 and do not modify the height of the cells although you are allowed to change the transistor sizing.
- Use only Metal 1, 2, and 3 (i.e., M1, M2, and M3) for connecting transistors; you have M2 VDD/VSS lines in the template and you can use M1-M2 vias to connect the VDD/VSS of the transistor to M2 VDD/VSS lines.
- Use VDD = 1.8V.

Procedure:

1. Create the schematics for a 32-bit parallel prefix adder. <u>You should analyze/estimate area, dealy, and power consumption of various parallel prefix adders before you choose a specific adder.</u>

2. I recommend that you should maintain a proper design heirchy for the easiness of design debugging.

3. Validate the correctness of your top-level schematic design using Verilog. You apply the follwing input pattern sequences to propagate the carries all the way through 32nd bit:

    a. (A, B, Cin) = (0x00000000, 0xffffffff, 0) -> (0xffffffff, 0x00000000, 1) [for HL delay]
    b. (A, B, Cin) = (0xffffffff, 0x00000000, 1) -> (0xffffffff, 0xffffffff, 0) [for LH delay]

4. Create a test-bench schematic for the adder by instantiating the symbol you created in Step 1. Attach an inverter symbol at each sum node (P=4.32um/N=2.16um).

5. You measure the HL dealy between the input and the output of all the sum nodes (not the output of the INV gates you attached).

6. Create the layouts for the adder using Cadence layout editor..

7. Extract the capacitance values of each node, annotate them to measure the LH and HL delay values with the same input you applied at Step 2.

Submission:

- README file that includes the paths for the schematic, layout, DRC/LVS reports.
- Verilog netlist w/ the test bench; you validate the correctness of your design using Verilog.
- Simulation wave forms using the Verilog logic simulator (for the full input combinations) and Spectre circuit simulator after finishing your layout and annotating the extracted capacitance values (only for the rise and fall delay measurements) for your final design.
- Final report that provides early design analysis to justify the choice of a specific adder; provide details of how you estimate the area, dealy, and power consumption before you choose a specific adder.