SoM-150ES

User Manual

REV. 1.2

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1 Introduction

This document provides information regarding EMAC's SoM-150ES SoM Carrier Board. The SoM-150ES is versatile SoM Carrier board ideal for evaluation and early development work. This Carrier can work with all EMAC 144 SODIMM type SoMs. However, to fully utilize the SoM Carrier's hardware, a SoM with USB, Audio and parallel SD card capabilities should be used with the SoM-150ES.

The SoM-150ES provides access to all of the 144 pin SoM's I/O through on-board connectors as well as a number of additional I/O expansion blocks such as A/D, D/A, Digital I/O, Audio, and MMC/SD flash disk. Full schematics of the SoM-150ES are provided giving the user a solid base with which to design their own SoM Carrier.

Although a good deal of customers will want a Carrier that is unique and is designed specifically for their application, the SoM-150ES, when coupled with a SODIMM SoM makes for a powerful Data Acquisition and Control system with USB and Ethernet capabilities. This allows the user to gather data and respond with Control commands via the Internet. An Enclosure and Power Supply are available options for the SoM-150ES.

When a unique custom board is required, the amount of design work required is greatly minimized by the SoM approach. The custom Carrier designer does not have to worry about the processor, memory, and standard I/O functions and can concentrate on the I/O and dimensional aspects required for the application.

In situations where a custom Carrier is required but the customer does not have the capability to design such a board in-house, EMAC's Custom to Order Services (COS) can be utilized. Using COS the customer can select from a library of standard I/O blocks. These blocks can be put together quickly into a form-factor of the customer's choosing, providing prototypes in as little as 30 days.

Note: This manual addresses two slightly different Revisions of the SoM-150ES Carrier board. At different points in the manual a Reference to Revision 1 or to Revision 2+ (2 and greater) may be made. Check the PCB Revision Label on your SoM-150 board to determine which applicable to you. Depending on what functionality is being used, different Software part numbers for the SoM module may be required, however this should be transparent to any application software running on top of the Operation System.

1.1 SoM Benefits:

- Faster time to market
- Cost savings
- Reduced risk
- Scalable CPU choices
- Decreased customer design requirements
- Small footprint

1.2 Standard Features

- **Small, Half EBX mounting hole form factor (4.37" x 6.00")**
- **10/100 BASE-T Ethernet with on-board Magnetics and RJ45**
- **4 serial RS232 ports and 1 RS232/422/485 port (ports must also be supported by the SoM)**
- **1 CAN port (port must also be supported by the SoM)**
- **30 PLD controlled General Purpose digital I/O lines in addition to any SoM I/O lines**
    - **22 digital input / output lines**
    - **8 high drive digital output lines**
- **24 key, keypad interface**
- **Character LCD interface**
- **Battery for nonvolatile RAM and Real Time Clock**
- **MMC/SD Flash Card Socket**
- **Power and MMC/SD status LEDs**
- **System Reset button**

1.3 On-Board Options

- **Analog:** Analog I/O Upgrade Includes:
    - 8 channel 12-bit A/D
    - 2 channel 12-bit D/A
- **Audio:** I2S Audio Stereo CODEC (ports must also be supported by the SoM)
- **Reduced Cost "Bare Bones" Version**

1.4 Other Options

- **MBPC-200 Enclosure:** This MicroBox metal chassis is an ideal housing for the SoM-150ES and SoM.
- **PS-50A Power Supply:** A 50 watt switching power supply that has an AC input of 100 to 240 volts and DC outputs of +5 volts and +12 volts. The PS-50A is especially designed to operate with the MBPC-200 MicroBox chassis.
- **Wall-Mount Power Supply:** An inexpensive 5 Volt DC supply capable of 2.5 Amps of current.

2 Hardware

2.1 Specifications

- **VOLTAGE REQUIREMENTS:** 5 volt DC @ 1.5A board input voltage including SoM and USB. (Note: up to 1.0A of the 1.5A is required if USB Host is providing power to USB devices.)
- **CURRENT REQUIREMENTS:** 300 ma. @ 5 Volts Typical including SoM with no USB sourcing.
- **OPERATING TEMPERATURE:** 0 - 70 degrees Celsius, humidity range without condensation 0% to 90% RH.
- **DIMENSIONS:** Half EBX mounting hole form factor with dimensions of 4.37" x 6.00".
- **DIGITAL I/O:** 22 digital input / output lines, 8 open collector High-Drive Digital outputs with 500 ma. sink drive capability, status LEDs, and a maximum total I/O drive of 1500 ma. for these 8 lines. All Digital I/O lines terminate to standard 50 pin, I/O Rack compatible header connectors.
- **OPTIONAL ANALOG INPUTS:** 8 analog inputs are multiplexed into a single 12-bit A/D converter with Sample and Hold. The analog input voltage range for each channel is 0 – 2.5 Volts.
- **OPTIONAL ANALOG OUTPUTS:** 2 analog outputs implemented using a 2 channel, 12-bit D/A. The analog output voltage range for each output is 0 – 2.5 Volts with a drive capability of 5 mA.

2.2 Jumpers

This section describes the Jumpers and Jumper Blocks of the SoM-150ES.

JB1

Boot Mode 1 The function of this jumper is determined by the SoM that is being utilized (see SoM user manual). This jumper is tied to SoM pin 41 (Boot Option1). If the jumper is in the EBI position then this line is pulled high. If the jumper is in the DBI position then the line is tied low.

JB2

Boot Mode 2 The function of this jumper is determined by the SoM that is being utilized (see SoM user manual). This jumper is tied to SoM pin 74 (Boot Option2). If the jumper is in the NFD position then this line is tied high. If the jumper is in the NFE position then the line is pulled low.

JB3

CAN Termination JB7 controllers CAN termination resistors on the CAN port. When the jumper is in the T position, a 120 Ohm resistor is connected in parallel between the CANH and CANL signal lines. When the jumper is in the O position, no on-board termination is utilized.

JB6

LCD Configuration LCD configuration jumpers. These Jumpers allow for different types of LCDs and backlight control. The Backlight Control is connected to the PLD (U9) pin 81.

Jumper	A&B, C&D	backlight always on
Jumper	C&D	port line control (BACKLIGHT_EN) of backlight through software
Jumper	G&C	allows the use of certain graphic LCDs

JB7

Voltage Option Place a jumper in the 5V position to provide 5V to JB8. Place a jumper in the 12V position to route pin 4 of HDR2 (normally 12V) to JB8. JB8 controls the pull-up voltage of the High Drive Output lines and determines what voltage is present on pin 49 of HDR1.

JB8

Pull-up Voltage Option JB8 controls the pull-up voltage of the High Drive Output lines and determines what voltage is present on pin 49 of HDR1. The right side of the jumper controls pin 49 and the left side controls the pull-up voltage of Port C. Leaving the right side shunt off leaves pin 49 open and leaving the left side shunt off sets the High Drive Outputs to no pull-up voltage. The voltage at the top two pins is defined by JB7.

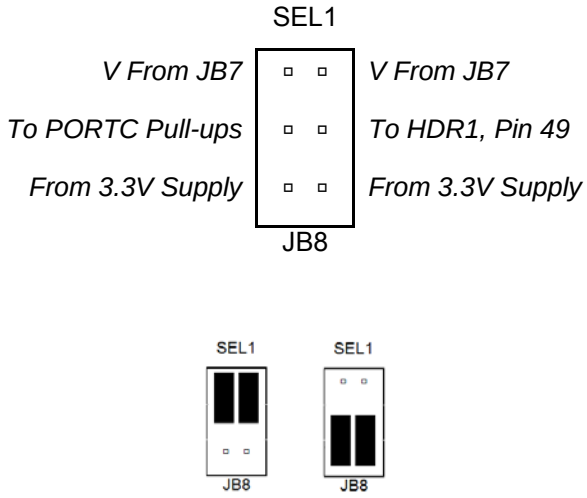

Figure 1: Typical shunt positions.

With both shunts in the upper position, the voltage selected by JB7 will be applied to pin 49 and Port C will be pulled up to that voltage. With both shunts in the lower position, 3.3V will be applied to pin 49 and Port C will be pulled up to 3.3V.

JB9

Battery Disconnect Place a jumper in the ON position to connect the battery to the SoM and place a jumper in the OFF position to disconnect the battery from the SoM. It is good to disconnect the battery when storing the SoM-150 with a module inserted for extended periods of time.

2.3 JTAG Header

This multipurpose header provides an in-circuit programming interface to the Max II CPLD that resides on the SoM-150ES as well as any PLD or Debug port on the SoM itself. This header can be used to reprogram the onboard CPLD and any other CPLDs detected on the chain (on the module). This connector is a 14 pin standard and a JTAG Debugger should be able to be directly connected. EMAC also provides an adapter board (PER-ADP-00020) which makes Carrier's PLD JTAG come out to a standard 10 pin header and also provides the alternate 20 pin JTAG connector for the module.

This requires an interface cable, such as the ByteBlasterMV. Several models are available from P&E Microcomputer Systems http://www.pemicro.com/. Also, more inexpensive versions and open schematics can be obtained via the Internet, i.e. http://www.cmosexod.com/.

Table 1: JTAG Header (HDR7)

Pin	Signal	Pin	Signal
1	3.3Vdc	2	GND
3	JTAG_TRST	4	GND
5	JTAG_TDI	6	PLD_JTAG_TDI
7	JTAG_TMS	8	PLD_JTAG_TMS
9	JTAG_TCK	10	PLD_JTAG_TCK
11	JTAG_TDO	12	NC
13	NC	14	PLD_JTAG_TDO

2.4 Module Based IO

The Module I/O connector, HDR4 is made up primarily of direct connections from the modules SODIMM connector. This 50-pin header connector consists of grounds on one side allowing 25 signals on the other side and maintaining compatibility with standard 50 pin, I/O Rack compatible header connectors. The only signals that do not directly come from the module are the Slave Selects, which are decoded from the first 2 SPI slave selects of the module in Revision 1, and the PLD Handy I/O lines in Revision 2.

Table 2: SoM I/O Connector (HDR4)

Pin	Rev1 DESCRIPTION – FINGER #	Rev2+ DESCRIPTION – FINGER #	Pin	DESCRIPTION
1	MS10 – 57	PLD_HNDY_03	2	GND
3	MS8 – 55	PLD_HNDY_01	4	GND
5	MS6 – 51	IRQC – 40	6	GND
7	GPIO1/IRQD – 42	GPIO1/IRQD – 42	8	GND
9	MS4 – 49	PLD_HNDY_06	10	GND
11	MS3 – 48	GPIO15 – 136	12	GND
13	MS5 – 50	CAN_TX – 96	14	GND
15	MS9 – 56	PLD_HNDY_02	16	GND
17	GPIO16 – 105	CAN_RX – 95	18	GND
19	GPIO2/IRQE – 87	IRQA – 75	20	GND
21	IRQA/GPIO – 75	1WIRE/I2C_SCL – 116	22	GND
23	GPIO 3/IRQF – 80	I2C_SDA – 88	24	GND
25	8 MHZ CLK – 114	8 MHZ CLK – 114	26	GND
27	200 KHZ CLK – 115	200 KHZ CLK – 115	28	GND
29	14.3 MHZ CLK – 117	14.3 MHZ CLK – 117	30	GND
31	SPI_SCK – 120	SPI_SCK – 120	32	GND
33	GPIO4 – 125	SPI_MO – 121	34	GND
35	GPIO6 – 127	GPIO6 – 127	36	GND
37	GPIO12 – 133	GPIO12 – 133	38	GND
39	GPIO5 – 126	GPIO14 – 135	40	GND
41	GPIO14 – 135	SPI_MI – 122	42	GND
43	GPIO13 – 134	GPIO13 – 134	44	GND
45	Carr_PLD_SPI_CS1 – 41	PLD_HNDY_04	46	GND
47	Carr_PLD_SPI_CS2 – 40	PLD_HNDY_05	48	GND
49	3.3Vdc	3.3Vdc	50	GND

2.5 CPLD Based General Purpose Digital I/O

The SoM-150ES provides 16 general-purpose 3.3V IO pins and 8 High-Drive output pins connected to header HDR1. These pins are controlled by an Altera Max II device, which is an in-circuit programmable, instant on, CPLD. By default this is the EPM240T100C5 model, which provides 150 internal logic elements, but it is pin-compatible with some larger devices. This CPLD provides powerful reconfigurable combinational and sequential logic, for an almost unlimited number of applications. Through Altera's free Quartus II environment this device can be easily reconfigured as digital IO, counters, UARTs, SPI, even flash and RAM. The CPLD interfaces through the address/data bus of the carrier, and has access to clocks and an IRQ for advanced control logic. When the SoM-150ES is built, it is pre-loaded with a configuration that it stores in its internal flash, and instantly loads on power-up. This configuration uses the pins in a specific manner, which is described in the rest of this section, but could be easily reprogrammed to be something else. EMAC provides free drivers and development software for interfacing with the standard configuration.

2.5.1 General purpose digital ports

The default program creates 3 8-bit digital ports, Ports A, B, and C. Port A and Port B are independently bit programmable as outputs or inputs. When programmed as inputs the input lines should not exceed 3.3Vdc and if programmed as outputs, these lines are capable of driving 25 mA loads. The open collector high drive output Port C (PC0 – PC7) has drive 500 mA sink drive capability and a maximum total I/O drive of 1500 mA. The PLD has it input capabilities on these 8 lines for modularity reasons, but they are not useable as such in the actual system. The voltage on pin 49 as well as the pull-up voltage for Port C is controlled by jumpers JB7 and JB8. See Jumper section for additional details. Six additional PLD "Handy" lines are provided on HDR4. These lines are programmed as independently bit programmable input or output lines by default.

Table 3: CPLD Based Digital I/O Connector (HDR1)

Pin	Signal	Pin	Signal
1	PA0 (3.3V)	2	GND
3	PA1 (3.3V)	4	GND
5	PA2 (3.3V)	6	GND
7	PA3 (3.3V)	8	GND
9	PA4 (3.3V)	10	GND
11	PA5 (3.3V)	12	GND
13	PA6 (3.3V)	14	GND
15	PA7 (3.3V)	16	GND
17	PB0 (3.3V)	18	GND
19	PB1 (3.3V)	20	GND
21	PB2 (3.3V)	22	GND
23	PB3 (3.3V)	24	GND
25	PB4 (3.3V)	26	GND
27	PB5 (3.3V)	28	GND
29	PB6 (3.3V)	30	GND
31	PB7 (3.3V)	32	GND
33	PC0 (High D)	34	GND
35	PC1 (High D)	36	GND
37	PC2 (High D)	38	GND
39	PC3 (High D)	40	GND
41	PC4 (High D)	42	GND
43	PC5 (High D)	44	GND
45	PC6 (High D)	46	GND
47	PC7 (High D)	48	GND
49	3.3 / 5 / 12V	50	GND

2.5.2 Memory Map

The SoM-150ES's PLD is connected to the SoM's processor data bus and uses SODIMM pin 108 as its select line. The Base Address of the PLD is SoM dependent.

For the EMAC SoM-9260M it is mapped to NCS4, which gives it a base address of 0x50000000.

See the manual that accompanied the SoM for further details. Additional PLD registers exist. See the Keypad and LCD section for details on these PLD registers.

Within the PLD are several registers that are referenced as offsets from the PLD Base address. They are defined as follows:

Table 4: Default CPLD Memory Map (Revision 1)

Offset	Register	Description
0	LCD Data	Read/Write LCD data bus
1	LCD Control	Set LCD control lines
2	PortA Data	Digital State
3	PortA Configuration	Input/Output Mapping
4	PortB Data	Digital State
5	PortB Configuration	Input/Output Mapping
6	PortC Data	Digital State
7	PortC Configuration	Input/Output Mapping
8	Keypad Register	Read Keypad Data
15	Key Register	PLD Core Version Key (0xC0)

Table 5: Default CPLD Memory Map (Revision 2)

Offset	Register	Description
0	LCD Data	Read/Write LCD data bus
1	LCD Control	Set LCD control lines
2	PortA Data	Digital State
3	PortA Configuration	Input/Output Mapping
4	PortB Data	Digital State
5	PortB Configuration	Input/Output Mapping
6	PortC Data	Digital State
7	Keypad Register	Read Keypad Data
8	Control Register	Control and Configuration Data
9	Serial 5 CTS	Serial 5 CTS State
10	Handy I/O Data	PLD Handy line digital state
11	Handy I/O Configuration	Input/Output Mapping
15	Key Register	PLD Core Version Key (0xC1)

Descriptions

Port Data Registers

The bits of these ports are mapped to the data lines of the physical ports. Writing to these bits latches Vcc or GND value (1 or zero respectively) to the appropriate pin. Pins are mapped according to their respective positions on the header, i.e. PB4 has its value latched by the 4th bit of the Port B configuration register.

Latching a bit will result in a voltage change at the pin if the pin is configured to be an output with the corresponding configuration register bit. Reading from this address will return the current state (1 or zero for Vcc or GND) of the pin.

Port Configuration Registers

This port is bitwise mapped to the configuration of the ports. Setting a bit to 1 sets the corresponding pin to an output, Setting a bit to 0, sets it as an input, example: Setting the Port B configuration register to 0x10 would set PB4 to be an output and place its current latched state (see the Data Register description) on the pin.

Keypad Register

Reading this register returns the last value latched from the keypad. The high nibble is the row; the low nibble is the column. The keypad sets its interrupt line when a button is pressed and releases it when data is read from this register.

LCD Data Register

This is used to latch data to the LCD data bus. This latched data is always present except during a read cycle. Which must be manually implemented from software (EMAC provides software for this) through the control lines.

LCD Control Register

This register latches the state of the control lines.
Bit 0 – RW control – 1 sets RW high, 0 sets RW low
Bit 1 – RS control – 1 sets RS high, 0 sets RS low
Bit 2 – Backlight control – 1 for on, 0 for off, when in software control mode.

Control and Configuration Register

This register provides several configuration lines for the carrier board hardware and control.
Bit 0 – RS485/422 RTS Polarity – 0 for no inversion, 1 for inversion
Bit 1 – Serial 5 RTS – 1 sets Serial 5 RTS high, 0 sets Serial 5 RTS low
Bit 2 – COMB 232 Buffer Enable – 1 disables COMB 232 buffer, 0 enables COMB 232 buffer
Bit 3 – RS485/422 Rx Enable – 1 enables the COMB 4xx receive driver, 0 to disable
Bit 4 – RS485/422 Rx Enable Mode – 1 for manual mode, 0 for auto mode
Bit 5 – Powerdown 232 – 1 to power down the COMB 232 Driver, 0 enables the driver

Note: Internal logic is used to determine the state of the RS485/422 control lines according to the signals above. The RS485/422 drivers are disabled regardless of control state when the RS232 buffer is enabled, so Bit 2 must be set to 1 before the RS485/422 control lines may be manipulated. The COMB RTS line is used to control the RS485/422 transmit driver enable signal. Most modules have an “Auto 485 toggle” mode that can be set in the processor to enable RTS flow control in hardware. However, some modules use RTS as an active high signal in this mode while others keep RTS active low (as in RS232) while in this mode, requiring inversion before connecting to the transmit enable on the driver. Bit 0 controls this polarity (no inversion is the default, which will work with the SoM-9260M). The RS485/422 receive enable signal has two modes in the PLD: manual and auto, which are controlled by Bit 5. If Bit 5 is low, Bit 4 will be gated with the RS485/422 transmit enable output, so that it will automatically be disabled when the transmitter is enabled. This prevents RS485/422 echo without the use of software control. With Bit 5 set high, RS485/422 receive enable will be in manual mode, so that Bit 4 directly controls the RS485/422 enable line for COMB.

2.6 Analog Channels

The SoM-150ES optionally provides a 12-bit, 8-channel A/D. In addition to the A/D, the SoM-150ES optionally provides 2 D/A channels with 12-bit resolution. These optional converters communicate with the processor through the on-board SPI. The A/D input channel accepts 0 – 2.5 Volt inputs. The D/A channels provide 0 – 2.5 Volt outputs with a drive capability of 5 mA. In order to access the optional 12-bit A/D (MCP3208) and D/A (MCP4922) communication must take place using the SoM’s SPI port. The A/D uses SPI_CS0 and the D/A uses SPI_CS1.

In addition to the Carrier A/Ds, some SoM modules also provide module based A/Ds. The Analog connector provides 4 pins for these potential connections. If the module does not have A/D capability then these pins will not work in that capacity.

Table 6: Analog I/O (HDR8)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	AIN00	4	AIN01
5	AIN02	6	AIN03
7	AIN04	8	AIN05
9	AIN06	10	AIN07
11	SoM AIN0	12	SoM AIN1
13	SoM AIN2	14	SoM AINI3
15	AOUT00	14	AOUT01
17	GND	18	GND
19	VCC +5VDC	20	Vref +2.5VDC

2.7 Ethernet

The SoM-150ES provides for the magnetics and RJ45 connector for a standard 10/100 Base-T port. Additionally, two LEDs are provided for Activity and Link status. The RJ45 is pinned as a standard 10/100 BaseT Ethernet port and thus should work with any standard router or switch.

2.8 USB

The SoM-150ES provides for a dual USB host port and a single USB device port. The USB host ports are fused with automatically reset-able Polyfuses. If a USB device tries to draw more than 500 milliamps the fuses will open. Once the drawing source is removed the fuses will automatically reset. The USB ports are pinned as standard USB host and device ports and thus should work with any standard USB mating device or host.

2.9 Serial Ports

2.9.1 RS 232 SERIAL COMA

Serial UART COMA is a dedicated RS232 serial port accessible via a 10-pin header connector with no handshaking signals. EMAC provides a Male DB9 DTE serial cable that plugs into this header and provides a standard interface. Note: the baud rate and other serial settings are determined by the SoM being used. Refer to the SoM manual for this information. The pin-out of the header and the DB9 cable are as follows:

Table 7: Serial Port COMA (HDR11)

#	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD
3	RxD	TxD
4	NC	NC
5	TxD	GND
6	NC	NC
7	NC	NC
8	NC	NC
9	GND	NC
10	NC	-

2.9.2 RS 232/422/485 SERIAL COMB

The SoM-150ES provides one multi-mode serial port. This port is software configurable as either RS232, RS422, or RS485, with the default being RS232. When used as an RS232 port, two handshake lines are provided, CTS and RTS. Switching from RS232 to RS422 or RS485 is controlled by four SoM-150ES based PLD signals. The signals are 232_LBUFFEN, 232_OUTCNTRL, 422-485_TXOUTEN, and 422-485_LBUFFEN. The 422-485_LBUFFEN line is used to enable the RS422/485 transmitter. When used in the RS485 mode some processors support Auto Direction via the RTS line. The RTS line is an input to the PLD thus allowing Auto Direction through the PLD. For low-level information on how to interface with the CPLD default program see: Section 2.5 CPLD Based General Purpose Digital I/O. Note: the baud rate and Auto Direction is determined by the SoM being used. Refer to the SoM manual for this information.

The Tables below describe the state of the control signals for the various serial port modes.

Table 8: Serial Port COMB RS232 (default) Mode

Signal	PLD Pin#	State
232_LBUFFEN	95	Low
232_OUTCNTRL	92	High
422-485_TXOUTEN	91	Low
422-485_LBUFFEN	90	High

Table 9: Serial Port COMB RS422 Mode

Signal	PLD Pin#	State
232_LBUFFEN	95	High
232_OUTCNTRL	92	Low
422-485_TXOUTEN	91	High
422-485_LBUFFEN	90	Low

Table 10: Serial Port COMB RS485 Transmit Mode

Signal	PLD Pin#	State
232_LBUFFEN	95	High
232_OUTCNTRL	92	Low
422-485_TXOUTEN	91	High
422-485_LBUFFEN	90	High

Table 11: Serial Port COMB RS485 Receive Mode

Signal	PLD Pin#	State
232_LBUFFEN	95	High
232_OUTCNTRL	92	Low
422-485_TXOUTEN	91	Low
422-485_LBUFFEN	90	Low

The connections to serial port COMB are through a 10-pin header. EMAC provides a Male DB9 DTE serial cable that plugs into this header and provides a standard interface. Note: when wiring for RS485 mode short TX+ and RX+ and short TX- and RX- together. The pin-out of the header and the DB9 are as follows:

Table 12: Serial Port COMB (HDR9)

#	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	422/485_TX-	422/485_TX-
2	NC	232RX_422/485_TX+
3	232RX_422/485_TX+	232TX_422/485_RX+
4	RTS	422/485_RX-
5	232TX_422/485_RX+	GND
6	CTS	NC
7	422/485_RX-	RTS
8	NC	CTS
9	GND	NC
10	NC	-

2.9.3 RS 232 SERIAL COMC

The SoM-150ES provides one dedicated RS232 serial port accessible via a Male DTE DB9 connector that has a full complement of handshaking signals. Note: the baud rate and the number of handshaking signals are determined by the SoM being used. Refer to the SoM manual for this information.

Table 13: Serial Port COMC (CN1)

Pin	DB9 Description
1	DCD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

2.9.4 RS 232 SERIAL UART COMD & COME (Debug)

Serial UART COMD (SoM pins 48 & 49) and COME (SoM pins 46 & 47) are dedicated RS232 serial ports accessible via two 10-pin header connectors. COMD has RTS/CTS handshaking via the PLD and COME has no handshaking. These are not officially defined by the SoM-144 Pin Specification but taken from the Module Specific section to allow processors with more than three serial ports access to them. EMAC provides Male DB9 DTE serial cables that plug into these headers and provides a standard interface to these ports. COME is also referred to as a Debug port as some processors and Operating Systems may optionally utilize this serial port for that purpose. Note: the baud rate is determined by the SoM being used. Refer to the SoM manual for this information. The pin-out of the header and the DB9 are as follows:

Table 14: Serial Port COMD (HDR10)

#	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD
3	RxD	TxD
4	RTS	NC
5	TxD	GND
6	CTS	NC
7	NC	RTS
8	NC	CTS
9	GND	NC
10	NC	-

Table 15: Serial Port COME/Debug (HDR12)

#	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD
3	RxD	TxD
4	NC	NC
5	TxD	GND
6	NC	NC
7	NC	NC
8	NC	NC
9	GND	NC
10	NC	-

2.10 Controller Area Network (CAN)

The SoM-150ES revision 2+ provides a CAN interface connected to the CAN pins on the SODIMM socket. Some SoM processors provide a CAN interface on these pins while others do not. The SoM must support a CAN interface for the CAN port to work correctly. The CAN lines are also directly connected to HDR4 for use as GPIO lines on modules that do not support CAN. The signal pin-out for the CAN connections on HDR13 is shown in Table 13. CAN signal termination is selectable through JB3.

Table 16: CAN (HDR13)

#	Pin Description for 10-Pin Header
1	NC
2	NC
3	CANL
4	CANH
5	GND
6	NC
7	NC
8	NC
9	GND
10	NC

2.11 Audio

The SoM-150ES optionally provides an I2S Stereo CODEC with standard line level input and output jacks. The CODEC used on the SoM-150ES is the Cirrus Logic CS4271. Jack JK6 is the audio input and JK5 is the audio output. Volume and balance are controlled through software using SPI1 with SPI1_CS0 (using a SoM-9260) when using Rev 1 Carrier boards. For Revision 2+, SPI0 is used with SPI_CS2. Note: I2S audio must be supported by the SoM for the audio port to function.

2.12 LCD

The LCD interface currently supports 2 and 4 line character LCDs and some graphic LCDs. The LCD is connected to the SoM-150ES's on-board CPLD. The CPLD provide 4 data lines requiring the LCD to use 4-bit mode. EMAC provides software for controlling the LCD in its development packages. The LCD interface uses jumper JB6 in order to configure the LCD's backlighting. The backlighting can be controlled via software via a PLD line. See the jumper section of this manual for more information. For low-level information on how to interface with the CPLD default program see: Section 2.5 CPLD Based General Purpose Digital I/O.

Table 17: LCD Interface (HDR3)

Pin	Signal	Pin	Signal
1	VCC	2	GND
3	RS	4	CNTR
5	E	6	R/W*
7	NC	8	NC
9	NC	10	NC
11	D5	12	D4
13	D7	14	D6
15	K (JB6 Pin4)	16	A (JB6 Pin3)

2.13 Keypad

This header provides an interface for a 4x4, 4x5, or 4x6 matrix Keypad. These row and column scan lines are directly connected to the SoM-150ES's on-board CPLD. The CPLD automatically scans the keypad and issues an interrupt to the SoM module when a key has been pressed. When scanning, the keypad columns are connected to output lines and the rows are connected to input lines.

Table 18: KEYPAD (HDR5)

Pin	Signal
1	COL6
2	COL5
3	COL4
4	COL3
5	COL2
6	COL1
7	ROW1
8	ROW2
9	ROW 3
10	ROW 4
11	ESD SHIELD

2.14 Multi-Media (MMC) / Secure Digital (SD) Card Socket

The SoM-150ES provides a standard MMC/SD type socket, which accepts SD, MMC, and SDIO cards. This Socket is connected to the processor's SPI/MCD bus and uses the 4-bit parallel mode provided by both SD and MMC standards. On Revision 1 SoM-150 boards SPI/MCD lines are used to drive the SD card slot which contends with the SPI bus. In order to alleviate this, Revision 2+ boards use a dedicated MCI port on SoM lines 50 through 57. See the SoM 144 Pin Specification for additional information.

Table 19: MMC Socket (SOK2) for Revision 1 Carriers

SDPin	SoM Signal	Som/PLD Pin	SD Signal
1	SPI_CS0	SoM - 123	Data 3
2	SPI_MO	SoM - 121	CMD
3	GND	-	GND
4	3.3V	-	Vcc
5	MS7	SoM- 54	CLK
6	GND	-	GND
7	SPI_MI	SoM - 122	Data 0
8	SPI_CS2	SoM - 110 / PLD - 88	Data 1
9	NC	SoM - 124 / PLD - 87	Data 2
10	GPIO7	SoM - 128	Card Present
11	NC	-	WP Switch
12	GND	-	GND

Table 20: MMC Socket (SOK2) for Revision 2+ Carriers

SDPin	SoM Signal	Som/PLD Pin	SD Signal
1	MS10	SoM - 57	Data 3
2	MS6	SoM - 51	CMD
3	GND	-	GND
4	3.3V	-	Vcc
5	MS7	SoM- 54	CLK
6	GND	-	GND
7	MS5	SoM - 50	Data 0
8	MS8	SoM - 55	Data 1
9	MS9	SoM - 56	Data 2
10	GPIO7	SoM - 128	Card Present
11	NC	-	WP Switch
12	GND	-	GND

3 Software

The SoM-150ES is programmable via a selection of free software tools and open source EMAC software. Software Board Support Packages (BSPs) and Software Development Kits (SDKs) are available for most SoM processor modules. Linux, Real Time Linux, and WinCE 6.0 are examples of supported Operating Systems.

3.1 Eclipse SoM-150ES-SDK

EMAC provides its codebase as a project within the free Eclipse IDE. Eclipse is a powerful open-source Java based IDE. It has plug-ins for Java and C, development and debugging, as well as several other languages.

http://www.eclipse.org/

EMAC offers a free download of Eclipse, complete with JDK and the pre-integrated with appropriate SDK for the chosen Module.

ftp://ftp.emacinc.com/Controllers/SoM

EMAC also offers a pre configured Linux Desktop Computer (LDC) which allows the user to hit the ground running and not have to worry about setting up Linux Machine with the development environment. This is an ideal solution for Windows users who are not familiar with Embedded Linux.

http://www.emacinc.com/operating_systems/linux_ldc.htm

3.2 Quartus II Web Edition

Altera offers powerful free tools for programming the Max II plus PLD of the SoM-100ESR2. These tools include free and flexible modules for implementing UARTs, I2C, counters, RAM, Flash, etc.

https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp

