CS 5220 – 2015-09-10 Preclass Questions

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1. In order to draw a roofline model for the totient nodes, we need to know the peak memory bandwidth and the peak floating-point performance. The peak memory bandwidth is 59 GB/s, and the peak floating-point performance is 120 GFLOPs/s. The roofline diagram generated from these parameters can be found in Figure 1. With the addition of the Phi boards, the max flops would increase, but the memory bandwidth would remain constant.

2. Imagine you have two independent processes executing on two distinct cores. There are some overheads in communication between the two cores whenever the two processes need to communicate. On the other hand, a hyperthreaded core can run both processes on the same core and reduce the overhead of communication.

3. The Phi architecture arranges cores using a ring network. This means that memory access is non-uniform. A processor can access the memory of its neighbor faster than it can connect to the memory of a node on the other side of the ring.

4. Assume we have p processors, each vector is of size n, performing a flop takes time f, and communicating a double takes time c. Serially, the dot product takes $2nf$ time. With p processors, it takes time $\frac{2nf}{p} + pc$ time. This is a speedup of

$$\frac{2nf}{\frac{2nf}{p} + pc}$$

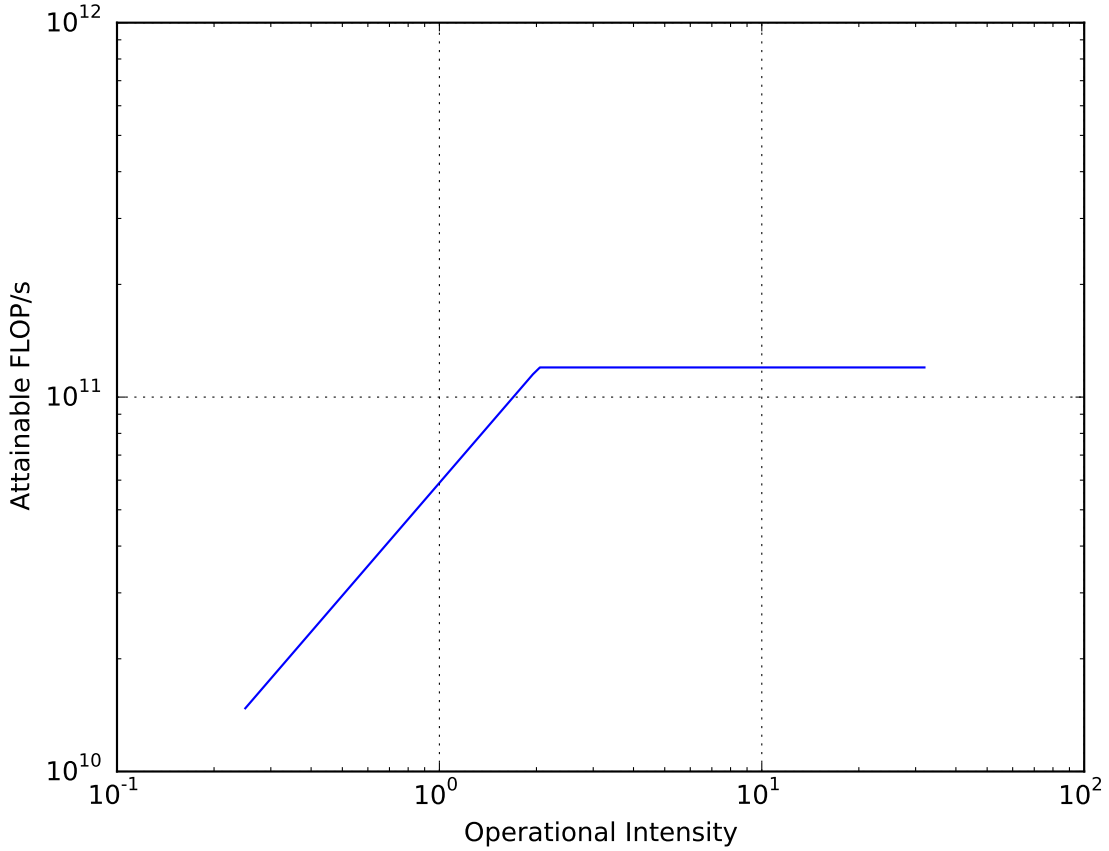

Figure 1: Roofline for Totient Node