Matthew Wojick

860-510-3317 matthew.wojick@gmail.com Portfolio LinkedIn Github

SKILLS

JavaScript • Ruby • React/Redux • Ruby on Rails • RSpec • SQL • HTML/CSS • Ajax • Webpack • GraphQL • Apollo Client • MongoDB • Node.js • Git • Linux • Perl • Matlab • VLSI • Verilog

PROJECTS

TreatPal (React/Redux, Ruby on Rails, Google Maps API) live | github

A clone of the site MealPal, a lunch/dinner service

- Implemented a search bar that searches by location or item by sending Ajax calls to the server on user input.
- Integrated Google Maps API to dynamically search for shops based on the map bounds.
- Implemented reservations using the CRUD cycle in order for user to make reservations for the next day, and modify/cancel them.
- Incorporated the CSS Grid system in the index page to create a smooth and responsive user experience regardless of the display size.

2D-Portal (JavaScript, HTML5 Canvas) live | github

A 2D version of portal, a popular puzzle-platformer game

- Developed player physics in which the player responds to collisions, gravity, friction, and user input.
- Devised a custom teleport function to move player between portals by checking the side of the block the portal is on and correctly transfering vertical and horizontal positions/velocities of the player.
- Created a custom, scalable bitmap editor to easily add on additional levels using sprites.

HackBox (MERN Stack, GraphQL, Websockets, Apollo Client) live | github

A multiplayer party game platform inspired by Jackbox.tv

- Integrated GraphQL on the frontend using Apollo Client to make queries, mutations and subscriptions throughout our components.
- Implemented subscriptions (websockets) on the back and front end to create seamless connections between users.
- Deployed our app to Heroku by building our create-react-app and providing it to our server.

JPEG Image Compressor - VLSI Design II @ UMich

- Designed a JPEG image compressor using configurable approximate computing with multiple voltage rails.
- Developed standard cell layout and characterization, block level auto place and route, and final integration to achieve less than 5% total area overhead from the original design.

16-bit 2-Stage RISC Processor - VLSI Design I @ UMich

- Built a custom 16-bit 2-stage RISC processor using custom designs in Cadence Virtuoso, and synthesized blocks using verilog and Synopsys Design Compiler.
- Implemented a custom 16-bit booth-encoded multiplier with a modified Sklansky tree adder.

EDUCATION

App Academy (San Francisco) - Full stack web development bootcamp with a <3% acceptance rate *2018-2018*

University of Michigan, Ann Arbor - *MS Electrical Engineering (VLSI / Computer Architecture)* *2015-2017*

University of Massachusetts, Amherst - *BS Electrical Engineering* *2011-2015*

EXPERIENCE

Co-op Engineer (Physical Design)

Advanced Micro Devices (AMD) May 2016 - Aug 2016

- Generated Perl test scripts for standard cell libraries in an advanced process.
- Ran synthesis and trial routes of standard cells on an RTL block using Synopsys and Cadence CAD tools.
- Resolved bugs in the library packaging tool (proprietary software) by collaborating with the international CAD team.

Undergraduate Researcher

Nanodevices and Integrated Systems Laboratory (UMass) Dec 2013 - Sept 2014

- Investigated the process of forming an all-silicon memristive device using a one-step thermal oxidation process.