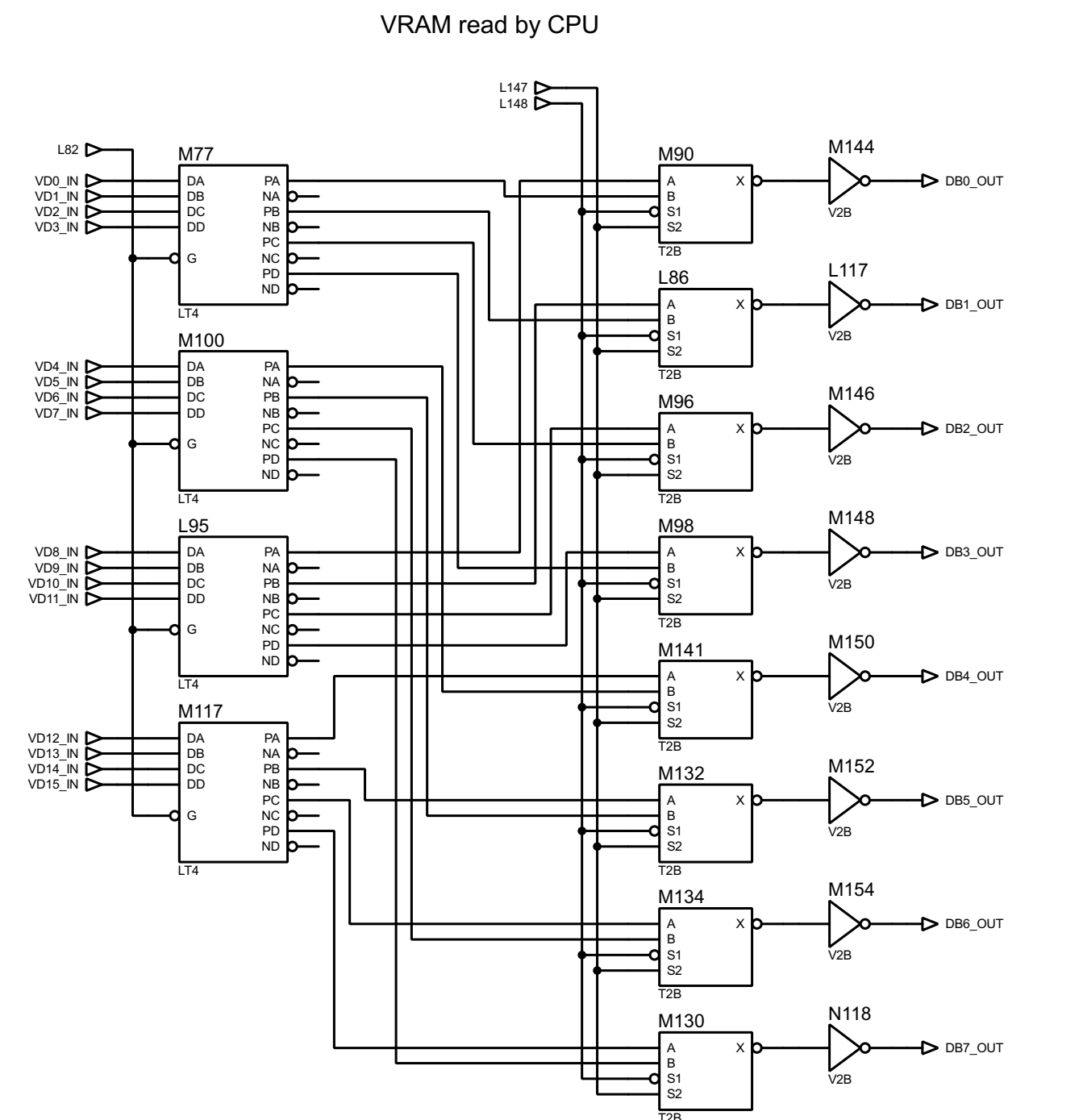
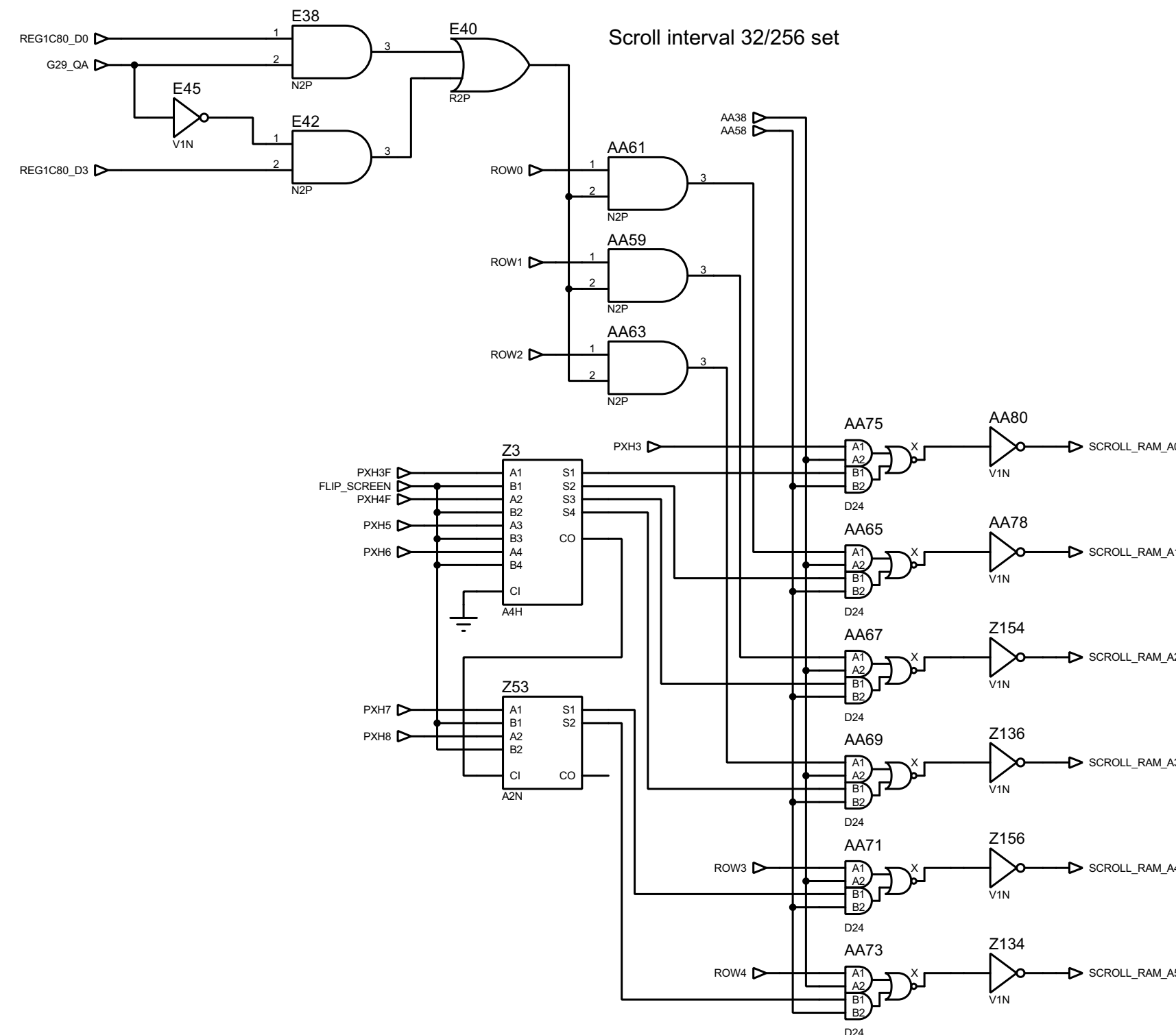
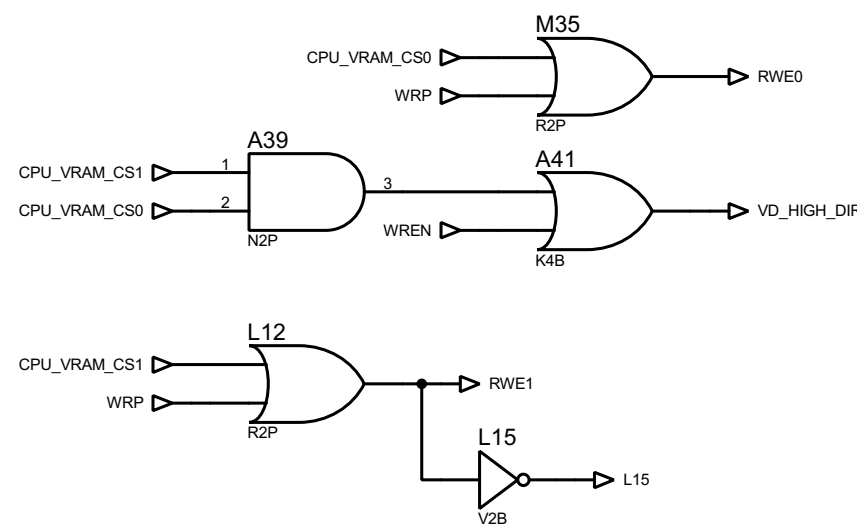


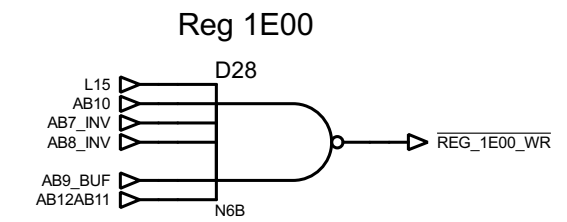
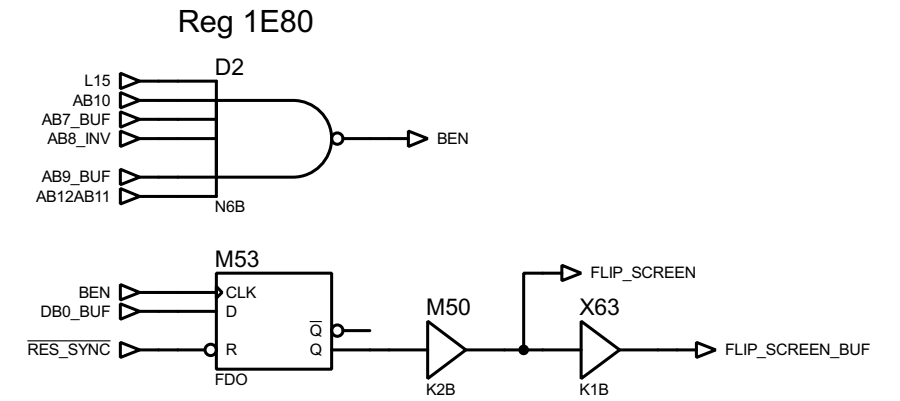
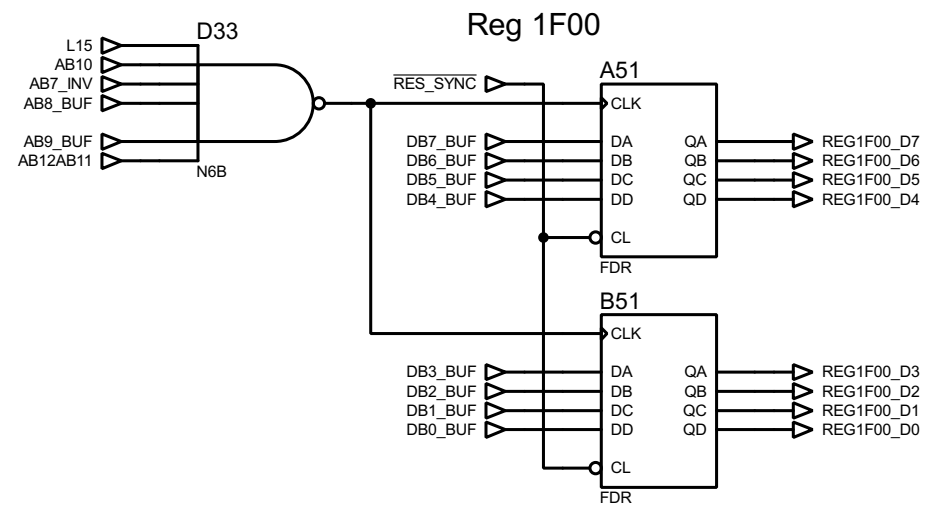
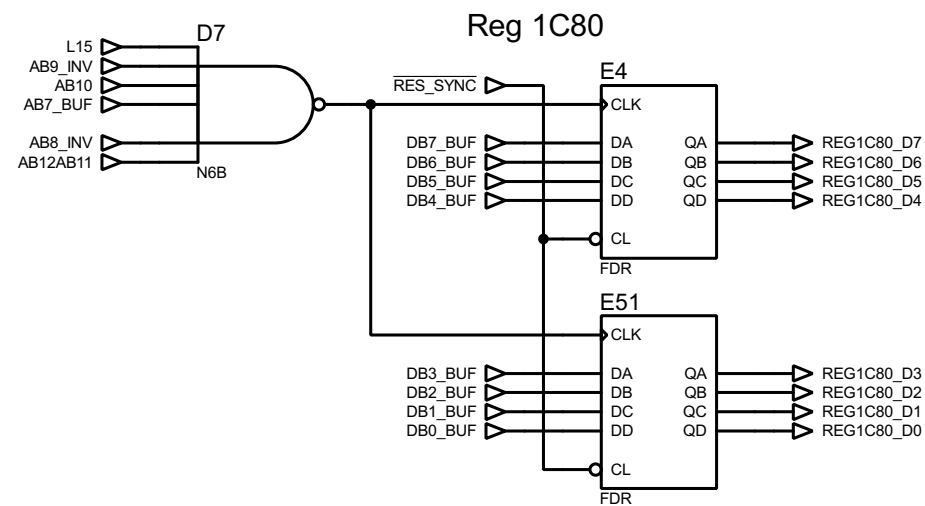
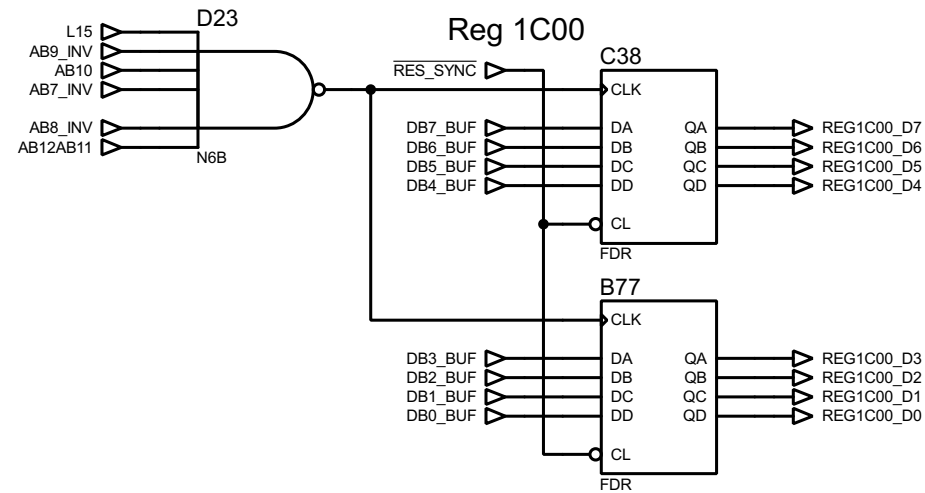
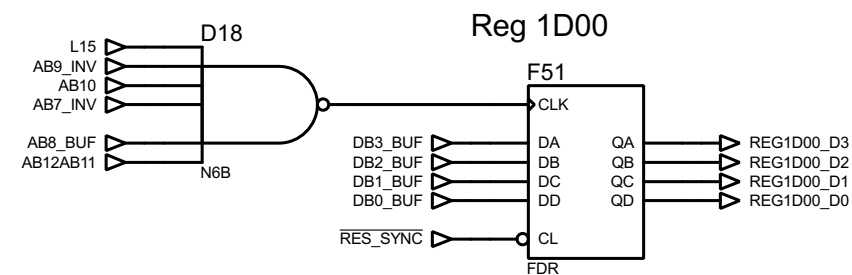
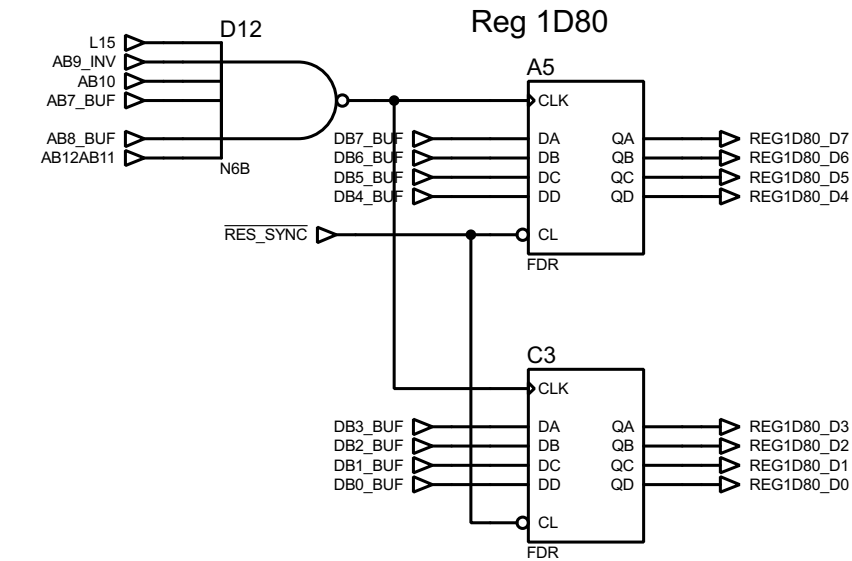
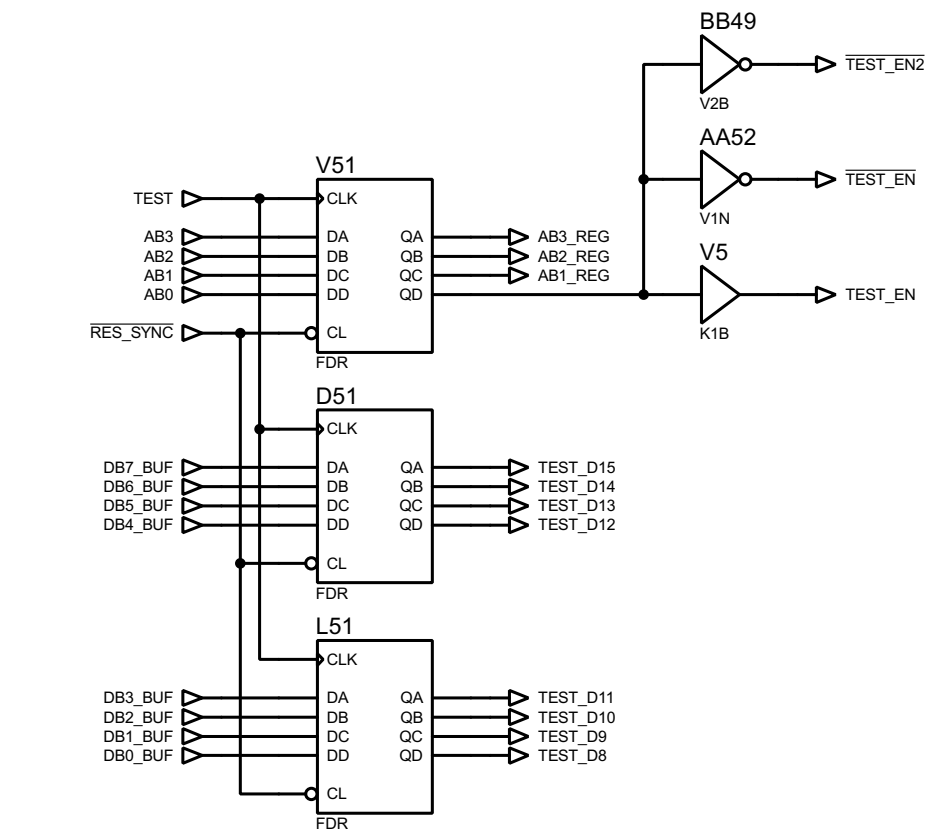
Reg 1C00 bits 0 and 1  
used for VRAM map and  
chip configuration

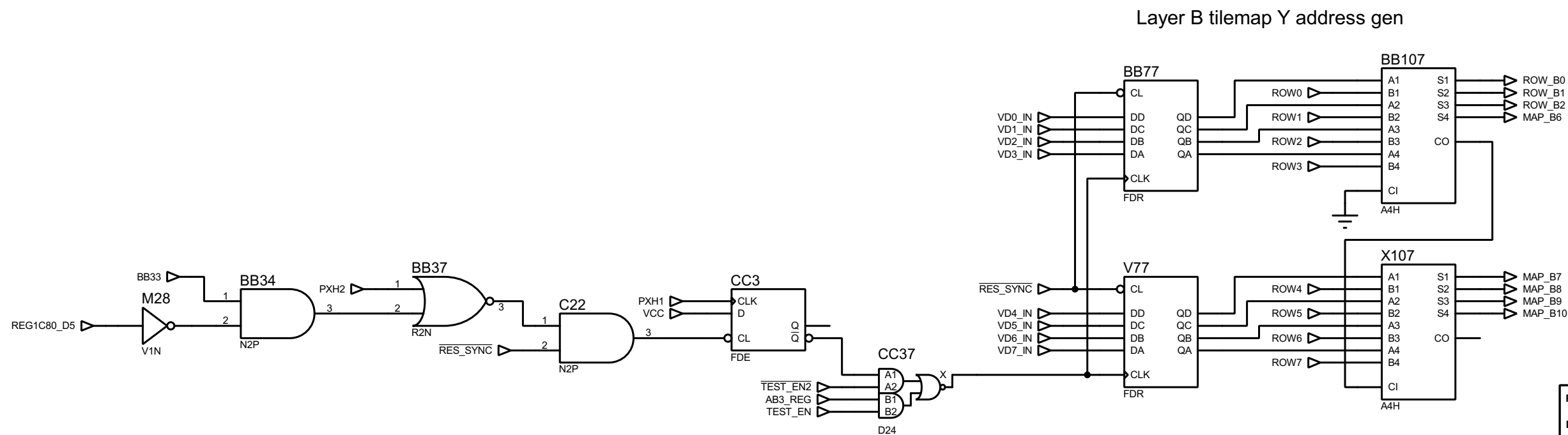
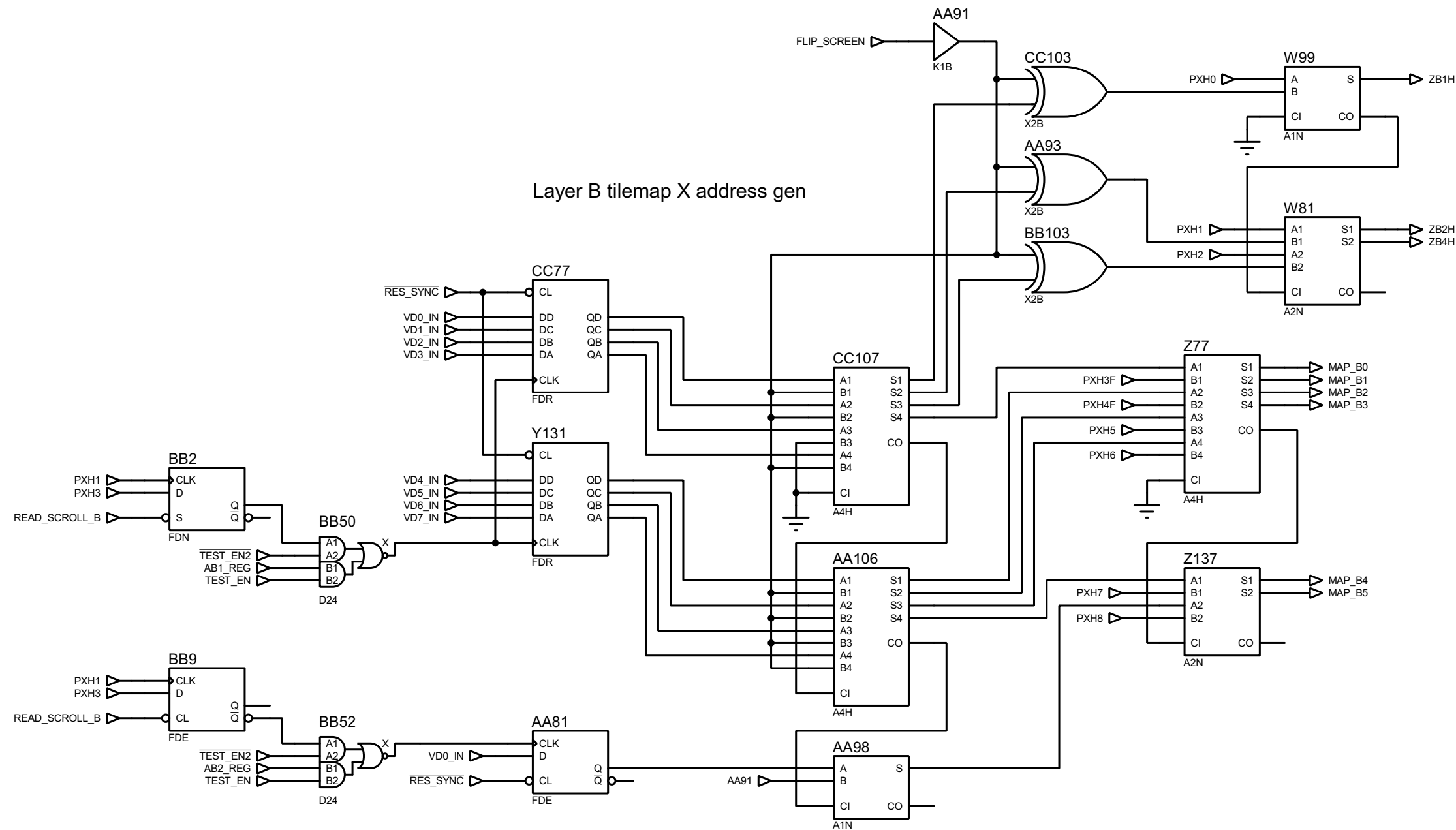
REG1C00\_D[1:0] :

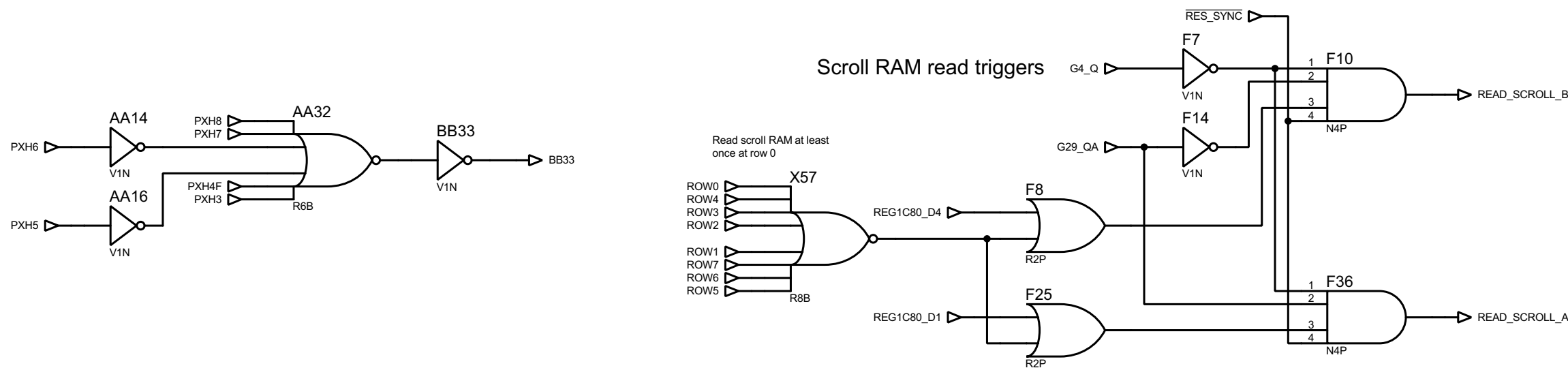
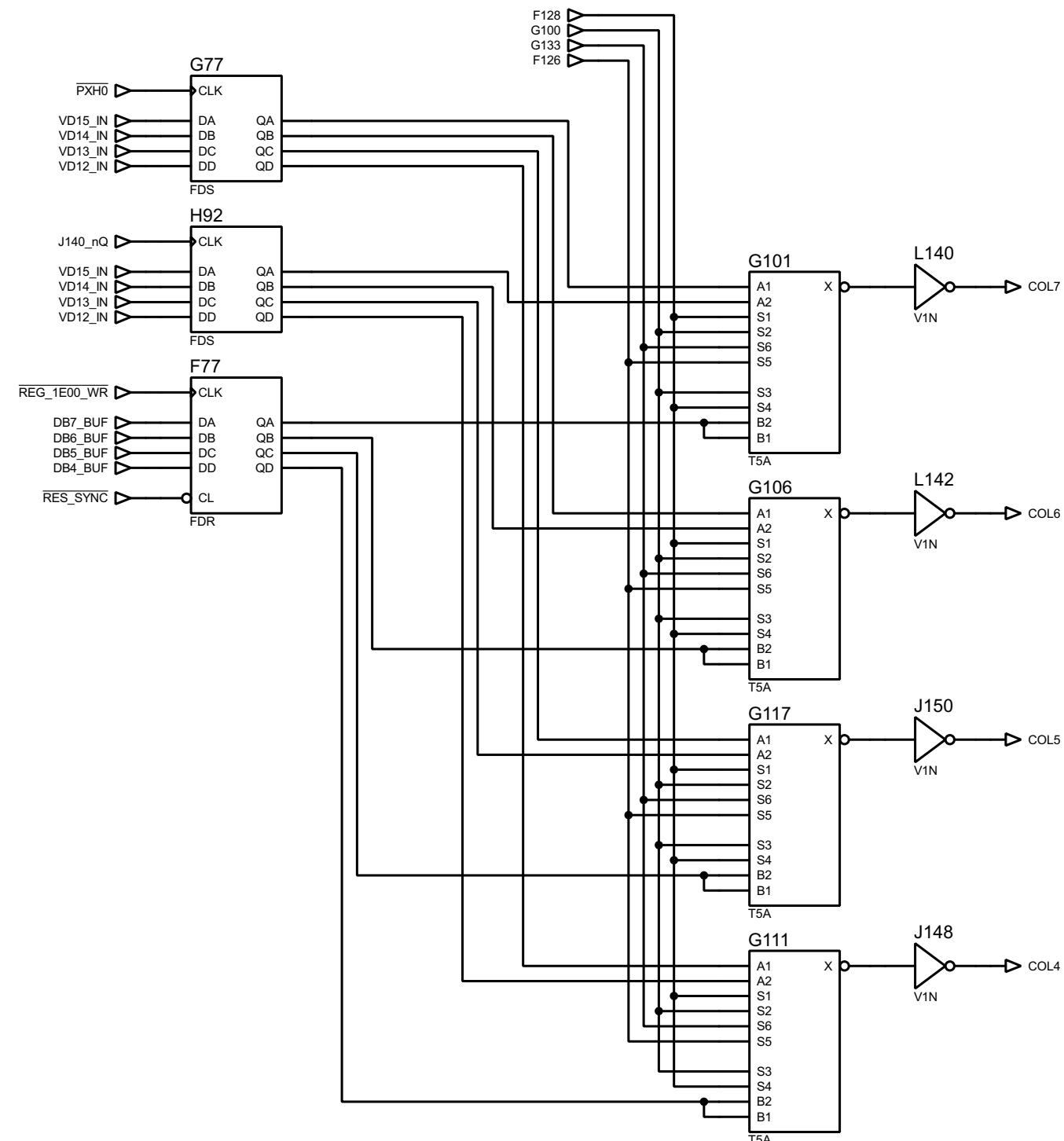
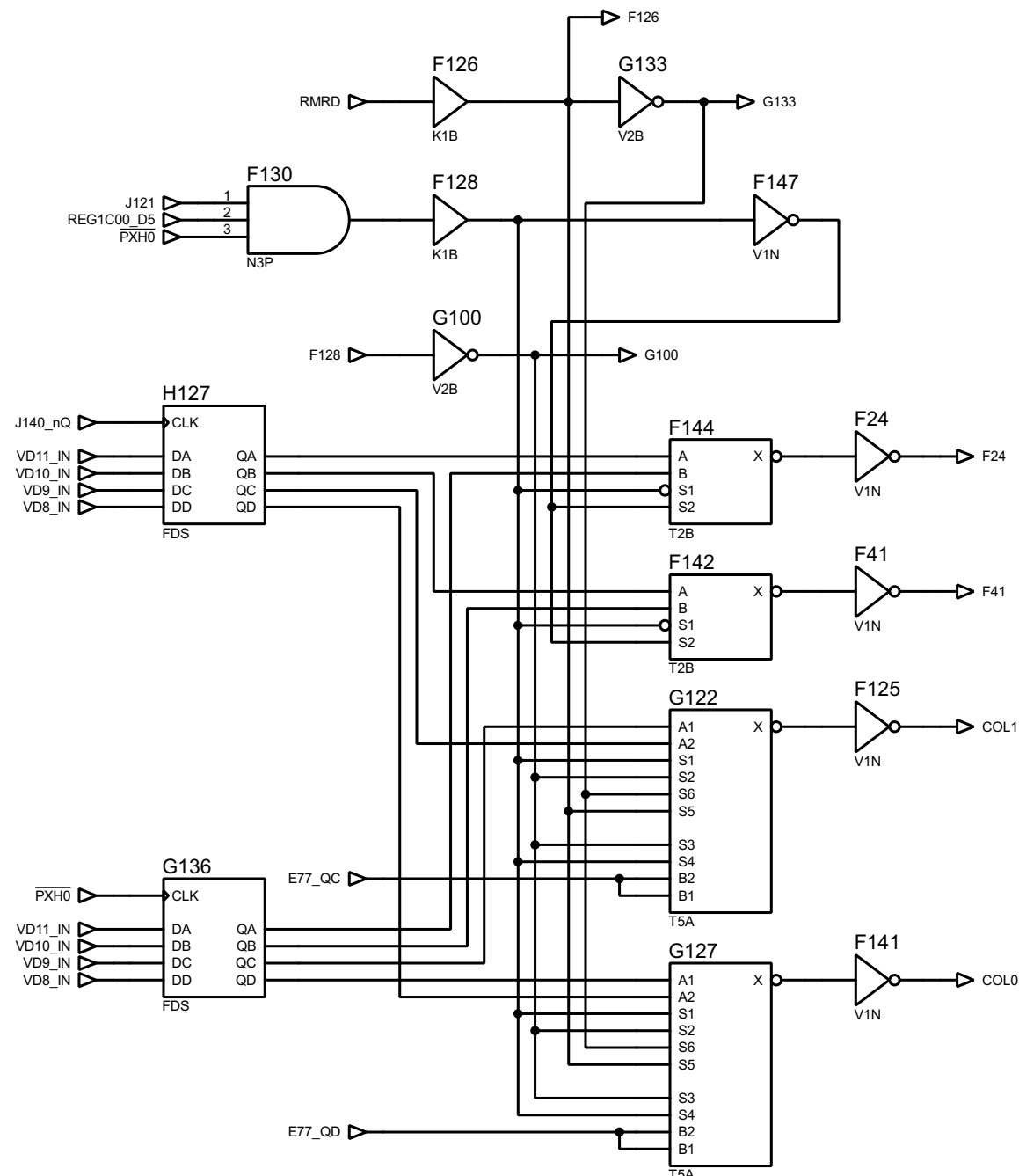
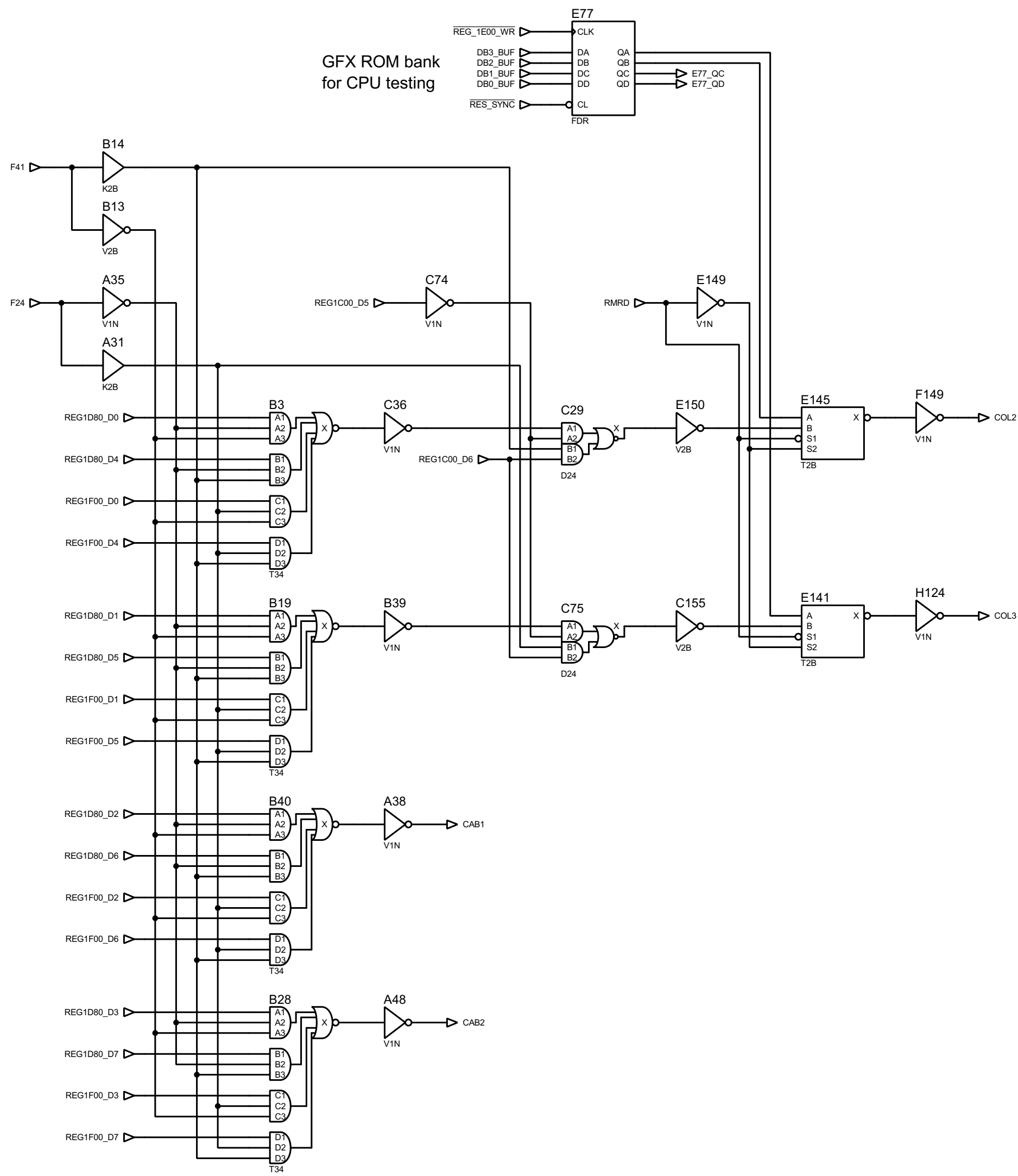
00	0~1	2~3	4~5
01	2~3	4~5	6~7
10	4~5	6~7	8~9
11	6~7	8~9	A~B



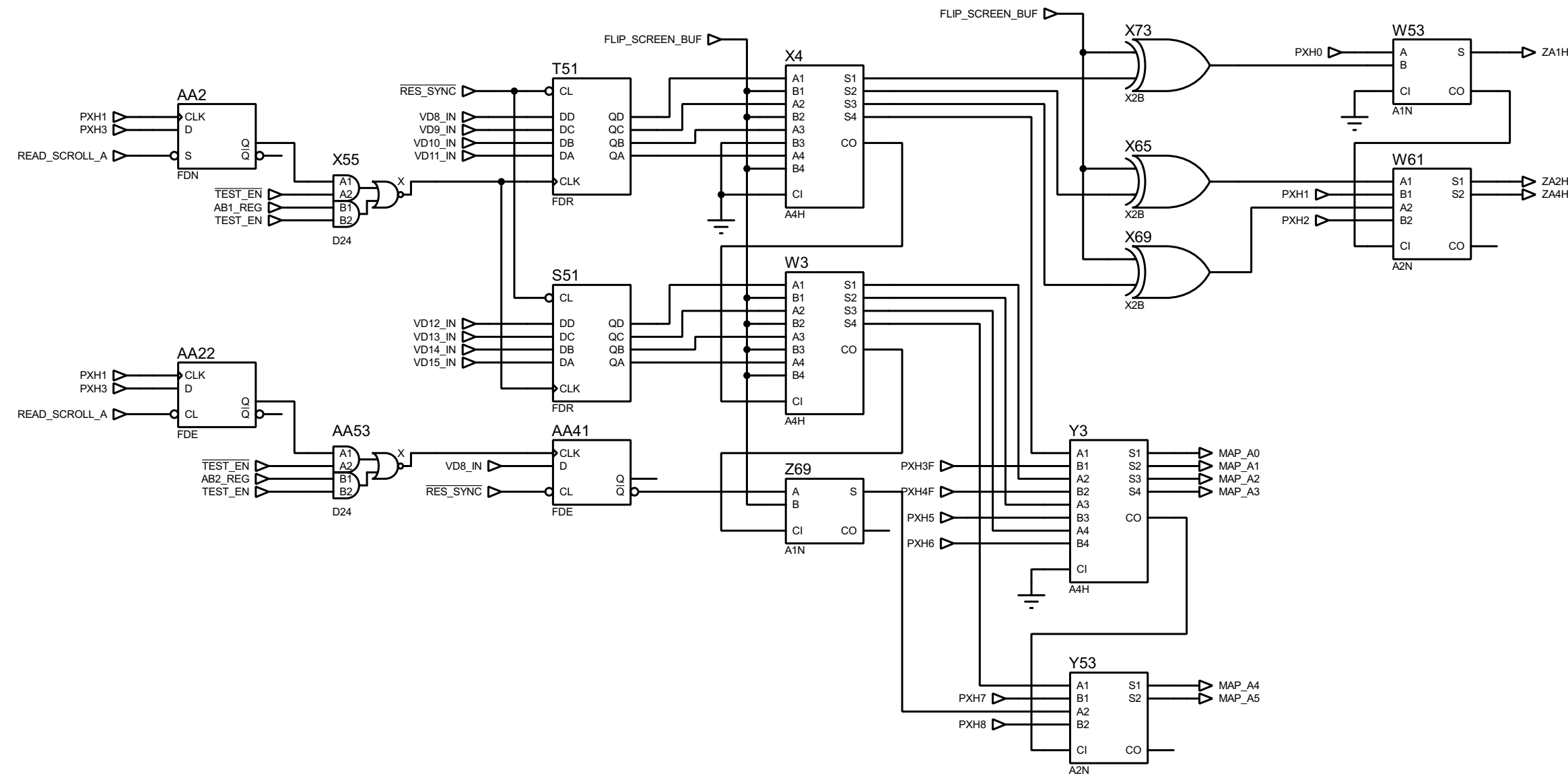








Layer A tilemap X address gen



Layer A tilemap Y address gen

