FOC Transformations v4.2 User Guide

Introduction (Ask a Question)

In a three-phase motor, the sum of three phase voltages or currents at any instant is equal to zero. Hence, it is sufficient to have only two currents or voltages to represent the motor behavior. However, the actual three-phase quantities are displaced by 120° and therefore, they are not completely decoupled. In order to decouple the two-phases that are used to represent the motor dynamics, Clarke transformation is applied to a, b, c phases to transform them to alpha–beta vectors. Clarke transform preserves the magnitude vectors while transforming them from three-phase a, b, c to two-phase alpha–beta. Similarly, inverse clarke transformation is used to convert alpha–beta to a, b, c components because the motor needs actual three-phase voltages to be applied to its stator terminals.

When the motor is rotating, alpha–beta quantities appear as sinusoidal quantities whose frequency depends on the speed of the motor and the number of motor poles. It is easier to control DC quantities than time-varying sinusoidal quantities, because of which, Park transformation is used to transform time-varying alpha–beta vectors to constant d–q vectors. This is called transforming from stator reference frame to rotor reference frame. After the d–q vectors are controlled to get the required motor dynamics, they have to be transformed back to stator reference frame using inverse park transformation.

Summary (Ask a Question)

Core Version	This document applies to Field Oriented Control (FOC) Transformations v4.2.
Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.8 or later releases.
Licensing	Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout is performed with Libero software. FOC Transformations is licensed with encrypted RTL that must be purchased separately. For more information, see FOC Transformations.

Features (Ask a Question)

FOC Transformations has the following key features:

- Computes clarke, inverse clarke, park, and inverse park transformations
- To reduce the resource count, only one math block is shared by all the transformations

Implementation of IP Core in Libero Design Suite (Ask a Question)

IP core must be installed to the IP Catalog of the Libero® SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core can be manually downloaded from the catalog.

Once the IP core is installed in the Libero SoC software IP Catalog, the core can be configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Device Utilization and Performance (Ask a Question)

The following table lists the device utilization used for FOC Transformations.

Table 1. FOC Transformations Utilization

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	628	368	200	0	0	1	0
PolarFire	MPF300T	689	368	200	0	0	1	0
SmartFusion® 2	M2S150	673	370	150	0	0	1	0

Important:

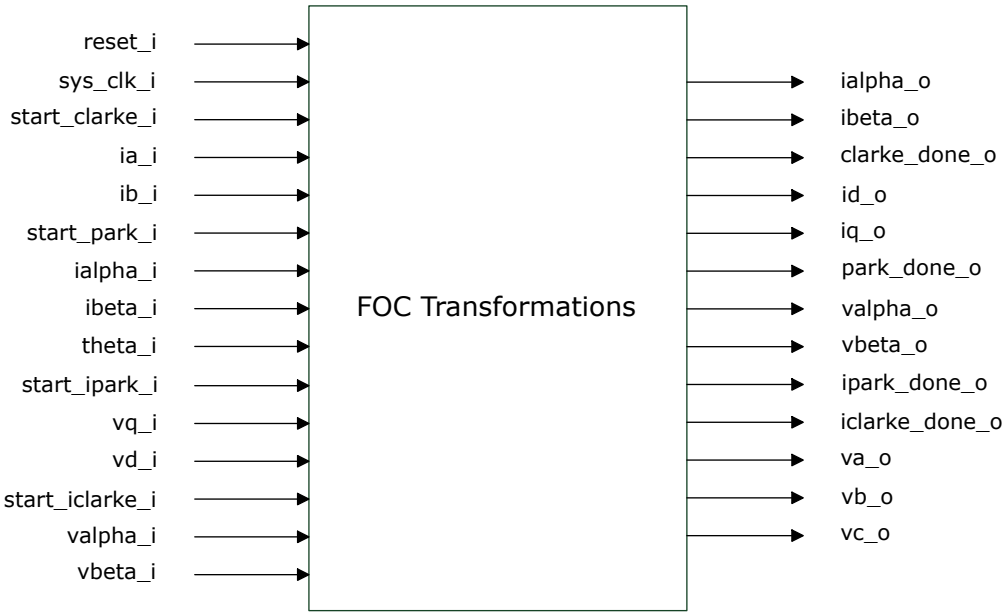
1. The data in this table is captured using typical synthesis and layout settings. CDR reference clock source was set to **Dedicated** with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Table of Contents

1. Functional Description (Ask a Question)

This section describes the implementation details of the FOC Transformations block implemented in the SmartFusion® 2 System-on-Chip (SoC) Field Programmable Gate Array (FPGA) device.

Figure 1-1. FOC Transformations Block Diagram



The FOC Transformations block consists of four transformation blocks (clarke, inverse clarke, park, and inverse park), which share a common math block, which perform addition, subtraction, and multiplication. The entire system is synchronized with a system clock, which is available at sys_clk_i.

Each computation is triggered by a rising edge at the start input signal (start_clarke_i, start_park_i, start_ipark_i, and start_iclarke_i) and a rising edge on the corresponding done signal (clarke_done_o, park_done_o, iclarke_done_o, and ipark_done_o) that indicates the completion of the computation.

The clarke computation is triggered by a rising edge at the start_clarke_i input, and the inputs ia_i and ib_i are sampled at this time. At the end of the computation, the outputs ialpha_o and ibeta_o are valid when the clarke_done_o signal goes high.

The park computation is triggered by a rising edge at the start_park_i input, and the inputs i_alpha_i and i_beta_i are sampled at this time. At the end of the computation, the outputs id_o and iq_o are valid when the park_done_o signal goes high.

The inverse park computation is triggered by a rising edge at the start_ipark_i input, and the inputs vq_iand vd_i are sampled at this time. At the end of the computation, the outputs valpha_o and vbeta_o are valid when the ipark_done_o signal goes high.

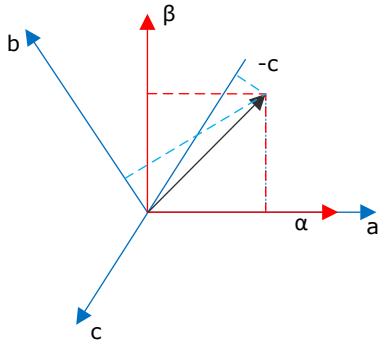
The inverse clarke computation is triggered by a rising edge at the start_iclarke_i input, and the inputs valpha_i and vbeta_i are sampled at this time. At the end of the computation, the outputs va_o, vb_o and vc_o are valid when the iclarke_done_o signal goes high.

Note:
The math block is shared by each computation block, and so, only one computation should be triggered at a time.

1.1 Clarke Transformation (Ask a Question)

The three-phase quantities are translated from the three-phase reference frame to the two-axis orthogonal stationary reference frame using Clarke transformation, as shown in the following figure.

Figure 1-2. Clarke and Inverse Clarke Computation



The general equation for Clarke transformation is:

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

$$\alpha = \frac{2}{3}a - \frac{1}{3}b - \frac{1}{3}c$$

Where,

a, b, and c are three-phase quantities and α and ß are two-phase orthogonal quantities.

Using a + b + c = 0, simplify the equations.

$$\alpha = a$$

$$\beta = \frac{a + 2b}{\sqrt{3}}$$

1.2 Inverse Clarke Transformation (Ask a Question)

The transformation from a two-axis orthogonal stationary reference frame to a three-phase stationary reference frame is accomplished using inverse clarke transformation, as shown in Figure 1-2. The inverse clarke transformation is expressed by the following equations:

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix}$$

$$a = \alpha$$

$$b = -\frac{1}{2}\alpha + \frac{\sqrt{3}}{2}\beta$$

$$c = -\frac{1}{2}\alpha - \frac{\sqrt{3}}{2}\beta$$

1.3 Park Transformation (Ask a Question)

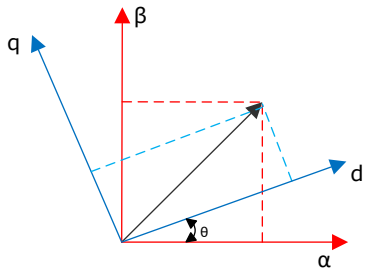
Park transformation, transforms quantities from stationary reference frame to rotating reference frame. As the rotor rotates, the rotor flux rotates in space and it is the position of the flux vector that is taken as reference for transformation. The park transformation is expressed by the following equations.

$$d = \alpha \times \cos\theta + \beta \times \sin\theta$$

$$q = -\alpha \times \sin\theta + \beta \times \cos\theta$$

Where, ɵ is rotor flux angular position, as shown in the following figure.

Figure 1-3. Park and Inverse Park Computation



1.4 Inverse Park Transformation (Ask a Question)

Inverse park transformation, transforms vectors from rotating reference frame to stationary reference frame. The same angle that is used for Park transformation is generally used for inverse park transformation. The inverse park transformation is expressed by the following equations.

$$\alpha = d \times \cos\theta - q \times \sin\theta$$

$$\beta = d \times \sin\theta + q \times \cos\theta$$

2. FOC Transformations Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the FOC Transformations GUI configurator and I/O signals.

2.1 Configuration Settings (Ask a Question)

The following table lists the description of the configuration parameters used in the hardware implementation of FOC Transformations. These are generic parameters that are customizable as per the requirement of the application.

Table 2-1. Configuration Parameters

Signal Name	Description
g_NO_MCYCLE_PATH	The number of clock delays required before the multiplication product ready signal is asserted.

2.2 Input and Output Signals (Ask a Question)

The following table lists the input and output ports of FOC Transformations.

Table 2-2. Inputs and Outputs of FOC Transformations

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal
sys_clk_i	Input	System clock
start_clarke_i	Input	Start signal for Clarke computation should be high for one system clock cycle
ia_i	Input	Phase A current input for Clarke computation
ib_i	Input	Phase B current input for Clarke computation
start_park_i	Input	Start signal for Park computation should be high for one system clock cycle
alpha_i	Input	Alpha-axis current input for Park computation
beta_i	Input	Beta-axis current input for Park computation
theta_i	Input	Angle value for park and inverse park computation
start_ipark_i	Input	Start signal for inverse park computation should be high for one system clock cycle
vq_i	Input	Q-axis voltage input for inverse park computation
vd_i	Input	D-axis voltage input for inverse park computation
start_iclarke_i	Input	Start signal for inverse clarke computation must be high for one system clock cycle
valpha_i	Input	Alpha-axis voltage input for inverse clarke computation
vbeta_i	Input	Beta-axis voltage input for inverse clarke computation
ialpha_o	Output	Alpha-axis current output from clarke computation
ibeta_o	Output	Beta-axis current output from clarke computation
clarke_done_o	Output	Indicates clarke computation is complete and the computation outputs are available. High for one system clock cycle.
id_o	Output	D-axis current output from Park computation
iq_o	Output	Q-axis current output from Park computation

.....continued

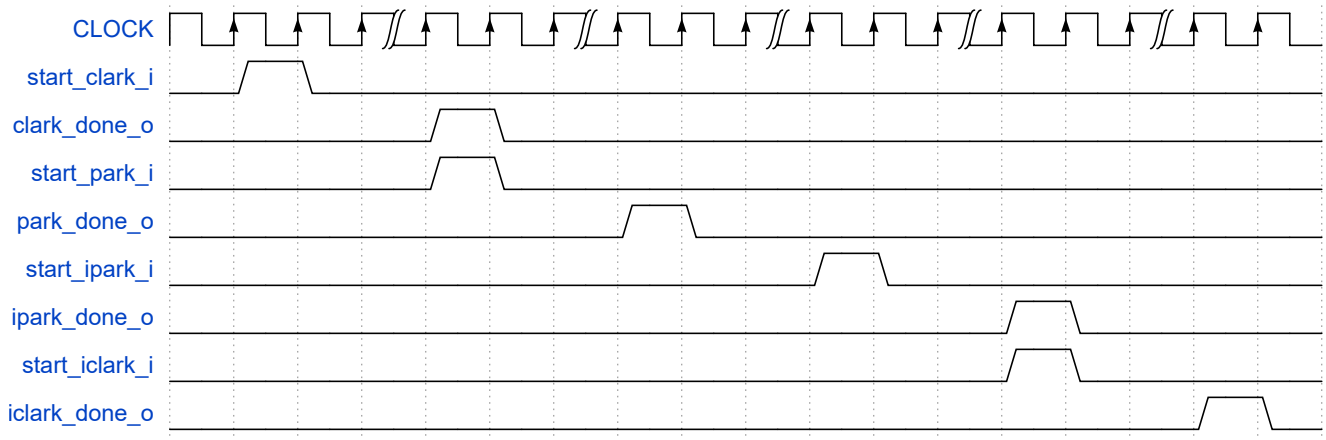
Signal Name	Direction	Description
park_done_o	Output	Indicates Park computation is complete and the computation outputs are available. High for one system clock cycle.
va_o	Output	A-phase voltage output from inverse clarke computation
vb_o	Output	B-phase voltage output from inverse clarke computation
vc_o	Output	C-phase voltage output from inverse clarke computation
iclarke_done_o	Output	Indicates inverse clarke computation is complete and the computation outputs are available. High for one system clock cycle.
valpha_o	Output	Alpha-axis voltage output from inverse park computation
vbeta_o	Output	Beta-axis voltage output from inverse park computation
ipark_done_o	Output	Indicates inverse park computation is complete and the computation outputs are available. High for one system clock cycle.

3. Timing Diagrams (Ask a Question)

This section discusses FOC Transformations timing diagram.

The following figure shows the timing diagram of FOC Transformations.

Figure 3-1. FOC Transformations Timing Diagram



4. Testbench (Ask a Question)

A unified testbench is used to verify and test FOC Transformations called as user testbench. Testbench is provided to check the functionality of the FOC Transformations IP.

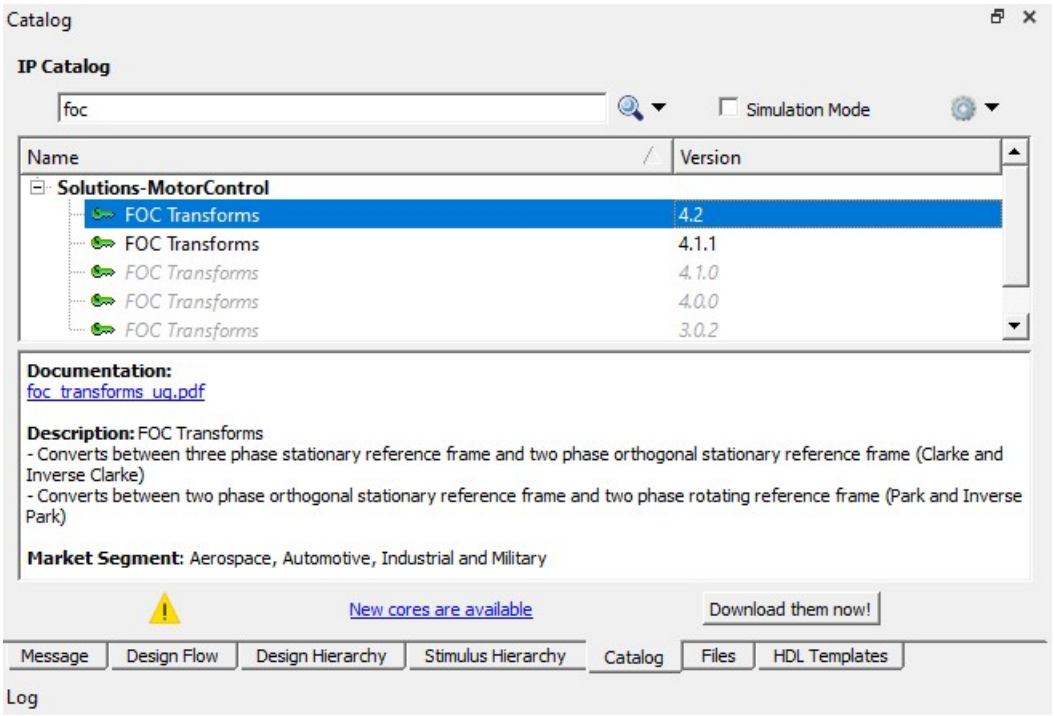
4.1 Simulation (Ask a Question)

The following steps describe how to simulate the core using the testbench:

1. Open the Libero SoC application, click **Catalog** tab, expand **Solutions-MotorControl**, double-click **FOC Transforms**, and then click **OK**. The documentation associated with the IP are listed under **Documentation**.

Important: If you do not see the **Catalog** tab, navigate to **View** > **Windows** menu and click **Catalog** to make it visible.

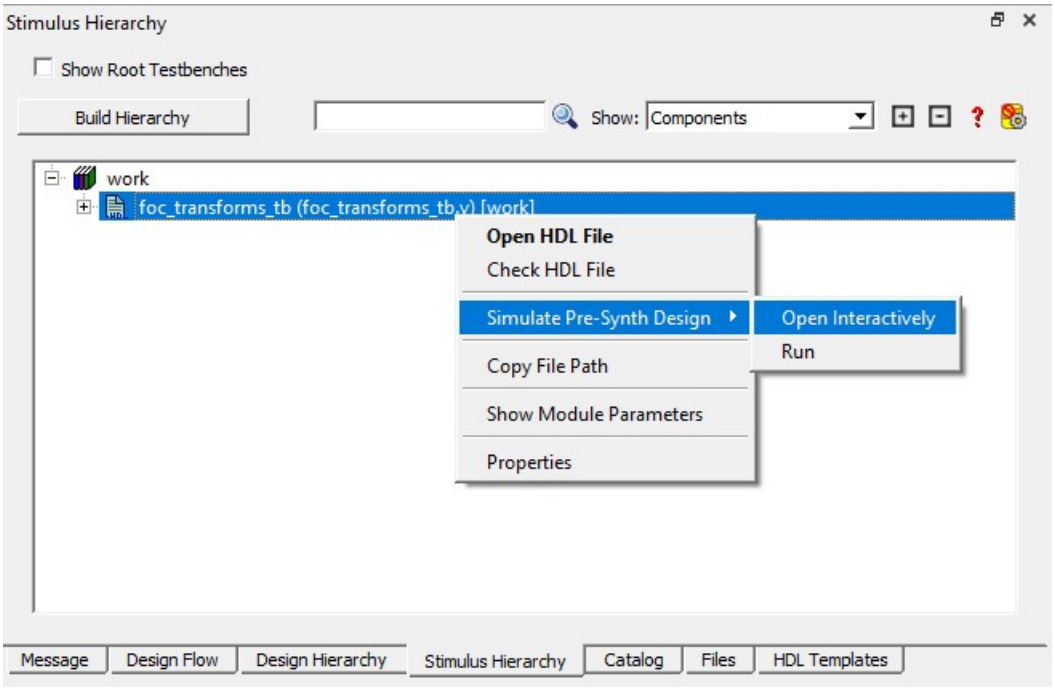
Figure 4-1. FOC Transformations IP Core in Libero SoC Catalog



2. On the **Stimulus Hierarchy** tab, click the testbench (`foc_transforms_tb.v`), right click and then click **Simulate Pre-Synth Design** > **Open Interactively**.

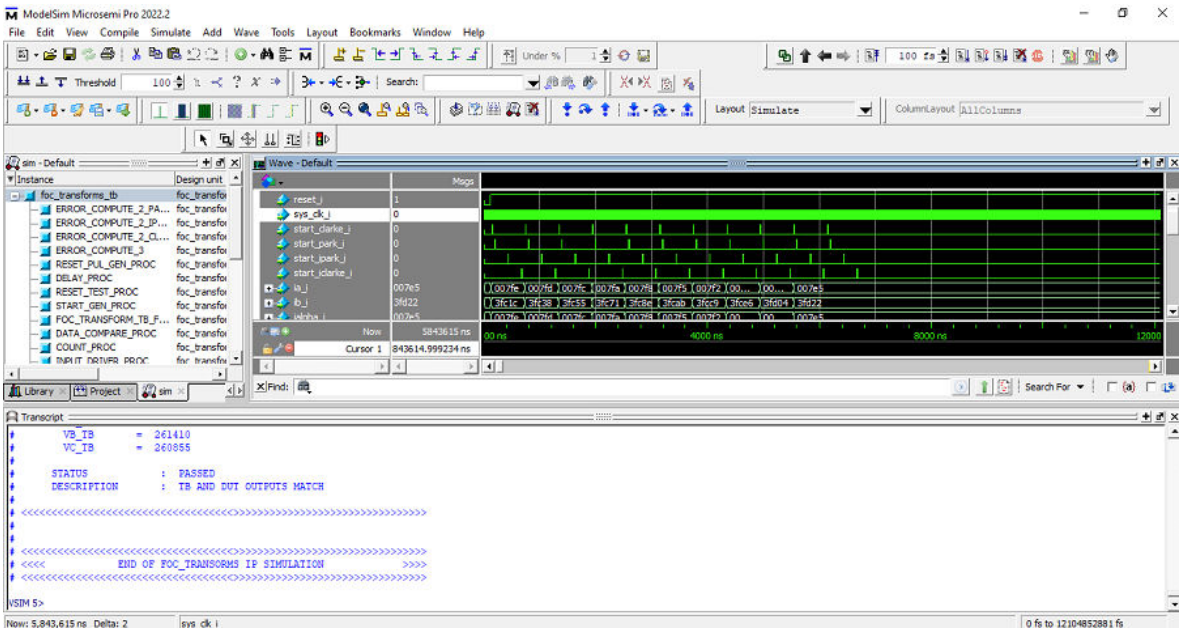
Important: If you do not see the **Stimulus Hierarchy** tab, navigate to **View** > **Windows** menu and click **Stimulus Hierarchy** to make it visible.

Figure 4-2. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file as shown in the following figure.

Figure 4-3. ModelSim Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the `.do` file, use the `run -all` command to complete the simulation.

5. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	03/2023	The following list of changes are made in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS00004921A from 50200607. • Added 3. Timing Diagrams. • Added 4. Testbench.
3.0	—	The following is a summary of changes made in this revision: • Added the IP version to the document title. • Removed g_STD_IO_WIDTH configuration parameter from Configuration Parameter section.
2.0	—	Updated Configuration Parameters section.
1.0	—	Revision 1.0 was the first publication of this document.

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