



1. Description

1.1. Project

Project Name	F407VET6_SmartDel_20201101
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	03/05/2021

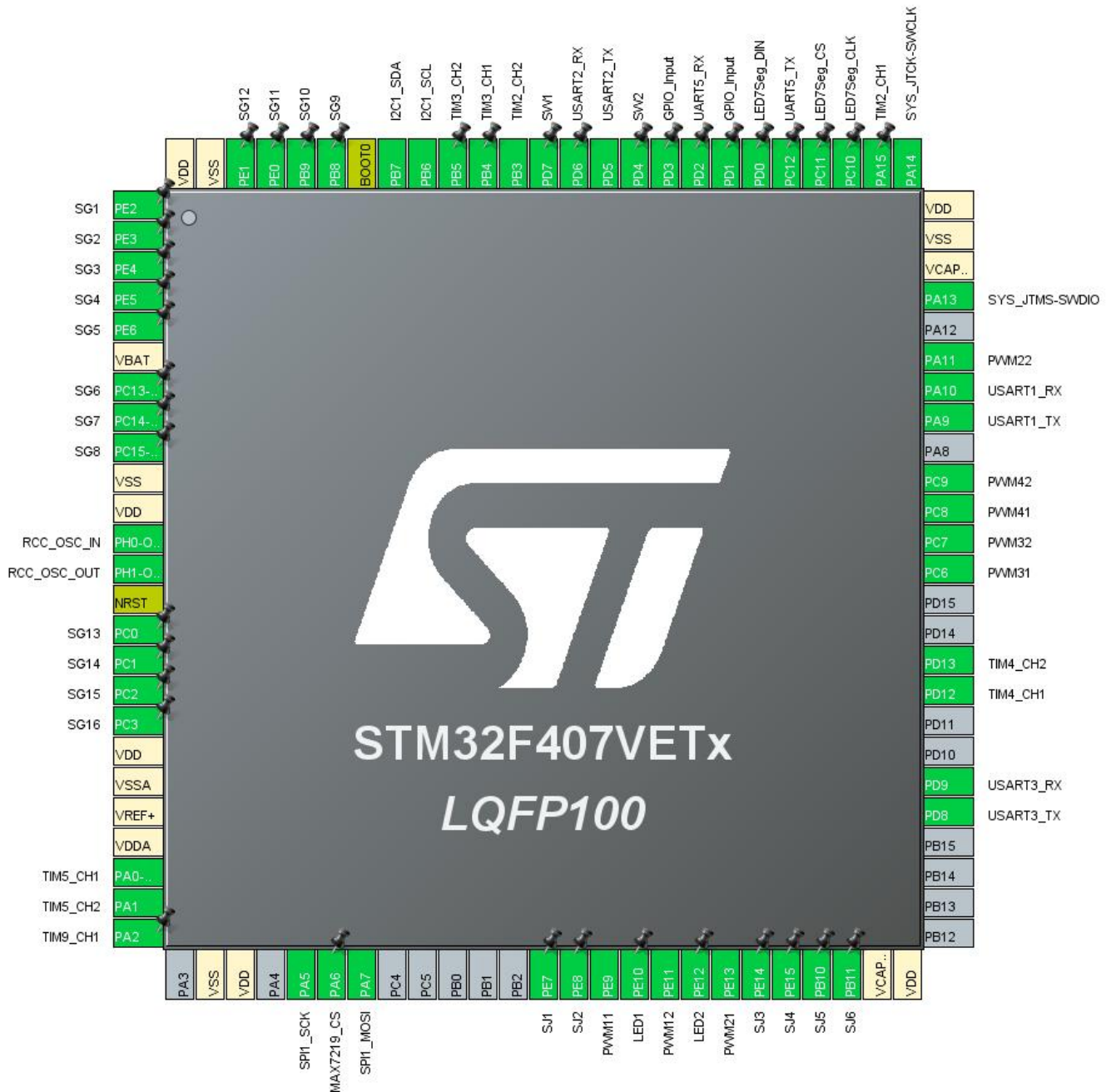
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4
---------	---------------

2. Pinout Configuration



3. Pins Configuration

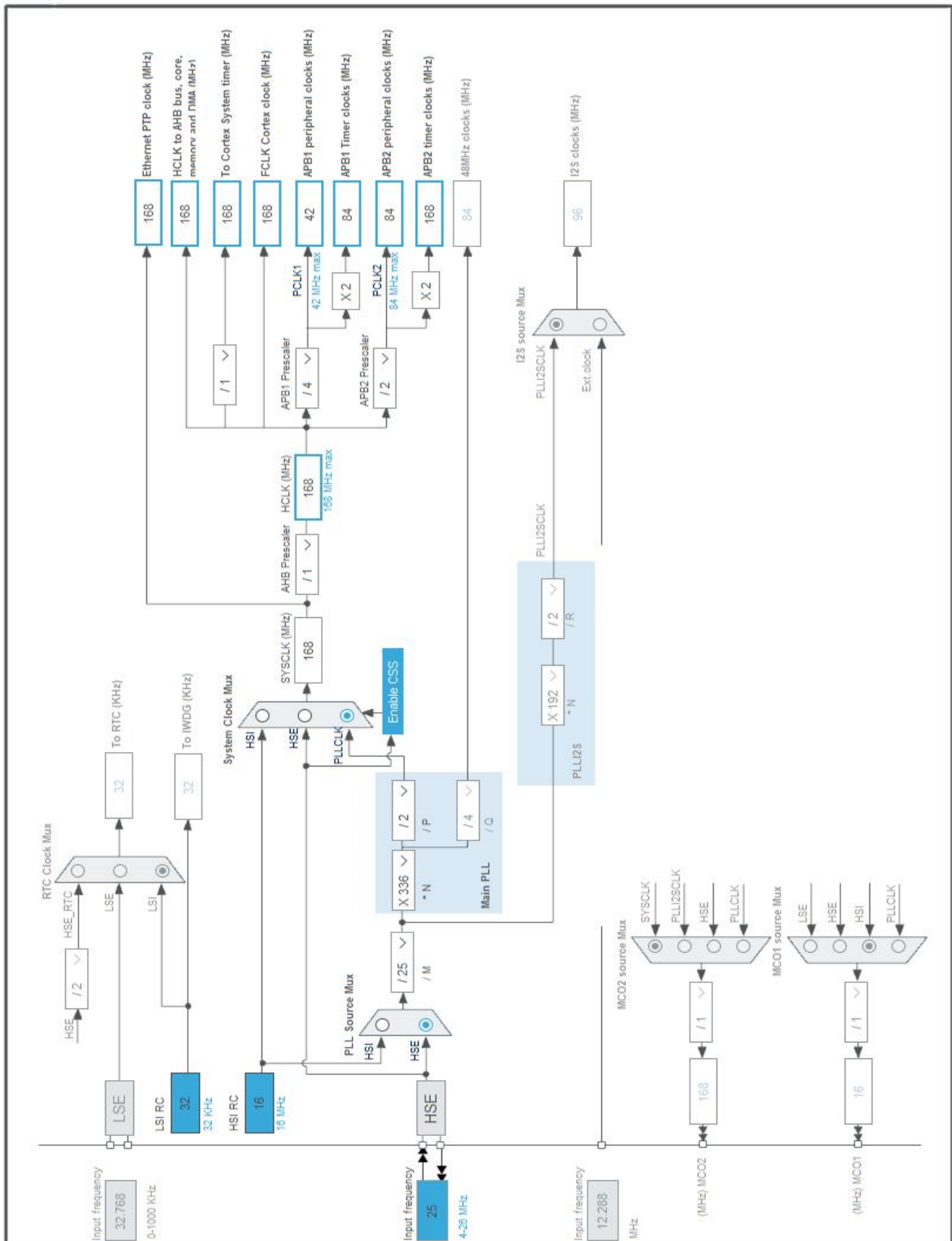
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	SG1
2	PE3 *	I/O	GPIO_Input	SG2
3	PE4 *	I/O	GPIO_Input	SG3
4	PE5 *	I/O	GPIO_Input	SG4
5	PE6 *	I/O	GPIO_Input	SG5
6	VBAT	Power		
7	PC13-ANTI_TAMP *	I/O	GPIO_Input	SG6
8	PC14-OSC32_IN *	I/O	GPIO_Input	SG7
9	PC15-OSC32_OUT *	I/O	GPIO_Input	SG8
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Input	SG13
16	PC1 *	I/O	GPIO_Input	SG14
17	PC2 *	I/O	GPIO_Input	SG15
18	PC3 *	I/O	GPIO_Input	SG16
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	
24	PA1	I/O	TIM5_CH2	
25	PA2	I/O	TIM9_CH1	
27	VSS	Power		
28	VDD	Power		
30	PA5	I/O	SPI1_SCK	
31	PA6 *	I/O	GPIO_Output	MAX7219_CS
32	PA7	I/O	SPI1_MOSI	
38	PE7 *	I/O	GPIO_Input	SJ1
39	PE8 *	I/O	GPIO_Input	SJ2
40	PE9	I/O	TIM1_CH1	PWM11
41	PE10 *	I/O	GPIO_Output	LED1
42	PE11	I/O	TIM1_CH2	PWM12
43	PE12 *	I/O	GPIO_Output	LED2

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	PE13	I/O	TIM1_CH3	PWM21
45	PE14 *	I/O	GPIO_Input	SJ3
46	PE15 *	I/O	GPIO_Input	SJ4
47	PB10 *	I/O	GPIO_Input	SJ5
48	PB11 *	I/O	GPIO_Input	SJ6
49	VCAP_1	Power		
50	VDD	Power		
55	PD8	I/O	USART3_TX	
56	PD9	I/O	USART3_RX	
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
63	PC6	I/O	TIM8_CH1	PWM31
64	PC7	I/O	TIM8_CH2	PWM32
65	PC8	I/O	TIM8_CH3	PWM41
66	PC9	I/O	TIM8_CH4	PWM42
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	TIM1_CH4	PWM22
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	TIM2_CH1	
78	PC10 *	I/O	GPIO_Output	LED7Seg_CLK
79	PC11 *	I/O	GPIO_Output	LED7Seg_CS
80	PC12	I/O	UART5_TX	
81	PD0 *	I/O	GPIO_Output	LED7Seg_DIN
82	PD1 *	I/O	GPIO_Input	
83	PD2	I/O	UART5_RX	
84	PD3 *	I/O	GPIO_Input	
85	PD4 *	I/O	GPIO_Input	SW2
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
88	PD7 *	I/O	GPIO_Input	SW1
89	PB3	I/O	TIM2_CH2	
90	PB4	I/O	TIM3_CH1	
91	PB5	I/O	TIM3_CH2	
92	PB6	I/O	I2C1_SCL	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
95	PB8 *	I/O	GPIO_Input	SG9
96	PB9 *	I/O	GPIO_Input	SG10
97	PE0 *	I/O	GPIO_Input	SG11
98	PE1 *	I/O	GPIO_Input	SG12
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	F407VET6_SmartDel_20201101
Project Folder	D:\shared documents\code projects\learn\Gxcode
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM1_Init	TIM1
4	MX_TIM2_Init	TIM2
5	MX_TIM5_Init	TIM5
6	MX_TIM6_Init	TIM6
7	MX_TIM8_Init	TIM8
8	MX_TIM9_Init	TIM9
9	MX_TIM3_Init	TIM3
10	MX_TIM4_Init	TIM4
11	MX_USART1_UART_Init	USART1

Rank	Function Name	Peripheral Instance Name
12	MX_I2C1_Init	I2C1
13	MX_USART2_UART_Init	USART2
14	MX_USART3_UART_Init	USART3
15	MX_SPI1_Init	SPI1
16	MX_UART5_Init	UART5

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

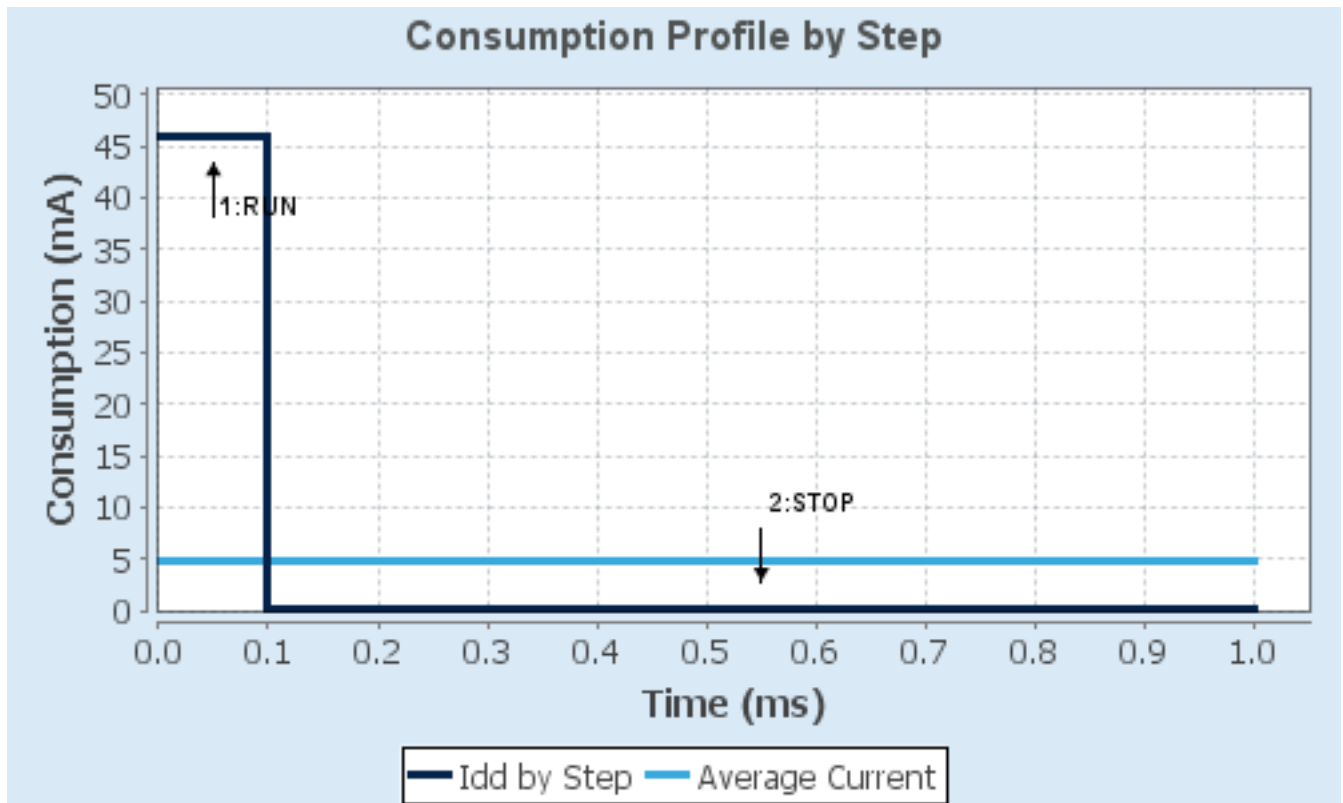
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μ A
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
-------------------------------	---------------------------------

7.3. SPI1

Mode: Half-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	42.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	16800-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Enable *
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Enable *
Off State Selection for Run Mode (OSSR)	Enable *
Off State Selection for Idle Mode (OSSl)	Enable *
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.6. TIM2

Combined Channels: Encoder Mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	65535 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode T11
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.7. TIM3

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode T11
--------------	------------------

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

____ Parameters for Channel 2 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.8. TIM4

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode T11
--------------	------------------

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

____ Parameters for Channel 2 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.9. TIM5

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	65535 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode T11
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.10. TIM6

mode: Activated

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	84-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
-------------------------	------------------------------

7.11. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	16800-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Enable *
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Enable *
Off State Selection for Run Mode (OSSR)	Enable *
Off State Selection for Idle Mode (OSSI)	Enable *
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.12. TIM9

mode: Clock Source

Channel1: PWM Generation CH1

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	(168-1) *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	(10000-1) *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	1500 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. UART5

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.14. USART1

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.15. USART2

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	1000000 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.16. USART3

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM11
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM12
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM21
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM22
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM31
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM32
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM41
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM42
TIM9	PA2	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	Very High *	
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	Very High	

F407VET6_SmartDel_20201101 Project
Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG1
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG2
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG3
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG4
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG5
	PC13- ANTI_TAMP	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG6
	PC14- OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG7
	PC15- OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG8
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG13
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG14
	PC2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG15
	PC3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG16
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAX7219_CS
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SJ1
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SJ2
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SJ3
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SJ4
	PB10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SJ5
	PB11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SJ6
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7Seg_CLK
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7Seg_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7Seg_DIN
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW2
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW1
	PB8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG9
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG10
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG11
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SG12

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	4	0
USART3 global interrupt	true	3	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
UART5 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART1 global interrupt	false	true	true
USART2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA		TIM1 ✓	I2C1 ✓			
GPIO ✓		TIM2 ✓	SP1 ✓			
NVIC ✓		TIM3 ✓	UART5 ✓			
RCC ✓		TIM4 ✓	USART1 ✓			
SYS ✓		TIM5 ✓	USART2 ✓			
		TIM6 ✓	USART3 ✓			
		TIM8 ✓				
		TIM9 ✓				

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00154959.pdf

Application note http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00213525.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00263732.pdf

Application note http://www.st.com/resource/en/application_note/DM00281138.pdf

Application note http://www.st.com/resource/en/application_note/DM00296349.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00373474.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00431633.pdf

Application note http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf