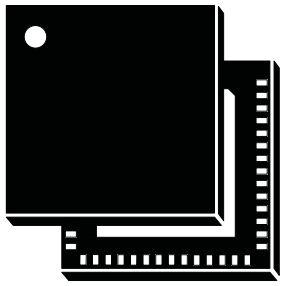
STHV800

Octal ±90 V, ±2 A, 3-level RTZ, high-speed ultrasound pulser

Datasheet - production data



TFLGA-56LD (8x8x0.9 mm)

Features

- 0 to ±90 V output voltage
- Up to 20 MHz operating frequency
- Power-up/down sequence free
- Low-power, high-voltage, high-speed PW, CW drivers
- Gate drivers self-biased architecture, no filtering capacitors required
- Optional synchronization of the input signals by an external clock
- Dual supplied half bridges (pulsed wave/continuous wave)
- Pulsed wave (PW) mode operations:
  - 3-level output waveform
  - ±2 A source and sink current
  - Down to 20 ps jitter
  - Anti-cross conduction function
  - Low 2nd harmonic distortion
- Continuous wave (CW) mode operations:
  - 130 mW max. power consumption/channel
  - ±0.3 A source and sink current
  - 95 fs RMS jitter [100 Hz-20 kHz]
- Fully integrated real clamping-to-ground function
  - 8.5 Ω synchronous active clamp
  - Anti-leakage on output node
  - ±2 A source and sink current
- Fully integrated T/R switch
  - 8.5 Ω ON resistance
  - Up to 300 MHz BW
  - Receiver multiplexing function
  - No DC consumption (high impedance/standby state)
- 1.8 V to 3.6 V CMOS logic interface
- Auxiliary integrated circuits
  - Noise blocking diodes
  - Anti-memory effect for all internal HV nodes during clamp state
  - Thermal protection / disable pin
- Latch-up free due to HV SOI technology
- Very few external passive components needed

Applications

- Medical ultrasound imaging
- Pulse waveform generators
- NDT ultrasound transmission
- Piezoelectric transducer drivers

Table 1. Device summary

Order code	Package	Packing
STHV800QTR	TFLGA-56LD	Tape and reel

This is information on a product in full production. www.st.com

Contents

1 Description

This monolithic, high-voltage, high-speed pulse generator features eight independent channels. It is designed for medical ultrasound applications, but it can also be used for driving other piezoelectric, capacitive, or MEMS transducers. The STHV800 is made up of a controller logic interface circuit (compatible with both 1.8 V and 3.3 V input signals), level translators, self-biased high-voltage MOSFET gate drivers, noise blocking diodes, high power P-channel and N-channel MOSFETs as the output stage for each channel, clamping to-ground circuitry, anti-leakage, anti-memory effect block, thermal sensor, and a T/R switch which guarantees an effective decoupling during the transmission phase. Moreover, the STHV800 includes self-biasing and thermal shutdown blocks. Each channel can support up to three active output levels with one half bridge. Each channel is comprised of two supplied output stages, respectively, used for pulsed wave (PW) and continuous wave (CW) operations. The PW output stage is able to provide up to ±2 A peak output current while, to reduce power dissipation and jitter during continuous wave mode, the fully optimized CW output stage delivers up to ±0.3 A.

The CW bridge has dedicated power supply pins HVP_CW and HVM_CW, whereby, the voltages relationship HVM_CW ≥ HVM and HVP_CW ≤ HVP during operative condition must be respected. This feature allows the use of dedicated power rails for the CW mode. As an option, the HVP_CW and HVM_CW pins can also be shorted, respectively, to the HVP and HVM ones, thus allowing the use of just a single dual HV power supply in the application.

The eight independent T/R switches can be used in both a dedicated RX chain per channel or in a multiplexing configuration.

The clamp circuit, used to carry output pin XDCR down to GND, has a current capability in excess of 2 A.

The STHV800 internal self-biasing circuitry prevents using dedicated external high voltage rails to drive the gates of the PW and CW bridges; besides this, it allows very low power consumption during the RX phase (down to 200 µW as global power consumption due to the fact that during this phase the PW and CW bridges do not switch).

The STHV800 requires very few external components: if the PW and CW bridges are supplied independently, then six decoupling capacitors to GND, tied to pins HVP (HVM) to HVP_CW (HVM_CW), VDDP, VDDM and a resistor for the pulling-up of the THSD pin are necessary. If the PW and CW bridges share the same dual high voltage supply, then four decoupling capacitors to GND tied to pins HVP/HVP_CW and HVM/HVM_CW and a resistor for the pulling-up of the THSD pin are necessary.

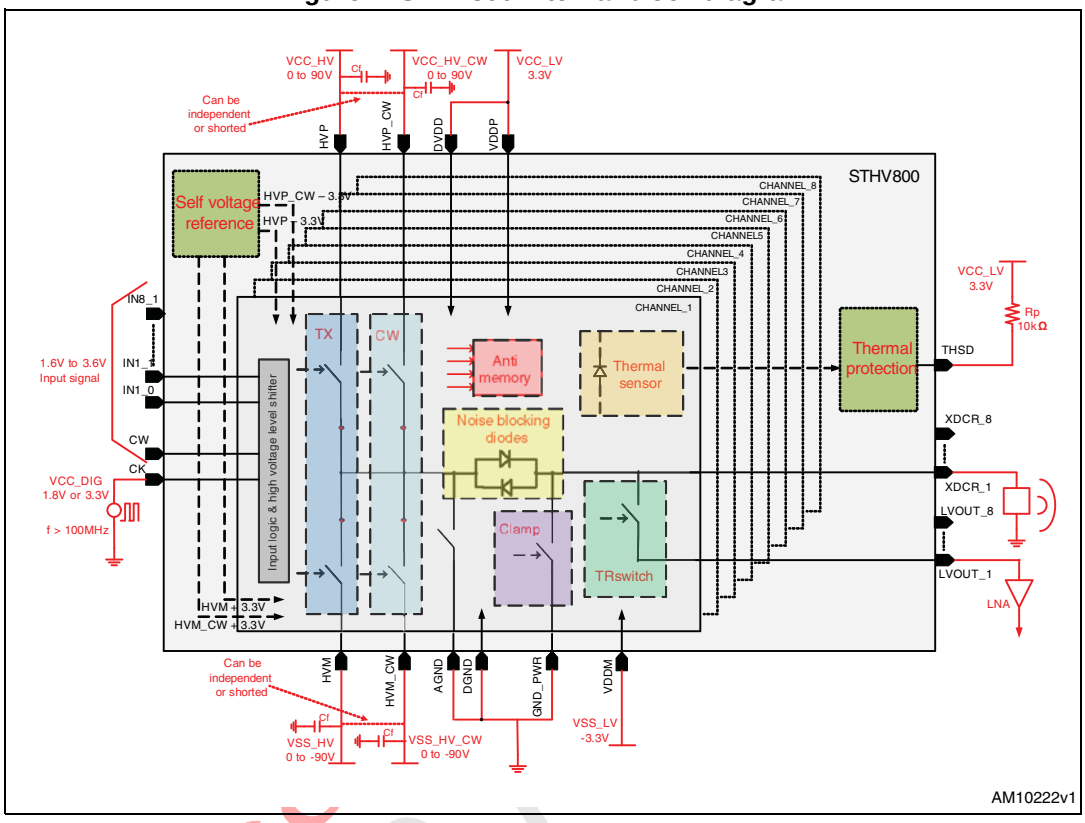
The reference voltage supplies for the gate drivers of the PW and CW bridges do not require any external dedicated pins.

Each channel is independently controlled by means of 2 digital bits. An external clock can be used to synchronize all the control input signals, allowing the optimization of both the jitter and the HD2 performance of the device. This feature is, however, optional: if the CK pin is tied to ground the device works in asynchronous mode.

The STHV800 is fully power-up and power-down sequence free.

2 Typical application circuit

Figure 1. STHV800 internal block diagram



With regard to *Figure 1*, Cf are the filtering capacitors tied to the high-voltage power supply pins HVP, HVM, HVP_CW, and HVM_CW; the low-voltage power supply pins the low-voltage power supply pins, VDDP and VDDM require LV filtering capacitors.

The CK pin allows the synchronization of the control input signals CW, INX_0, and INX_1 (X=1 to 8) by means of an external clock.

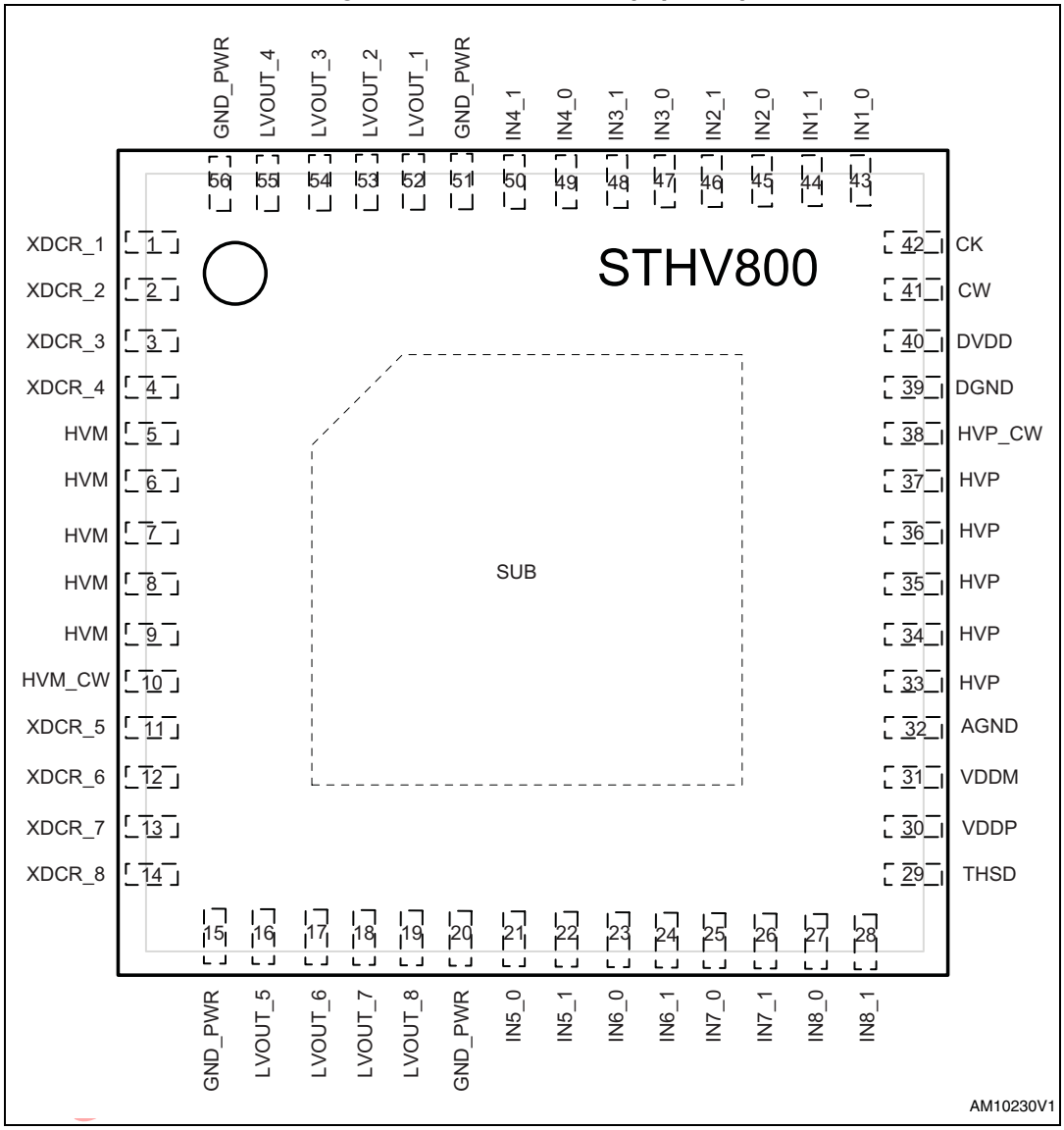
Moreover, pin CK can also be tied to ground: in this case, the STHV800 is controlled solely by means of the control input signals CW, INX_0, and INX_1 (X=1 to 8) and it works in asynchronous mode.

THSD is a thermal flag. Being the output stage of the thermal protection circuitry an open-drain N-channel MOSFET, an external pull-up resistor (Rp >10 kΩ) connected between a positive low-voltage supply and pin THSD (see *Figure 1*) is required. If the internal temperature surpasses 153 °C, THSD goes down and all STHV800 channels are in the HZ state. The thermal protection can be disabled, by tying the THSD pin to a positive low-voltage supply. THSD can also be shared between several STHV800s on the same PCB.

Should this be the case, if one STHV800 enters into thermal protection state, all other devices are forced into high impedance state. Moreover, THSD can be forced to ground by an external user in order to put all channels in high impedance (HZ), independently by inputs state.

3 Pin settings

Figure 2. Pin connection (top view)



3.1 Pin description

Table 2. Pin description

Pin n.	Name	Function	In/out	Type(1)
1	XDCR_1	Channel 1, high-voltage output	O	P
2	XDCR_2	Channel 2, high-voltage output	O	P
3	XDCR_3	Channel 3, high-voltage output	O	P
4	XDCR_4	Channel 4, high-voltage output	O	P
5	HVM	Negative high-voltage supply	I	P
6	HVM	Negative high-voltage supply	I	P
7	HVM	Negative high-voltage supply	I	P
8	HVM	Negative high-voltage supply	I	P
9	HVM	Negative high-voltage supply	I	P
10	HVM_CW	Negative high-voltage CW supply	I	P
11	XDCR_5	Channel 5, high-voltage output	O	P
12	XDCR_6	Channel 6, high-voltage output	O	P
13	XDCR_7	Channel 7, high-voltage output	O	P
14	XDCR_8	Channel 8, high-voltage output	O	P
15	GND_PWR	Power ground	I	P
16	LVOUT_5	Channel 5, low-voltage output	O	A
17	LVOUT_6	Channel 6, low-voltage output	O	A
18	LVOUT_7	Channel 7, low-voltage output	O	A
19	LVOUT_8	Channel 8, low-voltage output	O	A
20	GND_PWR	Power ground	I	P
21	IN5_0	Input signal channel 5	I	D
22	IN5_1	Input signal channel 5	I	D
23	IN6_0	Input signal channel 6	I	D
24	IN6_1	Input signal channel 6	I	D
25	IN7_0	Input signal channel 7	I	D
26	IN7_1	Input signal channel 7	I	D
27	IN8_0	Input signal channel 8	I	D
28	IN8_1	Input signal channel 8	I	D
29	THSD	Thermal shutdown pin / disable pin	I/O	D
30	VDDP	Positive low-voltage supply	I	A
31	VDDM	Negative low-voltage supply	I	A
32	AGND	Signal ground	I	A
33	HVP	Positive high-voltage supply	I	P

Table 2. Pin description (continued)

Pin n.	Name	Function	In/out	Type(1)
34	HVP	Positive high-voltage supply	I	P
35	HVP	Positive high-voltage supply	I	P
36	HVP	Positive high-voltage supply	I	P
37	HVP	Positive high-voltage supply	I	P
38	HVP_CW	Positive high-voltage CW supply	I	P
39	DGND	Clock ground	I	D
40	DVDD	Positive clock supply	I	D
41	CW	Input signal shared for CW mode	I	D
42	CK	Clock signal	I	D
43	IN1_0	Input signal channel 1	I	D
44	IN1_1	Input signal channel 1	I	D
45	IN2_0	Input signal channel 2	I	D
46	IN2_1	Input signal channel 2	I	D
47	IN3_0	Input signal channel 3	I	D
48	IN3_1	Input signal channel 3	I	D
49	IN4_0	Input signal channel 4	I	D
50	IN4_1	Input signal channel 4	I	D
51	GND_PWR	Power ground	I	P
52	LVOUT_1	Channel 1, low-voltage output	O	A
53	LVOUT_2	Channel 2, low-voltage output	O	A
54	LVOUT_3	Channel 3, low-voltage output	O	A
55	LVOUT_4	Channel 4, low-voltage output	O	A
56	GND_PWR	Power ground	I	P
Exposed-Pad(2)		Substrate (SUB)	NC / I	P

1. P = power, A = analog, D = digital, NC = not connected.
2. The exposed pad is internally connected to the substrate of the device. It can be either left floating or connected to ground via a 100 V capacitor, in order to reduce the noise during the receiving phase.

4 Single channel block description and truth table

Figure 3. Single channel block

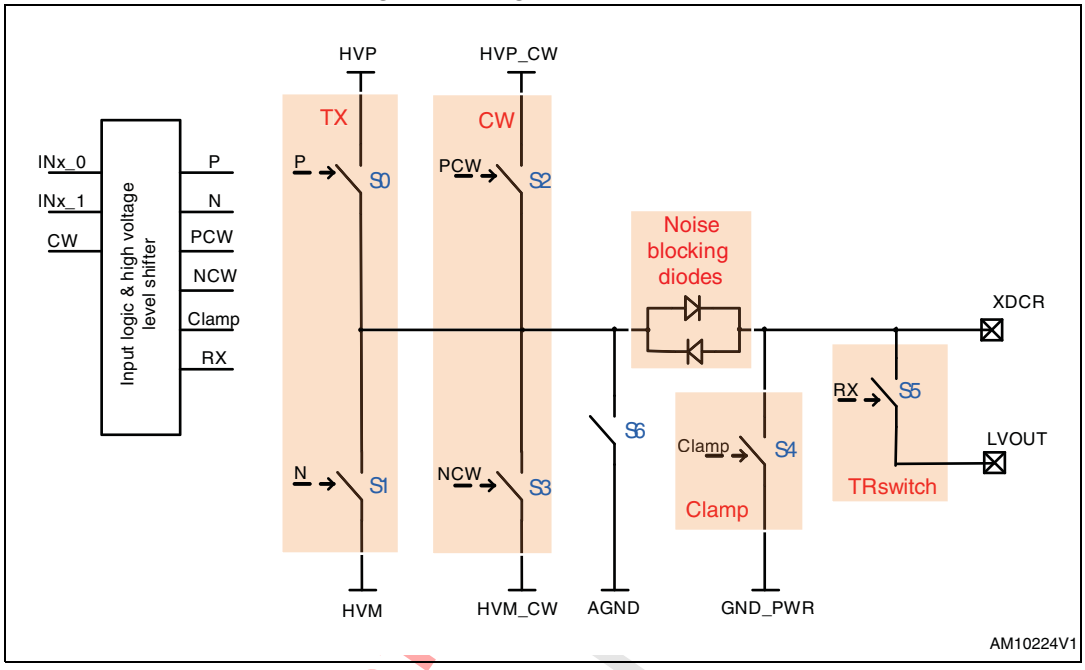


Table 3. Truth table per channel

THSD	CW	INx_0	INx_1	State	S0	S1	S2	S3	S4	S5	S6
Global		Per channel(1)									
1	x	0	0	Clamp	0	0	0	0	1	0	1
1	0	0	1	HVM	0	1	0	0	0	0	0
1	0	1	0	HVP	1	0	0	0	0	0	0
1	0	1	1	RX	0	0	0	0	0	1	1
1	1	0	1	HVM_CW	0	0	0	1	0	0	0
1	1	1	1	HVP_CW	0	0	1	0	0	0	0
1	1	1	0	RX	0	0	0	0	0	1	1
0	x	x	x	HZ	0	0	0	0	0	0	0

1. INx_0, INx_1 control CHx; where x=1 to 8 is the concerned channel.

5 Power-up / power-down voltage sequence

The device is fully power-up/power-down sequence free, meaning that there is no recommended sequence to follow in order to power up/down the STHV800. While away, in operative conditions the relationship HVM_CW ≥ HVM and HVP_CW ≤ HVP must be respected.

6 Electrical data

6.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AGND	Analog ground reference(1)	0	V
DGND	Digital ground	-300 to 300	mV
GND_PWR	Power ground	-1.2 to 1.2	V
VDDP	Positive supply voltage	-0.3 to 3.9	V
VDDM	Negative supply voltage	0.3 to -3.9	V
DVDD	Positive logic voltage	-0.3 to 3.9	V
HVP	TX0 high-voltage positive supply	95	V
HVP_CW	TX1 high-voltage positive supply	95	V
HVM	TX0 high-voltage negative supply	-95	V
HVM_CW	TX1 high-voltage negative supply	-95	V
XDCR	High-voltage output	-95 to 95	V
LVOUT	Low-voltage output	-1 to 1	V
THSD	Thermal shutdown status (active low)	-0.3 to 3.9	V
DIG I/O	Digital input specified in *Figure 2*	-0.3 to VDDP + 0.3	V
T_{OP}	Operating temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. AGND is the ground reference for all the other voltages.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th,JA}$	Thermal resistance junction-ambient	30(1)	°C/W

1. This value is given for a two-layer PCB (2S2P) and it is strongly sensitive to PCB layout. Increasing the number of PCB layers and/or heatsink vias, the thermal resistance Rth,JA decreases.

7 Operating supply voltages and maximum average currents

Unless otherwise specified, only one channel is on, XDCR pin loaded with 300 pF//100 Ω, HVP=90 V, HVM=-90 V, HVP_CW=5 V, HVM_CW=-5 V.

Table 6. Supply voltages

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDDP	Positive supply voltage		2.7	3.3	3.6	V
I_{VDDP}	Positive supply current	CW mode(1)		20		mA
VDDM	Negative supply voltage		-2.7	-3.3	-3.6	V
I_{VDDM}	Negative supply current	CW mode		40		mA
DVDD	Positive logic voltage		1.6	3.3	3.6	V
I_{DVDD}	Logic supply current	PW mode(2)		90		µA
HVP	High-voltage positive supply		0		90	V
I_{HVP}	HV positive supply current	PW mode		80		mA
HVM	High-voltage negative supply		-90		0	V
I_{HVM}	HV negative supply current	PW mode		80		mA
HVP_CW	CW high-voltage positive supply		0		90	V
I_{HVP_CW}	CW HV positive supply current	CW mode		80		mA
HVM_CW	CW high-voltage negative supply		-90		0	V
I_{HVM_CW}	CW HV negative supply current	CW mode		70		mA

1. In CW mode the average current is measured over one period of the output waveform (eight channels in parallel with same phase).
2. In PW pulse wave mode the average current is measured over time interval T_w time (see *Table 8*).

7.1 Digital inputs

Table 7. Digital inputs

Symbol	Parameter	Min.	Max.	Units
IN#, CW, CK, THSD	Input logic high-voltage	0.4xVDDP	VDDP	V
IN#, CW, CK, THSD	Input logic low-voltage	0	0.2xVDDP	V

7.2 Output signals

Table 8. Output signals

Symbol	Parameter	Condition	Min.	Max.	Units
XDCR	High-voltage output		-90	90	V
LVOUT	Low-voltage output		-1	1	V
VTHSD	THSD pin voltage	In thermal shutdown condition VCC_LV=3.3V, Isink_max=0.33 mA (at Rpull-up=10 kΩ)	0	0.4	V

8 Electrical characteristics

Table 9. Static electrical characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_p	Saturation current S0	HVP = 60 V	1.7	2		A
I_N	Saturation current S1	HVM = -60 V	1.7	2		A
I_{PCW}	Saturation current S2	HVP_CW = 5 V	130	180		mA
		HVP_CW = 10 V		350		mA
I_{NCW}	Saturation current S3	HVM_CW = -5 V	130	180		mA
		HVM_CW = -10 V		350		mA
I_L	Output leakage current	HVP = 90 V, HVM = -90 V, HVP_CW =90 V, HVM_CW= -90 V			10	µA
I_{CL}	Clamp current	HVP = 60 V, HVM = -60 V	1.7 (2)	2		A
P_{RX}	Total power dissipation	All channels in RX state		250	320	µW
P_{CL_CW}	Power dissipation in clamp state	CW mode, CW =1, HVP_CW = 5 V HVM_CW = -5 V		7	10	mW
P_{CL_PW}	Power dissipation in clamp state	PW mode, CW = 0, HVP = 60 V HVM = -60 V		200	240	mW
T_{OTP}	Overtemperature threshold	HVP# = 10 V, HVM# = -10 V	130	153	160	°C
T_{HYS}	OTP hysteresis	HVP# = 10 V, HVM# = -10 V		40		°C
R_{ON}	T/R SW ON resistance (S4)	XDCR= 0, LVOUT = 0.1 V		8.5	10	Ω
R_{OFF}	T/R SW OFF resistance (S4)		1			GΩ
$C_{T/R\ SW}$	T/R SW capacitance			35		pF

1. Operating conditions, unless otherwise specified, HVP = 60 V, HVM = -60 V, HVP_CW=5 V, HVM_CW= -5 V, VDDP =DVDD= 3.3 V, VDDM = -3.3 V, T_{ROOM}= 25 °C.
2. Guaranteed by bench characterization

Table 10. AC electrical characteristics(1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
f	Maximum output frequency	PW mode, 5 pulses	1		20 (2)	MHz
f_{CW}	Maximum output frequency CW	Continuous wave mode	1		20 (2)	MHz
f_{CK}	Clock frequency		25	100	200	MHz
$t_{j\text{-}CW}$	CW output jitter	HVP1=5V, HVM1=-5V, continuous wave mode		95		fs, rms

Table 10. AC electrical characteristics(1) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
t_f	Fall time			22		ns
t_r	Rise time			22		ns
t_{dr}	Rise propagation delay			14		ns
t_{df}	Fall propagation delay			14		ns
$t_{T/R\ SW}$	T/R SW turn-on / turn-off time			50		ns
HD2	2nd harmonic distortion	1 period; f = 5 MHz		-40		dBc
		5 periods; f = 5 MHz		-40		dBc
HD2PC	Pulse cancellation	f = 5 MHz original and inverted pulse		-40		dBc
BVD	Burst voltage drop	CW mode, 1st to 128th pulse		2		%
P_{D_CW}	Power dissipation, per channel	CW mode, f = 5 MHz, no load		130	150	mW
$P_{D\_CW\_max}$	Power dissipation, all channels			920		mW
T/R SW_{SPIKE}	T/R SW spike on LVOUT			100		mV_{pp}
$^{X}TALK$	Cross talk between channels.	Ampl(2ch)/Ampl(1ch)		-55		db

1. Operating conditions, unless otherwise specified, HVP = 60 V, HVM = -60 V, HVP_CW = 5 V, HVM_CW = -5 V, VDDP = 3.3 V, VDDM = -3.3 V, DVDD = 3.3 V, f_{CK} = 100 MHz, XDCR load C = 300 pF//R = 100 Ω, LVOUT load C 20 pF//200 Ω, T_{ROOM} = 25 °C.
2. Guaranteed by bench characterization.

9 Clock

An external clock can be used to synchronize all the control input signals CW, INX_0, and INX_1 (X=1 to 8) of the STHV800. This option allows the optimization of both the jitter and the HD2 performance. The embedded synchronization logic circuitry samples the input signals on the rising edge of the clock. This feature is optional: if pin CK is tied to GND, the device works in asynchronous mode.

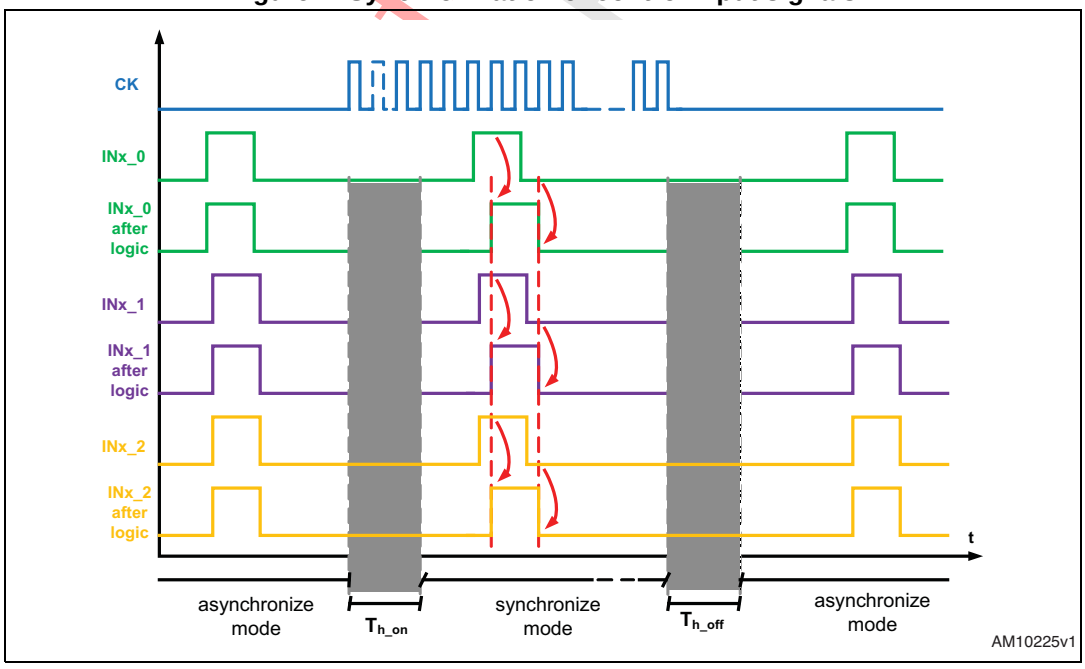
With regard to *Figure 4*, for the STHV800 to switch from an asynchronous mode to a synchronous one, a time delay Th_on, in excess of 80 ns, must elapse in order for the control input signals CW, INX_0, and INX_1 (X=1 to 8) to be correctly read by the device.

For the STHV800 to switch from a synchronous mode to an asynchronous one, subsequent to the prior tying to GND of the CK pin, a time delay Th_off, in excess of 80 ns, must elapse in order for the control input signals CW, INX_0, and INX_1 (X=1 to 8) to be correctly read by the device.

Therefore, for a correct use of the STHV800, the reading of all control input signals CW, INX_0, and INX_1 (X=1 to 8) during time intervals Th_on and Th_off is not activated by the STHV800 and the conditions for a correct operation are:

- T_{h_on} > 80 ns
- T_{h_off} > 80 ns

Figure 4. Synchronization of control input signals



10 Receiving phase timings

Before and after a RX state, a clamping to GND of switch S8 (*Figure 3*) is necessary for the STHV800 to remove the accumulated charge in the device, due to the internal parasitic capacitances.

Moreover, during an RX state, the overall power consumption gets as low as 200 µW.

With regard to *Figure 5*, when the last channel enters in RX state, a procedure starts to power down the embedded reference supplies (supply voltages for the gate drivers of the PW and CW bridges). For a transmitter phase to start again, it is necessary that one channel exits from RX state.

The above information and the correct timing to manage a receiving phase are summarized in *Figure 6*, whereby:

- T_{clamp_preRX}: is a necessary clamping state time interval before an RX state. It allows a reduction of charge injection on the LVOUT pins.
- T_{PW_off} (3 µs): is the time transient needed for the reference supplies to turn-off.
- T_{SW_on} (50 ns): is the time transient needed for the TR_switch to turn-on.
- T_{ECHO}: is the time interval during which the echoed signal is correctly received.
- T_{SW_off} (50 ns): is the time transient needed for the TR_switch to turn-off. After this delay, a high impedance condition returns between pins XDCR and LVOUT.
- T_{clamp_postRX}: is a necessary clamping state time interval after an RX phase. It is needed for turning off the TR_switch and powering up the reference supplies.

Figure 5. RX timing for all channels

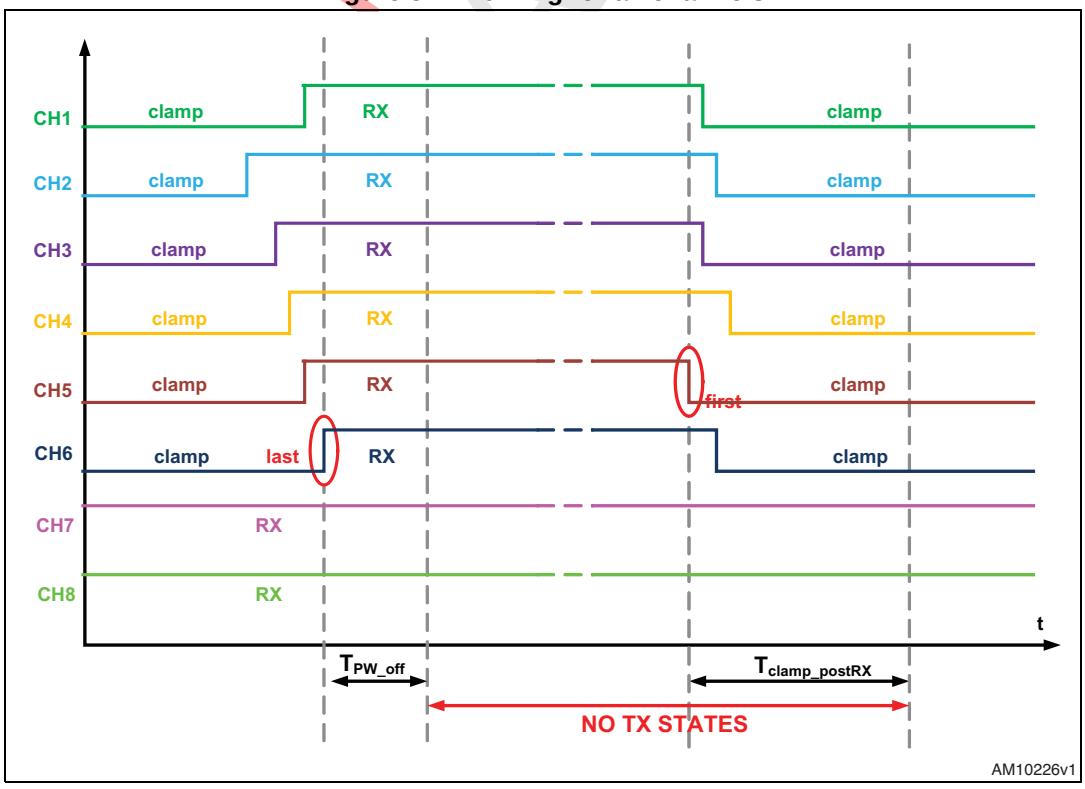


Figure 6. RX timing for one channel

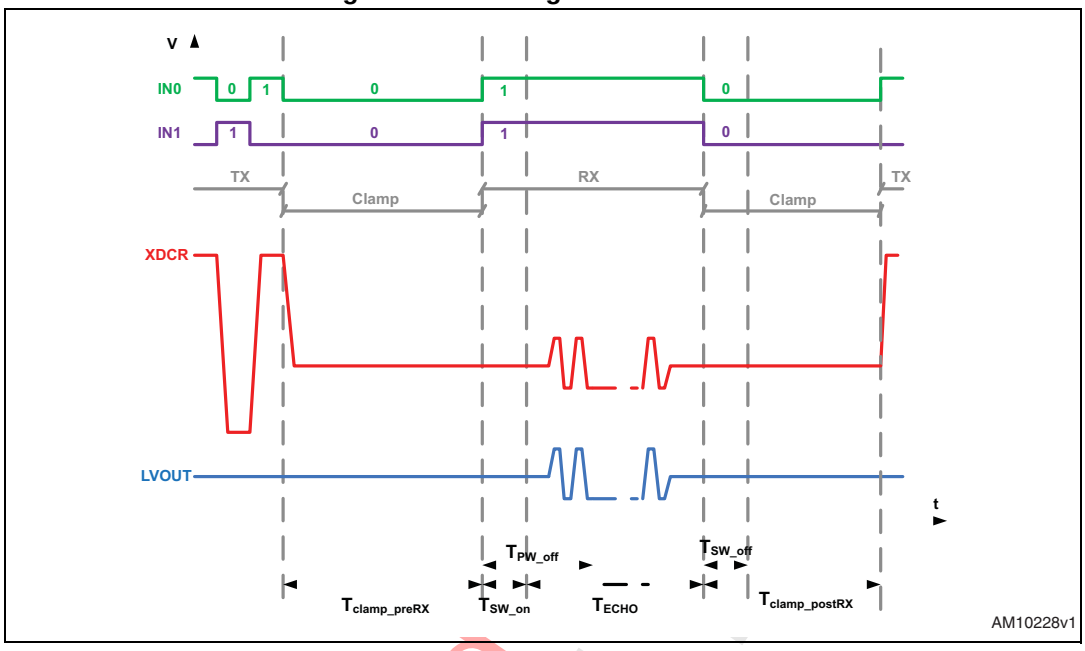


Table 11. Pre/post RX timing

Name	Time
T_{clamp_preRX}	≥ 600 ns
T_{clamp_postRX}	≥ 3 µs

The above conditions are suggested for correct functionality of the STHV800.

11 Working condition

Figure 7. PW example 5 periods, first pulse positive

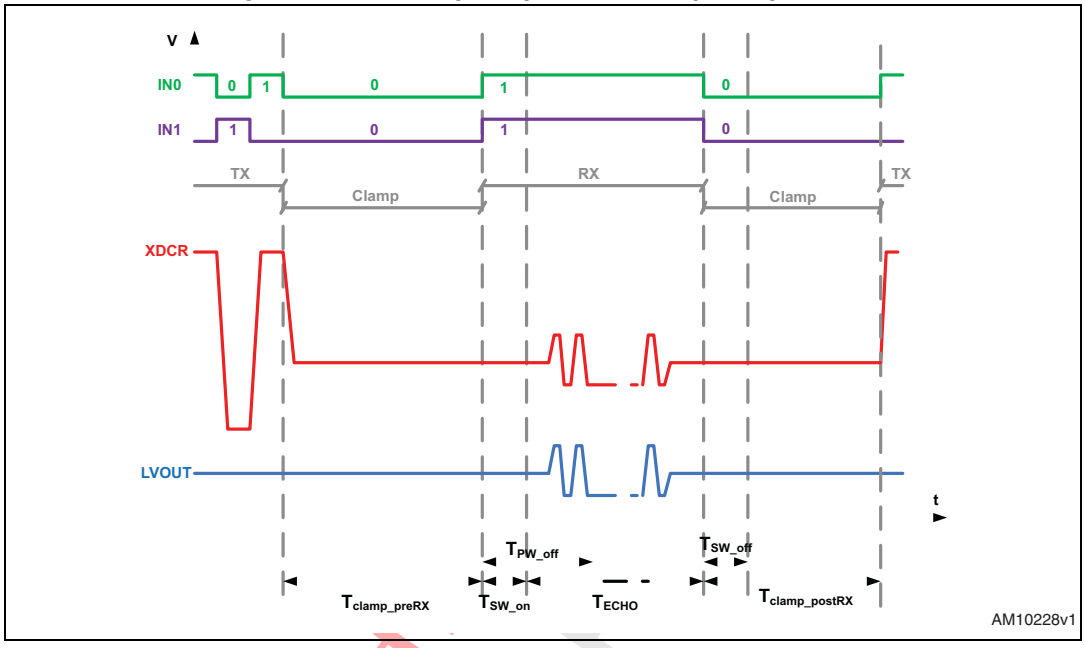


Figure 8. CW example

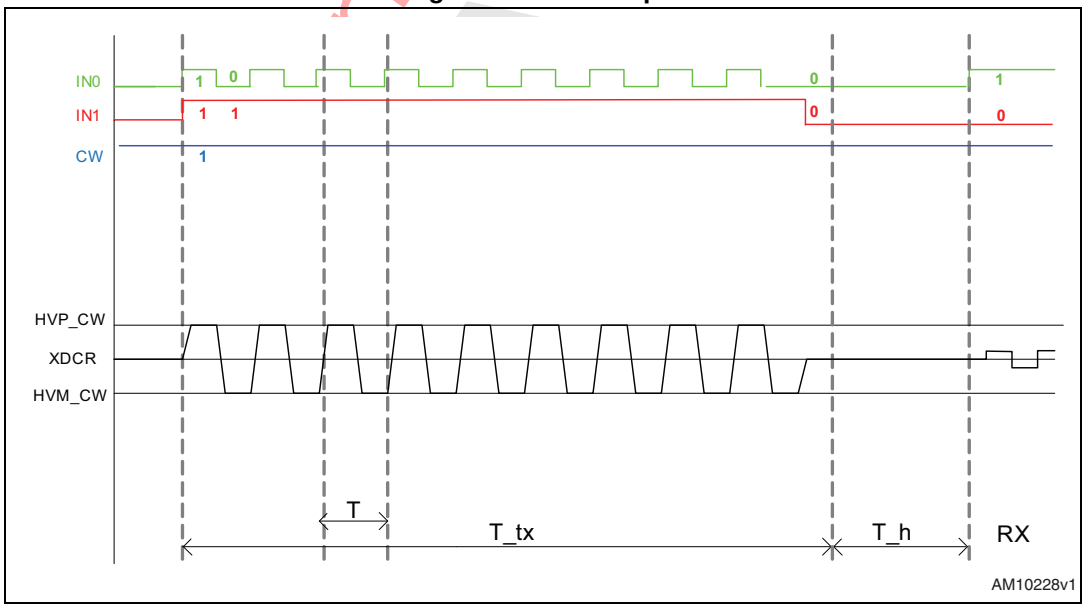


Figure 9. PC example

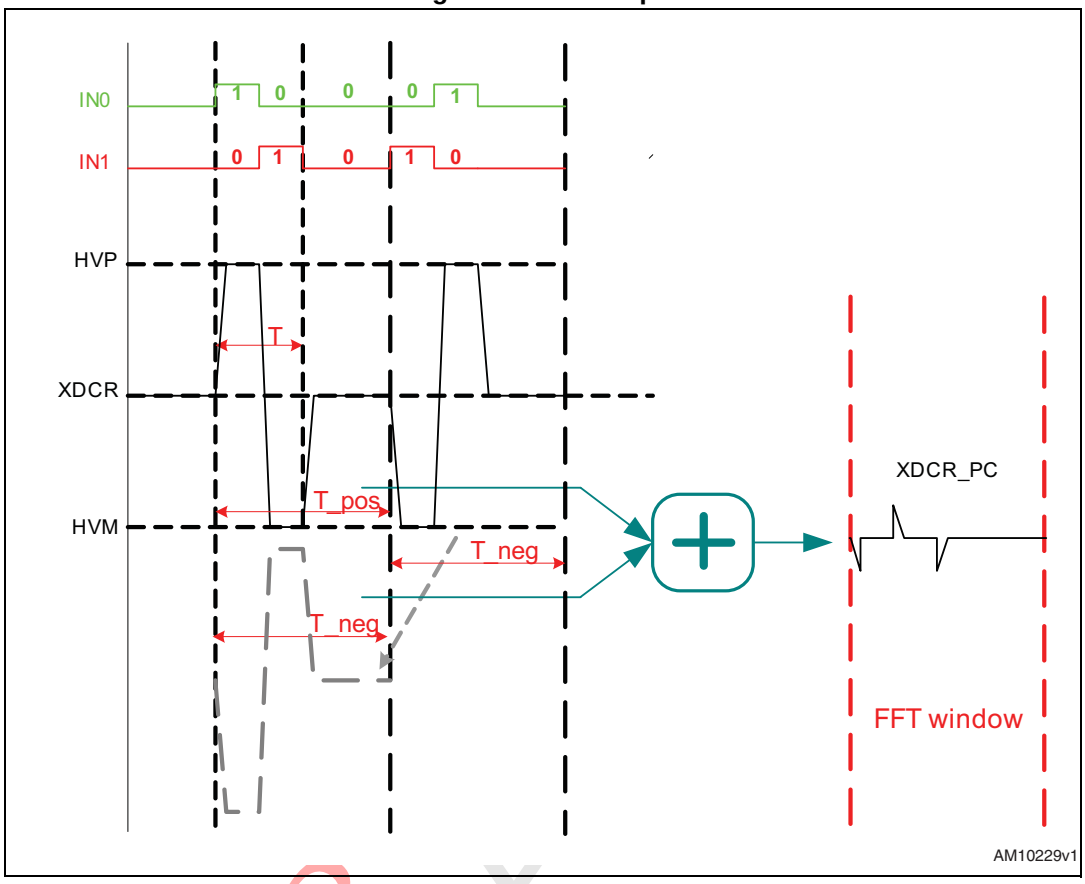
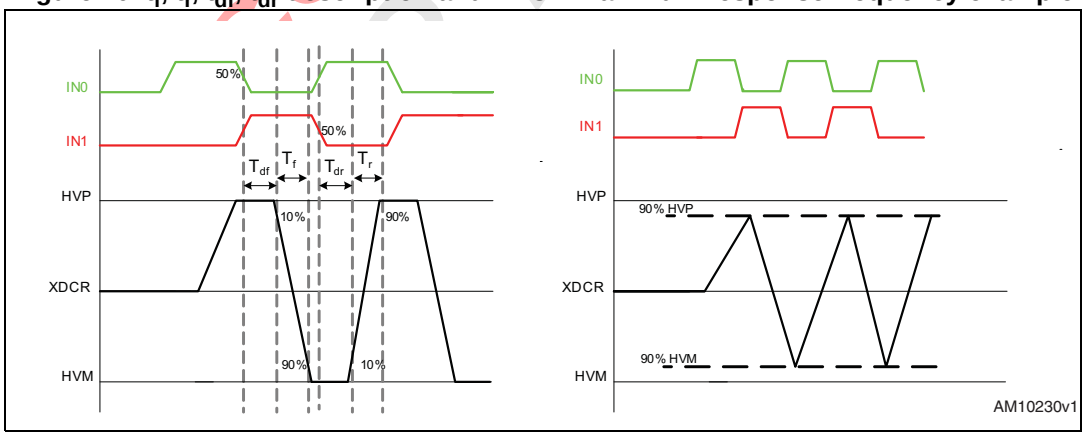


Figure 10. t_f, t_r, t_{df}, t_{dr} description and XDCR maximum response frequency example



12 Output phase noise measurement in CW mode

12.1 Typical performance characteristics

Unless otherwise stated, the following conditions apply:

VDDP = +3.3 V, VDDM = -3.3 V, DVDD = +3.3 V, Exp-PAD = -5 V, HVP = ??, -HVM = 5 V, no load, F_{in}= 5 MHz, T_A = 25 °C.

Figure 11. Measurement setup - CK1 = 640 MHz; CK2 = 5 MHz

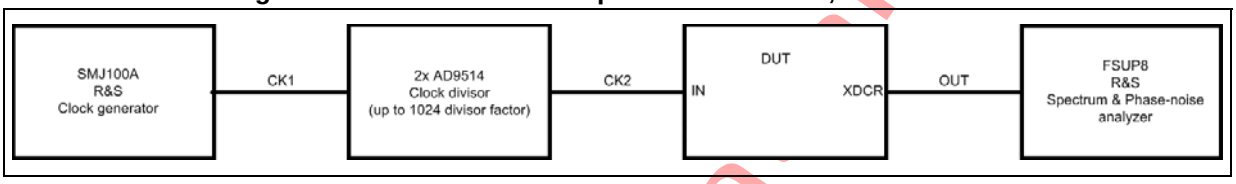
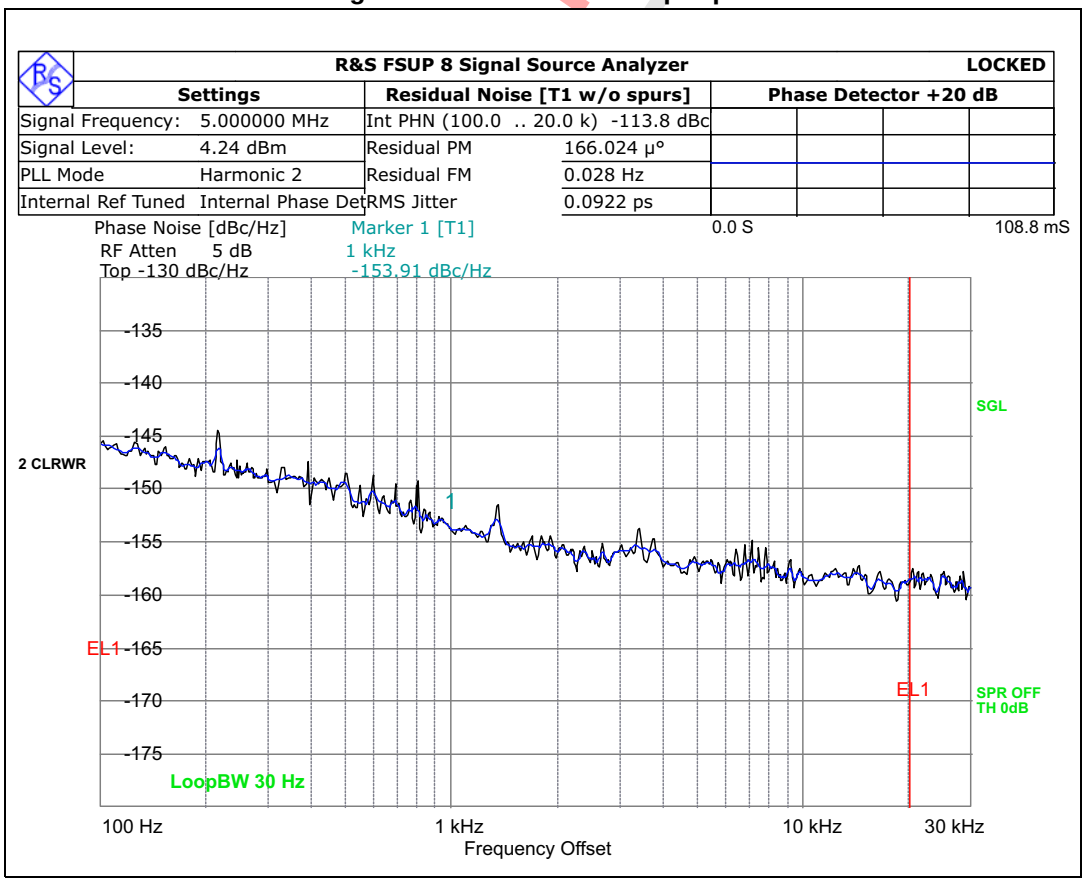


Figure 12. Phase noise output plot



Significant results from the output have been extracted[(a)]:

- Phase noise @1 kHz: -154 dBc/Hz
- RMS jitter [BW 100 Hz - 20 KHz]: 95 fs

a. Values measured leave room for improvement. As such, they are affected by a non-optimized setup.

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

13.1 TFLGA-56LD (8x8x0.9 mm) package information

Figure 13. TFLGA-56LD (8x8x0.9 mm) package outline

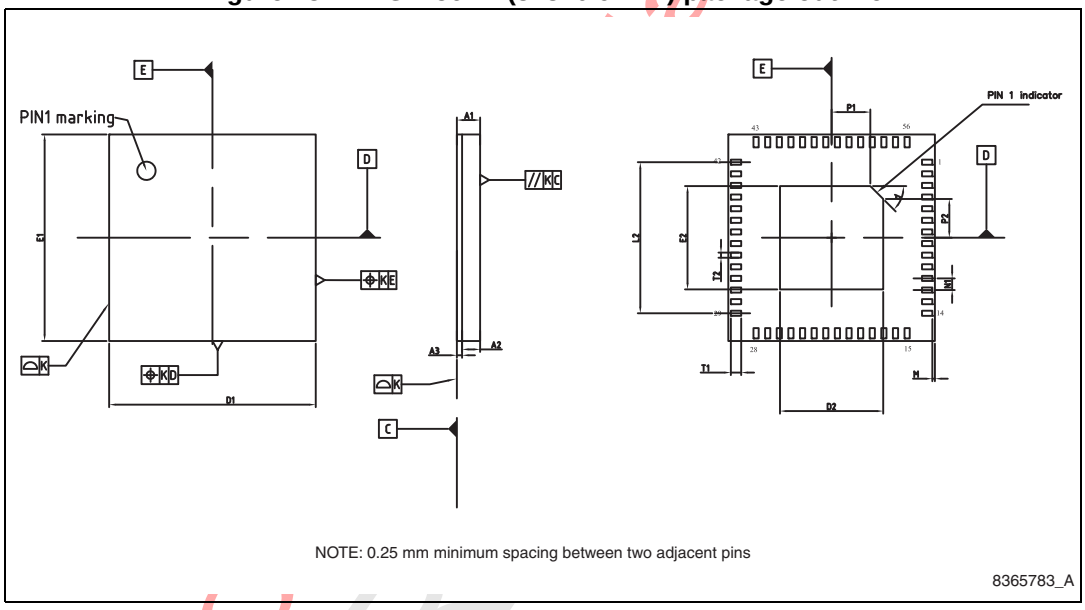


Table 12. TFLGA-56LD (8 x 8 x 0.9 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1		0.900	
A2		0.700	0.20
A3		0.200	
D1	7.850	8.000	8.150
E1	7.850	8.000	8.150
N1		0.450	
D2		4.000	
E2		4.000	
L2		5.850	
T1	0.350	0.400	0.450
T2	0.150	0.200	0.250
P1		1.500	
P2		1.500	
d		45°	
M		0.100	
k		0.050	

14 Revision history

Table 13. Document revision history

Date	Revision	Changes
27-Mar-2013	1	Initial release.
31-Jan-2014	2	Added: - I_{CL} clamp current row *Table 9 on page 12*.
15-Jan-2016	3	– Updated Features on the coverpage and output jitter data in *Table 10*. – Added *Section 12: Output phase noise measurement in CW mode* – Reformatted *Package information* section to current standards.

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