AN4471
Application note

STEVAL-IME009V1 evaluation board based on the STHV800 high voltage pulser

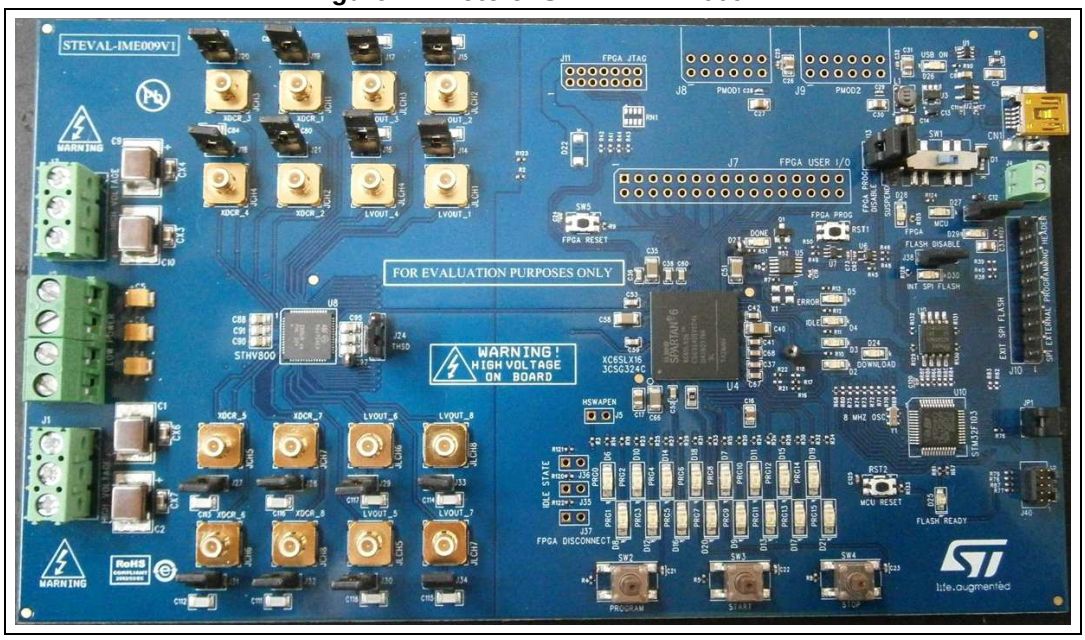
Introduction

The STEVAL-IME009V1 is an evaluation board designed around the STHV800 transmission pulser, which is a state-of-the-art product for ultrasound imaging applications.

The system permits four transducers to be driven as 8-channel transmitters; the output waveforms can be displayed directly on an oscilloscope by connecting the scope probe on the relative BNCs.

16 preset waveforms are available to test the HV pulser under different conditions.

Figure 1. Photo of STEVAL-IME009V1



Warning: **Before applying any voltage to the STEVAL-IME009V1, please read the instructions in this document carefully.**

Contents

1 Board features

- Suitable for ultrasound imaging applications
- 8 monolithic channels, 3-level high voltage pulser
- Integrated T/R switch
  - On-board equivalent piezoelectric load implemented by means of R/C equivalent network
- USB interface to upload customized output waveforms
- 4 Mb serial Flash memory for storing customized waveforms
- Memory expansion connector to expand the serial Flash size
- High voltage and low voltage connectors to power the STHV800
- 25 LEDs to check evaluation board status and proper operation
- Human Machine Interface to select, start and stop the stored output waveforms

2 Getting started

The STEVAL-IME009V1 is shipped by STMicroelectronics and is ready to use in Normal mode. The user only needs to:

1. Connect the right power supply to the board (see *Section 3.1*)
2. Connect the BNC to the oscilloscope
3. Check that switch SW1 is set on the FPGA position (see *Table 1* in *Section 3.1*)
4. Check that the LED labeled “DONE” (D23) is on
5. Check that FPGA is in the idle state (LED D4 is on)
6. Select the waveform with the Program button; the corresponding program LED (D6-D21) turns on
7. Press the START button to run the selected program; the START LED (D2) turns on
8. The selected waveform is output until the STOP button is pressed and the relative LED (D3) turns on. After the program ends, the FPGA returns to the idle state (LED D4 is on)
9. To run the same program again, restart from step 7; to run another program, restart from step 6

For Programming mode, please refer to UM1083.

3 Hardware layout and configuration

The STEVAL-IME009V1 evaluation board is designed around the STHV800. The hardware block diagram (*Figure 2*) illustrates the main connection between STHV800, the FPGA, the STM32F103C8T6 and the SPI Flash memory. *Figure 3* will help you to locate connectors, LEDs and features on the board.

Figure 2. Hardware block diagram

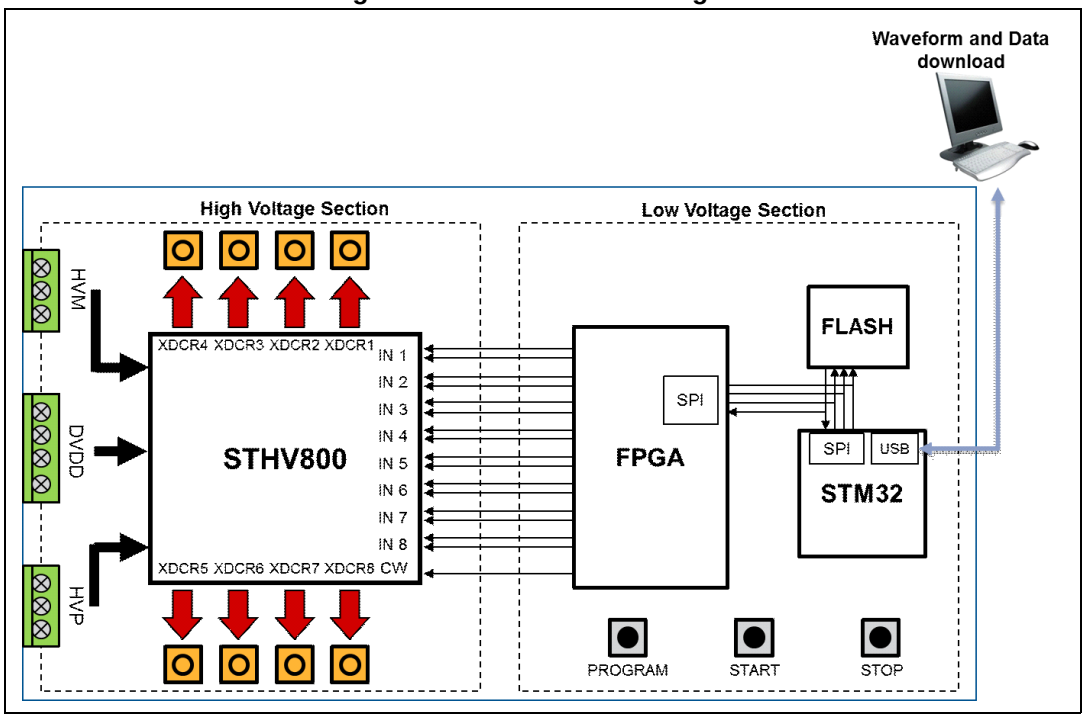
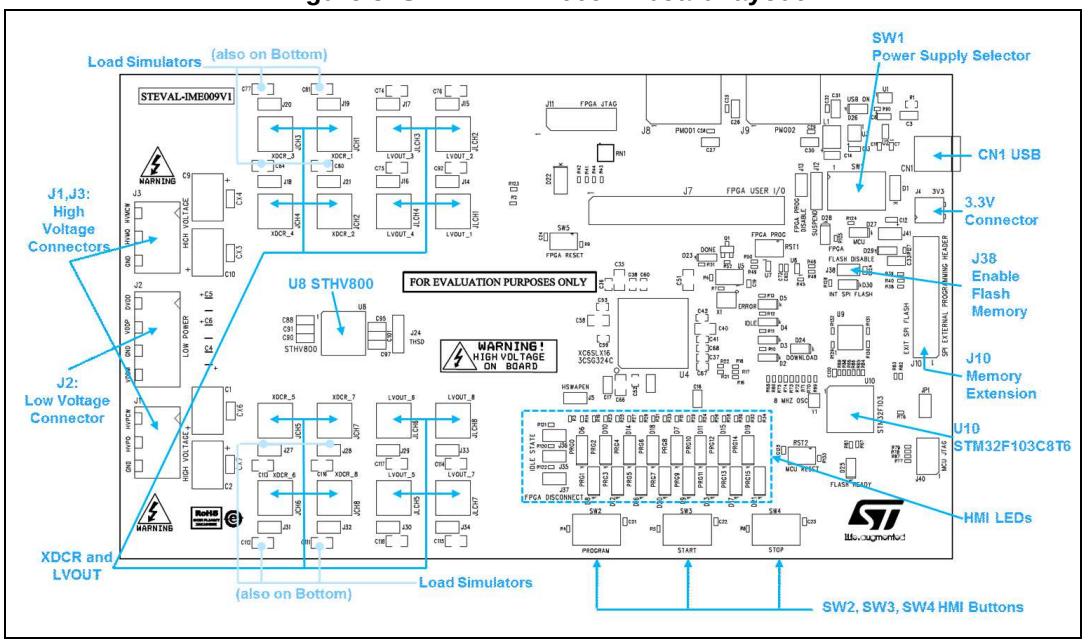


Figure 3. STEVAL-IME009V1 board layout



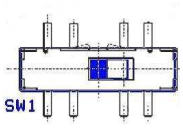
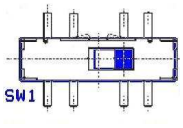
3.1 Power supply

The low voltage block of the STEVAL-IME009V1 board is designed to be powered by:

- 3.3 V DC connected to J4 to supply the FPGA and SPI Flash memory in Normal mode
- 5 V DC through USB mini-B connector to supply the STM32 and SPI memory in Programming mode

The power supply is configured by setting SW1 and J41 as described in *Table 1*.

Table 1. Power related jumpers

	Description	
SW1	 LEFT (1)	For normal operation mode, to power supply FPGA and SPI Flash memory. Default setting
	 RIGHT (1)	For update operation mode, to power supply STM32F103 and SPI Flash memory
J41 (2)	FPGA and SPI Flash memory are power supplied by DVDD (J2). Default setting: Not Mounted on PCB	

1. Left and right are conceived by looking the board as depicted in *Figure 1*.
2. The fitting of J41 can create voltage mismatch between J4 and J2 when one of these is not 3.3 V.

LED D26, D27 and D28 show the power supply configuration as described in *Table 1*.

Table 2. Power supply LEDs

	Color	Name	Description
D26	Red	USB ON	The USB cable is connected
D27	Red	MCU	Programming mode, to supply power to STM32F103 and SPI Flash memory
D28	Red	FPGA	Normal mode, to supply power to FPGA and SPI Flash memory

The high voltage block of the STEVAL-IME009V1 is designed to be powered by (see *Table 15* for maximum rating):

- HVPCW: Continuous wave high voltage positive supply (J1 conn.)
- HVP0:TX High voltage positive supply (J1 conn.)
- GND: Ground (J1 conn.)
- DVDD: Logic voltage, 3.3 V (J2 conn.)
- VDDP: Positive supply voltage 3.3 V (J2 conn.)

- VDDM: Negative supply voltage -3.3 V to 0 (J2 conn.)
- GND: Ground (J2 conn.)
- HVMCW: Continuous wave high voltage negative supply (J3 conn.)
- HVM0: TX high voltage negative supply (J3 conn.)
- GND: Ground (J3 conn.)

3.2 MCU

The STM32F103C8T6 updates the waveform and the FPGA bit stream on the SPI Flash memory. It is already pre-programmed as a DFU (device firmware upgrade) device and can upgrade internal and external Flash memory. The STM32F103 manages all the DFU operations, such as the authentication of product identifier, vendor identifier, Firmware version as well as the alternate setting number (Target ID). This is used to upgrade the SPI Flash memory hosted on the STEVAL-IME009V1 and render the upgrade more secure.

Note: See AN3156, UM0412 and UM1083 for further details about the upgrade through DFU.

3.3 SPI Flash memory

The STEVAL-IME009V1 hosts a Micron N25Q032 (U9), it is a 32-Mbit (4 Mb x 8) serial Flash memory with advanced write protection mechanisms. It can be accessed by a high speed SPI-compatible bus and can even work in XIP (eXecution in Place) mode.

The N25Q032 also supports the high-performance quad I/O instructions used by the FPGA to quadruple the transfer bandwidth for read and program operations.

If extra data memory is needed, the user can connect external Flash memory to the J10 connector. When the external Flash is plugged, LED D29 is on *Table 3*.

Table 3. SPI Flash memory LED

	Color	Name	Description
D29	Green	EXT SPI-FLASH	The external SPI-Flash module is connected
D30	Red	On-board SPI-FLASH	The on-board SPI-Flash is used

The Flash memory is configured by setting J38 as described in *Table 4*.

Table 4. SPI Flash memory jumper

	Status	Description
J38	Closed	Fitted (default setting): enable the power supply to the on-board SPI Flash memory (U9).
	Open	Unfitted: disable the power supply to the on-board SPI Flash memory.

3.4 FPGA

The STEVAL-IME009V1 includes a Xilinx Spartan®-6 XC6SLX16 FPGA that drives the STHV800 pulser by generating a suitable sequence of digital control signals (called “program”). The board can store 16 individually selectable programs. The main features of the waveforms generated by a program are summarized in *Table 5*.

Table 5. Programmable waveforms main features

Feature	Min.	Default	Max.
Programmable waveforms number	1	6	16
Pulse time resolution	-	5 ns	-
Pulse pattern duration (1)	40 ns	-	20.48 µs
Cycle period (PRF)	40 ns	-	2621.44 µs
Cycles number	1	-	255
Infinite cycle	Defined by the program		

1. Time period of the pulse sequence pattern. (2) Time period of a pulse repetition cycle.

The data required to generate a program is stored in the SPI Flash memory. When the program starts, the data is downloaded from Flash memory and stored in the FPGA internal RAM blocks. The data is then managed in order to generate the high-speed STHV800 digital control signals.

The SPI Flash also contains FPGA configuration data (bit stream) which is automatically loaded during start-up or following an FPGA reset (SW5).

The FPGA is configured by setting jumpers as described in *Table 6*.

Table 6. FPGA jumper

	Description	
J5	J5 controls FPGA I/O pull ups during configuration. It should be fitted to enable I/O pull ups during FPGA configuration. Default setting: Not Mounted.	
J12	Force FPGA into Suspend mode	
	Allow STM32 to control FPGA Suspend mode (Default setting)	
J13	J13 is used to prevent FPGA programming from the configuration source. Fitted: disable FPGA programming. Unfitted: enable FPGA programming. (default setting: unfitted)	

Table 6. FPGA jumper (continued)

	Description	
J35 and J36	Configure J35 and J36 to setup outputs idle state as follows: (default setting: Not Mounted)	
	High Z	J35 and J36 unfitted
	Clamp / TRswitch	J35 fitted, J36 unfitted
	High Z	J35 and J36 fitted
	Clamp	J35 unfitted, J36 fitted
J37	Configure J37 to connect FPGA outputs to STHV800 (default setting: Not mounted)	
	Fitted: disconnect FPGA outputs (High Z)	
	Unfitted: connect FPGA outputs	

Once the FPGA has been configured, the LED DONE (D23) turns on and the FPGA state machine enters the idle state (LED D4 turns on).

In order to generate a programmed waveform, the user selects the desired waveform (refer to *Section 3.4.1*) through the Program button. The selected program is given by the illumination of its corresponding LED (D6, D8, … D21 represent Program 0, Program 1, … Program 15, respectively). Program selection loops back to Program 0 after the last installed program.

By pressing the START button, the selected program starts running and the START LED (D2) turns on. When the program ends, the FPGA returns to the IDLE state (LED D4 is on).

If a continuous wave program has been selected, the STOP button must be pressed to stop program execution. The FPGA returns to the idle state and the STOP LED (D3) turns on. The LEDs associated with FPGA operations are described in *Table 7*.

Table 7. FPGA LED

	Color	Name	Description
D2	Green	START	A program is running following activation of the start button SW5.
D3	Green	STOP	The stop button SW4 has been pressed.
D4	Green	IDLE	The FPGA state machine is in the idle state.
D5	Red	ERROR	An error has occurred during FPGA state machine execution.
D23	Green	DONE	The FPGA has been successfully configured.
D6-D21	Yellow	PROG 0-15	The corresponding program is selected

The FPGA state machine can be also controlled by an external digital device through the FPGA USER I/O connector (J7), see *Table 24* for the naming and pinout positioning of the

FPGA USER I/O connector. The REMOTE_ENABLE pin must be set high to enable remote control of the board.

The waveform program can be selected by setting the PROG<3:0> port. If an uninstalled program is selected, the ERROR output signal goes high. Alternatively, the idle state can be selected through the IDLE_SEL<1:0> port.

If remote control is enabled, the Program, Start and Stop push buttons are disabled.

A waveform program can be started via the REMOTE_START signal (active high), and stopped by setting the REMOTE_STOP signal high. Both the FPGA reset (SW5) and REMOTE_RESET signal can be used to reset the FPGA.

Some internal FPGA control signals can be inspected through the FPGA USER I/O connector (regardless of whether remote control is enabled or disabled). *Figure 4* and *Figure 5* show the expected behavior of these timing control signals.

Figure 4. FPGA timing control signals (beginning of cycle n)

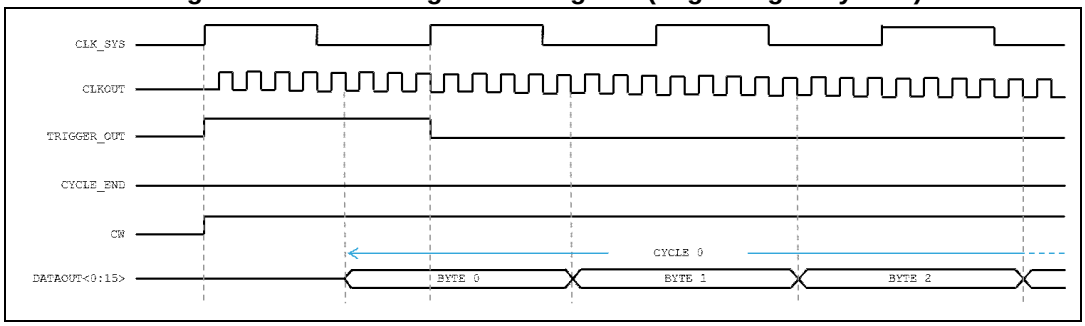
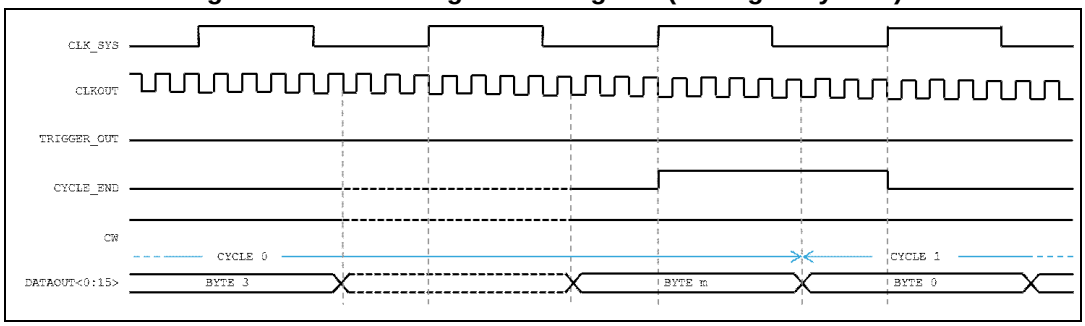


Figure 5. FPGA timing control signals (ending of cycle n)



3.4.1 Stored patterns

The STEVAL-IME009V1 can memorize up to 16 patterns in the on-board Flash memory to show the achievable performance for each pulser output. A default set of five selectable patterns are already stored in the Flash memory and ready to use.

A detailed description of the settled programs is listed below.

3.4.2 Pattern program 0

The first pattern stored in the SPI Flash is described in *Table 8*, where the output pulses are in phase. Its state sequence is indicated in *Table 9*. In order to appreciate the waveforms shown in *Figure 20* the following test conditions have been applied:

– HVP0 = HVP1 = + 80 V

– HVM0 = HVM1 = - 80 V
– Load: 300 pF // 100 Ω

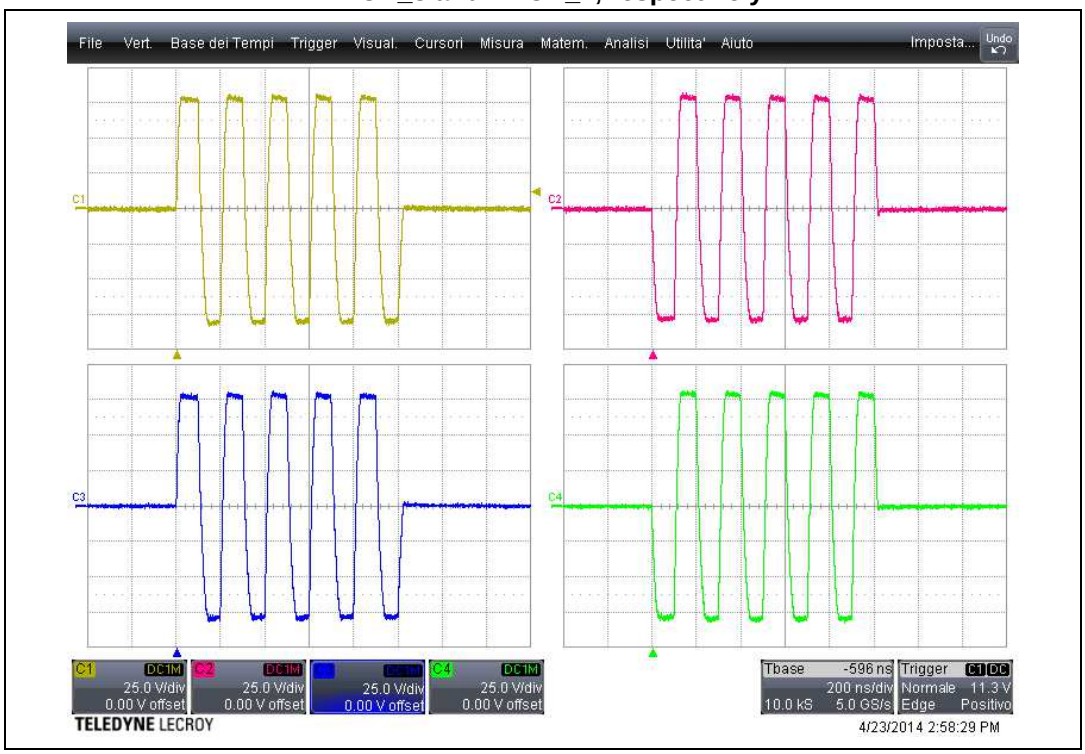
Table 8. Program “0”

	Mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PW	5	10	positive	300 µs	HV_TX
XDCR_2	PW	5	10	negative	300 µs	HV_TX
XDCR_3	PW	5	10	positive	300 µs	HV_TX
XDCR_4	PW	5	10	negative	300 µs	HV_TX
XDCR_5	PW	5	10	positive	300 µs	HV_TX
XDCR_6	PW	5	10	negative	300 µs	HV_TX
XDCR_7	PW	5	10	positive	300 µs	HV_TX
XDCR_8	PW	5	10	negative	300 µs	HV_TX

Table 9. State sequence Program “0”

XDCR_1, XDRC_3, XDCR_5, XDCR_7		XDCR_2, XDRC_4, XDCR_6, XDCR_8	
CLAMP	2 µs	CLAMP	2 µs
HVP	100 ns	HVM	100 ns
HVM	100 ns	HVP	100 ns
HVP	100 ns	HVM	100 ns
HVM	100 ns	HVP	100 ns
HVP	100 ns	HVM	100 ns
HVM	100 ns	HVP	100 ns
HVP	100 ns	HVM	100 ns
HVM	100 ns	HVP	100 ns
HVP	100 ns	HVM	100 ns
HVM	100 ns	HVP	100 ns
CLAMP	2 µs	CLAMP	2 µs
RX	295 µs	RX	295 µs

Figure 6. Acquisition by Program “0”, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4, respectively



3.4.3 Pattern Program 1

The second pattern stored in the SPI Flash is described in *Table 10*, where the output pulses are delayed by 10 ns each. Its state sequence is indicated in *Table 11*. In order to appreciate the waveforms shown in *Table 7* and *Table 8*, the following test conditions have been applied:

– HVP0 = + 80 V
– HVM0 = - 80 V
– Load: 300 pF // 100 Ω

Table 10. Program “1”

	Mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PW	5	10	positive	300 µs	HV_TX
XDCR_2	PW	5	10	negative	300 µs	HV_TX
XDCR_3	PW	5	10	positive	300 µs	HV_TX
XDCR_4	PW	5	10	negative	300 µs	HV_TX
XDCR_5	PW	5	10	positive	300 µs	HV_TX
XDCR_6	PW	5	10	negative	300 µs	HV_TX
XDCR_7	PW	5	10	positive	300 µs	HV_TX
XDCR_8	PW	5	10	negative	300 µs	HV_TX

Table 11. State sequence Program “1”

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
CLAMP	2 µs	CLAMP	2.01 µs	CLAMP	2.02 µs	CLAMP	2.03 µs
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	295 µs	RX	294.99 µs	RX	294.98 µs	RX	294.97 µs
XDCR_5		**XDCR_6**		**XDCR_7**		**XDCR_8**	
CLAMP	2.04 µs	CLAMP	2.05 µs	CLAMP	2.06 µs	CLAMP	2.07 µs
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	294.96 µs	RX	294.95 µs	RX	294.94 µs	RX	294.93 µs

Figure 7. Acquisition by Program “1”, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_7 and XDCR_8, respectively

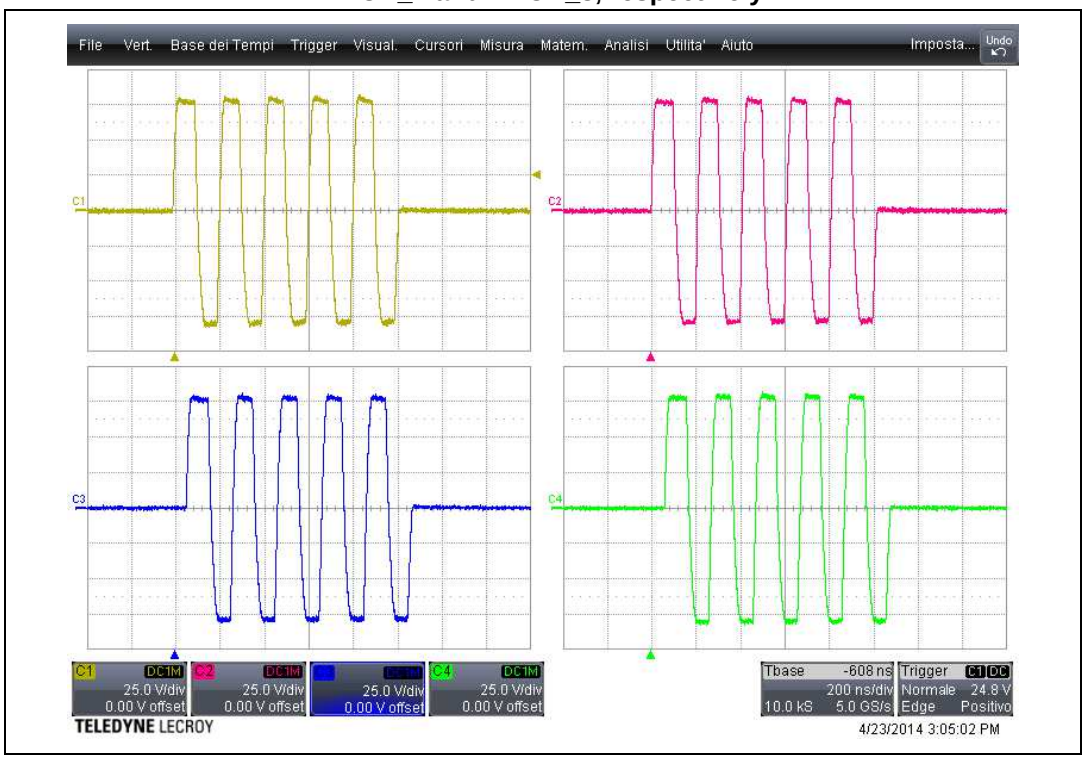
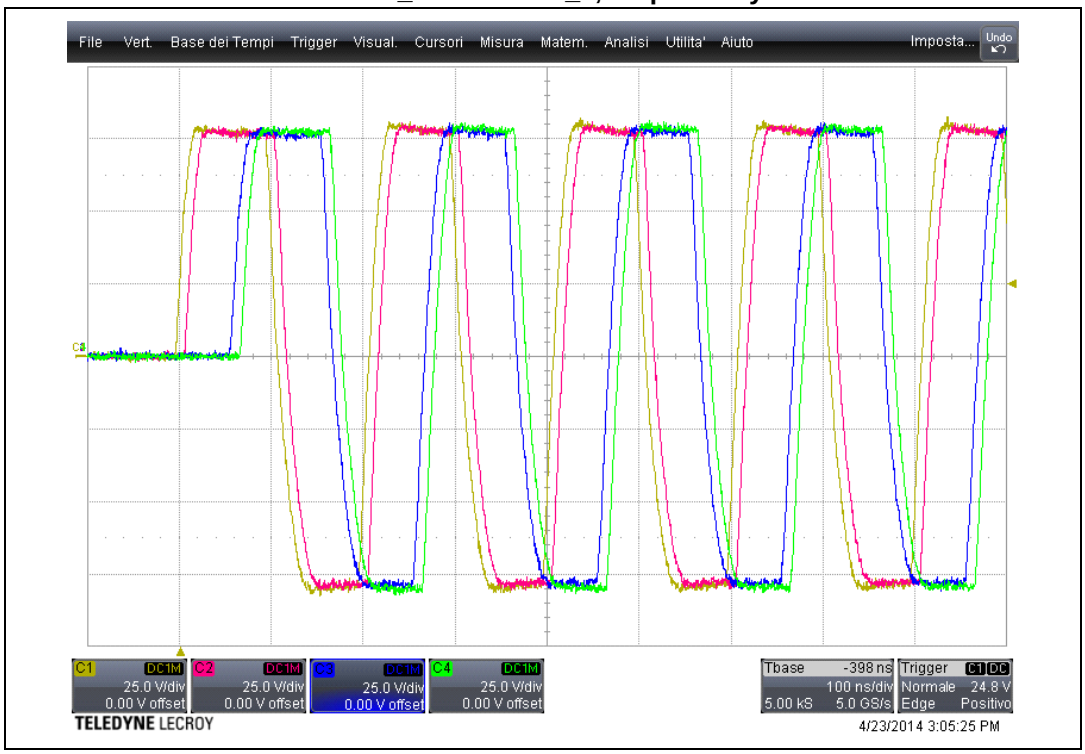


Figure 8. Acquisition by Program “1”, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_7 and XDCR_8, respectively



3.4.4 Pattern Program 2

The third pattern stored in the SPI Flash is described in *Table 12*, where the output pulses are in phase. Its state sequence is indicated in *Table 13*. In order to appreciate the waveforms shown in *Figure 9*, the following test conditions have been applied:

- HVP_CW = + 10 V
- HVM_CW = - 10 V
- Load: 300 pF // 100 Ω

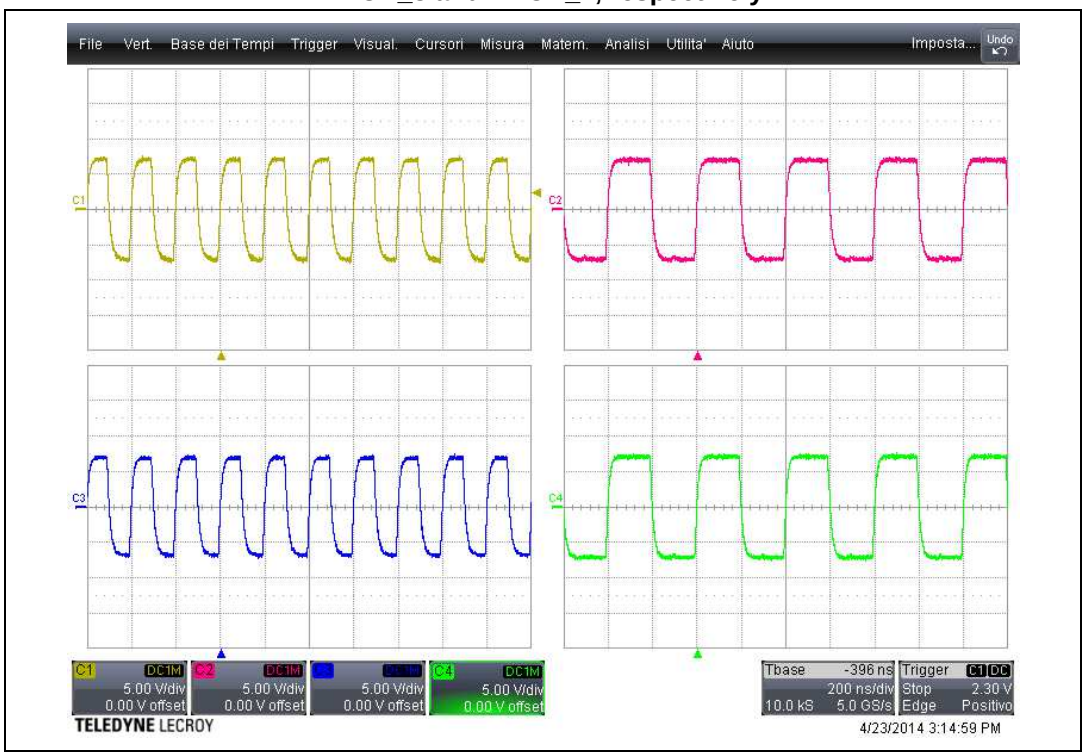
Table 12. Program “2”

	Mode	Frequency [MHz]	Number of pulses	Initial pulse	H-Bridge
XDCR_1	CW	5	continuous wave	positive	HV-CW
XDCR_2	CW	2.5	continuous wave	positive	HV-CW
XDCR_3	CW	5	continuous wave	positive	HV-CW
XDCR_4	CW	2.5	continuous wave	positive	HV-CW
XDCR_5	CW	5	continuous wave	positive	HV-CW
XDCR_6	CW	2.5	continuous wave	positive	HV-CW
XDCR_7	CW	5	continuous wave	positive	HV-CW
XDCR_8	CW	2.5	continuous wave	positive	HV-CW

Table 13. State sequence Program “2”

XDCR_1, XDRC_3, XDCR_5, XDCR_7		XDCR_2, XDRC_4, XDCR_6, XDCR_8	
HVP_CW	100 ns	HVP_CW	200 ns
HVM_CW	100 ns	HVM_CW	200 ns
HVP_CW	100 ns	HVP_CW	200 ns
HVM_CW	100 ns	HVM_CW	200 ns
HVP_CW	100 ns	HVP_CW	200 ns
HVM_CW	100 ns	HVM_CW	200 ns
HVP_CW	100 ns	HVP_CW	200 ns
HVM_CW	100 ns	HVM_CW	200 ns

Figure 9. Acquisition by Program “2”, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4, respectively



3.4.5 Pattern Program 3

The fourth pattern stored in the SPI Flash is described in *Table 14*, where the output pulses are in delayed by 10 ns each. Its state sequence is indicated in *Table 15*. In order to appreciate the waveforms shown in *Figure 10* and *Figure 11*, the following test conditions have been applied:

– HVP_CW = + 10 V
– HVM_CW = - 10 V
– Load: 300 pF // 100 Ω

Table 14. Program “3”

	Mode	Frequency [MHz]	Number of pulses	Initial pulse	H-Bridge
XDCR_1	CW	5	continuous wave	positive	HV-CW
XDCR_2	CW	5	continuous wave	positive	HV-CW
XDCR_3	CW	5	continuous wave	positive	HV-CW
XDCR_4	CW	5	continuous wave	positive	HV-CW
XDCR_5	CW	5	continuous wave	positive	HV-CW
XDCR_6	CW	5	continuous wave	positive	HV-CW
XDCR_7	CW	5	continuous wave	positive	HV-CW
XDCR_8	CW	5	continuous wave	positive	HV-CW

Table 15. State sequence Program “3”

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
HVP_CW	20 ns	HVP_CW	30 ns	HVP_CW	40 ns	HVP_CW	50 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	80 ns	HVP_CW	70 ns	HVP_CW	60 ns	HVP_CW	50 ns
XDCR_5		**XDCR_6**		**XDCR_7**		**XDCR_8**	
HVP_CW	60 ns	HVP_CW	70 ns	HVP_CW	80 ns	HVP_CW	90 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	100 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	100 ns
HVP_CW	40 ns	HVP_CW	30 ns	HVP_CW	20 ns	HVP_CW	10 ns

Figure 10. Acquisition by Program “3”, where C1, C2, C3 and C4 are XDCR_1, XDCR_3, XDCR_6 and XDCR_8, respectively

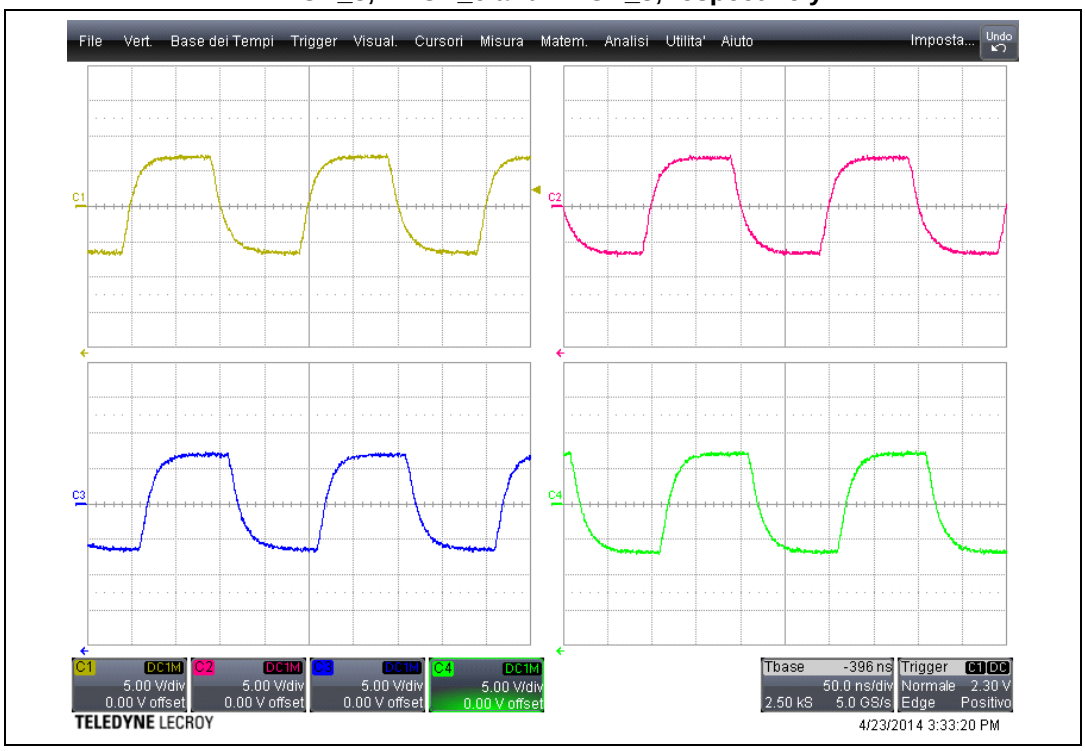
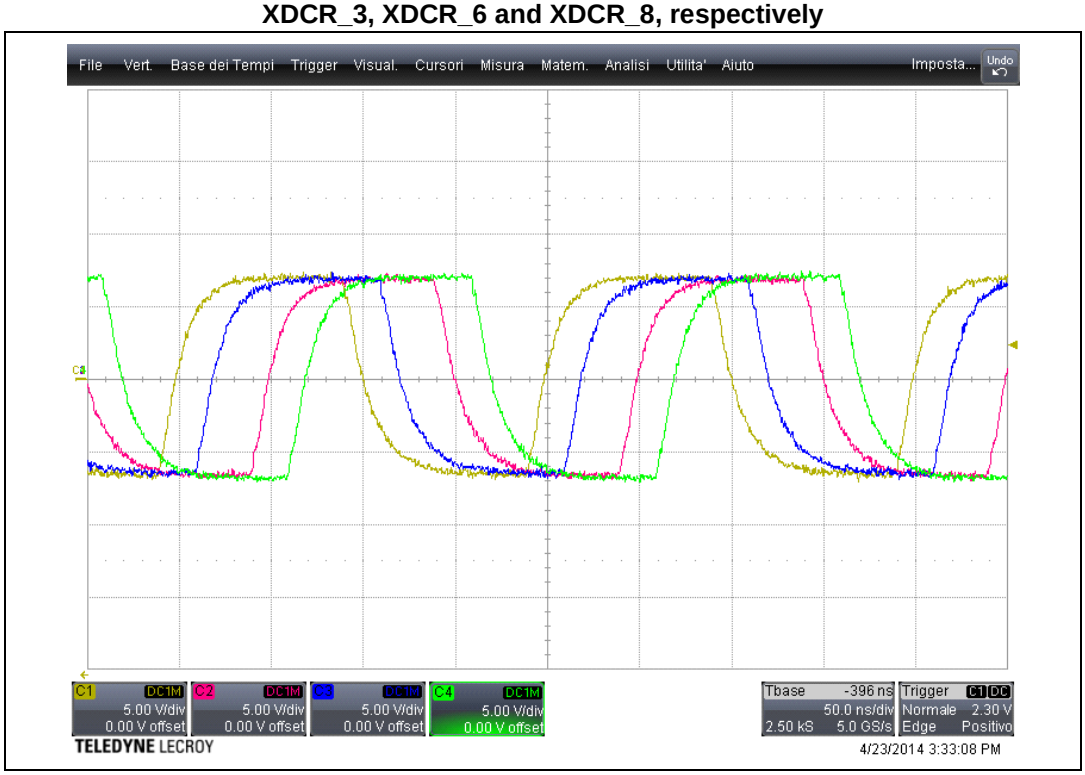


Figure 11. Acquisition by Program “3”, where C1, C2, C3 and C4 are XDCR_1, XDCR_3, XDCR_6 and XDCR_8, respectively



3.4.6 Pattern Program 4

The fifth pattern stored in the SPI Flash is described in *Table 16*, where the output pulses are in phase. Its state sequence is indicated in *Table 17*. In order to appreciate the waveforms shown in *Figure 12* and *Figure 13*, the following test conditions have been applied:

- HVP = +80 V
- HVM = -80 V
- Load: 300pF // 100 Ω

Table 16. Program "4"

	Mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PC	2.5	3	positive	300 µs	HV_TX
XDCR_2	PC	2.5	3	negative	300 µs	HV_TX
XDCR_3	PC	5	3	positive	300 µs	HV_TX
XDCR_4	PC	5	3	negative	300 µs	HV_TX
XDCR_5	PC	2.5	2	positive	300 µs	HV_TX
XDCR_6	PC	2.5	2	negative	300 µs	HV_TX
XDCR_7	PC	5	2	positive	300 µs	HV_TX
XDCR_8	PC	5	2	negative	300 µs	HV_TX

Table 17. State sequence Program "4"

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVM	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVP	100 ns
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVM	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	295.4 µs	RX	295.4 µs	RX	295.7 µs	RX	295.7 µs
XDCR_5		**XDCR_6**		**XDCR_7**		**XDCR_8**	
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVP	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVM	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	HVP	2 µs
RX	295.6 µs	RX	295.6 µs	RX	295.8 µs	HVM	295.8 µs

Figure 12. Acquisition by Program “4”, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4, respectively

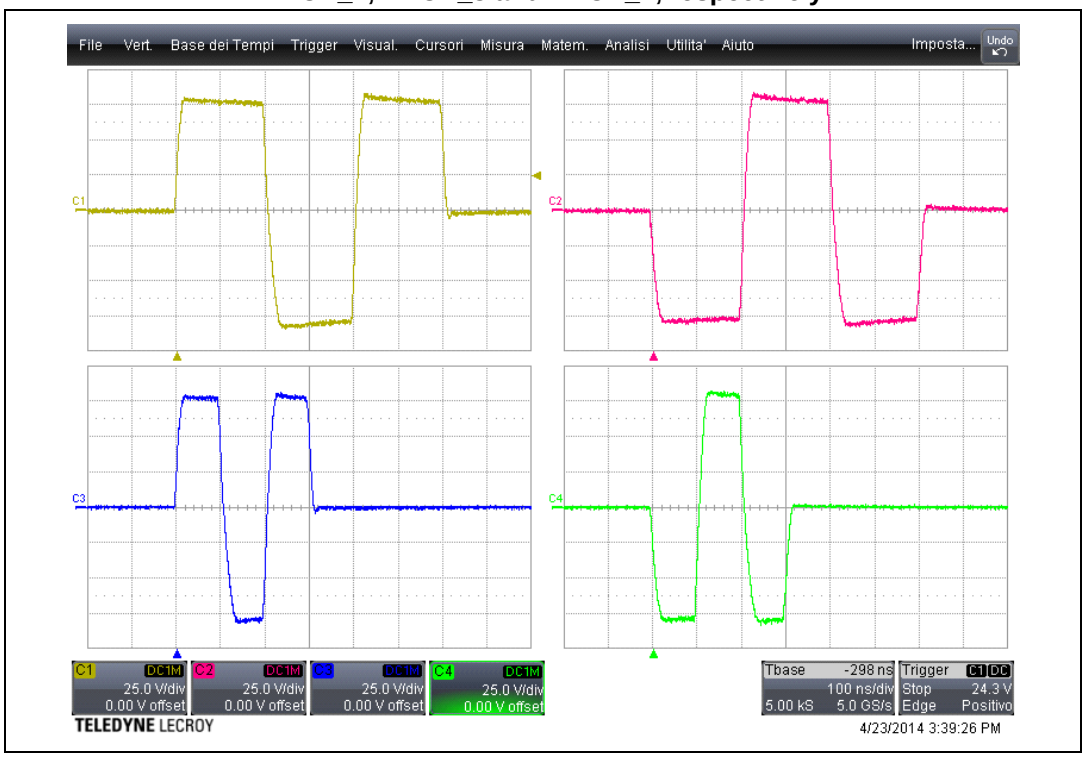
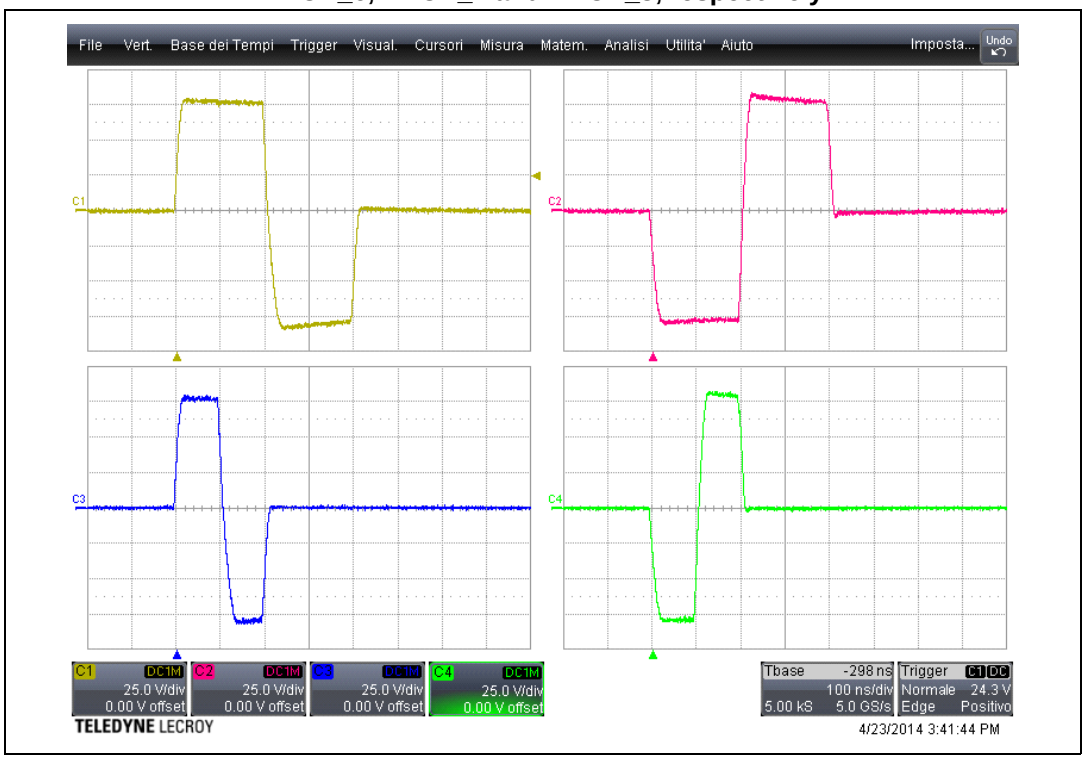


Figure 13. Acquisition by Program “4”, where C1, C2, C3 and C4 are XDCR_5, XDCR_6, XDCR_7 and XDCR_8, respectively



Further customized patterns based on test requirements for final applications can be uploaded by the user into the remaining memory slots (through the.dfu file - see user manual UM1083).

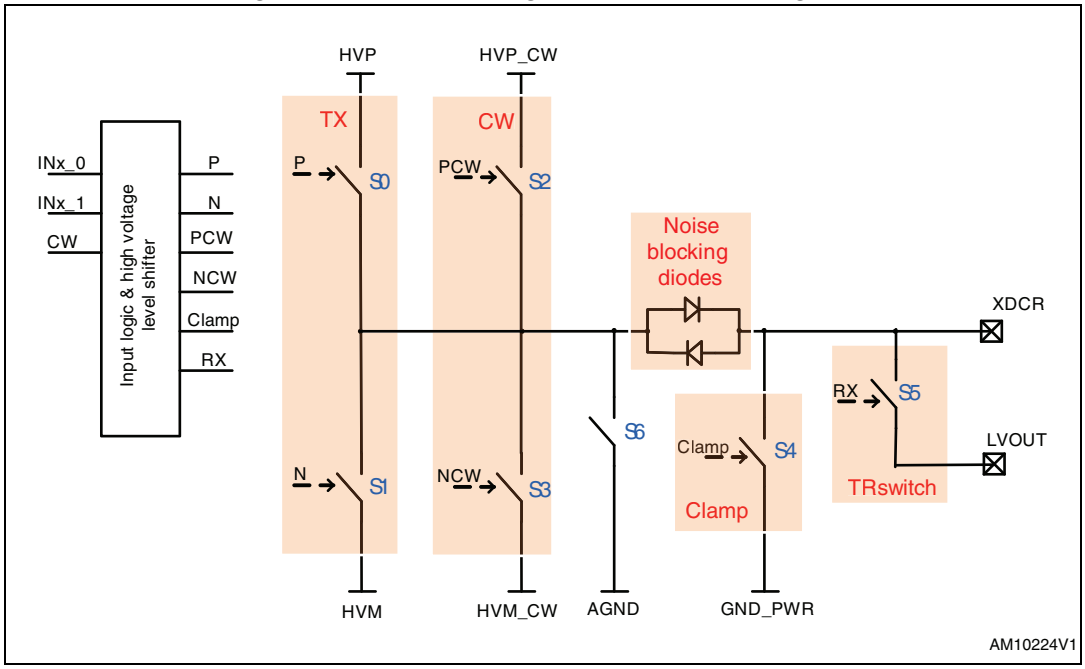
3.5 STHV800 stage

The STHV800 high-voltage, high-speed pulser generator features eight independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive or MEMS transducers.

The device contains a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes and high-power P-channel and N-channel MOSFETs as output stages for each channel. It also includes clamping-to-ground circuitry, anti-leakage, an anti-memory effect block, a thermal sensor and a HV receiver switch (HVR_SW) that ensures strong decoupling during the transmission phase.

The STHV800 also features self-biasing and thermal shutdown blocks (see *Figure 14*).

Figure 14. STHV800 single channel block diagram



Each channel can support up to three active output levels with one half-bridge. Each channel consists of two supplied output stages for pulsed wave (PW) and continuous wave (CW) operations. The PW output stage is able to provide up to ±2 A peak output current while, to reduce power dissipation and jitter during continuous wave mode, the fully optimized CW output stage delivers up to ±0.3 A.

Note: For further information, please refer to the STHV800 datasheet.

The STEVAL-IME009V1 allows the user to configure the special pins on the STHV800, see *Table 18*. A brief explanation of the use and functionality of these pins is given below:

- THSD is a thermal flag. The output stage of the THSD pin is a NMOS channel open-drain, so it is necessary to connect the external pull-up resistance ($R \geq 10\ k\Omega$) to the positive low-voltage supply (see *Figure 11*). If the internal temperature exceeds 160 °C, THSD

goes down and puts all the channels into the HZ state. By externally forcing THSD to a positive low-voltage supply, the thermal protection is disabled.

- EXPOSED-PAD is internally connected to the substrate. It is accessible on the bottom side of the board and it is floating. The user can connect a 100 V capacitance to ground in order to reduce noise during the receiving phase.

More information on the THSD pin is described in *Table 18*.

Table 18. STHV800 special pin configuration

Special pins on the PCB demo		
Name	**Description**	**Status on board**
THSD (pin 29)	Thermal shutdown pin	Active (J24 closed between 1 and 2 - forced to 3 V through R58 = 10 kΩ). The user can monitor the THSD status on TP3 (test point). Moreover the user can give the control to FPGA by shorting J24 between 2 and 3

The STHV800 output waveforms for each channel Ch 1/2/3/4/5/6/7/8 can be displayed directly using an oscilloscope by connecting the scope probe to the XDCR_x (with x= 1, … 8) BNC connectors.

The user can also select whether or not to connect the on board equivalent load, a 270 pF 200 V capacitor paralleled with a 100 Ω, 2 W resistor (through J19, J21, J20, J18, J27, J31, J28, J32 respectively for Channel 1, ... 8). A coaxial cable can also be used to easily connect the user transducer. Eight low voltage outputs are also available to receive the transduced echo signal arriving from the piezo-element through the TRswitch (see *Table 5*) on the low voltage output BNC (JlCh1, JlCh2, …).

Once the STHV800 performance is appreciated, users can make their own boards. The main issues to be wary of during the PCB design are the capacitance values to ensure good filtering and effective decoupling between the low voltage inputs and the HV switching signals. The best way to ensure this is through layer separation.

3.6 Operating supply conditions

Table 19. DC working supply conditions

Operating supply voltages					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
VDDP	Positive supply voltage	2.7	3	3.6	V
VDDM	Negative supply voltage	- 2.7	- 3	- 3.6	V
VDD	Positive logic voltage	1.6	3	3.6	V
HVP	TX high voltage positive supply			95	V
HVP_CW	CW high voltage positive supply			95	V
HVM	TX high voltage negative supply	- 95			V
HVM_CW	CW high voltage negative supply	- 95			V

Table 20. Current consumption in CW mode, @ 5 MHz, HVP/M_CW = ± 5 V, no-load

Operating supply voltages			
Symbol	**Parameter**	**Value**	**Unit**
IVDDP	Positive supply current	2	mA
IVDDM	Negative supply current	6	mA
IHVP1	TX1 high voltage positive supply current	14.5	mA
IHVM1	TX1 high voltage negative supply current	11	mA

4 Connectors

4.1 Power supply

The STEVAL-IME009V1 board has to be powered by J4, J1, J2 and J3 connectors as shown in the following figures.

Figure 15. Power supply connector J4

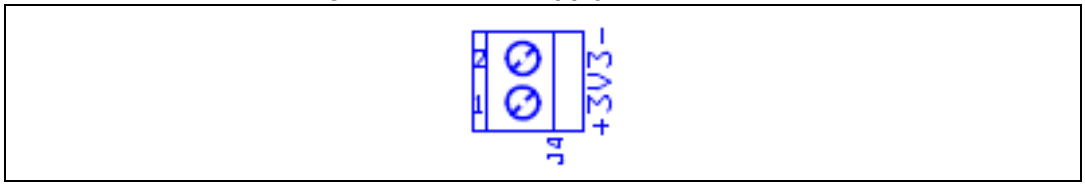


Figure 16. Power supply connector J1

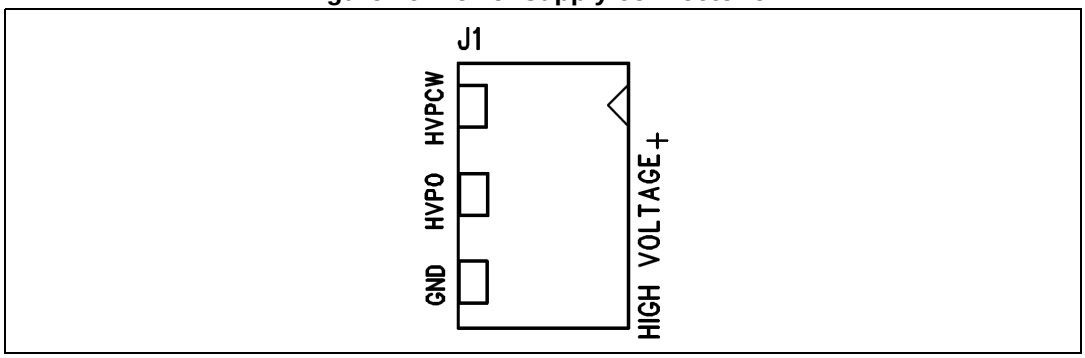


Figure 17. Power supply connector J2

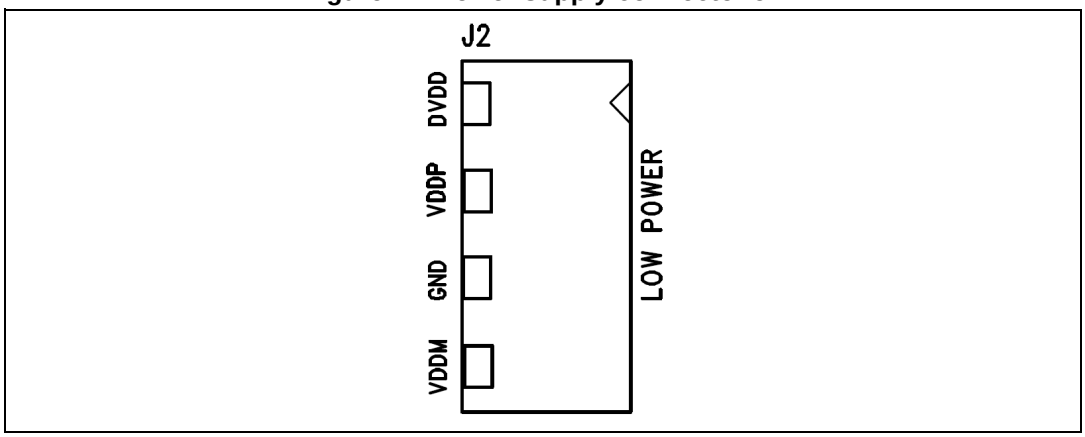
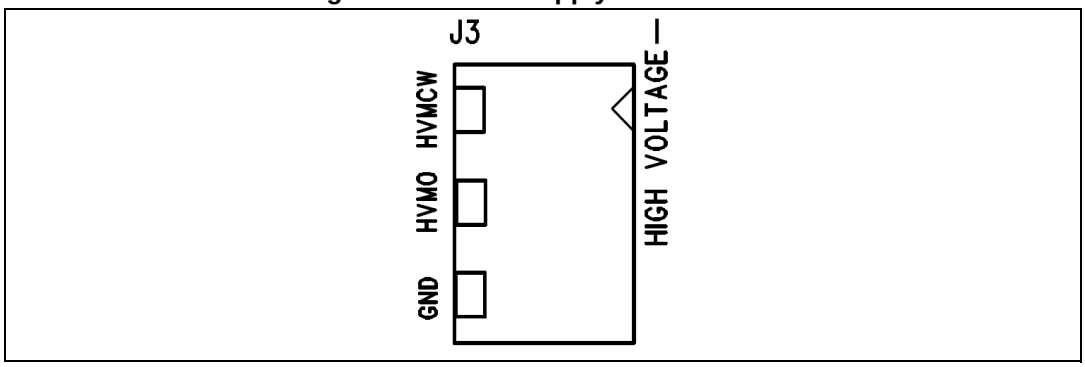


Figure 18. Power supply connector J3



4.2 Power-up sequence

The device is fully power-up/power-down sequence free, so there is no recommended sequence to follow in order to power up/down the STHV800. In any case, the relationships HVM_CW ≥ HVM and HVP_CW ≤ HVP must be respected during operation.

4.3 MCU

Figure 19. USB mini-B connector (CN1)

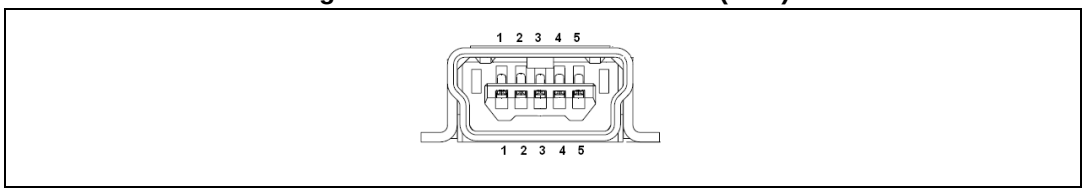


Table 21. USB mini-B connector pinout

Pin number	Description
1	Vbus (power)
2	DM (STM32 PA11)
3	DM (STM32 PA11)
4	N.C.
5	Ground

Figure 20. SWD (J40)

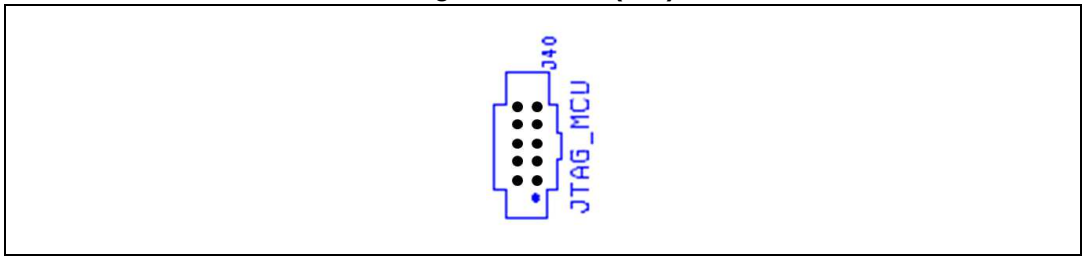


Table 22. JTAG/SWD connector pinout

Pin number	Description
1	MCU_3V3
2	JTMS
3	GND
4	JTCK
5	GND
6	JTDO
7	GND
8	JTDI
9	GND
10	RESET#

4.4 SPI Flash memory

Figure 21. Memory expansion connector (J10)

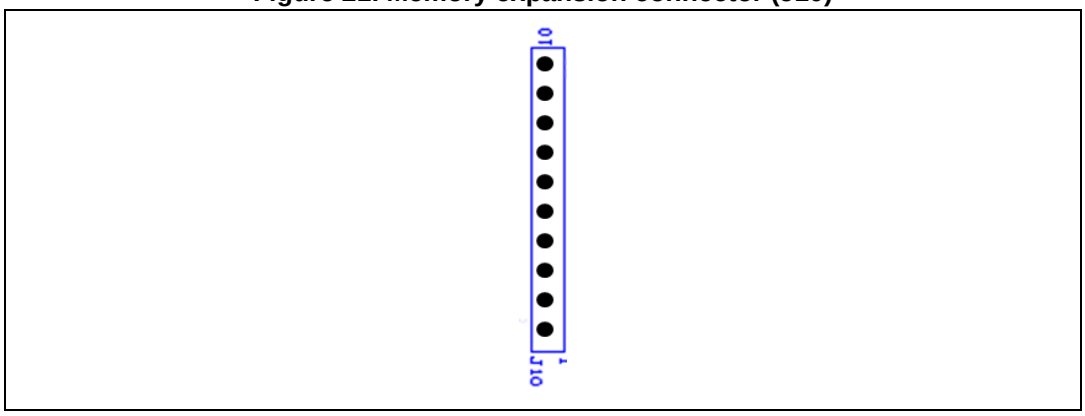


Table 23. Memory expansion connector pinout

Pin number	Description
1	MCU_FPGA_PROG (not used)
2	SPI MISO3
3	SPI MISO2
4	SPI CS
5	SPI MOSI
6	SPI MISO
7	SPI CLK
8	GND
9	3.3V
10	CHECK

Note: This memory is mutually exclusive with the on-board Flash memory, disconnect J38 before plugging an expansion memory over J10; relative LED (D29) turns on.

4.5 FPGA

FPGA USER I/O connector (J7) connector is used for debugging purposes; it allows the user to directly interface with FPGA I/Os.

Table 24. FPGA USER I/O connector pinout

Pin number	Description	Pin number	Description	Direction
1	GND	2	CW	OUTPUT
3	GND	4	TRIGGER_OUT	OUTPUT
5	GND	6	CLKOUT	OUTPUT
7	GND	8	CYCLE_END	OUTPUT
9	GND	10	THSD_EN	OUTPUT
11	GND	12	ERROR	OUTPUT
13	GND	14	PROG<0>	IN/OUT
15	GND	16	PROG<1>	IN/OUT
17	GND	18	PROG<2>	IN/OUT
19	GND	20	PROG<3>	IN/OUT
21	GND	22	IDLE_SEL<0>	IN/OUT
23	GND	24	IDLE_SEL<1>	IN/OUT
25	GND	26	REMOTE_ENABLE	INPUT
27	GND	28	REMOTE_START	INPUT
29	GND	30	REMOTE_STOP	INPUT
31	GND	32	REMOTE_RESET	INPUT

Table 25. FPGA PMOD connectors (J8) not mounted on the board

Pin number	Description	Pin number	Description
1	Not used	2	Not used
3	Not used	4	Not used
5	GND	6	3.3 V
7	Not used	8	Not used
9	Not used	10	Not used
11	GND	12	3.3 V

Table 26. FPGA PMOD connectors (J9) not mounted on the board

Pin number	Description	Pin number	Description
1	Not used	2	Not used
3	Not used	4	Not used
5	GND	6	3.3 V
7	Not used	8	Not used
9	Not used	10	Not used
11	GND	12	3.3 V

Two right-angle, 12-pin (2 x 6 female) Peripheral module (PMOD) headers (J8, J9) are interfaced with the FPGA, with each header providing 3.3 V power, ground and eight I/O's, see *Table 25* and *Table 26*. These headers may be utilized as general-purpose I/Os or may be used to interface to PMODs to enable additional user customization. J8 and J9 are placed in close proximity (0'9" - centers) on the PCB in order to support dual PMODs.

Table 27. FPGA JTAG connectors (J11) not mounted on the board

Pin number	Description	Pin number	Description
1	GND	2	3.3 V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	Not used
13	GND	14	Not used

The STEVAL-IME009V1 evaluation board supports the serial peripheral interface (SPI Flash) method of configuring the FPGA. The default configuration mode (determined by pull-up/pull-down resistors R17, R18, R21, and R22) is “Master Serial / SPI” mode, which allows the FPGA to be configured from the SPI Flash device. Spartan-6 devices have a dedicated four-wire JTAG port (always available to the FPGA regardless of the mode pin settings) that enables the Boundary-scan configuration method.

Configuring the FPGA via Boundary-scan requires a JTAG download cable to be attached to the 14-pin 2 mm spaced keyed header J11 (to be mounted) with a ribbon cable. Resistors RN1, R41 - R44 and diode D22 must also be mounted.

Jumper J13 is used to prevent FPGA programming from the configuration source. It must be open (default) to enable FPGA programming. LED D23, labeled “DONE” on the board, illuminates to indicate when the FPGA has been successfully configured.

5 Schematics

Figure 22. STEVAL-IME009V1- Part 1

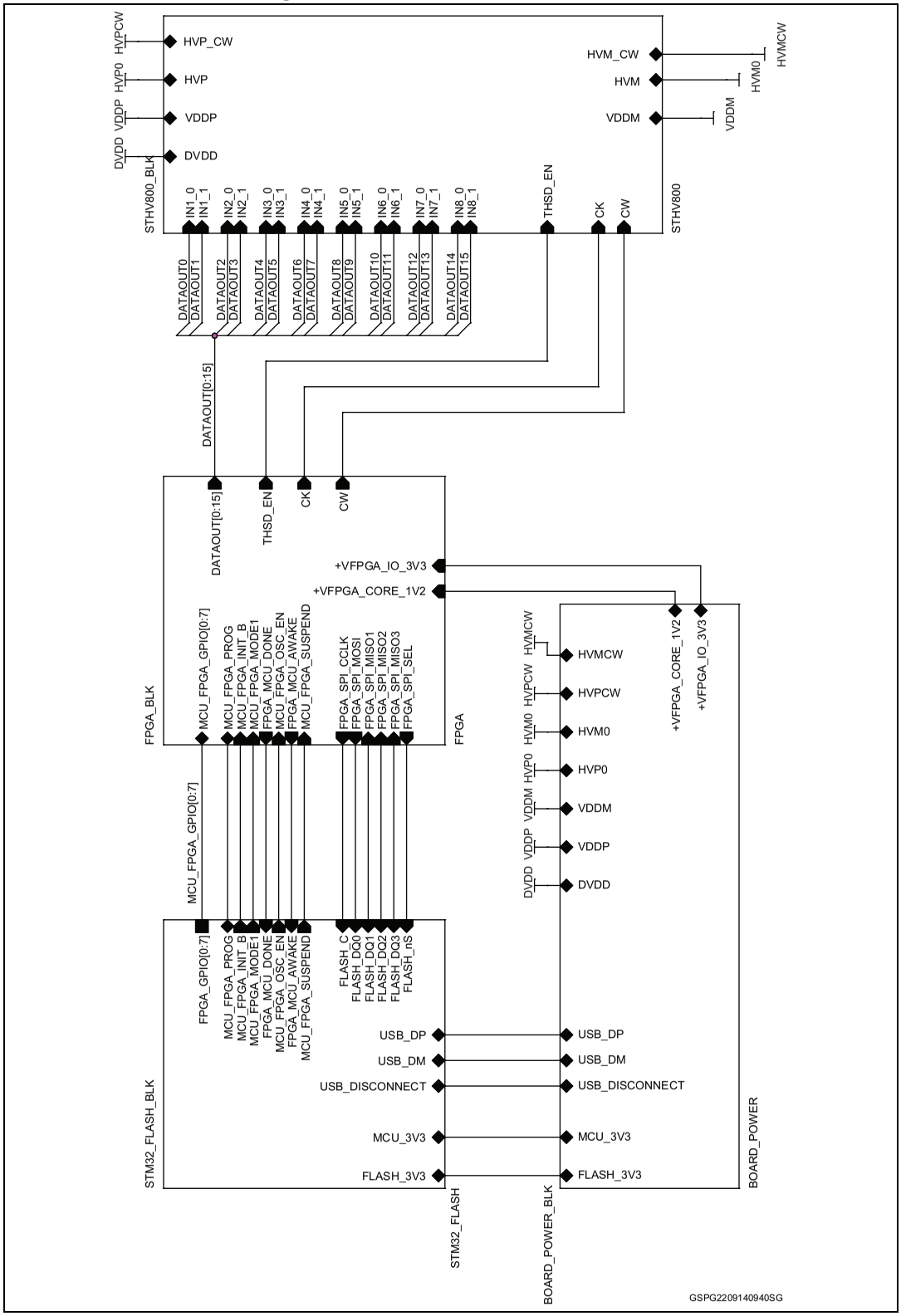


Figure 23. STEVAL-IME009V1- Part 2

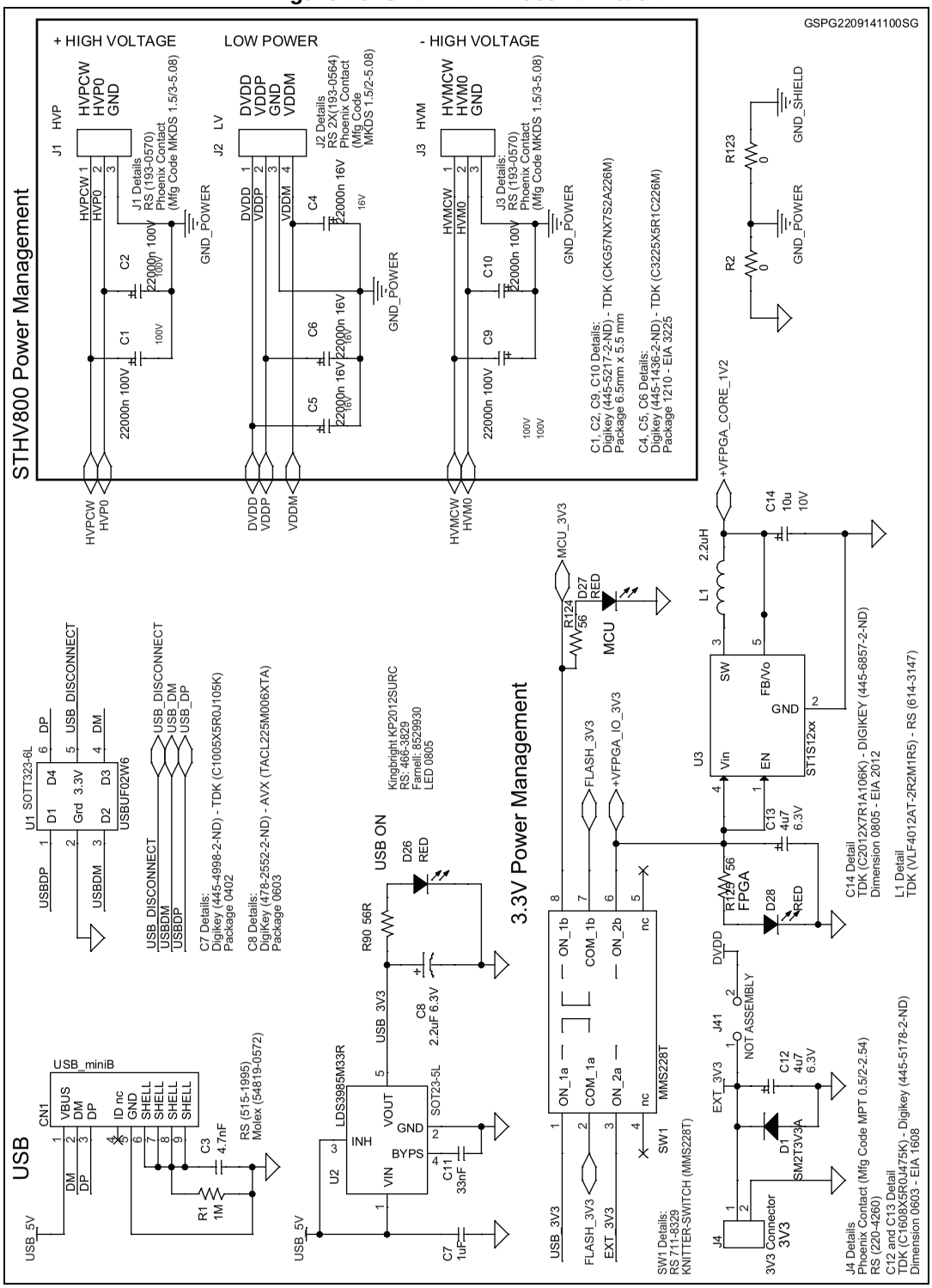


Figure 24. STEVAL-IME009V1- Part 3

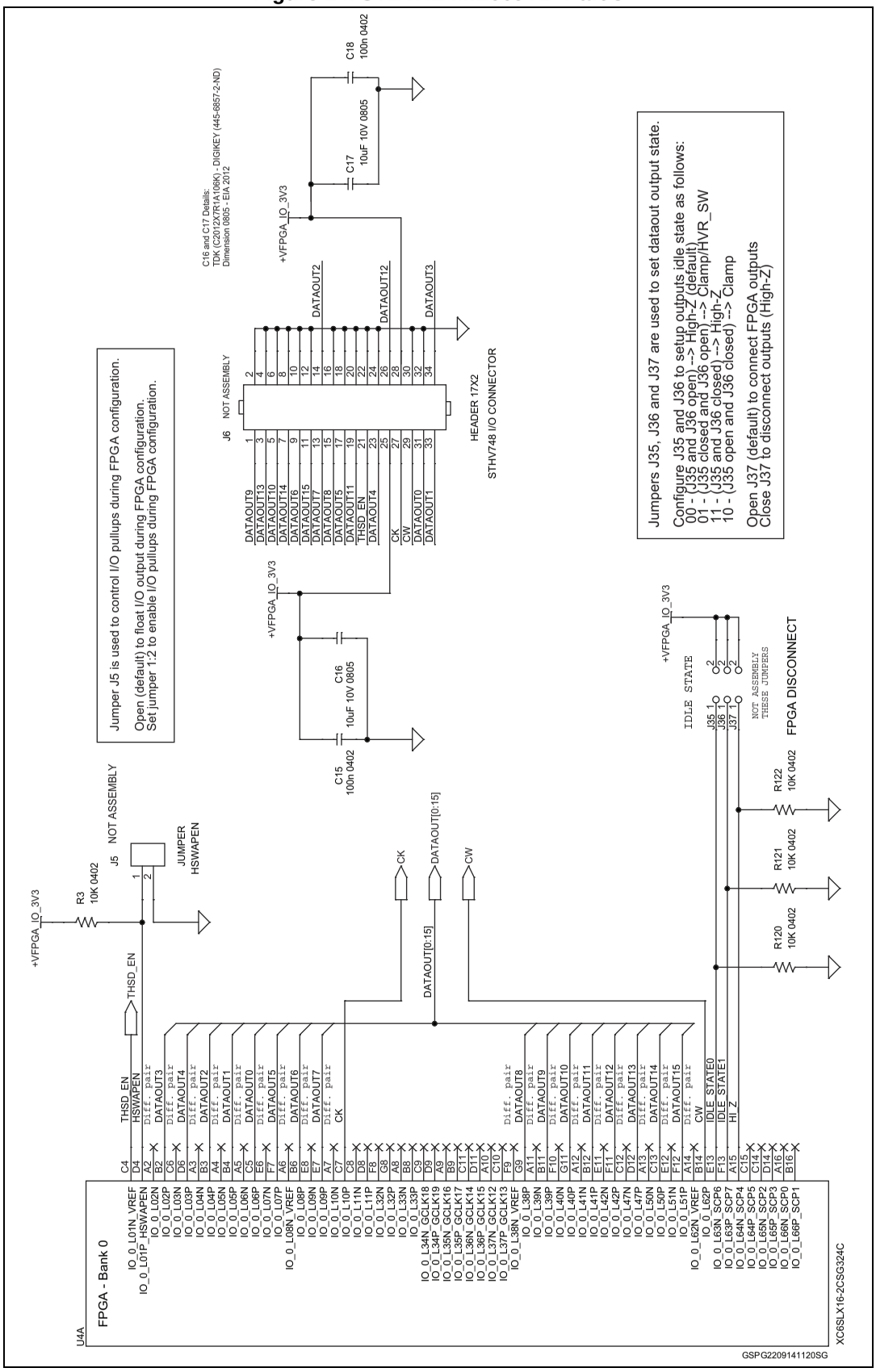


Figure 25. STEVAL-IME009V1- Part 4

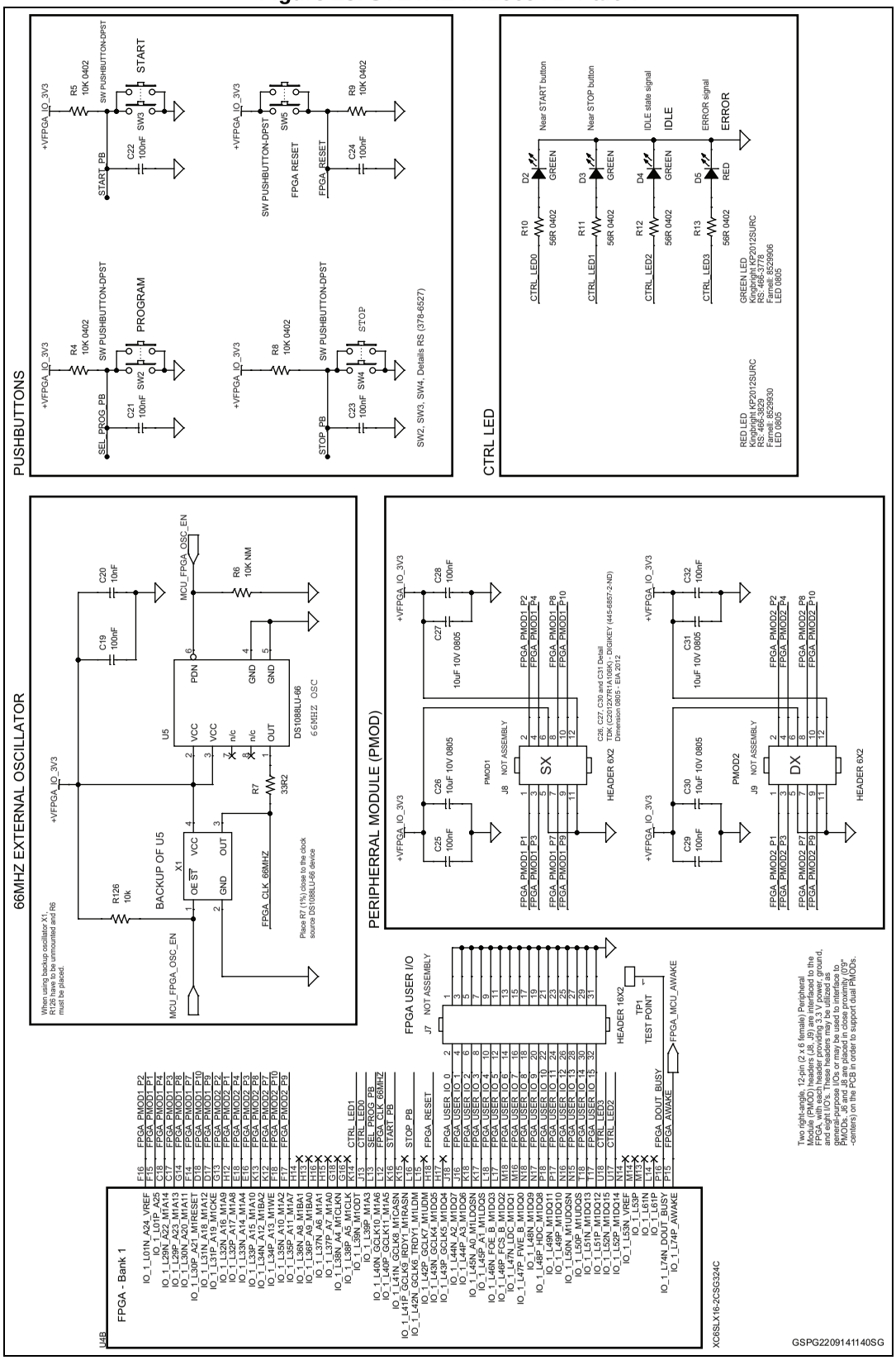


Figure 26. STEVAL-IME009V1- Part 5

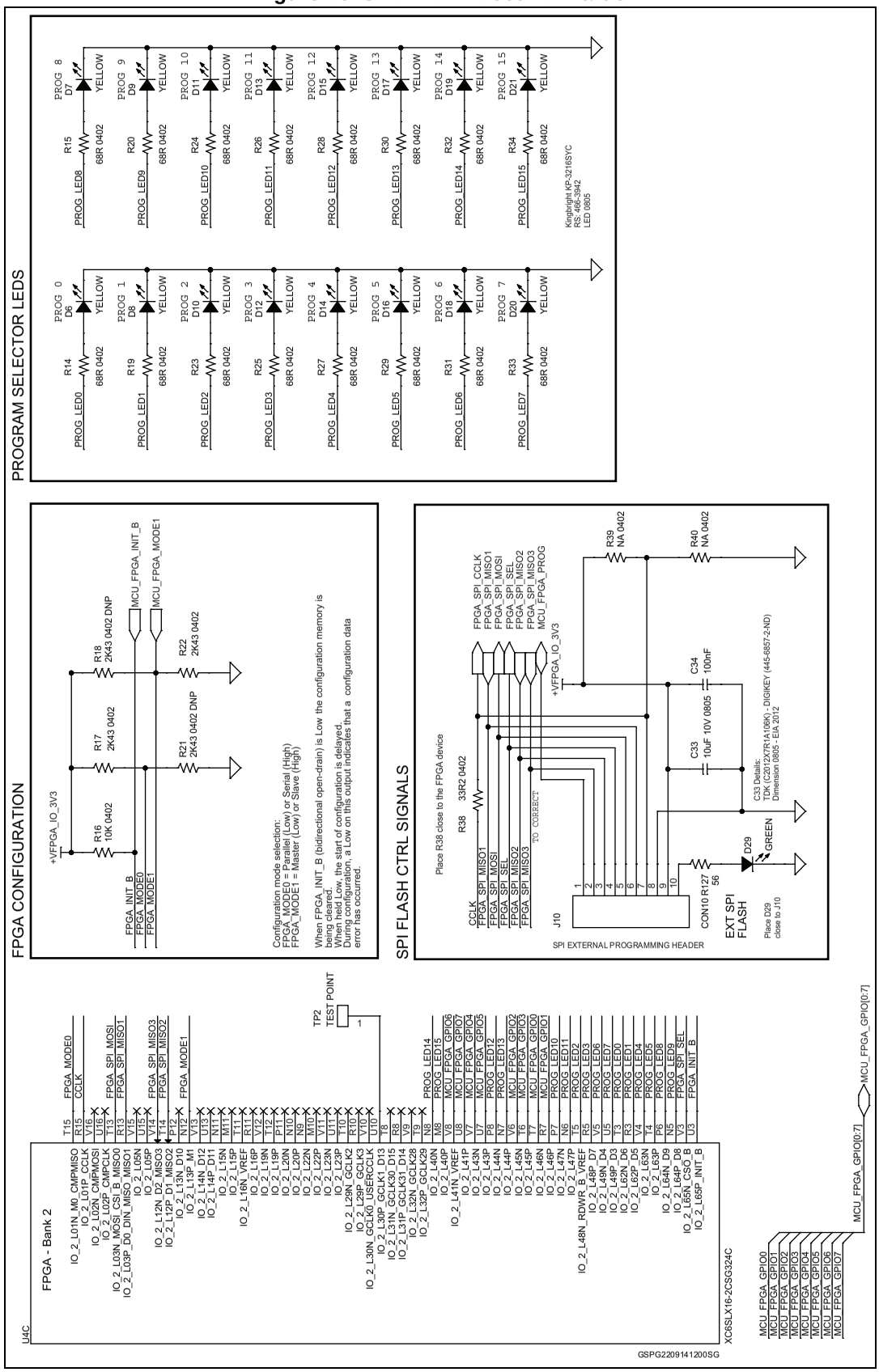


Figure 27. STEVAL-IME009V1- Part 6

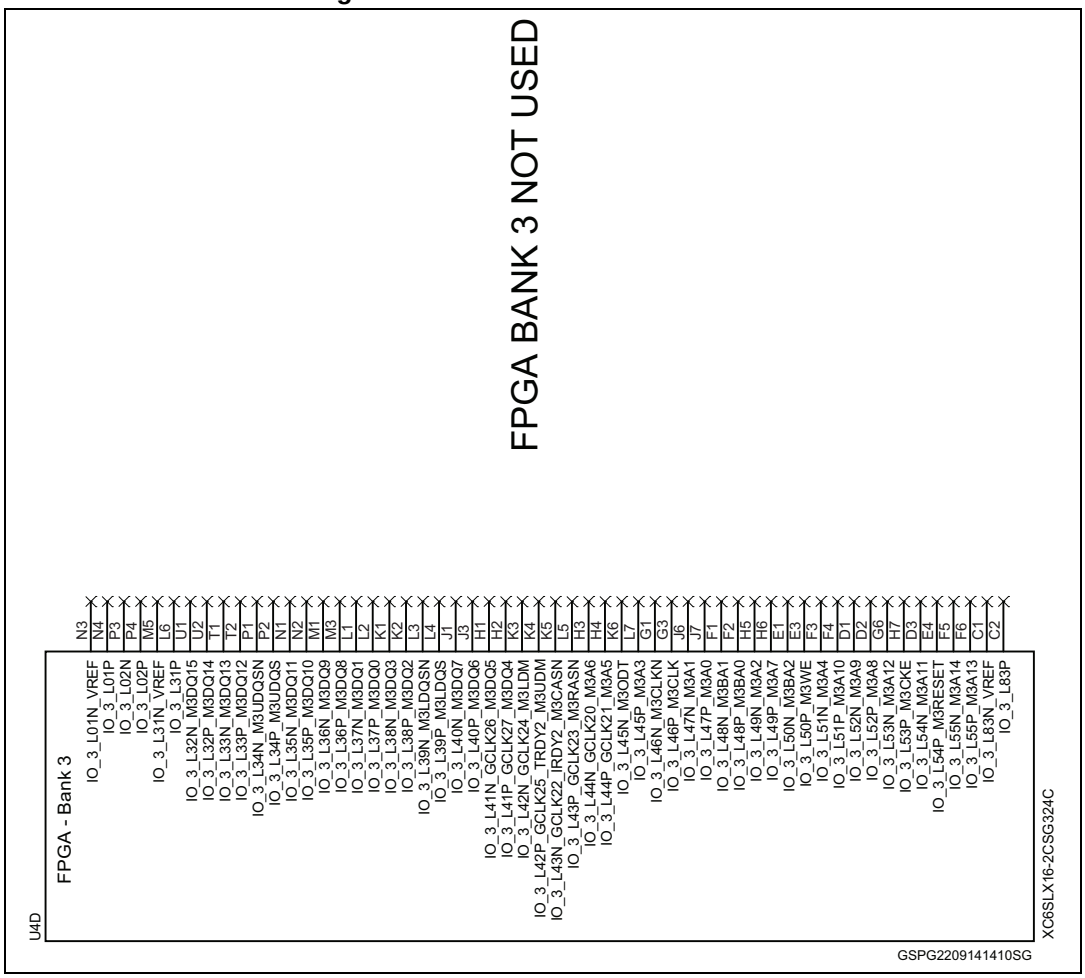


Figure 28. STEVAL-IME009V1- Part 7

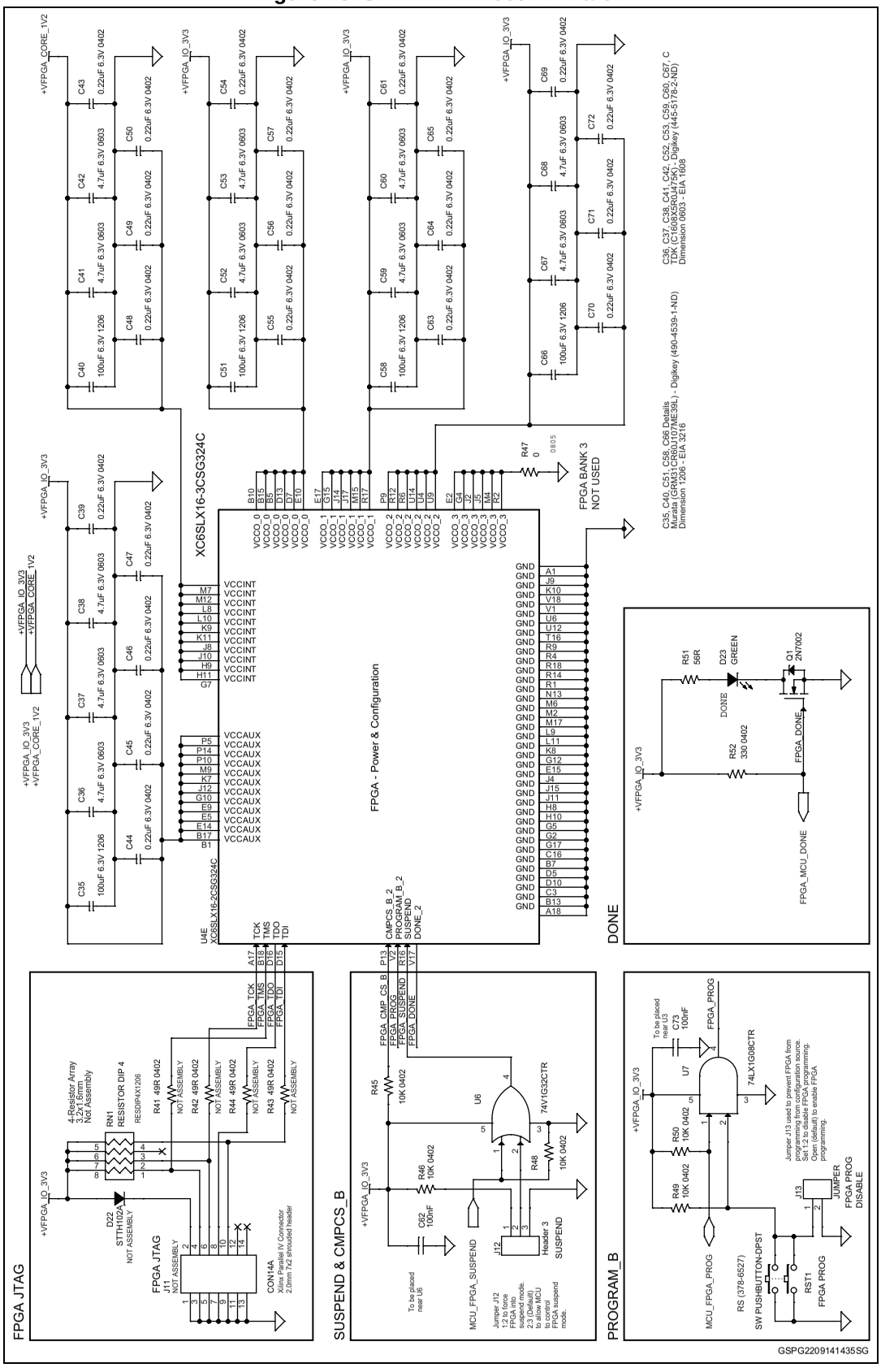


Figure 29. STEVAL-IME009V1- Part 8

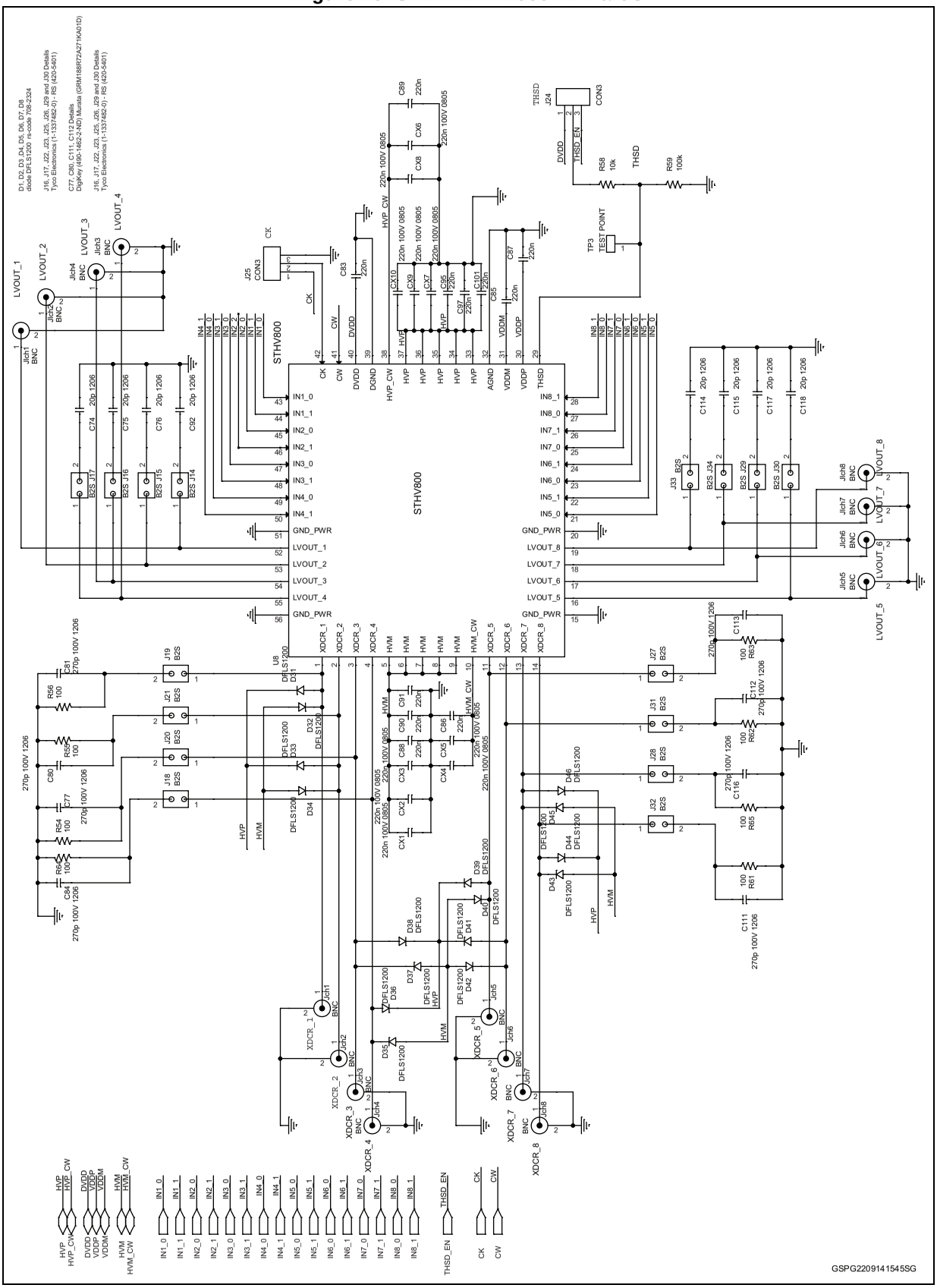
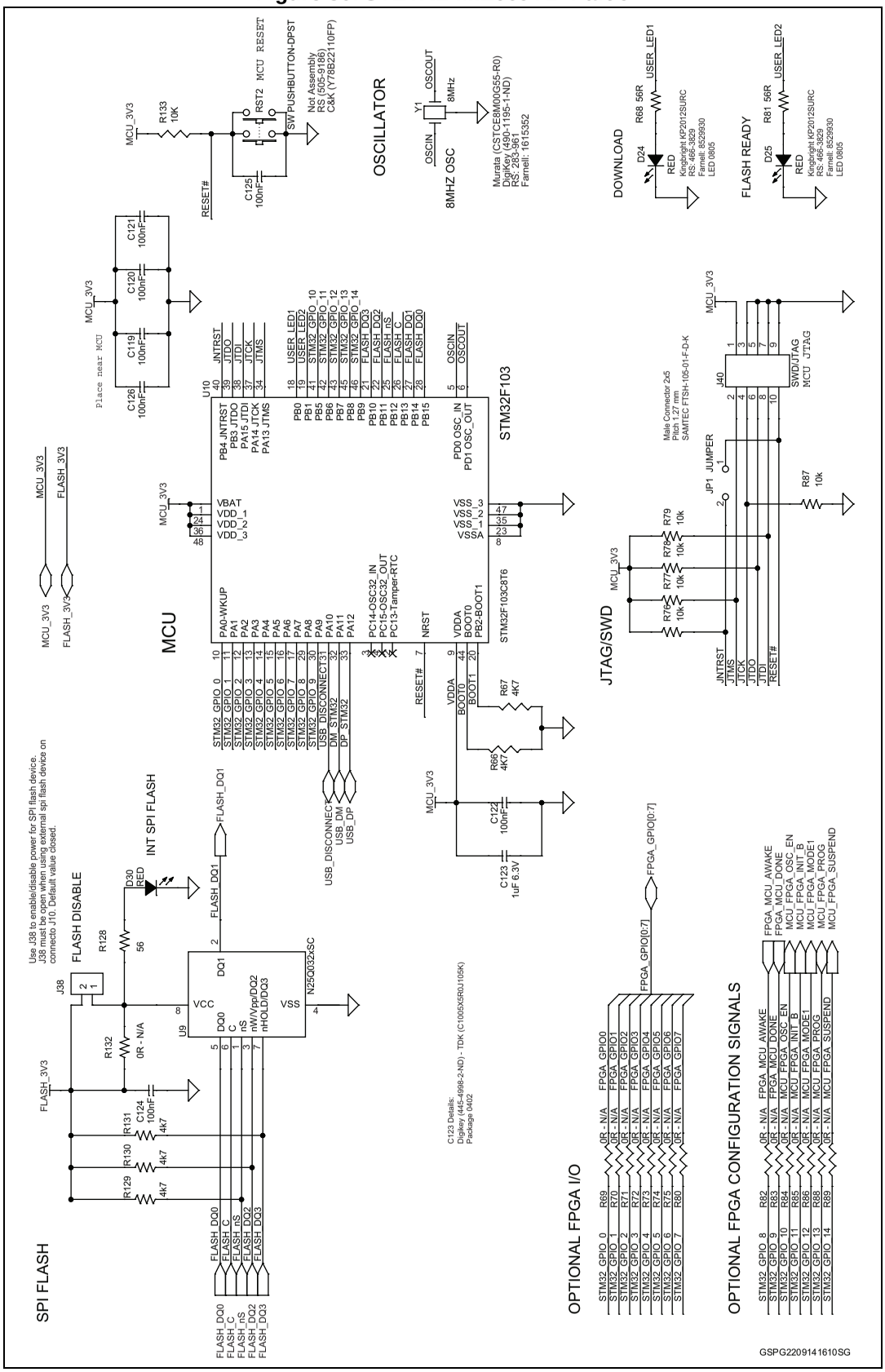


Figure 30. STEVAL-IME009V1- Part 9



6 Revision history

Table 28. Document revision history

Date	Revision	Changes
22-Oct-2014	1	Initial release.