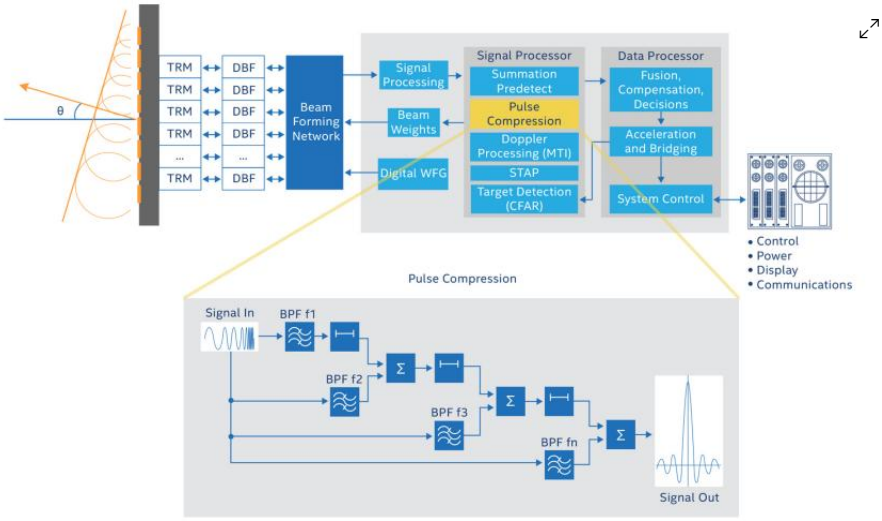
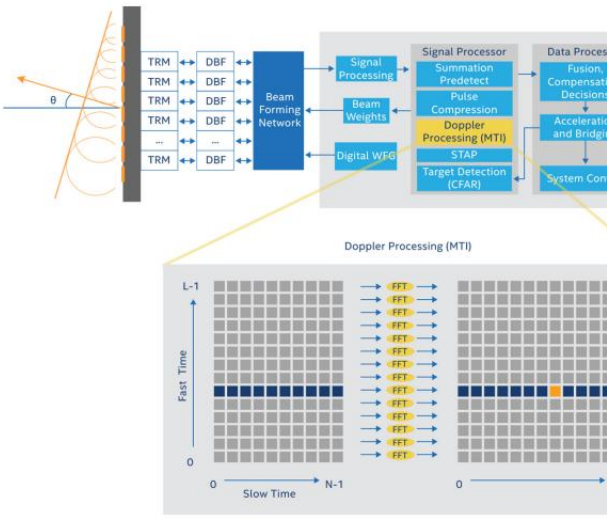
Military Applications

Radar and Sensors



Radar has been a foundational technology area in which the semiconductor industry has played a large role for the last two decades. In today's modern radar systems, Active Electronically Scanned Array (AESA) is the most popular architecture. Going forward, next-generation radar architectures such as digital phased array and synthetic aperture radar (SAR) with ground moving target indicator (GMTI) will be the emerging technology. To achieve this, parameters such as high-performance data processing, ultra-wide bandwidth, high dynamic range, and adaptive systems needed for diverse mission requirements are some of the most common challenges to system designers. An FPGA is an ideal, and in some cases necessary, solution in addressing these challenges. Using floating-point technology with Intel® Stratix® FPGA series and variable-precision digital signal processing (DSP) allows the designer to define the needed precision for each stage of the design. Logic and DSP resources are used efficiently while reducing power consumption.

In the AESA architecture shown in the figure below, one can easily identify several stages where an FPGA is necessary and where an FPGA provides a significant processing advantage.

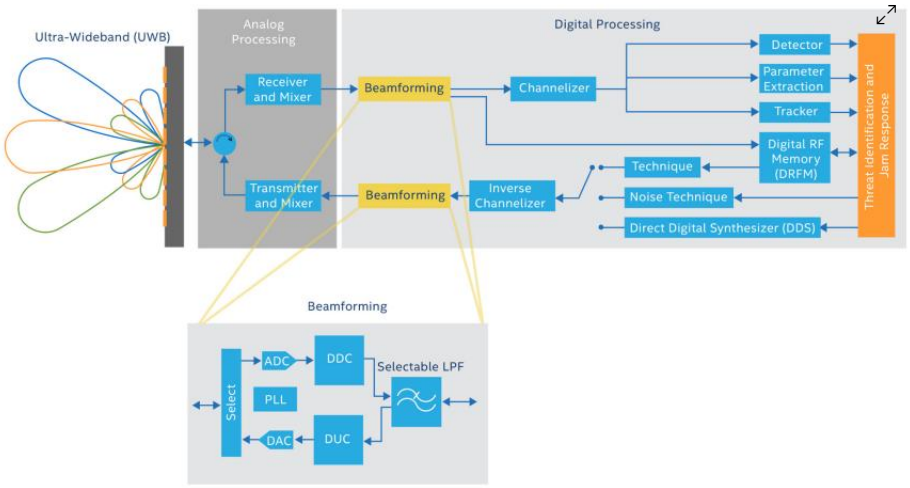


The 28 nm Stratix® V FPGAs address the unique design requirements of radar and advanced sensor technologies. With 825 Gbps full-duplex serial transceiver bandwidth, large DSP counts, excellent signal integrity, highly scalable embedded processing blocks, and logic density leadership up to 950K logic elements (LEs), Stratix® V FPGAs offer true system-on-chip (SoC) possibilities for military radar and sensor designs.

With next-generation Intel® Arria® 10 and Intel® Stratix® 10 devices, the large DSP counts will be supplemented with the addition of hard floating-point IEEE-754 single precision DSP blocks. This will allow up to 1.5 TeraFLOPs in Intel® Arria® 10 FPGAs and up to 10 TeraFLOPs in Intel® Stratix® 10 FPGAs. Designers can infer these blocks using the OpenCL™ flow, DSP Builder for Intel FPGAs, and other Intel FPGA intellectual property (IP) blocks.

To enable shorter development time, Intel complements our silicon solutions with IP cores, reference designs, development kits, and system-level design tools. For specific radar reference designs and radar application support, please contact us.

Electronic Warfare



In electronic warfare systems, key drivers for continuous enhancements are electronic counter-counter-measures (ECCM), stealth technologies, closely interlinked smart sensor networks, and intelligent guided weapons. These systems must be able to rapidly analyze and respond to multiple threats in very short time frames. In attempting to find target signatures in broadband noise, architects are seeking to perform complex processing such as fast Fourier transforms (FFTs), Cholesky decomposition, and matrix multiplication. Multiple software-generated waveforms are then transmitted to provide false targets, while powerful wideband signals provide overall cover. These shifting tactical responses require agile, high-performance processing. The entire system frequently resides in an airborne platform and must meet strict requirements for heat dissipation along with size, weight, power, and cost (SWaP-C) constraints.

A typical system design, uses a channelizer and inverse-channelizer to process high-bandwidth input signals. The number of channels are flexible so system designers can allocate hardware resources versus system performance as needed.

FPGAs offer an ideal solution to these performance requirements in the critical high-speed processing-intensive paths, a typical electronic warfare system with different electronic attack (EA) techniques.

Floating-Point Performance at Minimum Power

Electronic warfare designers can optimize digital signal processing (DSP) resources while still meeting SWaP-C constraints at the highest energy efficiency (GFLOPS/Watt) in any FPGA device across the industry. Using FPGA tools from Intel, DSP pipelines can be implemented quickly and optimized to up to 1.5 TFLOPS on Intel® Arria® 10 FPGAs and up to 10 TFLOPS on Intel® Stratix® 10 FPGAs.

Sensor and Backplane Interface

Stratix® V FPGAs have transceivers with speeds to 28 Gbps. A complete portfolio of transceivers is available to support a wide variety of backplane interfaces at minimum latency.

Shorter Time to Market and Less Engineering Risk

Intel has a complete set of intellectual property (IP) cores, reference designs, development kits, and system-level design tools. For specific electronic warfare reference designs and support, please contact us.

Secure Communication

Today's secure communications devices are faced with a number of design challenges. Wireline products must meet aggressive demands for data bandwidth to achieve 40-Gbps and 100-Gbps throughput, while often providing a tamper-resistant platform for cryptographic services for applications such as the JIE. Wireless products are developed under strict requirements for reduces size, weight, and power (SWaP) to enable next-generation mobility for military radios that can simultaneously support multiple waveforms such as SRW, WNW, and MUOS.

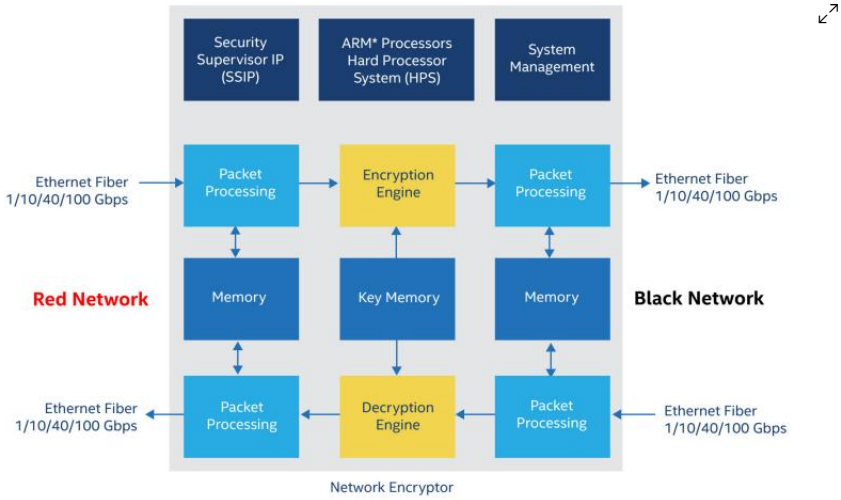
Secure Communications Systems

Secure communications design challenges apply to wired and wireless systems. Cryptographic functionality is an additional problem that is common to both systems.

Wireline Secure Communication

Information assurance systems with cryptographic capabilities including the Global Information Grid (GIG) support network performance in 40G to 100G and beyond. Net-centricity insures that what the warfighter sees on the ground can be linked to airborne and ground based assets.

Network Encryptor

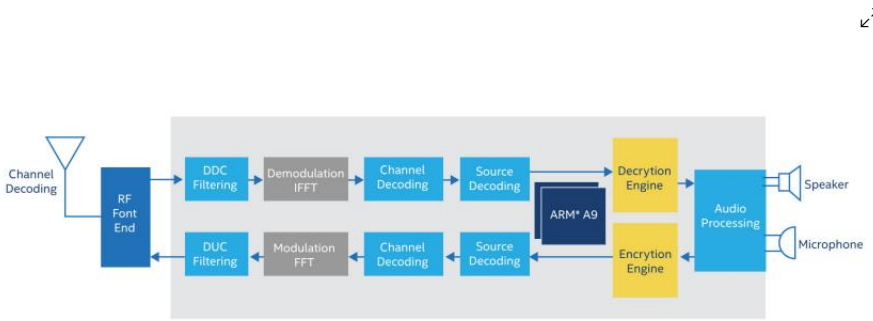


All the core functions of a typical network encryptor can be implemented in Intel FPGAs within the tamper boundary. The 28 nm Stratix® V FPGA provides up to 930 Gbps of transceiver bandwidth at the lowest power consumption with support for over 50 industry-standard protocols. Large DSP counts, scalable embedded processing, and logic density leadership offer true system-on-programmable-chip (SoPC) for wireline secure communications. The Intel® Arria® 10 SoC further reduces power, adds security features, and provides a dual-core ARM* Cortex*-A9 hard processor system for control plane processing.

Wireless Secure Communication

Enhanced wireless radios require interoperability and security using commercial, AES, Suite A, and Suite B encryption algorithms. These enhanced radios link firefighters, emergency, medical, and law enforcement systems together while optimizing size, weight, power and cost (SWaP-C). Next generation military-grade trusted communications and SDR platforms must generate compatible waveforms, assuring operational compatibility while at the same time supporting multiple platforms and missions with field update capability. Intel®FPGAs enable wireless communications systems to meet these challenges.

Software Defined Radio



Intel® Cyclone® V SoC meets the demands of the lowest system cost and power, and the Intel® Arria® V SoC balances cost and performance. Intel SoC FPGAs consolidate your overall footprint with embedded dual-core ARM* A9 cores featuring 2.5 MIPS of Dhrystone performance.

Cryptographic Capabilities

Strong encryption is key to ensuring communications and data security at ever increasing data throughput rates. Strong cryptographic algorithms implemented on FPGAs that are secure by design provide the foundation for trusted information assurance systems.

The Cyclone III LS FPGA with design separation capability enables high security at low power. Information assurance platforms benefit from the low-cost, low-power Cyclone® V FPGA, while data rates of 100 Gbps and beyond can be achieved with the Stratix® V and Intel® Arria® 10 FPGAs.

Military Temperature

To meet today's market demands, Intel offers the following devices qualified to operate at military temperatures:

- FPGAs
  - Intel® Arria® 10 10AX660, 10AX570, 10AX480, 10AS480, 10AX220, 10AX160 military-grade -3 speed-grade devices in selected packages.
  - Stratix® V 5SGXA7, 5SGSD5 military-grade -4 speed-grade devices in selected packages.
  - Stratix® IV EP4SGX70, EP4SGX110, EP4SGX180, EP4SGX230, and EP4SE230 military-grade -3 speed-grade devices in selected packages.
  - Stratix® III EP3SL50, EP3SE50, EP3SL70, EP3SE80, EP3SL110, EP3SE110, and EP3SL150 industrial-grade -3 speed-grade devices in all packages.

The table below lists the temperature ranges for these devices.

Temperature Ranges

Altera Device	Extended	Industrial	Military	Temperature
Intel® Arria® 10 FPGA/SoC	0°C to 100°C	-40°C to 100°C	-55°C to 125°C	Junction
Intel®Stratix®10 FPGA/SoC	0°C to 100°C	-40°C to 100°C<	-55°C to 125°C	Junction
Altera Device	**Commercial**	**Industrial**	**Military**	**Temperature**
Stratix® V FPGA	0°C to 85°C	-40°C to 100°C	-55°C to 125°C	Junction
Stratix® IV FPGA	0°C to 85°C	-40°C to 100°C	-55°C to 125°C	Junction
Stratix® III FPGA	0°C to 85°C	-40°C to 100°C	-55°C to 125°C	Junction

Altera Device	Extended	Industrial	Military	Temperature
Stratix® II FPGA	0°C to 85°C	-40°C to 100°C	-55°C to 125°C	Junction
Intel® Stratix® FPGA	0°C to 85°C	-40°C to 100°C	-55°C to 125°C	Junction

Intel characterizes current industrial devices when operating over the military temperature range. These devices operate within specification, but run to a reduced speed grade timing model. For details about designing with and using these devices, refer to the related documentation indicated in the tables below.

For additional details regarding Intel's military temperature offerings, contact your local sales office or distributor.

Product Families Supported

The table below lists the military temperature offerings for Arria 10 FPGAs and SoCs.

Arria 10 FPGA/SoC Military Temperature Offerings

Notes: All packages support military temperatures.

Device	Package	Ordering Part Number	Operational Speed Grade	Availability
10AX016C	U484	Coming Soon	-3	2016
10AX016E	F760	Coming Soon	-3	2016
10AX022C	U484	Coming Soon	-3	2016
10AX022E	F760	Coming Soon	-3	2016
10AX048E	F760	Coming Soon	-3	2016
10AS048E	F760	Coming Soon	-3	2016
10AX048K	F1152	Coming Soon	-3	2016
10AS048K	F1152	Coming Soon	-3	2016
10AX057K	F1152	Coming Soon	-3	2016
10AX066K	F1152	Coming Soon	-3	2016
10AX057K	F1517	Coming Soon	-3	2016
10AX066K	F1517	Coming Soon	-3	2016

Stratix V FPGA Military Temperature Offerings

Notes: For details, refer to the Stratix V Military Temperature Range Support Technical Brief (PDF).

Stratix V Military Temperature Range Support Technical Brief

Device	Package	Ordering Part Number	Operational Speed Grade	Availability
5SGSD5H	All	Coming Soon	-4	2015
5SGSD5K	All	Coming Soon	-4	2015
5SGXA7H	All	Coming Soon	-4	2015
5SGXA7K	All	Coming Soon	-4	2015

Stratix IV FPGA Military Temperature Offerings

Notes: For details, refer to the Stratix IV Military Temperature Range Support Technical Brief (PDF).

Stratix IV Military Temperature Range Support Technical Brief

Device	Package	Ordering Part Number	Operational Speed Grade	Availability
EP4SGX70D	F780	EP4SGX70DF29M3	-3	Now
EP4SGX70H	F1152	EP4SGX70HF35M3	-3	Now
EP4SGX110D	F780	EP4SGX110DF29M3	-3	Now
EP4SGX110H	F1152	EP4SGX110HF35M3	-3	Now
EP4SGX180D	F780	EP4SGX180DF29M3	-3	Now
EP4SGX180H	F1152	EP4SGX180HF35M3	-3	Now
EP4SGX180K	F1517	EP4SGX180KF40M3	-3	Now
EP4SGX230D	F780	EP4SGX230DF29M3	-3	Now
EP4SGX230H	F1152	EP4SGX230HF35M3	-3	Now
EP4SGX230K	F1517	EP4SGX230KF40M3	-3	Now
EP4SE230	F780	EP4SE230F29M3	-3	Now

Stratix III FPGA Military Temperature Offerings

Notes: For details, refer to the Stratix III Military Temperature Range Support Technical Brief (PDF).
All packages support military temperatures.

Stratix III Military Temperature Range Support Technical Brief

Device	Package	Ordering Part Number	Operational Speed Grade	Availability
EP3SL50	All	EP3SL50xxxI3	-4	Now
EP3SE50	All	EP3SE50FxxxI3	-4	Now
EP3SL70	All	EP3SL70FxxxI3	-4	Now
EP3SE80	All	EP3SE80FxxxI3	-4	Now
EP3SL110	All	EP3SL110FxxxI3	-4	Now
EP3SE110	All	EP3SE110FxxxI3	-4	Now
EP3SL150	All	EP3SL150FxxxI3	-4	Now

For additional details regarding Altera's military temperature offerings and characterization report, contact your local sales office or distributor.

Ecosystem

Intel works closely with commercial off-the-shelf (COTS) board partners to assure that customers can easily deploy the latest validated intellectual property (IP) onto proven production boards to lower system design and schedule risk when implementing complex high-performance systems. We can help with board and mezzanine-card selection to meet specific needs, device-type requirements, and design-time constraints. Our COTS partner ecosystems encompass development software for hardware and FPGA interfaces that utilize advanced application programming interfaces (APIs) and high-level languages. Our COTS partner ecosystems use Intel® Quartus® Prime Software along with DSP Builder for Intel® FPGAs (Advanced Blockset) for board design implementation as well as proprietary Intel and third-party software.

Intel's military COTS board partners include:

Military COTS Board Partners

Partner	Description
Annapolis Micro Systems	Annapolis is a world leader in FPGA-based COTS boards, targeting high I/O bandwidth computationally intensive problems, such as radar, SIGINT, digital signal processing, encryption, and image processing, with exceptional application development support. Annapolis has COTS hardware and software solutions for OpenVPX, VME/VXS, PCIe*, and AMC and the highest density, largest selection of interface cards: A/Ds, D/As, Ethernet/Infiniband. The12.5Gb and 14Gb transceivers and the 10Gb, 40Gb and 100Gb IP on Stratix® V devices help to lay the foundation for our WILD OpenVPX Ecosystem, with chassis, special high-speed backplanes, FPGA-based processing boards, switch solutions, and storage cards. For more information, visit www.annapmicro.com .
BittWare	BittWare designs and deploys high-end signal processing board-level solutions that significantly reduce technology risk and time-to revenue for its OEM customers. BittWare's solutions leverage the latest FPGA technology from Intel and the Anemone FPGA co-processing chip, which reduces FPGA power and complexity by hosting C language aspects of a signal processing application. Products are based on industry standard COTS form factors including PCIe*, AMC, VPX / OpenVPX, VME / VXS, CompactPCI, PCI*, XMC, FMC (VITA 57), and PMC. When power and space-constrained challenges make it difficult to use industry-standard boards, BittWare can provide modified solutions, licensed designs, and/or chip-level products. For more info on BittWare's FPGA solutions, visit www.bittware.com .
Colorado Engineering Inc. (CEI)	CEI offers C-SWaP solutions for radar, C4ISR, EW, SIGINT, communications, and networking. CEI's out-of-the-box 3DR technology enables modular, scalable embedded computing with 3D mesh connectivity between Intel FPGA processing elements for unparalleled throughput, performance, and flexibility. In conjunction with CEI's data conversion technologies supporting multi-GHz of bandwidth, users can rapidly combine 3DR modules to create digital waveform generators, digital receivers, and signal processors for a variety of remote sensing and communication systems. CEI's cross-discipline engineering experience in RF, digital, software, and system design provides a high level of application expertise to help customers realize optimal solutions ranging from traditional small form factors to COTS 3DR to full custom approaches. For more information, visit http://coloradoengineering.com/ .
GiDEL	GiDEL is one of the market leaders in providing innovative COTS and application-specific solutions for high-performance, real-time signal processing and I/O applications. For over 15 years, GiDEL's cutting edge reconfigurable products have addressed OEM needs from prototype to production and span a variety of industry-standard platforms, including short PCI*, full size PCI*, PCI Express*, PCIe*-104, Mezzanine, modified COTS and low profile PCIe*. For more information on GiDEL's FPGA solutions, visit www.gidel.com .

Partner	Description
Mercury Systems	Mercury Systems provides commercially developed, open sensor and Big Data processing systems, software and services for critical commercial, defense and intelligence applications. Mercury delivers innovative solutions, rapid time-to-value and world-class service and support to our prime contractor customers. Mercury Systems has worked on over 300 programs, including Aegis, Patriot, SEWIP, Gorgon Stare and Predator/Reaper. The company's innovative capabilities span three strategic areas: Mercury Commercial Electronics, Mercury Defense Systems and Mercury Intelligence Systems. For more information on Mercury System's FPGA solutions, visit http://www.mrcy.com/ .
Nallatech	For more than twenty years, Nallatech has provided hardware, software, and design services to enable customer's success in FPGA-accelerated applications including real-time embedded computing, high-performance computing, and network processing. Today Nallatech utilizes latest-generation FPGAs to dramatically increase performance-per-watt over traditional computing architectures, while leveraging high-level design tools including OpenCL to reduce time to market. For SWaP constrained applications, Nallatech works with our parent company, www.isipkg.com to provide rugged, miniaturized FPGA systems. For more information on Nallatech's FPGA solutions, visit www.nallatech.com .
Parsec	Parsec develops and produces customized electronic subsystems and products for clients in the defence, industrial and telecommunications sectors. Parsecs VF360 is a 3U Open VPX module that leverages Stratix® V FPGAs technology to provide an ultra-high bandwidth processing platform, ideally suited for computation and bandwidth intensive applications such as radar, networking, SIGINT, electronic warfare, software defined radio, and video. Parsec partners with clients to provide start-to-finish solutions over the product life cycle, optimal sub-systems or products, while enhancing and leveraging its offerings through re-usability and use of its own intellectual property. For more information on Parsec's FPGA solutions, visit http://www.parsec.co.za .
Per Vices	Per Vices builds flexible radio platforms designed to satisfy the needs of a diverse customer base at the best possible value. Our high-bandwidth software defined radio products operate across broad frequency ranges, and have supported the most demanding applications required by defence and telecommunications customers. Our use of Intel FPGAs allows our products to transparently substitute for, and bridge the communication between, different wireless devices. This enables us to build tactical signals intelligence products that provide operators with the means to address the self-organizational capabilities afforded by modern communications infrastructure, without compromising strategic signals intelligence requirements. Our application agnostic technology provides powerful communications, signals intelligence, and (counter) electronic warfare capabilities offering a means to secure communications, surveil ambient wireless signals, and suppress objectionable sources. For more information, visit www.pervices.com/defence .

Partner	Description
Reflex CES	ReFLEX CES is an ISO 9001 company designing and manufacturing custom embedded and complex systems for industrial companies, military, and governmental organizations. The company specializes in Modified-Off-The-Shelf (MOTS) solutions. They also offer a complete portfolio of COTS boards, and several Instant-Development Kits for prototyping or production usages. Solutions delivered include: CPU, processing or acquisition boards or complete chassis (openVPX, VPX, CPCI, COMExpress, ETX, PCIe*...), high-speed data recorders, FPGA SoC, ASIC prototyping platforms. Their technology expertise covers: FPGA & SoC, CPU and embedded software/OS, state of the art PCB routing and board design, rugged equipment/system integration and qualification (EMC, ESD, temperature, shock, vibration, humidity). For more information, visit http://reflexces.com .

Partner Solution Demos

View all videos

Aerospace and military designers face a long list of challenges, including the need for high performance, a broad operating envelope, and a long system life, as well as the added constraints of limited system size and power budgets. Intel FPGAs enable designers to meet the requirements of the aerospace and military markets by supplying enhanced off-the-shelf FPGAs.

Enhanced Off-the-Shelf Silicon

Intel FPGAs meet strict size, weight, and power requirements (SWaP) with high tolerance to humidity, shock, and vibration along with lead-solder available on all families.

Military Temperature Support

The Intel Stratix® series of FPGAs is available in extended military temperatures (-55°C to 125°C).

SEU Detection and Mitigation

Intel's automatic cyclic redundancy check (CRC) compiler for the configuration RAM automatically checks for changes in configuration that might occur from a single-event upset (SEU). See SEU Mitigation .

"Intel provides highly integrated solutions that are low in power, consequently their products are key for our portable Soldier's Network HMS Manpack program with its need for low power, light weight, small size, and low cost."

General Dynamics, The Soldier's Network Defender of the Year

Military Digital Signal Processing

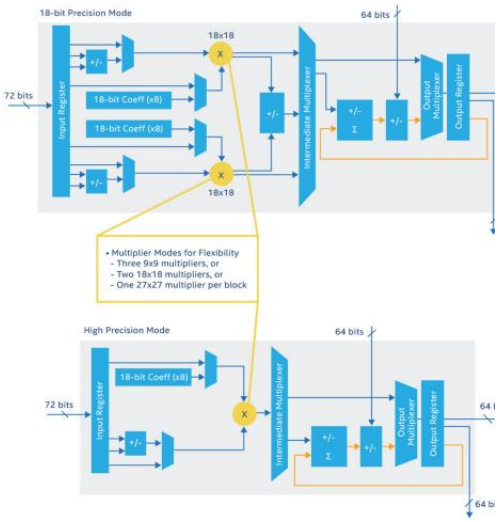
Radar, secure communications, and electronic warfare all have at their roots in high-performance digital signal processing (DSP) chains with a performance range from one GFLOPS to ten TFLOPS. Achieving this level of performance, while still maintaining reasonable size, weight, and power (SWaP), is a challenge.

System architects often develop their concepts and models in MathWorks's MATLAB, then a separate team quantizes the mathematical models for execution in fixed-point-capable hardware. This quantization step often introduces deviation from original model and suffers from possible dynamic range constraints or other system issues.

Intel® Arria® 10 and Intel® Stratix® 10 FPGAs will offer the industry highest GFLOPS/Watt ratio to help maintain SWaP. An IEEE 754- compliant floating-point processing chain can significantly reduce the processing burden, reducing the need for repeated normalization, and consequently increase the hardware efficiency. The floating-point capability of FPGAs can eliminate the quantization step between MATLAB and hardware implementation while maintaining the designer's original system specification. Intel® Arria® 10 and Intel® Stratix® 10 FPGAs will offer up to 1.5 & 10 TFLOPs respectively.

The following figure highlights some of the high-performance DSP capabilities in Stratix® V FPGAs. These include integrated coefficient registers, hard pre-adders, and three multiplier modes for flexibility. The DSP architecture along with DSP Builder for Intel FPGAs (Advanced Blockset) with fused data-path flow saves memory and routing resources while enabling designers to choose the precise blend of precision, utilization, and power.

18-bit and High-Precision Modes



Intel offers solutions, reference designs, and technical support to address military DSP applications. For more details, please contact us.

DO-254

The RTCA DO-254/Eurocae ED-80 standard provides guidance for design assurance of airborne electronic hardware, from conception through initial certification and subsequent post certification product improvements to ensure continued airworthiness. DO-254 defines objectives that must be met by avionics equipment manufacturers according to EASA and FAA guidelines.

The RTCA DO-254 standard defines five levels of criticality from level A (highest) to level E (lowest). These design assurance levels are required for all civil airborne electronic hardware. More recently, military airborne applications such as A400M are now requiring DO-254 compliance.

To support the DO-254 certification process, Intel and its partners are proposing a complete set of tools and intellectual property (IP) that provides the data to present to the certification authority (see the figure below). Intel's experience with developers of airborne systems yields the following recommendations, as shown in the figure below.

Full Design Cycle Partner Network Solutions

DO-254 Certification Support

Level	Description	Affected Area	Intel® Altera® Solutions
A	Failure will cause or contribute to a catastrophic failure of the aircraft.	Display unit, switch systems, airborne computing	FPGA or HardCopy® ASIC with cyclic redundancy check (CRC) feature
B	Failure will cause or contribute to a hazardous/severe failure condition.	Back-up power, heads-up display	FPGA or HardCopy ASIC with CRC feature
C	Failure will cause or contribute to a major failure condition.	Any	FPGA with or without CRC feature
D	Failure will cause or contribute to a minor failure condition.	Any	FPGA with or without CRC feature
E	Failure will have no effect on the aircraft or on pilot workload.	Any	FPGA with or without CRC feature

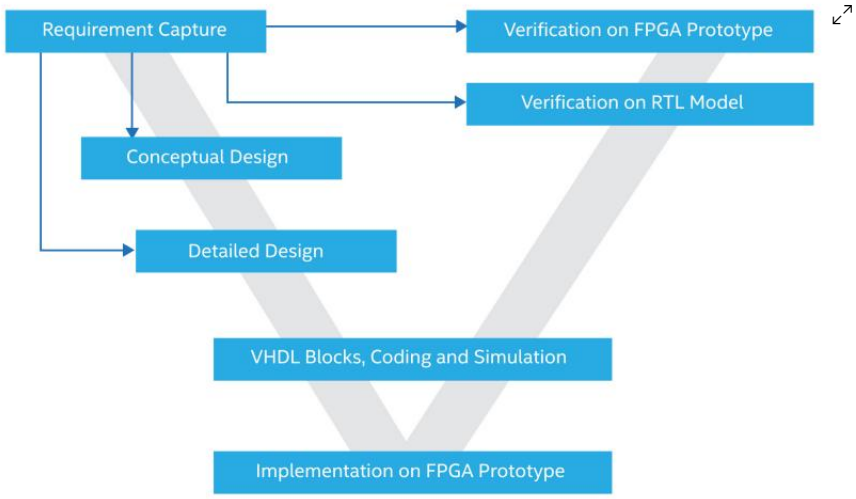
Nios® II DO-254 Certifiable Soft Core Processor

Recent FAA guidance has highlighted the necessity to supply additional design documentation when using a generic-purpose processor or a graphical chipset. The soft IP solution is a design path that offers a high degree of available design documentation. Recently, Intel announced the DO-254

certifiable soft processor: NIOS II_SC. This safety-critical version is provided through our partner Hcell Engineering. The NIOS II_SC package was developed under DO-254 design assurance levels, as well as a safety analysis in accordance with Appendix B of the DO-254 certification.

To comply with level A, several teams were involved in the design, verification, and validation process. A "V Cycle" design verification was performed. The requirement capture is done independently from design, validation, and verification. See Figure 2.

Design Verification Flow



NIOS II_SC Package

Intel and Hcell Engineering have developed a complete DO-254 certifiable package, including:

- NIOS II_SC Plan for Hardware Aspect of Certification (PHAC)
- NIOS II_SC design data:
  - Requirements identification are based on the Nios® II specification, plus design assurance considerations
  - Conceptual design data
  - Detailed design data
- Top-level drawing
- Verification data with Nios® II processor test procedures and test results
- NIOS II_SC configuration management
- NIOS II_SC reports
- NIOS II_SC accomplishment summary

Global Partner Network Members

Partner	Solutions
ALDEC	Compliance tool set for simulation and in-hardware verification
HighRely	Training and documentation

Intel Partners in DO-254 Certifiable IP

The following IP cores are either being assessed for certification or are currently going through a documentation and certification process for Intel customers. Each of these IP cores, and several others, represent customer opportunities to undergo certification with support of Intel and IP partners (see Tables below).

Microprocessors and Graphical Avionics Capability

IP Core	Provider	Function
NIOS II_SC	Hcell Engineering or Intel	32-Bit µP
Avalon® System Interconnect	Hcell Engineering or Intel	System Interconnect
Simple IP	Hcell Engineering or Intel	UART TIMER CFlash
Graphics	IMAGEM	Graphics IP

Network Avionics Capability

IP Core	Provider	Function
Time Triggered Protocol	TTTech	Time triggered protocol
Ethernet	MTIP	10/100 10/100/1000
1553 BC/RT	HCELL Engineering	Bus controller
ARINC 429	Barco and HCELL Engineering	Bus controller
PCI	PLDA	32/66 MHz
PCI Express	PLDA	Gen1
ARINC 818	Great River Technology	Avionics Digital Video Bus

What Customers are Saying About Intel's DO-254 Efforts

"Intel is a member of the DO-254 Users Group, since its creation in 2004, to unite the industry efforts in Europe. Altera, with the NIOS II_SC for DO-254, has made all the necessary efforts to understand the objectives for the requirements, development, production, and verification data for their NIOS II_SC processor."

Lionel Burgaud
DO-254 Group Founder and Chairman

"We have involved Altera and Hcell Engineering since the beginning of our project to have the right level of confidence and documentation to present to EASA."

Jerome Papineau
Program Manager at Thales Aerospace

"Together with the Cyclone® II and Cyclone II FPGAs and Nios® II embedded processor from Intel, we are able to address application requirements for very compact design of distributed embedded systems and smart sensor/actuator modules, that otherwise would require several components—thus reducing system cost and increasing reliability."

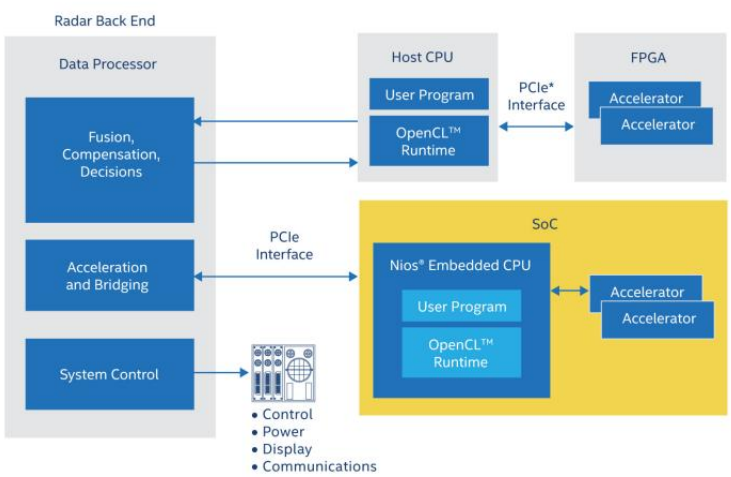
Guenter Motzet
Director Chip IP Design from TTTech

OpenCL

Radar backend processing is a compute-intensive operation using various algorithms such as a FIR filter, which utilize custom pipeline parallelism. Increased performance is achieved by off loading from the host processor onto an FPGA.

Custom processors can be created using the OpenCL™[1] toolflow that are more efficient than multicore CPUs or GPUs both in computational capability and power requirements.

Radar back end processings alternatives using OpenCL



Product Lifecycle

Military communication and weapons systems are now overwhelmingly composed of high density, modern electronic components. Developing an edge, or competitive advantage, in the military marketplace necessarily requires taking advantage of the latest technologies, fastest processing, and the highest integration of analog and digital processes to reduce detection and response times in intelligence systems and military equipment.

These same systems, however, are often brought into service and maintained over time periods that are many multiples, or even orders of magnitude, longer than the constituent components of these systems. This inevitably creates the problem of component obsolescence, which is a primary issue in the field of logistics, and fuels entire industries of component and product emulation, reverse engineering, and code transfer and qualification.

End of Life Strategies, Including Selecting the Lowest Risk Vendor

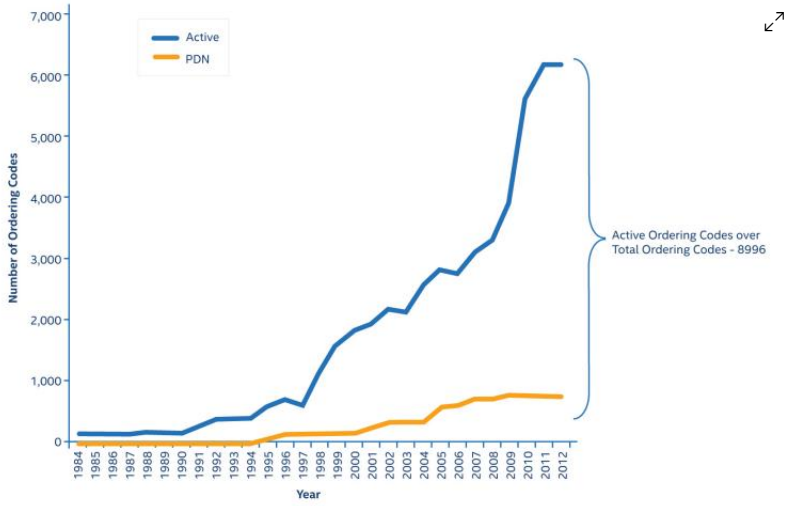
Obsolescence costs, especially for unscheduled product discontinuation or vendor dissolution due to bankruptcy or acquisition, cannot be avoided completely. However dual-sourcing and a few other strategies including vendor support agreements, 'Last Time Buys,' and inventory banking through distributors, have been used with various degrees of supportability and cost success. An additional strategy is to perform Past Performance Assessments of vendors based on product support, and selecting the lowest risk vendor.

Arguably, this strategy is not used widely enough in defense acquisitions. Traditional supplier profiles and past performance do look at a vendor's history, financial stability, and risk of the supplier as an on-going concern. However, these profiles don't necessarily look at the business structure, decisions, and factors that lead to product support and supportability decisions of their components in the long term.

Assessing Product Support Risk

The FPGA Product Support and EOL as Past Performance Indicators White Paper (PDF)

offers several statistical metrics with which to evaluate an FPGA provider's history of product support based on 30 years of FPGA development and product history. A full data set to use for developing your own metrics is available on the Military Portal. An example of one of these metrics is shown in the diagram below.



Additional Resources

Title	Description
Joint Webcasts with MathWorks	Using Mathworks MATLAB and Simulink to solve floating point challenges in developing radar applications
"Floating-Point FPGAs for DSP Bring High Precision to Radar and EW Systems"	Using floating point DSP in FPGAs to bring high precision and dynamic range while reducing power and latency
"Signal processing approaches for electronic warfare and signals intelligence spark debate"	Using COTs boards to shrink development times. A comparison of FPGA, GPU, and DSPs, in high performance military designs
"Radar Processing: FPGAs or GPUs?"	While general-purpose graphics processing units (GP-GPUs) offer high rates of peak floating-point operations per second (FLOPs), FPGAs now offer competing levels of floating-point processing. Moreover, Intel FPGAs now support OpenCL™, a leading programming language used with GPUs
White Paper: An Independent Analysis of Altera's FPGA Floating-point DSP Design Flow (PDF)	BDTI study validates and benchmarks floating point DSP tool performance and the ease-of-use

Military Solution Reference Links

Overview

Videos

Design

Documentation

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