Activity 02: Modeling and Implementation of Sequential Circuits in Verilog

Objective

Implement and verify operation of sequential circuits on Nexys 3 FPGA board.

Theory

Sequential circuits such as registers and memories have "memory" (state information) which typically changes on clock edges.

Practical:

Activity 3a: Implement a 1-bit D flip-flop (register) in Verilog

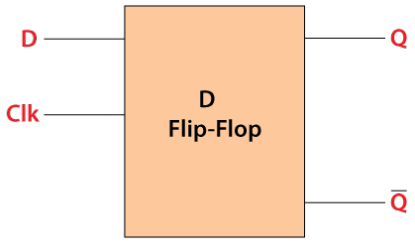

Figure 1

Activity 3b: Implement a 4-bit shift register in Verilog

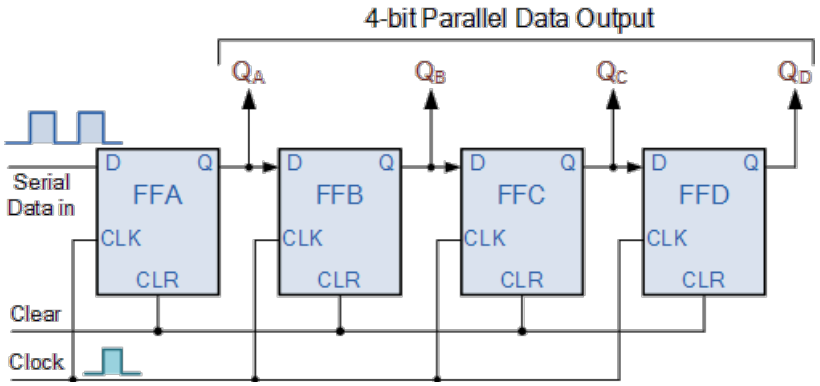

Figure 2

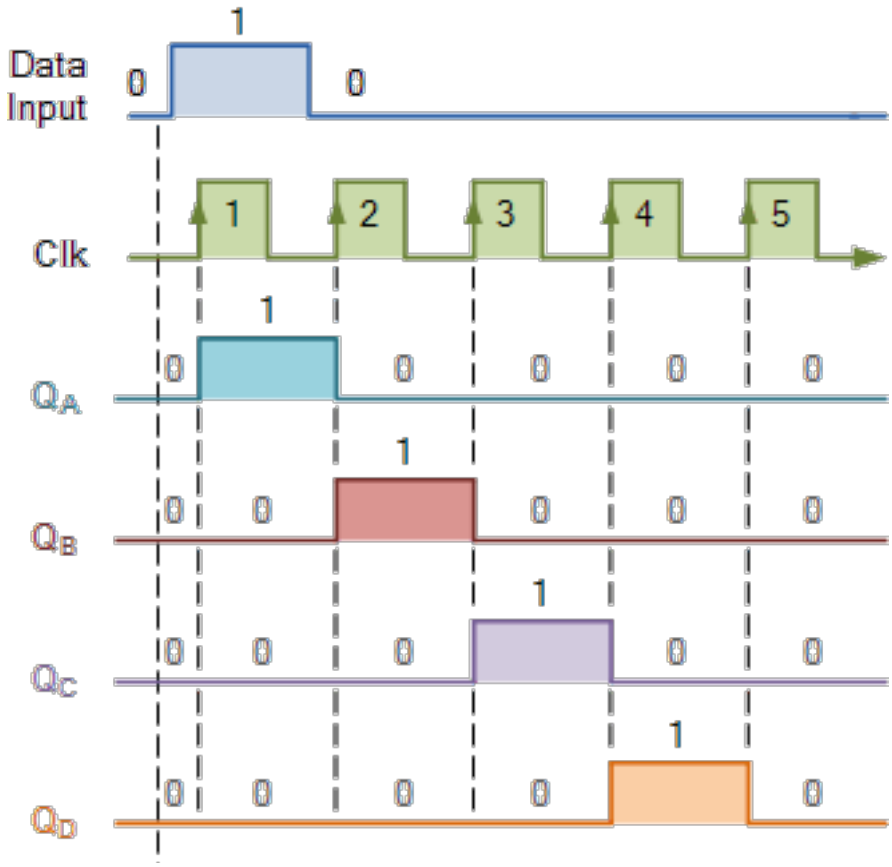

Figure 3