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A 10-Bit 500-MHz 55-mW CMOS ADC

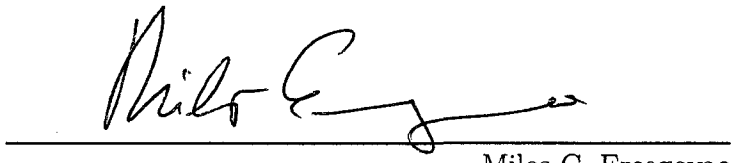
A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical Engineering

by

Ashutosh Verma

2009

The dissertation of Ashutosh Verma is approved.



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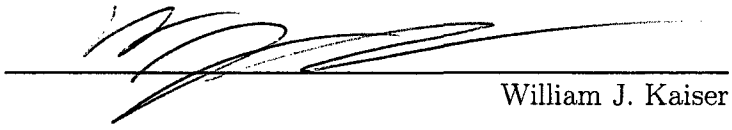

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ABSTRACT OF THE DISSERTATION

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Analog-to-digital converters (ADCs) are widely used in electronics systems with applications in communication systems, bio-medical systems and instrumentation. With continuous advancement in the CMOS technology many of the digital signal processing (DSP) based approaches to assist the inherent analog processing have now become viable, resulting in new architectures achieving either a low power dissipation or a high conversion rate or both.

This research proposes a pipelined ADC calibration technique that allows the use of high-speed, low-power, and yet inaccurate op amps. Designed in 90-nm CMOS technology, a 10-bit prototype digitizes a 233-MHz input with an SNDR of 53 dB, the highest combination reported in the literature for a power consumption of 55 mW. The prototype consists of 14 stages and calibrates capacitor mismatches and nonlinearity and gain error of op amps by means of a resistor-ladder DAC having 11-bit linearity. Employing a two-stage op amp with a bandwidth of 10 GHz and a gain of 25, the ADC achieves a DNL of 0.4 LSB, and INL of 1 LSB.

CHAPTER 1

Introduction

Recent work on analog-to-digital converters has made significant progress toward sampling rates of hundreds of megahertz and resolutions in the range of 10 to 11 bits [1,2]. Among the reported designs, those employing a single channel face a limited speed [3,4], while those incorporating interleaving suffer from a high power dissipation [2] or a low signal-to-noise+distortion ratio (SNDR) [5]. The need therefore exists for ADC architectures that combine high resolution, high speed, and low power dissipation in a single channel. Of course, interleaving can further increase the speed of such designs.

Among nyquist-rate ADC architectures, the pipelined architecture is well-suited for meeting the above requirements in a single channel. In this architecture, the input capacitance of the analog front-end is small (compared to a flash architecture of similar specification) and the conversion-rate (number of samples converted from analog to digital) is high due to the concurrent operation of the pipelined stages. The conversion-rate is ultimately limited by the speed of the op amp used inside the sample-and-hold amplifier (SHA) of each stage. Current CMOS technologies provide faster transistors with transition frequency, f_t, in the range of hundreds of GHz (for 90-nm CMOS technology, f_t is 135 GHz) which makes it possible to design op amps with high unity-gain frequency of up-to 10 GHz. However, such designs suffer from two issues. First, the intrinsic gain of transistors, $g_m r_o$ is quite low (around 10 dB) and that translates to a low open-

loop gain for the op amp. This results in increased gain error and nonlinearity of the op amp, which needs to be corrected. Second, the supply-voltage is reduced to avoid the oxide break-down and that decreases the available voltage swing at the output of the op amp. Since thermal noise (such as kT/C noise) does not change, it implies a large capacitor is needed to meet the SNDR requirement and that increases the power consumption.

Digital calibration techniques for correcting the imperfections (gain error and nonlinearity) of the op amp and the mismatch between the capacitors, have the advantage that they scale with the technology. In every new generation of CMOS technology, the supply voltage is scaled down. This reduces the power consumption given by, $P = CV^2f$, where C is the effective capacitance switching at a frequency f, and V is the supply voltage. The reduction is by a factor equal to the squared ratio of the old and the new supply voltages. As mentioned earlier, the transition frequency, f_t of the transistor improves and hence the speed of digital calibration also improves in every generation. Another advantage stems from the fact that the calibration can potentially allow the op amp to have higher output swings since its nonlinearity is corrected by the technique.

In this research, we have developed a calibration technique which leverages the advantages of the fine-line CMOS technology and demonstrated this on a pipelined ADC which works at a sampling frequency of 500 MHz and has an SNDR of greater than 53 dB and consumes only 55 mW from a 1.2 V supply [6]. This results in an excellent figure-of-merit (FOM) of 0.3 pJ/conversion-step.

This thesis is organized as follows. Chapter 2 provides background of the pipelined ADC architecture. It describes the trade-offs between noise, speed and power in a pipelined ADC, and sources of error that limit the performance. An overview of calibration techniques, and a method to measure mismatches between

small capacitors is also given. Comparison of different calibration algorithms at the architecture level requires modeling of critical analog blocks. Chapter 3 presents techniques for modeling the op amp and compares their advantages and disadvantages. A new calibration technique that corrects capacitor mismatch, gain error and nonlinearity is then described. The calibration technique relied on accurate reference levels coming from a DAC. Chapter 4 compares different DAC architectures and proposes a novel method for building a resistor ladder DAC that has better than 11-bits of linearity. Building blocks of the prototype ADC, the front-end sampling network, op amp, comparator, bootstrap switches, and the calibration hardware are presented in chapter 5. The ADC has been fabricated in 90-nm CMOS technology and its performance was measured. Chapter 6 presents the measurement results. Chapter 7 concludes this dissertation.

CHAPTER 2

Prior Art

2.1 Pipelined Architecture

In a pipelined data converter, the digital estimate of the analog input is determined in multiple stages [7]. Each stage works concurrently in a pipelined manner to maximize the throughput.

A block diagram of a pipelined data converter consisting of M stages is shown in Fig. 2.1. Each stage consists of a low-resolution analog-to-digital converter

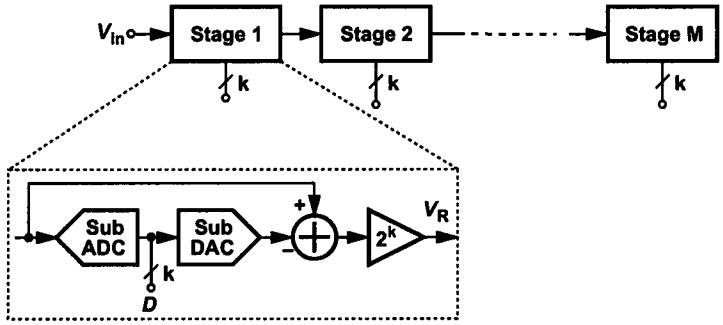


Figure 2.1: Block diagram of a pipelined data converter.

(sub-ADC), a low-resolution digital-to-analog converter (sub-DAC), a subtracter and a multiplier. In operation, the sub-ADC generates a k-bit digital estimate, D, of the analog input. The sub-DAC converts this digital estimate back to an analog value which is subtracted from the main input to generate the difference called the residue. This residue is then multiplied by 2^k to occupy the full output range. The

accuracy with which each of these operations, flash conversion, digital-to-analog conversion, subtraction and residue multiplication is performed, determines the accuracy of the converter. Redundancy is incorporated in the sub-ADC to sub-DAC conversion to relax the requirement on the design of the sub-ADC [7]. However, the sub-DAC conversion, subtraction and multiplication should have the required accuracy for the given specification and is explained in Section 2.4.

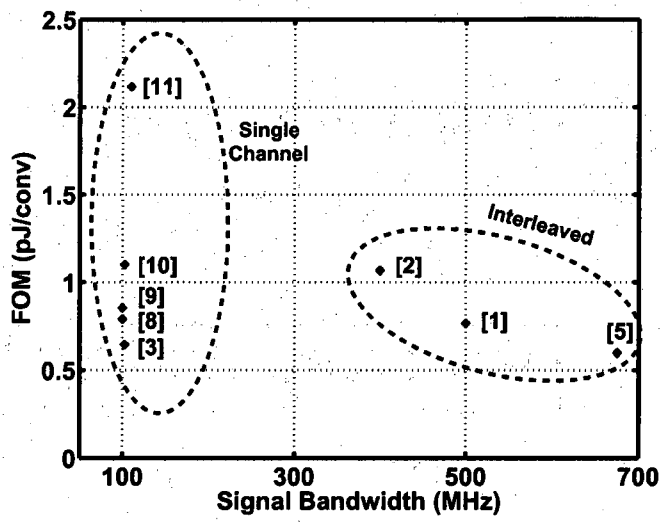


Figure 2.2: FOM comparison.

For a given design specification (resolution and speed), the best design choice minimizes the total power consumption. The figure-of-merit (FOM) frequently used to compare ADC designs is

$$FOM = \frac{Power}{(2^{ENOB})(2BW)}. \tag{2.1}$$

Here, *Power* is the total power consumption, $ENOB$ is the effective number of bits resolved, and BW is the highest input frequency digitized by the ADC. Figure 2.1 compares the FOM for ADCs with $ENOB$ in the range of 8-12 bits, and BW greater than 90 MHz [1–3,5,8–11] . It is interesting to note that designs

with signal bandwidth greater than 100 MHz [1,2,5] have employed interleaving and thus suffered from either a high power dissipation or a low SNDR. While, designs that have used a single channel [3,8–11] are limited to a signal bandwidth of 100 MHz or less. In our research, we have achieved signal bandwidth greater than 230 MHz (a 2X improvement!) using a single channel and a FOM of 0.3 pJ/conversion.

2.2 Switched Capacitor Implementation

The sub-DAC and the residue multiplier are realized using a single switched-capacitor circuit. This circuit is commonly known as a multiplying DAC (MDAC). Figure 2.2 shows a typical implementation of the MDAC. It consists of two ca-

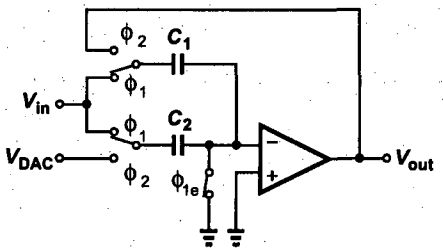


Figure 2.3: Switched capacitor implementation of MDAC.

pacitors C_1 and C_2, and a high gain op amp. The circuit works in two phases. In the sampling phase, capacitors C_1 and C_2 are connected to the input. Then, in the amplification phase, C_1 is connected to the output while C_2 is connected to the sub-DAC output voltage, V_{DAC}. Assuming an ideal op amp, the output voltage can be expressed as

$$V_{out} = (1 + \frac{C_2}{C_1})V_{in} - \frac{C_2}{C_1}V_{DAC}. \tag{2.2}$$

For the 1.5-bit/stage architecture [7], $C_1 = C_2 = C$, and V_{DAC} is $+V_R$, 0 or $-V_R$ based on V_{in}, where V_R is the reference voltage. Figure 2.4 plots the input/output characteristics (also called the residue plot) of such a stage.

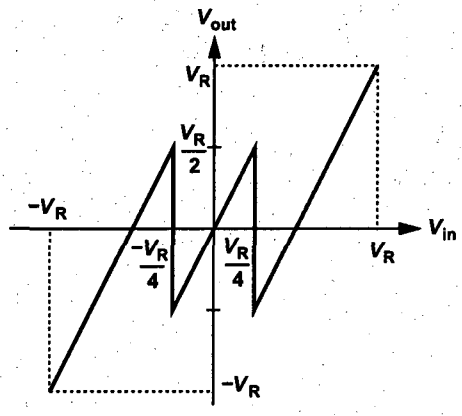


Figure 2.4: Residue plot of an ideal 1.5-bit pipelined stage.

2.3 Noise, Speed and Power Trade-offs

For a given specification, the first design choice is to select the appropriate values for capacitors C_1 and C_2 in Fig. 2.2. It has been shown that for a switched-capacitor circuit, the variance of the sampled noise on a capacitor is kT/C [12], where k is the Boltzmann's constant, T is the absolute temperature and C is the value of the capacitor. This noise is also called the kT/C noise for obvious reasons. Thus, variance of the sampled noise in Fig. 2.2 is

$$\overline{v_n^2} = \frac{kT}{C_1 + C_2}. \tag{2.3}$$

This noise should be kept small to cause minimal degradation in the SNDR. If the circuit of Fig. 2.2 is used in the first stage of a pipelined ADC then for a

sinusoidal signal with amplitude V_R the SNDR is

$$SNDR = 10\log_{10}\frac{V_R^2/2}{\frac{(2V_R/2^M)^2}{12}+\frac{kT}{C_1+C_2}}, \tag{2.4}$$

where, V_R is the reference voltage (half of full-scale voltage) and M is the resolution of the ADC. Equation (2.4) can be written as

$$C_1 + C_2 = \frac{kT}{\left(\frac{V_R^2}{2}\right)10^{-SNDR} - \frac{(2V_R/2^M)^2}{12}}. \tag{2.5}$$

This gives us the required minimum value for the sum, $C_1 + C_2$, once SNDR, V_R and M are known. For example, in a 10-bit system ($M = 10$) with 1 V full-scale range ($V_R = 0.5$ V) and 61 dB SNDR, the minimum value for $C_1 + C_2$ is 0.2 pF. Selecting this minimum size for the capacitors results in the lowest power consumption. However, other constraints such as matching of capacitors and charge-injection error of switches may require a larger size for the capacitors.

Later stages in the pipeline also add noise to the system [13]. To analyze their contributions, consider two consecutive MDAC stages shown in Fig. 2.3. The noise sampled by capacitors $C_{1,j}$ and $C_{2,j}$ of stage j consists of the op amp

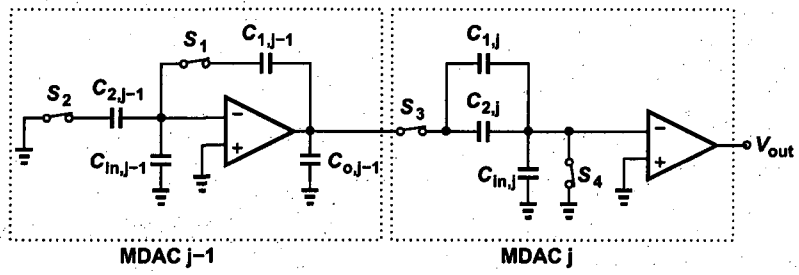


Figure 2.5: Noise analysis of MDAC in later stages.

noise of stage $j-1$ and the switch noise (on-resistance of switches $S_1 - S_4$). Assuming a single-pole transfer function for the op amp, thermal noise spectral density at the output can be written as $(1/\beta)^2 4kT\gamma/g_m$. Here, β is the feedback

factor defined as

$$\beta = \frac{C_{1,j-1}}{C_{1,j-1} + C_{2,j-1} + C_{in,j}}, \tag{2.6}$$

and γ and g_m are the noise-factor and the transconductance of the op amp, respectively. The total noise density at the output can then be approximated as

$$N_j(f) = 4kT \left[\left(\frac{1}{\beta}\right)^2 \frac{\gamma}{g_m} + r_{on,1} + \left(\frac{C_{2,j-1}}{C_{1,j-1}}\right)^2 r_{on,2} + r_{on,3} + r_{on,4} \right]. \tag{2.7}$$

The integrated input-referred noise of the stage j can be approximated as

$$N_j = \frac{1}{(A^{j-1})^2} \left[N_j(f) \frac{\pi}{2} BW \right]. \tag{2.8}$$

Here, A is the inter-stage gain (assumed same for all stages) and BW is the bandwidth of stage $j-1$ approximated as

$$BW = \frac{g_m \beta}{2\pi C_{eq}}, \tag{2.9}$$

where,

$$C_{eq} = C_{o,j-1} + C_{1,j} + C_{2,j} + \frac{C_{1,j-1}(C_{2,j-1}.C_{in,j-1})}{C_{1,j-1} + C_{2,j-1} + C_{in,j-1}}. \tag{2.10}$$

Summing the noise for all stages (assumed M here) in the pipeline gives

$$N_{Total} = \frac{kT}{C_{1,1} + C_{2,1}} + \sum_{j=2}^{M} N_j. \tag{2.11}$$

Substituting this in Eq. (2.4) the SNDR is

$$SNDR = 10 \log_{10} \frac{V_R^2/2}{\frac{(2V_R/2^M)^2}{12} + N_{Total}}. \tag{2.12}$$

This can be rewritten as

$$N_{Total} = \left(\frac{V_R^2}{12}\right) 10^{-SNDR} - \frac{(2V_R/2^M)^2}{12}. \tag{2.13}$$

Once $SNDR$, V_R and M are known, the value for N_{Total} can be determined. However, this is no longer a simple exercise as it depends on $C_{1,j}$, $C_{2,j}$, $C_{in,j}$,

$C_{o,j}$, γ, and A. In Eq. (2.8), the noise of stage j is scaled by $A^{2(j-1)}$ and that indicates a lower noise contribution by the later stages. Hence, having all the stages identical is not power efficient. It has been shown that for high-speed applications, stage-scaling by A is optimal [13, 14]. One good starting point is to allocate roughly 30% of the noise budget to the first stage and determine the value $C_{1,1}$ and $C_{2,1}$. Then scale the later stages by A, and run simulations to determine the total noise power. If this is larger than N_{Total} given by Eq. (2.11), then increase the capacitor sizes or vice versa.

The next choice is to select the inter-stage gain, A. For this, consider the equivalent circuit of the MDAC during amplification depicted in Fig. 2.3. Assuming

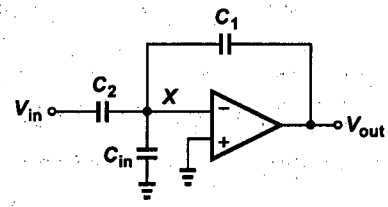


Figure 2.6: Equivalent circuit of MDAC during amplification.

a single pole system for the op amp, the small signal model for this can be drawn as shown in Fig. 2.3. After a rigorous analysis [15], we can find the transfer

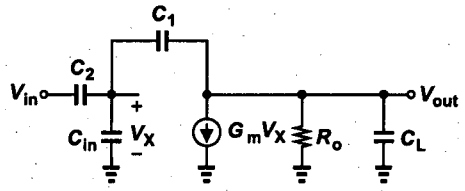


Figure 2.7: Small signal model for MDAC during amplification.

function of the system as

$$\frac{V_{out}}{V_{in}}(s) \approx \frac{-C_{eq}\frac{C_2}{C_2+C_{in}}(G_m - C_2 s)R_o}{R_o(C_L C_{eq} + C_L C_1 + C_{eq} C_1)s + G_m R_o C_2}, \tag{2.14}$$

obtaining a time constant of

$$\tau = \frac{C_L C_{eq} + C_L C_1 + C_{eq} C_1}{G_m C_1}, \tag{2.15}$$

where $C_{eq} = C_2 + C_{in}$. The inter-stage gain for the above configuration is

$$A = 1 + \frac{C_2}{C_1}. \tag{2.16}$$

Then if $C_{sum} = C_1 + C_2$, we can rewrite Eq. (2.15) as

$$\tau = \frac{C_{in} + C_{sum}}{G_m} + \frac{C_L}{G_m} A + \frac{C_{in} C_L}{G_m C_{sum}} A - \frac{C_{sum}}{A G_m}. \tag{2.17}$$

This shows that for a fixed value of C_{sum}, time constant is directly proportional to A. In the current design, higher speed is targeted, therefore, $A = 2$, and the stage-resolution is 1.5-bit.

The third design choice is to select the appropriate value for the transconductance, G_m, given the speed requirement (i.e. τ is known). Since transconductance depends on the device geometry, varying the transconductance changes the input capacitance as well. To consider this effect, the op amp in Fig. 2.2 is modeled as a single-stage op amp shown in Fig. 2.3. Assuming the square-law model for the

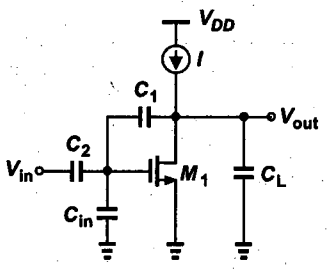


Figure 2.8: Single-stage op amp.

transistor M_1, transconductance is given by

$$G_m = \sqrt{2 I \mu_n C_{ox} W/L}, \tag{2.18}$$

and

$$C_{in} = C_{ox}WL, \tag{2.19}$$

where C_{ox} is the oxide capacitance and W and L are the width and the length of the transistor M_1, respectively. Combining Eq. (2.18) and Eq. (2.19) we get

$$I = \frac{1}{2}\frac{G_m^2 L^2}{\mu_n C_{in}}. \tag{2.20}$$

Substituting G_m from Eq. (2.15) and then finding the value of C_{in} that minimizes I, we get C_{in} as,

$$C_{in} = C_2 + \frac{C_1 C_L}{C_1 + C_L}. \tag{2.21}$$

That is the value of C_{in} that minimizes the power consumption is equal to the value of equivalent capacitance connected to it. Once C_{in} is known, G_m and I can be determined from Eq. (2.15) and Eq. (2.20) respectively. Although, the above relationship is derived for a single-stage op amp, a similar exercise can be carried out for a two-stage op amp to yield similar results.

2.4 Sources of Error

Each sub-block in a pipelined stage suffers from different error mechanisms that degrade the performance. In this section, these error sources are characterized with respect to a 1.5-bit/stage pipelined ADC. These errors are,

1. Comparator offset error,
2. Op amp offset and gain error,
3. Capacitor mismatch, and
4. Op amp gain nonlinearity.

The *comparator offset* changes the transition point in the residue plot as shown in Fig. 2.9. Here, the comparator threshold differs slightly from its ideal value of $-V_R/4$, where V_R is the reference voltage. Owing to the redundancy (residue multiplier gain is two, instead of four) the stage output, V_{out} does not exceed the full range, as long as the offset is less than $V_R/4$. When the offset is larger than this limit, the output saturates resulting in missing codes in the ADC transfer characteristics.

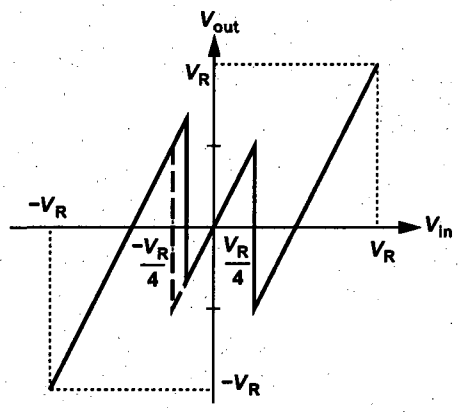


Figure 2.9: Residue plot with comparator offset.

The *op amp offset* adds a fixed voltage to the output and moves the residue plot up or down. Fig. 2.10 depicts the effect of a positive op amp offset on the residue plot. Since the offset is constant, it does not affect the linearity of the stage. Offsets in the later stages can be referred to the main input and added to get the input referred offset for the ADC.

In deriving Eq. (2.2), an ideal op amp was assumed. Finite gain of the op amp results in *gain error* and changes the slope of the residue plot from its ideal value of two. To characterize this effect, consider the 1.5-bit MDAC configuration shown in Fig. 2.11. Applying the principle of charge conservation at node N, the

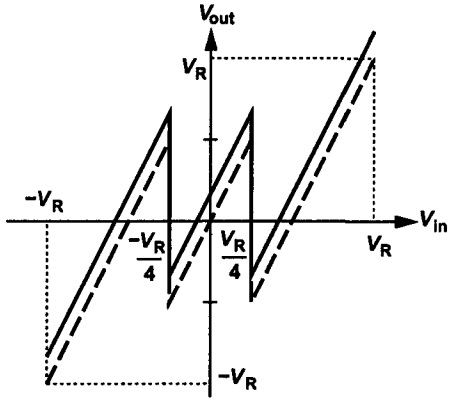


Figure 2.10: Residue plot with op amp offset.

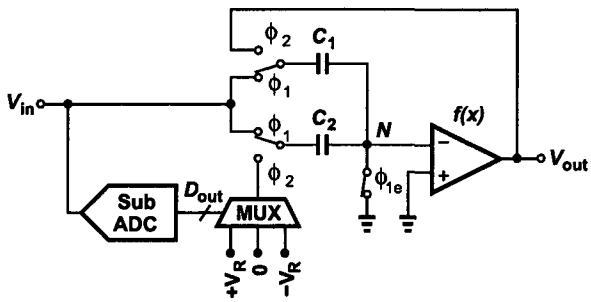


Figure 2.11: 1.5-bit MDAC

output voltage is given by (assume $C_1 = C_2 = C$)

$$V_{out} = \frac{2V_{in} - D_{out}V_R}{1 + \frac{2}{A}}, \tag{2.22}$$

where V_{in} is the input, D_{out} is the digital output and A is the op amp gain. For $2/A \ll 1$

$$V_{out} \approx (2V_{in} - D_{out}V_R)(1 - \epsilon_A), \tag{2.23}$$

where $\epsilon_A = 2/A$ is the gain error. Its effect on the residue plot is shown in Fig. 2.12. Expanding Eq. (2.23) for a pipelined ADC with M stages the input

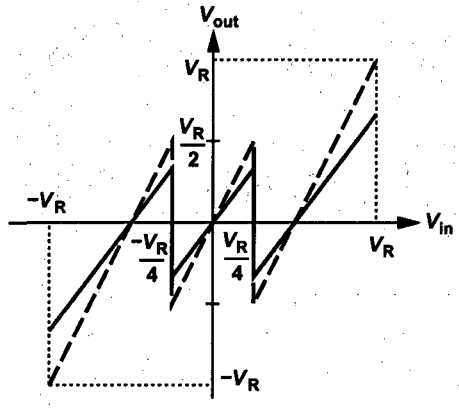


Figure 2.12: Stage transfer characteristic showing op amp gain error.

can be expressed as

$$\frac{V_{in}}{V_R} = \frac{1}{2}\sum_{j=1}^{M}\left(\frac{1}{2(1-\epsilon_A)}\right)^{j-1} D_{out,j} + \left[\frac{1}{2(1+\epsilon_A)}\right]^{M} \frac{V_{out,M}}{V_R}, \tag{2.24}$$

where $D_{out,j}$, is the digital output of stage j, $V_{out,M}$ is the residue output of stage M and ϵ_A is the gain error (assumed equal for all stages). Gain error results in missing codes at the ADC output characteristics and is shown in Fig. 2.13. It occurs because the digital codes are combined using the following relationship

$$D_{tot} = \frac{1}{2}\sum_{j=1}^{M}\left(\frac{1}{2}\right)^{j-1} D_{out,j}. \tag{2.25}$$

Whereas, the combination should be performed using slightly different coefficients for $D_{out,j}$ as shown in Eq. (2.24).

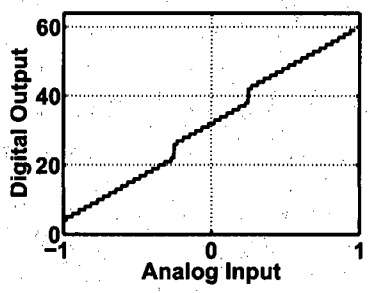


Figure 2.13: ADC transfer characteristic showing op amp gain error.

The mismatch between the capacitors also results in a nonlinear behavior of ADC. For analysis, consider the MDAC configuration in Fig. 2.11 incorporating the capacitor mismatch, i.e., $C_1 = C(1+\epsilon_C)$ and $C_2 = C(1-\epsilon_C)$. The output is given by

$$V_{out} = \frac{2V_{in} - DV_R(1-\epsilon_C)}{1+\epsilon_C}. \tag{2.26}$$

Note that the capacitor mismatch results in both a gain error and the digital-to-analog (D/A) conversion error. Mismatch between capacitors is usually small (for sizes chosen based on kT/C noise requirements) and is a concern only in ADCs with resolution greater than 8 bits.

Nonlinearity in the interstage op amp gain also causes the ADC to deviate from its ideal behavior. In Fig. 2.11 assume that the open-loop input/output characteristics of the op amp is modeled by $y = f(x)$. For simplicity assume that the capacitor match adequately, i.e., $\epsilon_C = 0$. The residue output is given by

$$V_{out} = 2V_{in} - D_{out}V_R - 2f^{-1}(V_{out}). \tag{2.27}$$

The error term, $[2f^{-1}(V_{out})]$, depends on the output voltage and causes nonlinearity. For smaller output voltages, the error is small and the residue plot is close

to ideal. But for higher output voltages, the error is large and the residue plot deviates from its ideal behavior and is depicted in Fig. 2.14.

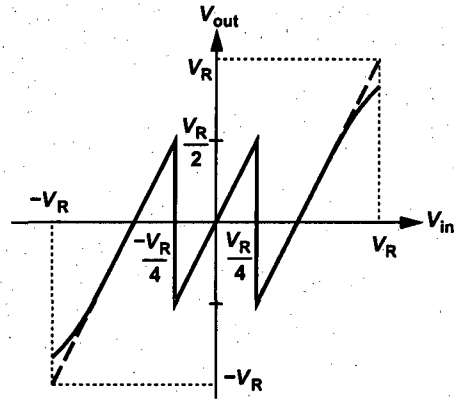


Figure 2.14: Stage transfer characteristic showing op amp nonlinearity.

2.5 Review of Calibration Techniques

In order to achieve the required performance, a number of calibration techniques have been proposed to *fix* the previously mentioned errors. The focus of some of the early techniques was to correct errors arising due to the capacitor mismatch and gain error of the op amp (nonlinearity of the op amp was ignored as it was suppressed by the high open-loop gain). In [16], trim capacitors with digital control for value-adjustment were added to all capacitors. At startup, a self calibration routine configured the digital control word to match capacitors with each other. In [17], a capacitor error-averaging technique was proposed to perform an accurate multiply-by-two function, and was demonstrated on a 12-bit 1-Msample/s pipelined ADC. This technique corrected errors resulting from capacitor mismatch and switch-feed through in the analog domain and no digital calibration or trimming was applied. In [18], a digital self-calibration algorithm

was proposed for a radix 1.93, 1-bit/stage pipelined ADC. During calibration, the difference in the residue voltage of a stage at the major carry transitions were digitally measured by the back end and stored. Then in normal operation, this difference was added to the output, whenever the digital output of the stage was one (i.e., whenever there was a carry). The algorithm corrected capacitor mismatch, finite op-amp gain, and comparator offsets. In [19], a self-calibration technique that digitally measured capacitor mismatch was described and was demonstrated on an algorithmic ADC. In [20], an LMS algorithm was presented that adaptively estimated the inter-stage gain in an algorithmic ADC. It adjusted the gain such that near the comparator threshold the digital output of the ADC differs by at most one LSB (as would be the case in an ideal ADC). In [21], a pipelined ADC was calibrated in the background using an algorithmic ADC, which itself was calibrated in the foreground. A similar technique that used a sigma-delta ADC for calibration was presented in [22]. In [23], a known calibration signal was injected and using correlation the inter-stage gain was determined. The calibration worked in background without interrupting the normal operation. In [24], a modified dynamic-element-matching technique was employed that along with a correlation based technique removed errors arising from capacitor mismatch and the gain error. In [25], a histogram-based method was used to remove both gain error and non linearity of an open-loop op amp. However, the overall linearity of the ADC was limited by the uncalibrated non-linearity in the input sample-and-hold amplifier (SHA) and its back end ADC. It also required considerable amount of time for the calibration to converge, as the input signal appeared as noise to the adaptive calibration loop. In [26], a bootstrapped calibration algorithm that used a capacitor DAC to calibrate gain error and non linearity of the op amp was described. Dynamic element matching was employed to improve the linearity of the capacitor DAC. However, the input

sample-and-hold nonlinearity (SHA) was not corrected and that led to a decrease in SNDR performance, when the ADC was calibrated in the background mode.

One of the big drawback of the techniques presented is that, even after calibration they required relatively accurate analog blocks. For example, the op amp used in [26] had 7-bit gain accuracy (approximately 350 was the value of open-loop gain). In [25], an open-loop op amp was used (which had low gain by design), but only in the second stage and it relied on an accurate back-end that used high gain op amps. In this thesis, we have used low-gain yet accurate op amp for all the stages and corrected for gain error and non linearity of the op amp using a highly accurate resistor ladder DAC. Relaxing the requirement on the open-loop gain of the op amp had resulted in a low power consumption and the complexity of the digital calibration logic is small enough to justify this choice. In the next section, we present a frequency-based approach for measuring the mismatch between small capacitors.

2.6 Frequency-Based Measurement of Mismatches Between Small Capacitors[1]

The need for measurement of mismatches between small capacitors arises in both process characterization and high-precision analog design. For example, multi-bit pipelined stages in analog-to-digital converters (ADCs) may incorporate a segmented digital-to-analog converter (DAC) having small unit capacitors whose matching determines the overall linearity. Similarly, charge-redistribution successive-approximation ADCs typically employ a capacitor DAC containing a large number of unit capacitors.

[1]This section is a reproduction of the paper presented in CICC, 2006 [27].

This paper introduces a capacitance-frequency conversion technique for the measurement of capacitor mismatches. Unlike voltage-based methods reported to date, the proposed approach provides the mismatch directly in digital form, simplifying the measurement and improving its reproducibility.

2.6.1 Capacitor Mismatch Measurement Issues

Since direct measurement of small capacitors is prone to errors due to pad capacitance mismatches and the resolution of the instrumentation, on-chip circuitry is often necessary to isolate the devices under test from other parasitics. Figure 2.15 depicts an example, where the left plate of C_1 and the right plate of C_2 are switched between 0 and V_{REF} in opposite directions and the change at node E is measured [16]. This technique suffers from several drawbacks:

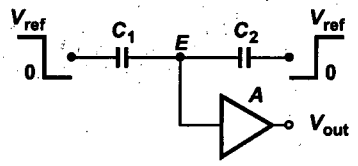


Figure 2.15: Voltage-based mismatch measurement.

1. The input capacitance and noise of the buffer A corrupt the measurement.
2. The small change in V_E (fundamentally a single-ended quantity) is prone to noise in the setup and difficult to measure.
3. The unknown initial charge at node E may require a periodic reset mechanism, thus leading to kT/C noise.

Interestingly, while the kT/C noise due to the *total* sampling capacitance in an ADC is negligible, that due to *unit* capacitors in a segmented array may not be.

Figure 2.16 illustrates another example, where a ramp is applied to X while Y is grounded and vice versa [28, 29]. The output voltage slopes, S_1 and S_2

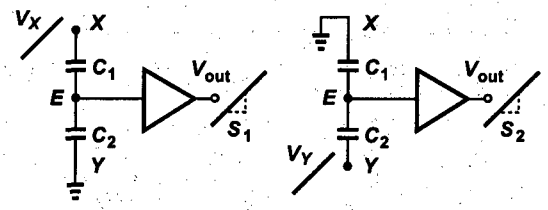


Figure 2.16: Ramp-based mismatch measurement.

are measured, and the difference between the slopes is translated to mismatch between C_1 and C_2:

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{S_1 - S_2}{S_1 + S_2}. \tag{2.28}$$

Owing to the "analog" nature of the measurement, this technique, too, suffers from inaccuracies due to the buffer and setup noise (and kT/C noise if E must be reset periodically). The above observations indicate a need for a capacitor mismatch characterization technique that does not rely on the measurement of voltages.

2.6.2 Proposed Technique

2.6.2.1 Basic Idea

Consider the conceptual arrangement shown in Fig. 2.17, where the oscillation frequency f_{out} is a function of C_1 or C_2. Thus, the relative mismatch between the capacitors, $\Delta C/C$, translates to a relative change in the frequency, $\Delta f_{out}/f_{out}$, if S_1 turns off and S_2 turns on. Since frequency quantities can be measured with much greater resolutions than voltage quantities, this approach potentially provides a high accuracy in capacitor mismatch characterization. For small mis-

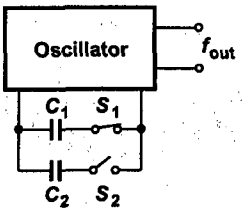


Figure 2.17: Frequency-based mismatch measurement.

matches, we can assume,

$$\frac{\Delta f_{out}}{f_{out}} = \alpha \frac{\Delta C}{C}. \tag{2.29}$$

Figure 2.18 depicts an embodiment of the above concept using a ring oscillator. In this topology, however, $\Delta f_{out}/f_{out}$ is a strong function of the delays of the

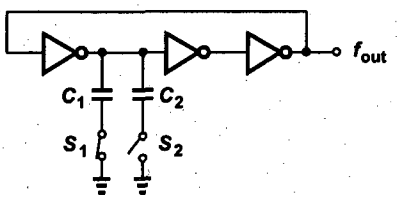


Figure 2.18: Possible realization of the concept in Fig. 2.17.

unloaded stages if C_1 and C_2 are small, making the relationship between $\Delta C/C$ and $\Delta f_{out}/f_{out}$ heavily process-dependent. (If C_1 and C_2 are so large that the unloaded stages contribute negligible delay, then the circuit may fail to oscillate.)

Figure 2.19 illustrates a modification that alleviates this dependence. In this

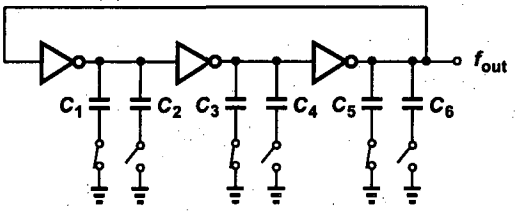


Figure 2.19: Uniformly-loaded ring oscillator.

uniformly-loaded ring, $\Delta f_{out}/f_{out}$ is about $(\Delta C/C)/3$ if C_1-C_6 are nominally equal. Furthermore, the structure provides three mismatch data points corresponding to the three pairs of capacitors, improving the efficiency of both layout and on-wafer measurements. Note that mismatches between the inverter delays slightly alter the value of α, but do not directly corrupt the capacitor mismatch results. For example, an inverter delay mismatch of 10% scales α by about 3.5%.

The high supply sensitivity of the inverters in Fig. 2.19 does present difficulties in on-wafer measurements. (In the first experimental prototype of this topology, the noise picked up by the probes and the dc drops along probe connections made it impossible to collect meaningful data.) The circuit is thus modified to the differential form shown in Fig. 2.20. While tolerating much greater common-

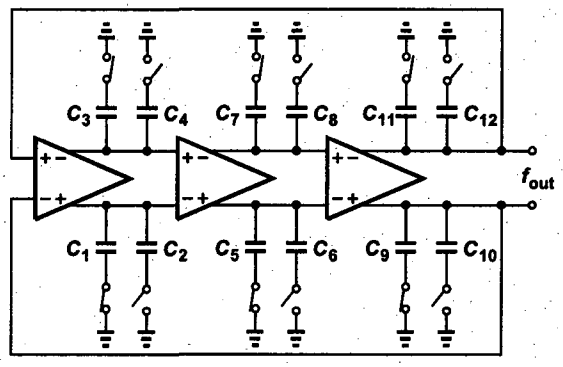


Figure 2.20: Uniformly-loaded differential ring oscillator.

mode noise, this implementation weakens the dependence of $\Delta f_{out}/f_{out}$ to approximately $(\Delta C/C)/6$. Each stage is realized as a simple differential pair with resistive loads. Note that the delays of such stages match more accurately than those of inverters, alleviating the dependence of α on stage delay mismatches.

2.6.2.2 Sources of Error

The proposed technique entails a few sources of error that impact the actual design of the test circuit and ultimately limit the precision with which the capacitor mismatch can be measured.

The first source of error relates to the mismatch between the on-resistances of S_1 and S_2 in Fig. 2.17 or their counterparts in Figs. 2.18, 2.19, and 2.20. If comparable with the driving resistance provided by the oscillator, the switch on-resistance, R_{on}, affects the oscillation frequency and, therefore, its mismatch becomes indistinguishable from capacitor mismatch. It is possible to increase the width of the switches to reduce their on-resistance and its mismatch, but the capacitance contributed by the switches creates other uncertainties (explained below). Alternatively, a large resistance can be placed in series with the output of each stage (Fig. 2.21) such that $R_T \gg R_{on1,2}$ (and $R_T \gg R_{on3,4}$), thus minimizing the effect of R_{on} on the frequency and making the mismatch between R_{on1} and R_{on2} (or R_{on3} and R_{on4}) a negligible contribution to $\Delta f_{out}/f_{out}$. Note that R_T can

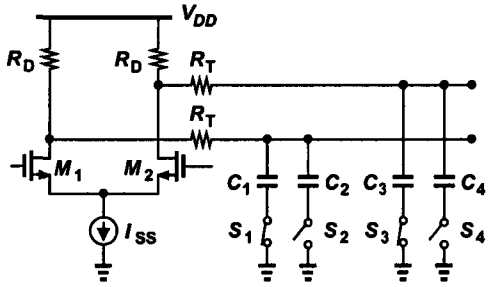


Figure 2.21: Differential pair with series resistance.

be almost arbitrarily large so long as its parasitic capacitance remains negligible, thereby overwhelming the mismatch between R_{on1} and R_{on2} (or R_{on3} and R_{on4}). Also, the mismatch between the two R_T's in Fig. 2.21 is unimportant.

The second source of error stems from the mismatch between the bottom-plate parasitics of the two capacitors under test (Fig. 2.22)[2]. When S_1 is on and S_2 is

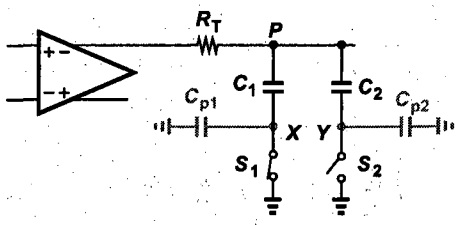


Figure 2.22: Differential pair with parasitic capacitance.

off, the total capacitance at node P is equal to $C_1+C_2C_{p2}/\left(C_2+C_{p2}\right) \approx C_1+C_{p2}$, because $C_{p2} \ll C_2$. After the switches change position, the capacitance becomes equal to C_2+C_{p1}. Thus, the relative change in the delay of one stage is given by,

$$\begin{aligned} \frac{\Delta T_D}{T_D} &= \frac{C_2+C_{p1}-(C_1+C_{p2})}{C+C_p} \\ &= \frac{\Delta C+\Delta C_p}{C+C_p}, \end{aligned} \tag{2.30}$$

where C denotes the mean value of C_1 and C_2, and C_p the mean value of C_{p1} and C_{p2}. Fortunately, if, for example, $C_p/C \approx 5\%$, then it is likely that $\Delta C_p \ll \Delta C$. This is because the capacitors and their bottom-plate parasitics equally benefit from averaging over their respective areas and hence should exhibit roughly equal relative mismatches.

The input capacitance of the stages in the ring oscillator affects the value of α in $\Delta f_{out}/f_{out} = \alpha(\Delta C/C)$ to some extent, especially if it is comparable with the capacitance under test. Thus a calibration circuit is necessary to determine the value of α (Section IV).

[2]The mismatch between the capacitances introduced by S_1 and S_2 at X and Y also translates to error, but with minimum-size devices, this component is negligible.

The output buffer necessary to drive external instrumentation also introduces some imbalance among the three stages. For this reason, each stage is loaded with a replica of the output buffer.

2.6.3 Experimental Results

In order to study the potential of the proposed technique, an extensive set of test circuits has been fabricated in 0.13-μm CMOS technology. Figure 2.23 shows the die photograph. The capacitor structures studied here are:

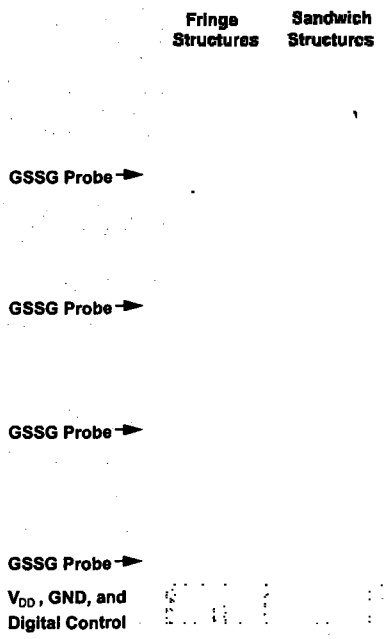


Figure 2.23: Die photograph.

1. Metal 7 - metal 6 - metal 5 sandwich, 10 μm $\times$ 10 μm,

2. Metal 7 - metal 6 - metal 5 sandwich, 15 μm $\times$ 15 μm,

3. Lateral fringe structure (metal 6, metal 5, metal 4), 10 μm $\times$ 10 μm,

4. Lateral fringe structure (metal 6, metal 5, metal 4), 15 μm $\times$ 15 μm.

Each finger in structures 3 and 4 has a width of 0.20 μm. Six pairs of each capacitor are included in a three-stage differential ring oscillator (Fig. 2.20) so as to provide six mismatch data points.

All oscillators share the same digital select lines. As illustrated in Fig. 2.23, the oscillators are powered and controlled by a set of probes on the bottom. The frequencies are then measured through high-speed ground-signal-signal-ground (GSSG) probes, which are stepped vertically from one site to the next. Only one phase of the differential output is brought to a pad, allowing two oscillators to share one GSSG footprint.

As mentioned above, the capacitances contributed by the differential pairs appear as a constant term in the stage capacitance, thereby introducing some error in the value of α (which must be equal to 1/6 in the ideal case). To eliminate this error, an unloaded differential ring oscillator (still including R_T and interconnect parasitics) serves as a calibration circuit.

The characterization proceeds as follows.

1. The oscillation frequency of the unloaded oscillator is measured on the wafer.

2. The value of R_T is adjusted in simulation to obtain the same unloaded oscillation frequency.

3. The oscillation frequency of a loaded oscillator is measured on the wafer.

4. The value of the capacitors is adjusted in simulations, so as to observe the same loaded oscillation frequency. This step also provides the nominal value of the capacitors under test, C_{nom}.

5. The loaded oscillator is simulated with a small capacitor mismatch to determine $\Delta f_{out}/f_{out} = \alpha(\Delta C/C)$ and hence the value of α.

6. With α known, the value of $\Delta f_{out}/f_{out}$ is measured on the wafer for each capacitor pair and translated to a value for $\Delta C/C$.

These steps are repeated for each of the four capacitor structures. The oscillation frequency is monitored by both a spectrum analyzer and a high-sensitivity frequency counter.

Figures 2.24(a)-2.24(d) plot the measured distributions for 36 pairs of each capacitor structure.

Noise picked up by the probes still limits the frequency resolution to about ± 5 kHz (with loaded oscillation frequencies ranging from 57 MHz to 215 MHz). Nonetheless, the results shown in Figs. 2.24(a)-2.24(d) provide an upper bound on the mismatches between the above capacitor structures. It is expected that the inclusion of a simple counter on the chip eliminates the effect of noise.

The experimental distributions depicted in Figs. 2.24(a)-2.24(d) indicate, for the first time, that lateral fringe capacitors exhibit greater mismatches than metal sandwich structures do. As expected, the narrow fingers provide a high lateral capacitance but suffer from substantial random variations in their width during fabrication.

2.7 Conclusion

All the above mentioned error sources make the pipelined ADC deviate from its ideal behavior. In order to get a near ideal performance one must correct these errors, either by design or by calibration. For example, one could design

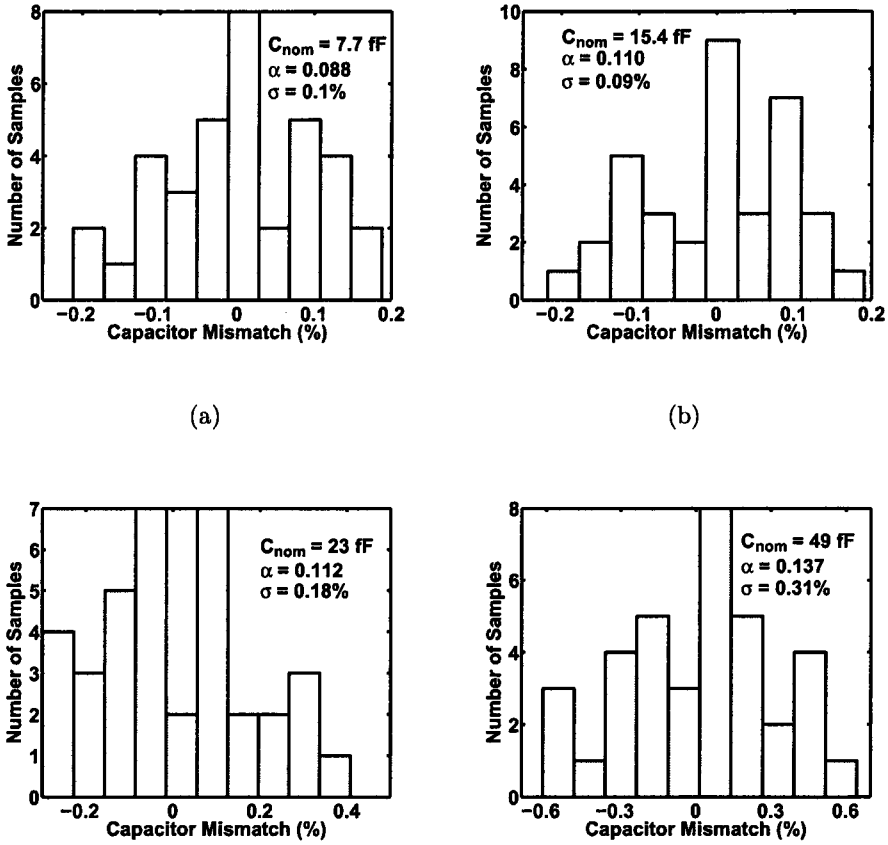


Figure 2.24: Mismatch distribution for (a) 10 μm × 10 μm sandwich structure, (b) 15 μm × 15 μm sandwich structure, (c) 10 μm × 10 μm lateral fringe structure, and (d) 15 μm × 15 μm lateral fringe structure.

the op amp with high open-loop gain so that the gain error does not degrade the performance. The other way is to somehow make an estimate of the gain and then use it to correct for the gain error, a technique better known as digital calibration. In modern CMOS technology with cheap digital transistors, calibration is often the preferred choice. However, one still needs to develop the calibration algorithm which can correct these errors. In the next chapter, we present our calibration algorithm, which corrects the errors arising due to low op amp gain, op amp nonlinearity and capacitor mismatch.

CHAPTER 3

Calibration Algorithm

3.1 Introduction

In this chapter, the details of a new calibration algorithm that corrects for the errors arising from low op amp-gain, op amp non-linearity and the capacitor mismatch is presented. The algorithm relies on on accurate on-chip reference DAC (described in chapter 4) and is able to compensate the imperfections of an op amp with open loop gain as low as 25. Methods for capturing the behavior of an op amp are also described.

3.2 Op Amp Behavioral Model

To develop the calibration algorithm for correcting the errors associated with the op amp, an analytical model for the op amp is developed first. The advantage here is that once it is done, different algorithms can be tested and compared conveniently in a short time. The op amp modeling can be done in different ways and three methods are presented here. This by no means is a comprehensive list, but still gives a good idea of the trade-offs involved in behavioral modeling.

3.2.1 Look-up Table

In the look-up table method, the op amp output is captured for a large number of input points and stored in a table. This technique has been widely used in computer science to save the run-time computation of complex functions. The advantage of this method is that both the direct and the inverse functions are available. The disadvantage is that there is a direct trade-off between the cost and the precision. If N bit precision is required at the op amp output then both the input and the output must be recorded, whenever, the output changes by one LSB. This implies that at least 2^N sample points must be stored with a precision of N bits requiring a memory of size

$$Memory\ Size = 2N \times 2^N, \tag{3.1}$$

and that indicates an exponential dependence of hardware cost on precision.

3.2.2 Hyperbolic Tangent Approximation

Since op amp transfer characteristics displays a saturating behavior, functions that have similar properties can be used as an approximation. Hyperbolic tangent $[y = \tanh(x)]$ is one such function and is plotted in Fig. 3.1 for reference.

Observe that the output is always bounded between ± 1 and its slope near zero is almost one. To fit this curve into the op amp characteristics, it is parameterized as $V_{out} = a \tanh(bV_{in})$, where a and b are chosen to get a best fit in the least-mean-squares sense. Another method is to select these parameter so that the resulting curve matches the slope near zero and has the same value near the extreme points [30] .

The advantage of this approach is the ease of its mathematical formulation and subsequent analysis as both the inverse and direct functions can be readily

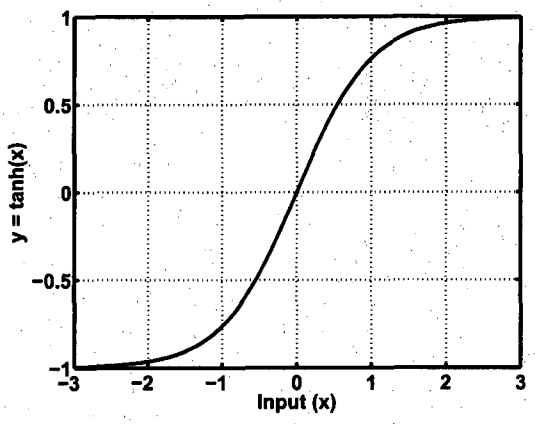


Figure 3.1: Hyperbolic tangent function

computed. However, the difficulty lies with actual implementation in hardware. Note that op amp is already modeled. The calibration logic that models the inverse function [$y = \tanh^{-1}(x)$] needs the extra hardware. The taylor series approximation of $y = \tanh^{-1}(x)$ only until the 7^{th} power is

$$\tanh^{-1}(x) = x + \frac{x^3}{3} + \frac{x^5}{5} + \frac{x^7}{7}. \tag{3.2}$$

The polynomial coefficients approach zero very slowly and care must be taken in computing values for a large x. Also, there is no even-order term in the expansion indicating that it can not model the even-order nonlinearities present in op amps.

The hardware cost can be reduced by using lesser number of terms. However, in that case it is better to independently choose the coefficients, a method commonly referred as the polynomial approximation.

3.2.3 Polynomial Approximation

In polynomial approximation, op amp output is expressed as a polynomial function of the input and is given by

$$V_{out} = \sum_{i=0}^{i=n} a_i V_{in}^i. \tag{3.3}$$

where n is the order of the polynomial. The polynomial coefficients, a_i are determined such that they minimize the mean-square error with respect to the actual op amp output. This error is a function of the number of terms used in the polynomial approximation. Higher number of terms lower the error and give a better fitting and vice versa. More terms also incur higher hardware cost and complexity. Since a fully differential op amp is used, ever order term are negligible in comparison to the odd order terms and therefore, neglected.

3.3 Closed-loop Op Amp Model

In closed-loop configuration both op amp and its feedback network can be modeled as one single amplification block as shown in Fig. 3.2.

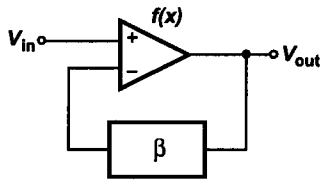


Figure 3.2: Op amp with feedback network.

If $f(x)$ describes the op amp characteristics then,

$$f(V_{in} - \beta V_{out}) = V_{out} \tag{3.4}$$

where V_{in} is the input, V_{out} is the output and β is the feedback factor. This can be written as,

$$V_{in} = f^{-1}(V_{out}) + \beta V_{out}. \tag{3.5}$$

The inverse function, $f^{-1}(V_{out})$ exists, as long as the op amp output has not saturated. Modeling this inverse function as an n^{th}-order polynomial of the form

$$f^{-1}(V_{out}) = \sum_{j=0}^{n} a_j V_{out}^j, \tag{3.6}$$

yields

$$V_{in} = \sum_{j=0}^{n} a_j V_{out}^j + \beta V_{out}. \tag{3.7}$$

It can be simplified further by observing that $f^{-1}(V_{out})$ must be an odd function for a fully-differential op amp, and βV_{out} can be added to the linear term in "$\sum$" expression, which gives

$$V_{in} = \alpha_0 + \sum_{j=0}^{m} \alpha_{2j+1} V_{out}^{2j+1}, \tag{3.8}$$

where, $\alpha_1 = a_1 + \beta$, and $\alpha_j = a_j$ for $j \neq 1$.

Observe that now the input is expressed as a polynomial function of the output. The reason for this is that while calibration, the output of the ADC is available as digital output and the aim is to recover the applied analog input. In the coming sections, the system model is described and is followed by the description of the calibration technique.

3.4 System Description

Pipelined ADCs, even with 1.5-bit stages, must deal with four critical issues: kT/C noise, capacitor mismatch, finite op amp gain, and op amp nonlinearity.

An efficient architecture selects capacitor values to satisfy kT/C noise requirements but not necessarily capacitor matching requirements, handling the latter by calibration, e.g., as in [18]. The two op-amp-related issues begin to manifest themselves, as it becomes increasingly more difficult to design high-gain, high-swing op amps using deep-submicron devices.

The pipelined ADC architecture along with the calibration back end is shown in Fig 3.3. It consists of thirteen 1.5-bit stages and one 1-bit stage. The first two

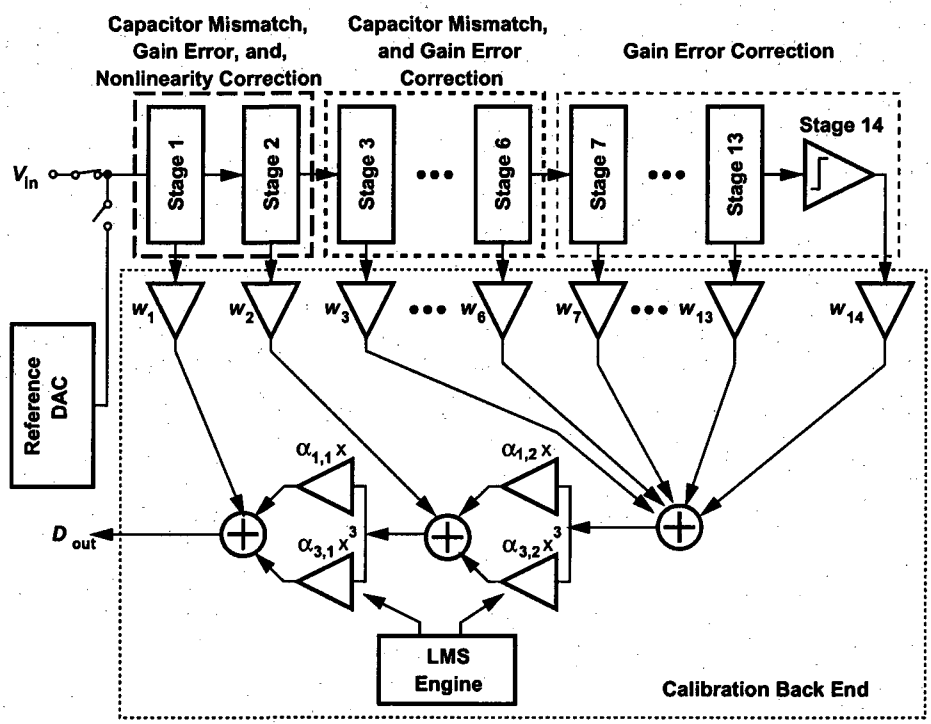


Figure 3.3: Pipelined ADC architecture.

stages are calibrated for residue gain error, digital-to-analog (D/A) conversion error, and op amp nonlinearity; the next four stages for residue gain and D/A conversion error; and the next seven stages for residue gain error.

The digital calibration back end consists of programmable gain coefficients,

w_j [ideally equal to $(1/2)^j$], and two programmable third-order polynomials of the form $\alpha_1 x + \alpha_3 x^3$, which approximates the inverse function of the input/output characteristic of each multiplying digital-to-analog converter (MDAC). With the aid of a highly-accurate on-chip reference DAC, the system applies a number of analog levels at the input and uses a least-mean-square (LMS) engine to adjust w_j and α_j, so as to drive a certain error function to zero.

3.5 Calibration Technique

Consider the 1.5-bit pipelined stage shown in Fig. 3.4, where the sub-ADC consisting of two comparators determines whether $-V_{REF}/4 < V_{in} < +V_{REF}/4$ or not, and the MDAC consisting of C_1, C_2, and the op amp generates the residue. In the ideal case, the residue is expressed as $V_{out} = 2V_{in} - D_{out}V_{REF}$, where D_{out}

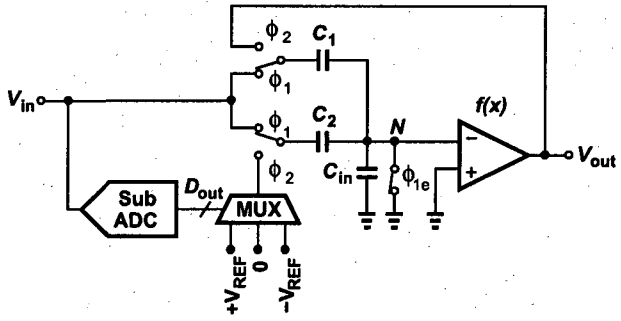


Figure 3.4: Switched capacitor implementation of 1.5-bit stage.

denotes the digital output of the sub-ADC. That is, the sampled analog input can be estimated as

$$V_{in} = \frac{1}{2}V_{out} + \frac{1}{2}D_{out}V_{REF}. \tag{3.9}$$

Capacitor mismatch and finite op amp gain give rise to a gain error while op amp nonlinearity introduces a nonlinear component. If $C_1 = C(1+\epsilon)$, $C_2 = C(1-\epsilon)$,

and the open-loop input/output characteristic of the op amp is represented by $y = f(x)$, then V_N in Fig. 3.4 is equal to $-f^{-1}(V_{out})$ and hence,

$$V_{in} = \frac{1}{2}(1+\epsilon)V_{out} + f^{-1}(V_{out}) + \frac{1}{2}(1-\epsilon)D_{out}V_{REF}. \tag{3.10}$$

Incorporating the effect of the finite input capacitance of the op amp C_p, we have

$$V_{in} = \frac{1}{2}(1+\epsilon)V_{out} + (1+\frac{C_p}{2C})f^{-1}(V_{out}) + \frac{1}{2}(1-\epsilon)D_{out}V_{REF}. \tag{3.11}$$

Note that capacitor mismatch, ϵ, appears in the first term, leading to a gain error, and in the last term, translating to a D/A conversion error. In Fig. 3.3, the coefficients $\alpha_{1,1}$ and $\alpha_{1,2}$ account for the former and w_j for the latter.

The op amp used in this work (Chapter 5.2) achieves a high speed and large output swings but suffers from a low gain (≈ 25). We therefore expect a relatively high closed-loop nonlinearity. On the other hand, the architecture of Fig. 3.3 assumes that the inverse transfer characteristic of each stage can be approximated by no more than third-order terms. To verify the validity of this assumption, we first rewrite Eq. (3.11) as

$$V_{in} = \alpha_1 V_{out} + \alpha_3 V_{out}^3 + \frac{1}{2}(1-\epsilon)D_{out}V_{REF}. \tag{3.12}$$

Next, we perform a transistor-level transient simulation on Fig. 3.4 (e.g., with $\epsilon = 0$ and forcing the multiplexer output to 0) whereby V_{in} is slowly varied from $-0.5V_{REF}$ to $+0.5V_{REF}$ (in differential implementation) and V_{out} is measured. Last, we estimate the values of α_1 and α_3 so as to obtain a good fit (e.g., with minimum mean-square error). If the residual error between the actual V_{in} and the value predicted by Eq. (3.12) remains well below 1 LSB, then the third-order approximation is justified. Figure 3.5 plots this error across the input range (with $\alpha_1 = 0.554$, and $\alpha_3 = 0.004\ V^{-2}$), revealing a maximum of about 0.15 LSB and implying that the approximation is reasonable.

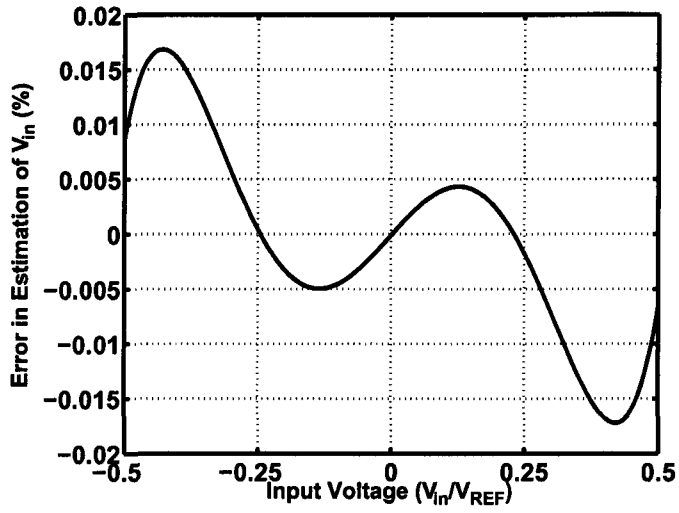


Figure 3.5: Error in V_{in} with third-order polynomial fitting.

3.5.1 Calibration Procedure

The calibration begins with the last stage and proceeds toward the front end. As a result, calibration of stage j can assume that the subsequent stages constitute an "ideal" back end. Figure 3.6 illustrates the calibration arrangement. The reference DAC applies dc inputs to stage j such that the sub-ADC of this stage produces $D_{out,j}$ and the back end generates D_{BK}. Note that D_{BK} accurately represents the residue output of stage j. Next, D_{BK} is subjected to $f^{-1}(\cdot)$ so as to "undo" the nonlinearity created by stage j, and is combined with $w_j D_{out,j}$ to arrive at the overall output, D_{tot}. In the ideal case, D_{tot} must be equal to the digital input of the reference DAC, D_{cal}. Thus, $D_{cal} - D_{tot}$ serves as the error function that must be minimized by the LMS algorithm.

The calibration procedure consists of two steps: estimation of α_1 and α_3 without interaction with w_j, and estimation of w_j with α_1 and α_3 set properly. These steps are described below.

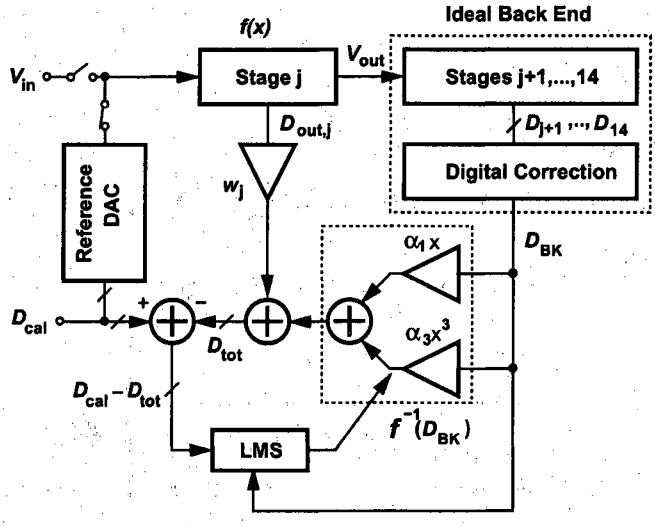


Figure 3.6: Digital calibration.

3.5.2 Estimation of α_1 and α_3

In the first step of calibration, dc inputs equal to $\pm V_{REF}/2$, $\pm V_{REF}/4$, and 0 are produced by the reference DAC in Fig. 3.6 and applied to stage j.Stage j is configured as a multiply-by-two circuit such that $D_{out,j} = 0$. Thus, in Fig. 3.6,

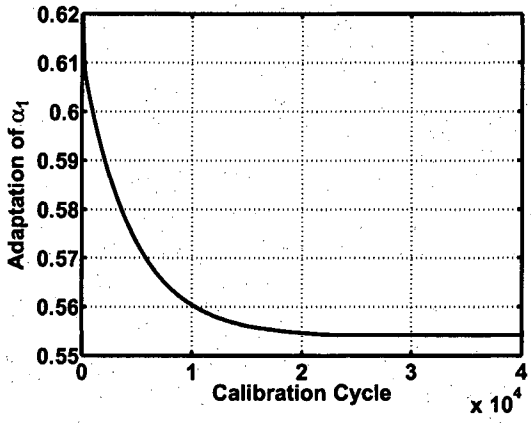
$$D_{tot} = \alpha_1 D_{BK} + \alpha_3 D_{BK}^3. \tag{3.13}$$

The LMS algorithm adjusts α_1 and α_3 so as to drive the mean square error of $D_{tot} - D_{cal}$ to zero. Specifically, α_1 and α_3 are updated according to the following equations:

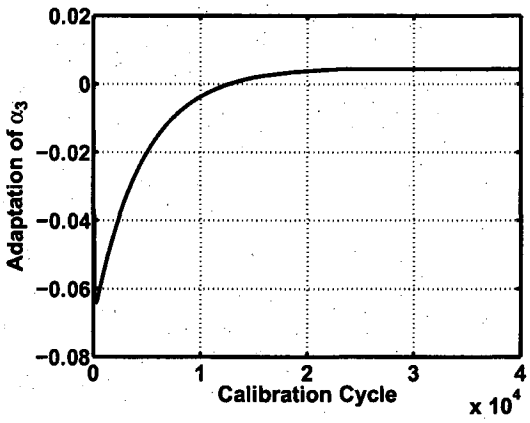
$$\alpha_1(k+1) = \alpha_1(k) + \mu_1(D_{cal} - D_{tot})D_{BK} \tag{3.14}$$

$$\alpha_3(k+1) = \alpha_3(k) + \mu_3(D_{cal} - D_{tot})D_{BK}^3. \tag{3.15}$$

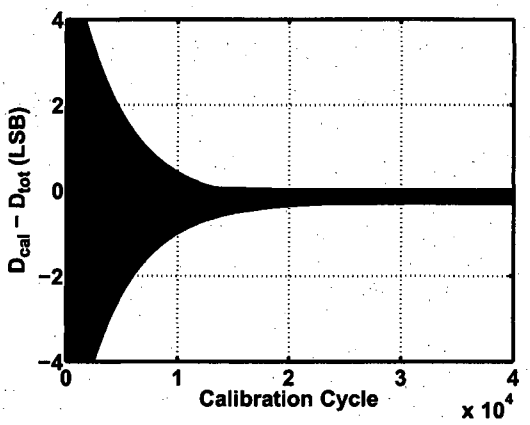
[Note that $(D_{cal} - D_{tot})^2$ is in fact the summation of squares of errors for the five input values provided by the reference DAC.] Figures 3.7(a) and 3.7(b) depict the convergence of α_1, α_3, and $D_{cal} - D_{tot}$ in a system-level simulation of the first stage.


0.62
0.61
0.6
0.59
0.58
0.57
0.56
0.55
Adaptation of α_1
0
1
2
3
4
Calibration Cycle
x 10^4

(a)


0.02
0
−0.02
−0.04
−0.06
−0.08
Adaptation of α_3
0
1
2
3
4
Calibration Cycle
x 10^4

(b)



(d)

Figure 3.6: Simulated convergence of (a) α_1, (b) α_3, and (c) $D_{cal} - D_{tot}$.

3.5.3 Estimation of w_j

The coefficients w_j correct for the effect of capacitor mismatch on D/A conversion [the last term in Eq. (3.12)]. In this case, the MDAC operates in the regular mode (sampling, D/A conversion, multiplication by 2). The reference applies a voltage equal to $+V_{REF}/2$ such that the digital equivalent of Eq. (3.12) plus $w_j D_{out,j}$ can be written as

$$D_{tot} = \alpha_1 D_{BK} + \alpha_3 D_{BK}^3 + w_j D_{out,j}. \tag{3.16}$$

The value of w_j is therefore adjusted to minimize the difference between D_{tot} and D_{cal}. The proposed calibration operates in the foreground potentially suffering from drifts with temperature. This issue is addressed in chapter 5.2.

3.5.4 Back-End Stages

The low open-loop gain of the op amp yields a closed-loop residue gain of only 1.7. Owing to this large departure from the ideal value of 2.00, a cascade of

n pipelined stages provides an overall gain substantially less than 2^n, failing to generate digital codes for the lower and upper ends of the range. For this reason, the architecture of Fig. 3.3 employs eight back-end stages to achieve five bits of resolution. (The digital outputs are eventually truncated to five bits after calibration logic.)

As indicated in Fig. 3.3, the last eight stages are calibrated for only residue gain error. Since capacitor mismatch is negligible here, only the finite gain of the op amp produces gain error. Moreover, since the mismatches among the gains of the op amps used in these stages are negligible at this resolution level, we assume that the stages exhibit *equal* gain errors and hence can be calibrated by a single variable.

To calibrate the back end, its first stage (stage number 7 in Fig. 3.3) is configured as a multiply-by-two circuit while sensing an input equal to $\pm V_{REF}/4$ provided by the calibration DAC. Coefficients w_j are then adjusted so as to minimize the difference between the digital output of this back end and D_{cal}. Calibration procedure for the back end can be explained with the aid of Fig. 3.7. Stage 7 is configured as a multiply-by-two circuit while sensing an input equal to $\pm V_{REF}/4$ provided by the calibration DAC. The back end output is

$$D_{tot} = \sum_{7}^{14} w_j D_j, \tag{3.17}$$

where $w_j = (1/2)w^{j-7}$ and D_j is the digital output of stage j ($j = 7 \cdots 14$). The update equation is

$$w(k+1) = w(k) + \mu_w(D_{cal} - D_{tot}). \tag{3.18}$$

The above recursion forces the difference between D_{cal} and D_{tot} to zero in a negative feedback loop. The value for the update coefficient is chosen such that the recursion converges.

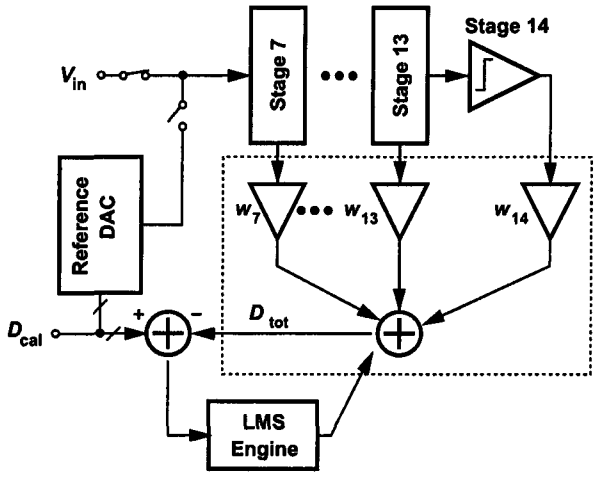


Figure 3.7: Digital calibration of the back end.

3.6 Conclusion

In this chapter we presented details of the calibration algorithm that corrects for D/A conversion error, gain error and nonlinearity of the op amp. The algorithm relied on accurate voltage levels derived from an accurate reference DAC and then used an LMS algorithm to adaptively adjust the calibration coefficients $\alpha_{1,j}$, $\alpha_{3,j}$, and w_j such that the mean square error between the applied voltage and its accurate digital representation tends to zero. In the next chapter we describe the details of the reference DAC used for calibration.

CHAPTER 4

Calibration DAC

4.1 Introduction

This chapter describes the implementation details of a reference digital-to analog converter (DAC) used by the calibration algorithm. The accuracy and precision of this DAC is critical in achieving the desired performance for the ADC. A brief description of different techniques for building the DAC is presented and their relative pros and cos are described. The DAC performance is measured by building a prototype with varying dimensions and those results are also presented.

4.2 DAC Architectures

There are three basic ways of building a DAC:

1. charge division using switched-capacitor arrays,
2. current division or multiplication, and
3. voltage division using resistor ladders.

4.2.1 Switched Capacitor DAC

A switched capacitor DAC is built using an array of capacitors and switches. Figure 4.1 shows a capacitor DAC with N identical capacitors. Their top plate is

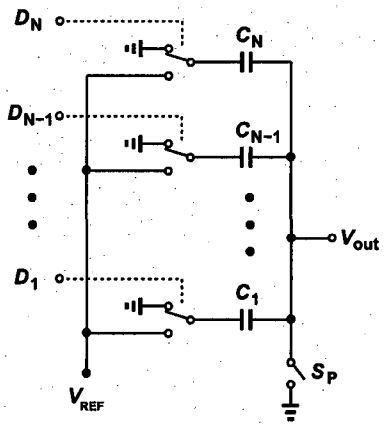


Figure 4.1: Switched Capacitor DAC

shared and bottom plate can be individually switched between V_{REF} and ground. First, the array is discharged by turning the switch S_P on and connecting bottom plates of all capacitors to ground. Then switch S_P is turned off and the switch array D_1 to D_N are configured according to a thermometer code. If j switches are connected to V_{REF}, then by applying the principal of charge conservation the output voltage is

$$V_{out} = \frac{jV_{REF}}{N}. \tag{4.1}$$

Linearity of the DAC depends on the matching between individual capacitors. For a matching of 10 bits are higher, large unit/area of capacitors are required, thereby increasing the power consumption. The other drawback of this architecture is that for driving resistive loads a voltage buffer is required. Linearity of the voltage buffer must be higher than the DAC linearity and therefore, an op amp with high open-loop gain is required. This makes the switched-capacitor DAC

unsuitable for the purpose of calibration in our system.

4.2.2 Current Steering DAC

A current steering DAC is built using an array of current sources and switches. Figure 4.2 shows an example. Here all the current sources are equal and switches

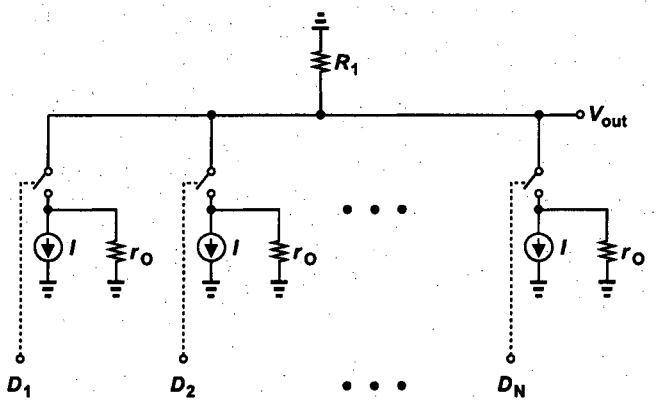


Figure 4.2: Current Steering DAC

are driven by a thermometer code. By turning switches on or off the output current, I_{out}, can be increased or decreased in steps of, the unit current, I. The output current is converted to a voltage using a resistor or a trans-impedance amplifier. There are three source of non-linearity in this DAC: mismatch between the current sources, finite output impedance of the current sources and non-linearity of the load resistor or the trans impedance amplifier. Matching between current sources can be improved by using larger device dimensions and using higher overdrive voltages. It also sets the minimum value for I. For better matching higher value of I is required. The output impedance of the current sources should also be much higher. It can be shown that in the current example if all the current sources have output impedance equal to r_o, then the maximum

value of integral non-linearity (INL) is

$$INL_{max} = \frac{NR_1}{4r_o}. \tag{4.2}$$

To boost the output impedance, cascode configuration is employed in the current source, which decreases the output swing. The low gain of the op amp used in the transimpedance amplifier also results in a gain error. These constraints make the design of the current steering DAC quite complex and not that suitable for the calibration DAC.

4.2.3 Resistor Ladder DAC

A resistor ladder DAC is built using a ladder of identical resistors and is as shown in Fig. 4.3. Here the switches are controlled by 1-of-n code. If switch j is turned

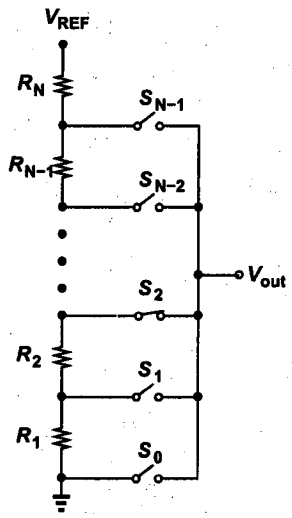


Figure 4.3: Resistor Ladder DAC

on then the output voltage is given by

$$V_{out} = \frac{jV_{REF}}{N}, \tag{4.3}$$

where, N is the total number of resistors in the ladder. Linearity of this DAC depends on matching between the individual resistors. There are two types of mismatches between the resistors: 1. mismatch due to linear gradient and 2. random mismatch. Mismatch due to linear gradient can be partially removed by folding the ladder. Random mismatch occurs due to uncertainties in geometry definition during processing. It has been shown in [31], that the output voltage of a resistor ladder follows a Gaussian distribution with a standard deviation equal to

$$\Delta V_j = \sqrt{\frac{j}{N^2}(1-\frac{j}{N})}\frac{\Delta R}{R}V_{REF}. \tag{4.4}$$

This reaches its maximum value of

$$INL_{max} = \frac{1}{\sqrt{4N}}\frac{\Delta R}{R}V_{REF} \tag{4.5}$$

at $j = N/2$. The advantage of this topology is that it is relatively simple to build and if the random mismatch in a given technology is small, it can also provide good linearity. To see its performance we constructed a number of ladder structures on silicon with varying dimensions and tested their performance. In order to minimize the variation due to contact resistance we built the ladder using a single polysilicon resistor and tapped equidistant points on it. For the calibration algorithm this topology is the most attractive as it is easy to build and can drive the capacitive loads for the purpose of calibration. We now describe the implementation detail of this DAC.

4.3 DAC Implementation

In the current CMOS process, the resistance value can be expressed as

$$R = \frac{\rho L}{Wt} + 2R_c, \tag{4.6}$$

where, ρ is resistivity, L is length, W is width, t is thickness of the resistor and R_c is the contact resistance. An example layout is shown in Fig. 4.4. The

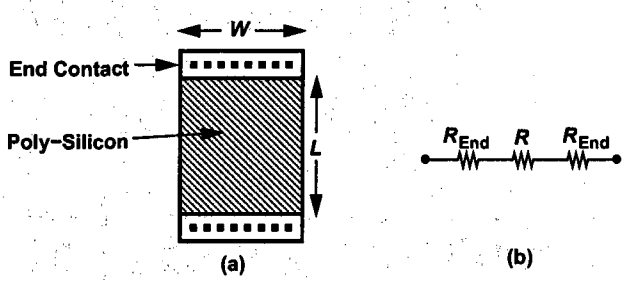


Figure 4.4: Polysilicon resistor

hatched area depicts the polysilicon and dark shaded area depicts the two end contacts. Now the relative mismatch between two resistors laid out with identical geometries can be found by taking the total differential of the above expression and dividing it by the resistance values as

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta L}{L} - \frac{\Delta W}{W} - \frac{\Delta t}{t} + 2\frac{\Delta R_c}{R}. \tag{4.7}$$

For better matching, all the terms in the above expression should be minimized. For a given process, ρ and t are fixed, therefore, only the terms corresponding to W and L can be minimized by increasing these values. However, there is a limit, as larger W and L will increase the parasitic capacitance and the chip area. Even after that the relatively large contact resistance and the poor definition of its value (depending on how much and how deeply the metal fills each contact window) [Fig. 4.5(a)] suggest that the current-carrying contacts can potentially introduce large errors in voltage division. It is therefore desirable to avoid such contacts along the ladder. Third, even contacts that carry no current and simply sense a voltage must create minimal disturbance in the flow of the current. This concern arises because the silicided area under each contact disturbs the current flow, and misalignment in its position leads to random disturbance [Fig. 4.5(b)].

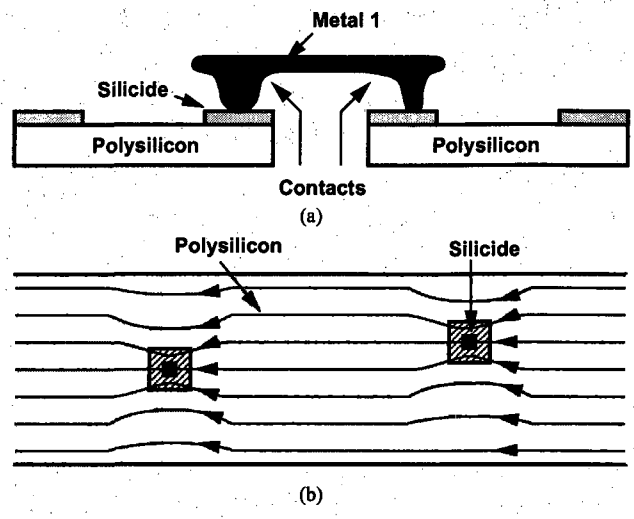


Figure 4.5: (a) Series poly resistors with current-carrying contacts, (b) continuous polysilicon ladder (top view).

Based on these observations, we propose the ladder structure shown in Fig. 4.6. The voltage-sensing contacts are placed on the edge, introducing negligible disturbance in the current flow. Also, since the poly segment between the end A and the tap B is not identical to that between taps B and C (due to the large number of contacts and their underlying silicided area at A), the full-scale references used for the ADC, $\pm V_{REF}$, are taken from the first and last taps rather than from the ends.

The ladder structure of Fig. 4.6 has been fabricated separately with different dimensions and its integral nonlinearity (INL) profile has been measured on 40 samples. Figure 4.7 plots the distributions of the maximum measured INL for four sets of dimensions: $W = 10$ μm and 20 μm, and $L = 32$ μm and 64 μm.

It is observed that the peak INL falls to a value of 0.027% for $W = 64$ μm and $L = 20$ μm. These dimensions are chosen for the reference ladder used in this work.

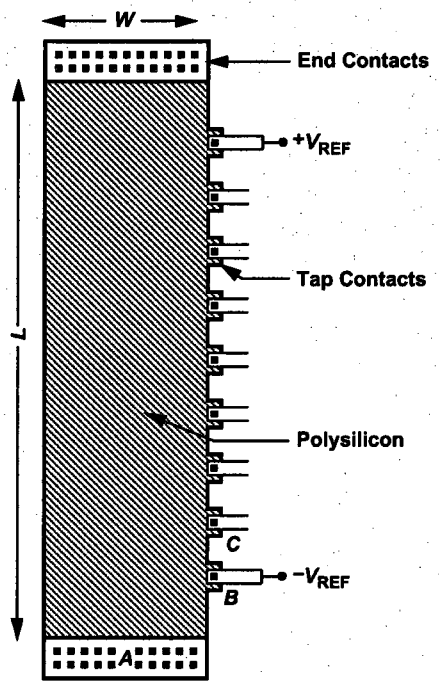


Figure 4.6: Reference DAC.

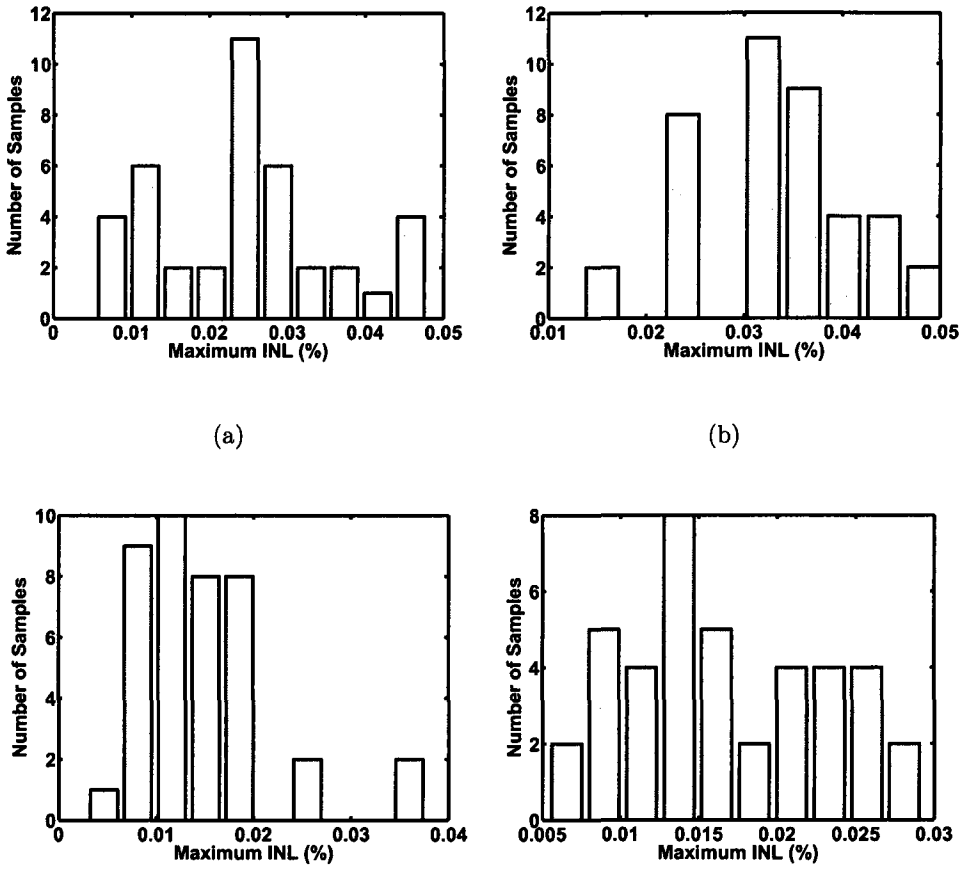


Figure 4.7: INL distributions for ladders of different dimensions, (a) W = 32 μm, L = 10 μm, (b) W = 32 μm, L = 20 μm, (c) W = 64 μm, L = 10 μm, and (d) W = 64 μm, L = 20 μm.

The high linearity of the resistor ladder makes it also attractive for use as an interstage multi-bit DAC in the main signal path (in pipelined or subranging architectures). However, the high resistance of the ladder gives rise to long settling times.

4.4 Conclusion

In this chapter we first discussed the different methods of building a DAC and their advantages and disadvantages. Then we described the DAC implementation using resistor ladder and how it is suitable for our application. After that we presented the test results and studied the error sources that limit the performance.

CHAPTER 5

ADC Design

The architecture of Fig. 3.3 has been realized in 90-nm CMOS technology. This chapter presents the implementation details.

5.1 Input Sampling Network

The first flash stage and MDAC sample the analog input simultaneously, facing potential timing mismatches and resulting in inconsistencies between the digital and residue outputs. Half a bit of redundancy alleviates this issue considerably, but reasonable path matching must be ensured to leave margin for other errors (e.g., comparator offset).

To determine the required matching between the two paths, consider the two sampling networks (MDAC and one of the comparators in the flash ADC) shown in Fig. 5.1. For simplicity, only those switches and the capacitors that are required for sampling are shown. The analog input, V_{in} is sampled by the switches S_1, S_2 and the equivalent capacitor C_{MDAC} in the MDAC, and by the switches S_3, S_4 and the capacitor C_{Comp} in one of the comparators in the flash ADC. Assume a sinusoidal input given by

$$V_{in} = A\sin(2\pi f_{in}t). \tag{5.1}$$

is applied to the system, where A is amplitude and f_{in} is frequency of the input

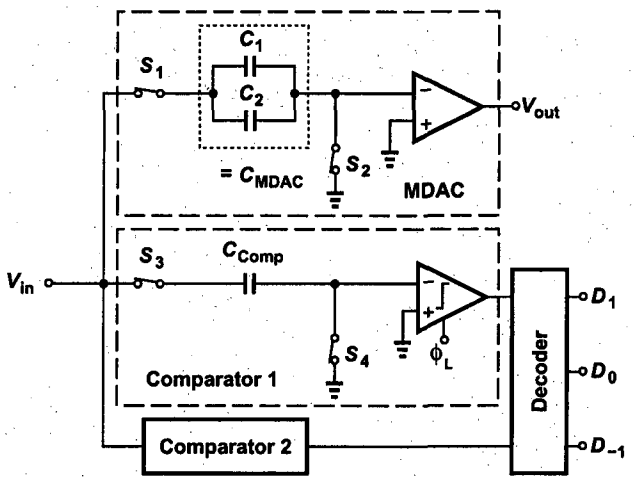


Figure 5.1: Input sampling network of MDAC and comparator.

signal. The voltages sampled by the MDAC and the comparator are then

$$V_{MDAC} = A\sin[2\pi f_{in}(t_1 - \tau_1)], \tag{5.2}$$

and

$$V_{Comparator} = A\sin[2\pi f_{in}(t_2 - \tau_2)], \tag{5.3}$$

respectively. Here t_1 and t_2 are the sampling instants and τ_1 and τ_2 are the RC-time-constants of the MDAC and the comparator input networks, respectively. The difference in the two sampled voltage is

$$\Delta V = V_{MDAC} - V_{Comparator} \tag{5.4}$$

$$= A\sin[2\pi f_{in}(t_1 - \tau_1)] - A\sin[2\pi f_{in}(t_2 - \tau_2)] \tag{5.5}$$

$$= 2A\cos\left[\frac{2\pi f_{in}(t_1 - \tau_1 + t_2 - \tau_2)}{2}\right]\sin\left[\frac{2\pi f_{in}\{(t_1 - t_2) - (\tau_1 - \tau_2)\}}{2}\right]. \tag{5.6}$$

Let $\Delta t_{tot} = (t_1 - t_2) - (\tau_1 - \tau_2)$ then,

$$\Delta V = 2A\cos\left[\frac{2\pi f_{in}(t_1 - \tau_1 + t_2 - \tau_2)}{2}\right]\sin\left(\frac{2\pi f_{in}\Delta t_{tot}}{2}\right) \tag{5.7}$$

$$\approx A\cos\left[\frac{2\pi f_{in}(t_1 - \tau_1 + t_2 - \tau_2)}{2}\right]2\pi f_{in}\Delta t_{tot}. \tag{5.8}$$

The maximum value for ΔV is given by

$$\Delta V_{max} = 2\pi f_{in}\Delta t_{tot}A. \tag{5.9}$$

Half a bit of redundancy between stages can tolerate an error up to $V_{REF}/4$, where V_{REF} is the reference voltage. Allocating half of this error budget to other sources of error, such as comparator offset, charge-injection error, etc. leaves $V_{REF}/8$ as the allowed error caused by the timing mismatch. In Eq. (5.9) substituting $A = V_{REF}$ for the amplitude of the input signal, the upper bound for timing mismatch Δt_{tot} is

$$\Delta t_{tot} < \frac{1}{16\pi f_{in}}. \tag{5.10}$$

This shows that the allowed timing mismatch is inversely proportional to the value of input frequency. For higher input frequencies, matching requirements are more stringent and for an input frequency of 250 MHz, the mismatch between the two sampling networks is limited to 80 ps. In the design, the same clock edge is used for sampling to minimize the mismatch in the sampling instants and two identical sampling networks are used to minimize the mismatch in the propagation delays (RC-time-constants).

Figure 5.2 shows the front-end input sampling network in the acquisition mode. To keep the two paths nominally identical, the input to the op amp and the comparator is disconnected in this mode. Switches S_1, S_2 and S_3 turn off before others, thus perform bottom plate sampling. The value of capacitors C_1 and C_2 is same in both the networks. The size of switch S_1 is twice that of S_2 and

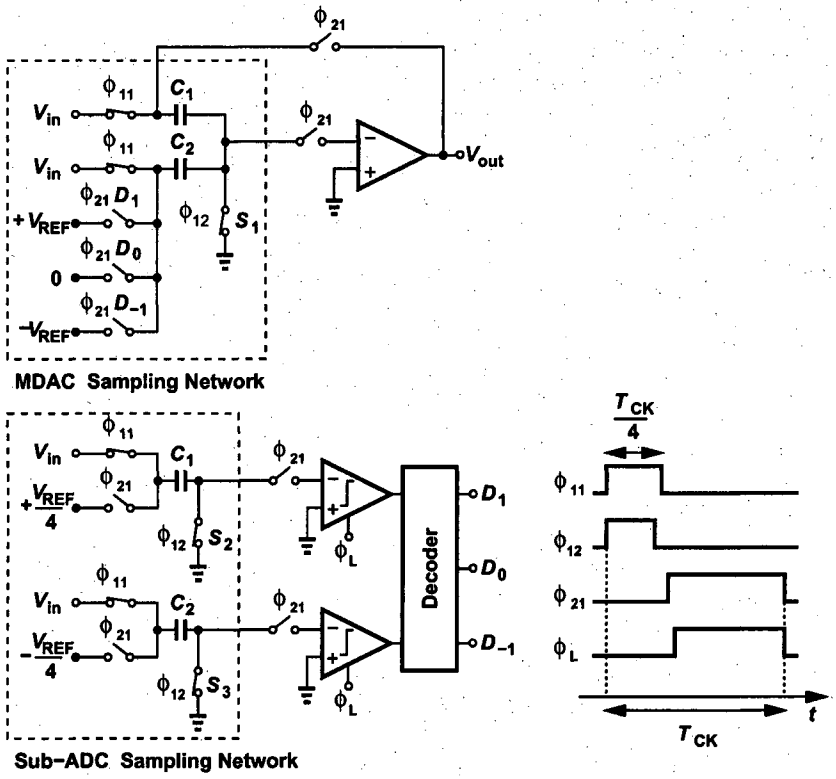


Figure 5.2: Input sampling networks and timing diagram.

S_3. Sizes of other switches that are *ON* in the acquisition mode are kept same. This ensures identical *RC* time constants for both networks and hence almost identical propagation delays.

Another critical issue in the front end is that the flash ADC conversion time must be minimized to allow sufficient settling time for the MDAC. The tight timing budget requires careful partitioning of the clock period, T_{CK}, among three operations: sampling, flash conversion, and residue generation. Since bootstrapped switches can provide a relatively short acquisition time, while achieving high linearity, this design allocates 25% of T_{CK} to sampling, and the other 75% to flash conversion and residue generation. These waveforms are dervied from an input clock frequency of 1 GHz, which is divided by 2 so as to generate quadrature phases. Two of the phases are then ANDed, producing the necessary 25% duty cycle.

In the timing diagram shown in Fig. 5.2, ϕ_{11}, and ϕ_{12} have 25% duty-cycle. For bottom-plate sampling, clock ϕ_{12} falls earlier than ϕ_{11}. Clock ϕ_{21} has 75% duty cycle, and the flash conversion and residue amplification takes place when it is high. Clock ϕ_L triggers the latch in the two comparators. It rises slighly later than ϕ_{21}, to allow subtraction and a settled input to be presented to the comparator.

The following stages in the pipeline see a held input and therefore allow flash conversion to take place in the non-overlap period of the two phase clock. This increases the available time for residue amplification and hence the following phases operate with a 50% duty cycle as shown for the second stage in Fig. 5.3. Since the second-stage samples the amplified output of the first stage, these clock edges should be synchronized with the first-stage clock. To ensure that the two 50% duty cycle clocks are derived by the same divide-by-2 circuit and is described

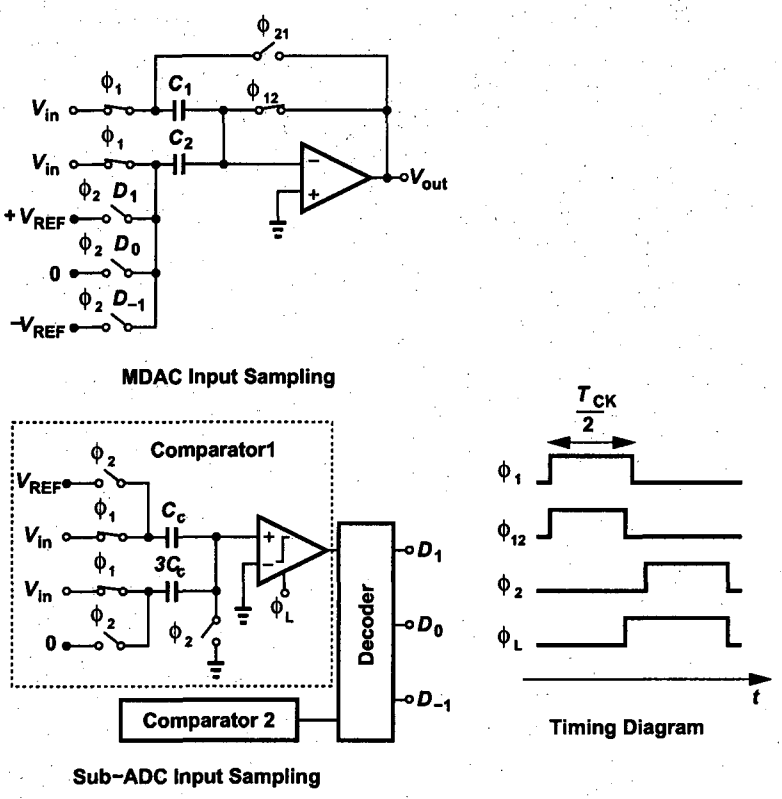
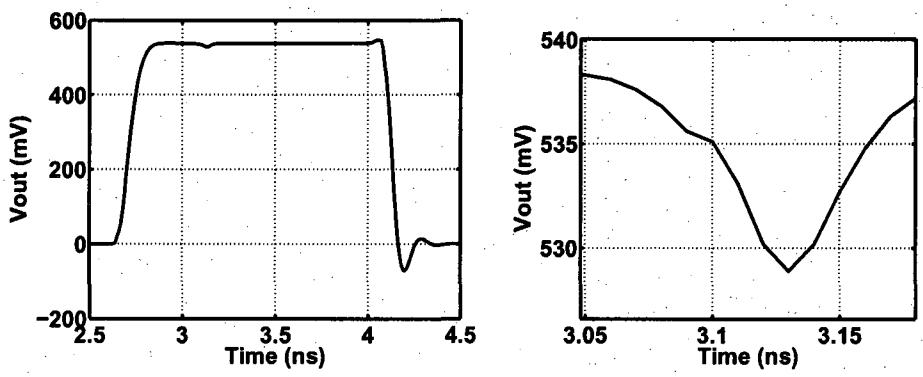


Figure 5.3: Timing diagram for the second-stage MDAC.

in Section 5.6

In operation, the capacitor C_C is precharged to V_{REF}, while capacitor $3C_C$ is precharged to common-mode in clock phase ϕ_2. Then, in the sampling mode, i.e., when clock ϕ_1 is high, a voltage equal to input minus $V_{REF}/4$ is available at the comparator input and the latch can be strobed as soon as the sampling is done, i.e., at the falling edge of ϕ_{12}. This allows extra time for residue amplification as the comparator decisions are available earlier compared to the first stage and using a 50% duty-cycle clock is sufficient.

The switching of the second-stage sampling capacitors to the output of the first MDAC generates a glitch. To see the effect, a transistor-level transient simulation was performed and the first stage output was observed. The output waveforms are shown in Fig. 5.4 that shows the glitch. The peak value of this glitch is about 15 mV [Fig. 5.4(b)] and it subsides over the next half cycle [Fig. 5.4(a)]. This glitch is smaller in magnitude due to the lower value of the



(a) (b)

Figure 5.4: Transient simulation of first stage (a) settling behavior and (b) glitch amplitude.

capacitors used in the second stage as compared to the glitch at the start of residue generation phase.

The absence of the op amp from the sampling network in Fig. 5.2 means that its offset is not removed. While benign in general ADCs, such a front end offset does create discrepancy in the calibration mode as the correcting third-order polynomial assumes that there is no offset present in the system. To cancel this offset, a zero dc input is applied and the resulting digital output D_{os} is stored in the memory. This digital output D_{os} is then subtracted from the overall output when the calibration coefficients are computed.

5.2 Op Amp

The speed and power consumption of the ADC are determined primarily by those of the op amp. This work views the op amp as an amplifier having large output swings and maximum speed with little attention to its open-loop gain. The large output swings relax kT/C noise requirements, directly leading to a lower power consumption.

The need for a high-swing op amp naturally points to a two-stage topology, and the desire for maximum speed, to the smallest number of poles, namely, two. From these observations emerges the op amp shown in Fig. 5.5. To maintain a true two-pole (uncompensated) behavior, the circuit avoids cascode devices. Moreover, to achieve fast common-mode (CM) settling, each stage employs a simple resistive feedback network. Note that the bias current of the output stage is defined as a multiple of I_{SS} through the current mirror action of the PMOS devices. Also, the output CM level is raised to $0.5I_1R_{C1,2} + V_{GS7,8}$ so that it reaches approximately $V_{DD}/2$.

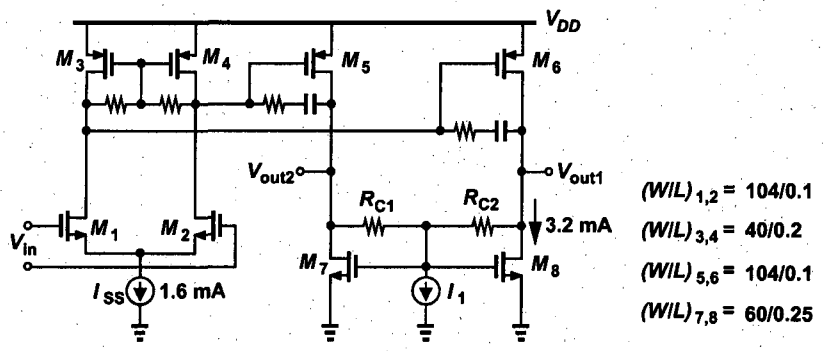


Figure 5.5: Two-stage op amp schematic.

In order to maximize the uncompensated pole frequencies, the circuit of Fig. 5.5 incorporates minimum-length transistors in the signal path, thus exhibiting an open-loop gain of only 25. As explained in Section II, the low gain yields substantial closed-loop nonlinearity, necessitating calibration. Figure 5.6 plots the simulated open-loop nonlinearity of the op amp for a peak-to-peak differential output swing of 1.2 V.

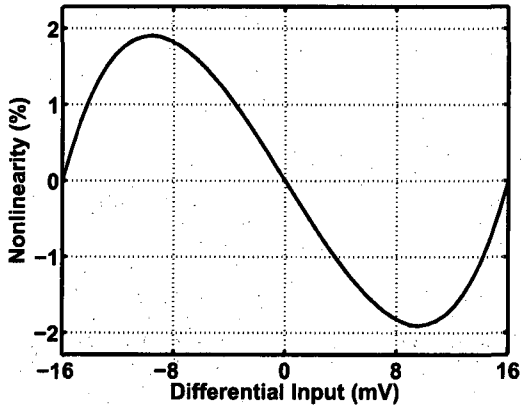


Figure 5.6: Simulated nonlinearity of the op amp.

The closed-loop gain of the op amp is given by

$$A_{closed} = \frac{A_{open}}{1 + A_{open}\beta} \tag{5.11}$$

where A_{open} is the open-loop gain of the op amp and β is the feedback factor. Taking derivative of this equation gives

$$\frac{dA_{closed}}{A_{closed}} = \frac{1}{1 + A_{open}\beta} \frac{dA_{open}}{A_{open}} \tag{5.12}$$

This shows that the open-loop nonlinearity is suppressed by the loop gain. For the current design $A\beta \approx 10$, resulting in a closed-loop nonlinearity greater than 0.1% necessiating calibration.

In order to study the behavior of the op amp in the MDAC environment, we construct the equivalent circuit shown in Fig. 5.7 (without the compensation network). Here, A_j and R_{outj} denote the voltage gain and output resistance

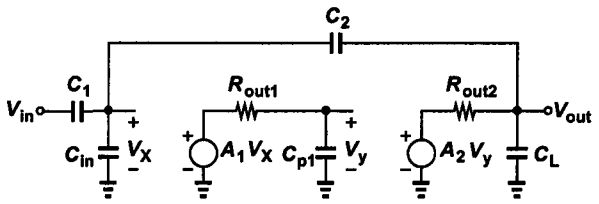


Figure 5.7: Small-signal model of MDAC before compensation.

of stage j, respectively, and C_{p1} models the total capacitance at the output of the first stage. Capacitors C_1, C_2, and C_L represent those required for MDAC operation.

The loop transmission, $T(s)$, can be obtained by setting V_{in} to zero, breaking the loop at V_X and computing the transfer function around the loop. It follows that

$$T(s) = \frac{\beta A_1 A_2}{(\frac{s}{\omega_{p1}} + 1)(\frac{s}{\omega_{p2}} + 1)}, \tag{5.13}$$

where $\beta = C_2/(C_1 + C_2 + C_{in})$ and

$$\omega_{p1} = \frac{1}{R_{out1} C_{p1}} \tag{5.14}$$

$$\omega_{p2} = \frac{1}{R_{out2}[C_L + \frac{(C_1+C_{in})C_2}{C_1+C_2+C_{in}}]}. \tag{5.15}$$

The magnitude of $T(s)$ falls to unity at a frequency given by

$$\omega_u^2 = \frac{-(\omega_{p1}^2 + \omega_{p2}^2) + \sqrt{(\omega_{p1}^2 + \omega_{p1}^2)^2 - 4\omega_{p1}^2\omega_{p2}^2[1 - (\beta A_1 A_2)^2]}}{2}. \tag{5.16}$$

In this design, $\omega_{p1} \approx 2\pi(1.28\text{ GHz})$, $\omega_{p2} \approx 2\pi(3.16\text{ GHz}) \approx 2.47\omega_{p1}$, $\beta \approx 0.303$, and $A_1A_2 = 30$. Thus, $\omega_u \approx 4.36\omega_{p1}$. The phase shift at ω_u is thus given by

$$\angle T(s = j\omega_u) = -(\tan^{-1}\frac{\omega_u}{\omega_{p1}} + \tan^{-1}\frac{\omega_u}{\omega_{p2}}) \tag{5.17}$$

$$= -138°. \tag{5.18}$$

The key observation here is that the phase margin is about 42° before compensation, thereby requiring only a moderate reduction of ω_{p1} so as to reach an adequate amount, e.g., 60°. This stands in contrast to the behavior of typical two-stage op amps, especially if loaded with a significant capacitance, which exhibit a negative or near-zero uncompensated phase margin. Compensated for a phase margin of 60°, the op amp of Fig. 5.5 provides a unity-gain bandwidth of 10 GHz.

The device dimensions and bias currents shown in Fig. 5.5 correspond to those in the first MDAC. The MDAC is scaled down by a factor of two in the second stage and four in the third stage. Stages 4 to 13 remain unscaled due to the small size of the capacitors (25 fF) and negligible power consumption.

The foreground calibration technique proposed herein assumes negligible drift of the MDAC characteristics with temperature. Since the op amp operates in a closed-loop configuration, variation of its characteristics is suppressed by the loop gain. Nonetheless, for a constant bias current, the op amp small-signal gain varies markedly with temperature, degrading the performance[1]. On the other hand, it

[1]The nonlinear terms vary negligibly.

was found from simulations that if the overdrive voltage of the input transistor is kept constant, so is the small signal gain. Using the bias circuit in [32] for this purpose, simulations suggest an SNDR degradation of about 2 dB if the circuit is calibrated at 27°C and the temperature rises to 75°.

5.3 Bootstrapped Switch

To satisfy the linearity requirement (> 60 dB for a 10-bit system) with high input swing (1.2 V peak-to-peak) and fast acquisition time (500 ps), bootstrapped switches [33, 34] are used to sample the analog input. Figure 5.8 shows the conceptual block diagram of the switch. It consists of a MOS transistor M_1,

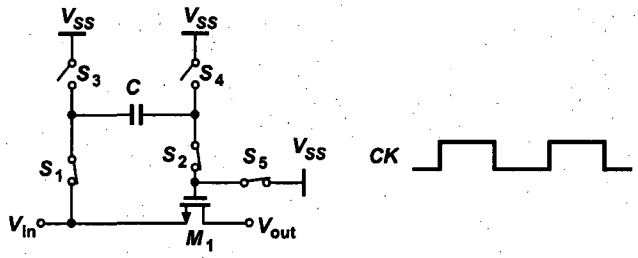


Figure 5.8: Block diagram of the bootstrapped switch.

auxiliary switches $S_1 - S_5$, and a capacitor C. The idea behind bootstrapping is to apply a constant gate-to-source voltage to the MOS transistor independent of the input voltage, V_{in}. It uses both the high and the low phases of the sampling clock, CK. In operation when CK is low, the capacitor C is charged to $V_{DD} - V_{SS}$ and the transistor M_1 is turned off. When CK goes high, the capacitor C *bootstraps* the gate-to-source voltage (V_{GS}) of M_1 to approximately $V_{DD} - V_{SS}$. As compared to V_{GS} in a CMOS switch, V_{GS} in a bootstrapped switch is independent of the input voltage and therefore, the bootstrapped switch exhibits better linearity.

Figure 5.9 shows the implementation of the above concept. Here, transistors

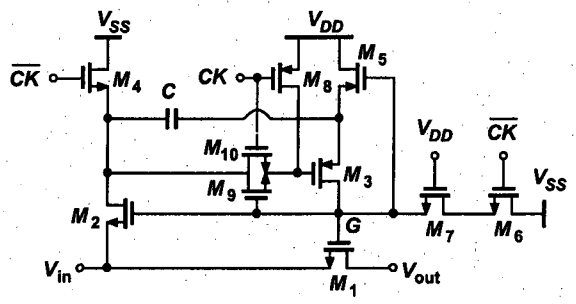


Figure 5.9: Circuit implementation.

$M_2 - M_6$ correspond to the auxiliary switches $S_1 - S_5$. Transistors $M_7 - M_{10}$ improve the reliability and allow rail-to-rail operation of the switch.

Charge on the capacitor, C, is shared by the parasitic capacitance, C_P, present at the gate of transistor M_1. This reduces the gate-source voltage of M_1 as

$$V_{GS} = \frac{C}{C + C_P}(V_{DD} - V_{SS}). \tag{5.19}$$

To mitigate this effect in the design, C is chosen to be approximately ten times larger than C_P to limit the reduction to only up to 10%. Transistors M_2 and M_3 are chosen to be large enough to charge capacitor C to $V_{DD} - V_{SS}$ in the reset phase. Sizes for transistors $M_8 - M_{10}$ are chosen to have a rise and fall time of approximately 50 ps.

Figure. 5.10 shows the simulation setup for testing the linearity of the switch. Here S_1 is the bootstrapped switch while S_2 and S_3 are the CMOS switches. Two non-overlapping clocks ϕ_1 and ϕ_2 control the switches. This arrangement is used as it very closely mimics the input sampling network of the MDAC. (This arrangement is slightly worse, as the capacitor is not reset here.) A single-ended version is shown here for simplicity. In actual simulation a fully-differential version is used.

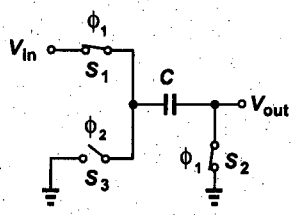


Figure 5.10: Simulation setup for measuring linearity.

The switch is tested by applying a full-scale input (1.2-V_{pp}) at the nyquist frequency (250 MHz). The spectrum of the sampled output is shown in Fig. 5.11. The SNDR is greater than 78 dB, adequate for the 10-bit prototype.

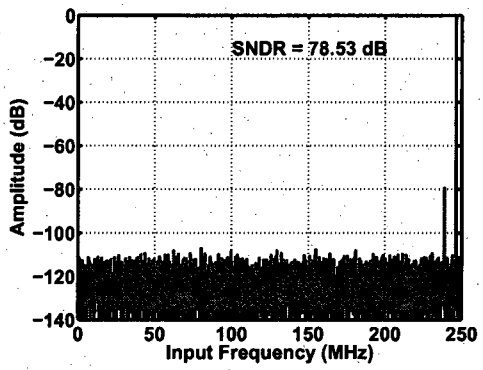


Figure 5.11: Output spectrum.

5.4 Comparator

The sub-ADC inside each stage comprises of two differential comparators with thresholds set at $\pm V_{REF}/4$. To allow rail-to-rail operation, a switched-capacitor input network is used. In the first-stage sub-ADC, the bandwidth of the network is matched with the MDAC, by having the same sizes for the capacitors and the switches, as described in Section 5.1. Later stages do not pose this restriction

and the capacitor sizes are chosen based on matching and common-mode injection errors. The input network for the first and the latter stages are shown earlier in Fig. 5.2 and Fig. 5.3 respectively.

The comparator consists of a pre-amplifier and a regenerative latch. Figure 5.12 shows the schematic. The pre-amplifier provides signal gain and acts as

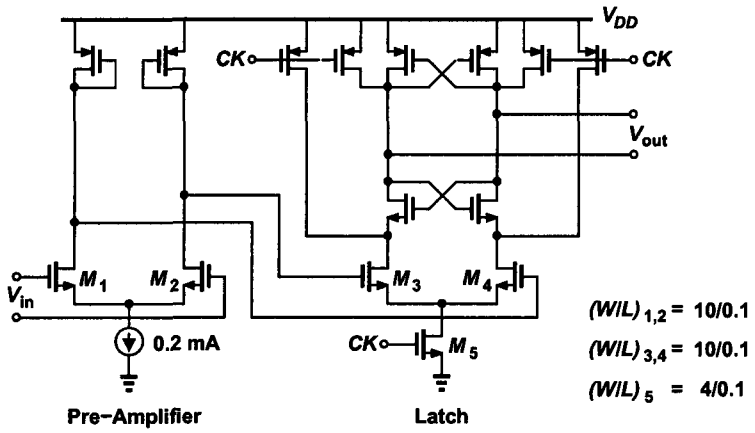


Figure 5.12: Comparator circuit.

a buffer to reduce the kick-back noise on the analog input. Since the redundancy allows large error-correction range, a dynamic latch with almost minimum-size transistors is used. This results in a small area as well as a low power consumption.

In operation, when CK is low, the input voltage is amplified by the pre-amplifier. When CK goes high, input transistors in the latch further amplify the input till the cross-coupled inverters turn on, which then regeneratively amplify the difference to rail-to-rail levels. The digital output is buffered by the inverters and then fed to the control digital circuit.

The devices dimensions shown in Fig. 5.12 are for the comparator used in the first stage. The comparator is scaled down by two in the second stage to reduce

the power consumption. Further scaling was not done, as the power consumption was small, and to minimize the design and layout efforts.

The offset of the comparator was found by simulation. This was done by introducing threshold-voltage mismatch in all the transistors and referred that to the input. The offset is dominated by the input differential pair of the pre-amplifier. The total input referred offset (σ) was found to be around 10 mV. The 3σ offset is therefore much smaller than the error correction range (150 mV) of the sub-ADC.

5.4.1 Metastability

Metastability occurs when the input to any of the comparators in the ADC is close to its threshold and the comparator takes a long time to resolve. In the pipelined ADC, since the comparator decision propagates to both the digital output and the sub-ADC, the inconsistency in interpreting the metastable state by the two circuits may lead to gross errors. As an example, consider the first stage of a 10-bit pipelined ADC implemented with 1.5-bit/stage architecture. The thresholds of the two comparators are set at $\pm V_R/4$, where V_R is the reference voltage. For an input that is very close to the threshold of the first comparator, i.e. $V_{in} = +V_R/4$, the comparator decision is in the metastable state. If the digital output circuit interprets that as a logical one, then $D_{out,1} = 2$, and if the sub-DAC interprets that as a logical zero, then the analog output of the stage is $V_{out,1} = 2V_{in} = V_R/2$. When this output is presented to the later stages in the ADC their combined digital output is $D_{out,BK} = 384$. Combining this with the first stage output gives the total digital output as $D_{out} = 896$. However, the correct digital output for the input at $+V_R/4$ is 640, an error of 256 or $1/4^{th}$ of the full-scale! Since this error occurs in the first stages it is most pronounced. Metastability

errors in the later stages are half as severe as the preceding stages due to the signal-gain of two in each stage.

For a uniformly distributed analog input, probability that a comparator is in the metastable state [35] is

$$P_{Meta} = \frac{V_o}{V_R A} e^{-t_r/\tau}. \tag{5.20}$$

where V_R is the reference voltage, V_o is the output voltage swing required for valid logic levels, A is the pre-amplifier gain, t_r is the resolution time of the latch, and τ is the regeneration time of the latch. For a 1.5-bit/stage pipelined ADC that consists of M stages the probability of a metastable event is

$$P_{Meta,Total} = \frac{2MV_o}{V_R A} e^{-t_r/\tau}. \tag{5.21}$$

However, this is not accurate as it assumes a uniform probability for all stages in the pipeline. For a 1.5-bit/stage architecture the uniform probability distribution at the input is shaped by the transfer function with more points in the range of $-V_R/2$ to $+V_R/2$. This results in slightly increased value of metastability probability for the later stages. It can be shown that for a uniformly distributed input to the ADC the metastability probability for a comparator in stage j is

$$P_{Meta,j} = \left(1 - \frac{1}{2^j}\right) \frac{2V_o}{V_R A} e^{-t_r/\tau}. \tag{5.22}$$

Proof Consider an ideal 1.5-bit stage with transfer function given by $V_{out} = g(V_{in}) = 2V_{in} - DV_R$, where D is the digital output of the stage. For a uniformly distributed input the probability density function is given by

$$f_{V_{in}}(V_{in}) = \frac{1}{2V_R}. \tag{5.23}$$

The probability density function at the output is then [36]

$$f_{V_{out}}(V_{out}) = \sum_k \frac{f_{V_{in}}(V_{in})}{|dg/dV_{in}|_{V_{in,k}=g^{-1}(V_{out})}} \tag{5.24}$$

For $V_{out} < -V_R/2$,

$$f_{V_{out}}(V_{out}) = \frac{f_{V_{in}}(V_{in})}{2} \tag{5.25}$$

$$= \frac{1}{4V_R}. \tag{5.26}$$

For $-V_R/2 < V_{out} < V_R/2$,

$$f_{V_{out}}(V_{out}) = \sum_{k=1}^{3} \frac{1/2V_R}{2} \tag{5.27}$$

$$= \frac{3}{4V_R}. \tag{5.28}$$

And for $V_{out} > V_R/2$,

$$f_{V_{out}}(V_{out}) = \frac{f_{V_{in}}(V_{in})}{2} \tag{5.29}$$

$$= \frac{1}{4V_R}. \tag{5.30}$$

Extending this further the probability density function at the input of stage j is

$$f_{V_{in,j}} = \frac{1}{2^j V_R} \; for \; V_{in,j} < -V_R/2 \tag{5.31}$$

$$= \frac{1 - \frac{1}{2^j}}{V_R} \; for \; -V_R/2 < V_{in,j} < +V_R/2 \tag{5.32}$$

$$= \frac{1}{2^j V_R} \; for \; V_{in,j} > V_R/2. \tag{5.33}$$

A comparator in stage j is metastable if $V_{in,j}$ lies in the region given by $V_{Th} - V_m < V_{in,j} < V_{Th} + V_m$, where V_{Th} is the threshold voltage of the comparator and $V_m = V_o/(Ae^{t_r/\tau})$. The probability of this is given by

$$P(V_{Th} - V_m < V_{in,j} < V_{Th} + V_m) = \int_{V_{Th}-V_m}^{V_{Th}+V_m} f_{V_{in,j}} dV_{in,j} \tag{5.34}$$

$$= \left(1 - \frac{1}{2^j}\right) \frac{2V_o}{V_R A} e^{-t_r/\tau}. \tag{5.35}$$

The probability of a metastable event for an ADC is the sum of metastability probability for all the comparators in the design. So for a pipelined ADC that consists of M 1.5-bit stages

$$P_{Meta,Total} = 2\sum_{j=1}^{M} P_{Meta,j} \tag{5.36}$$

$$= \frac{4V_o e^{-t_r/\tau}}{V_R A}\left[M - \left(1 - \frac{1}{2^M}\right)\right] \tag{5.37}$$

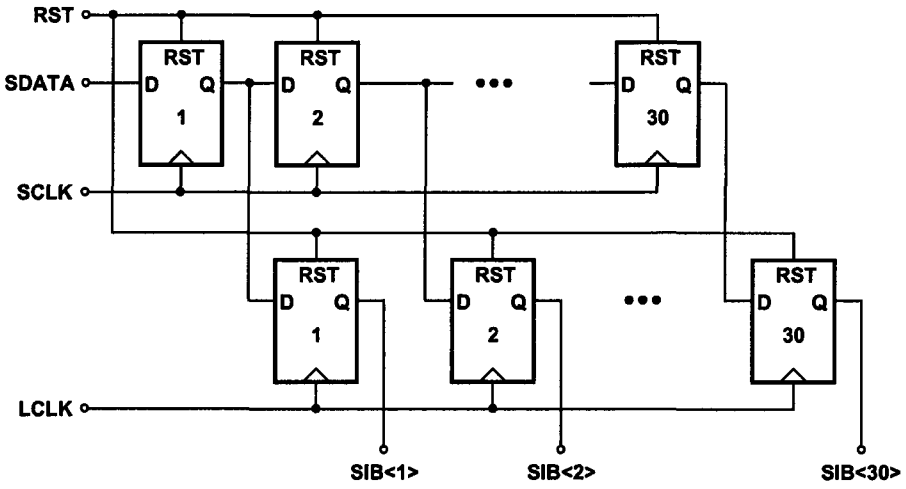
$$\approx \frac{4MV_o e^{-t_r/\tau}}{V_R A}. \tag{5.38}$$

Note that this is twice of what was predicted by Eq. (5.21).

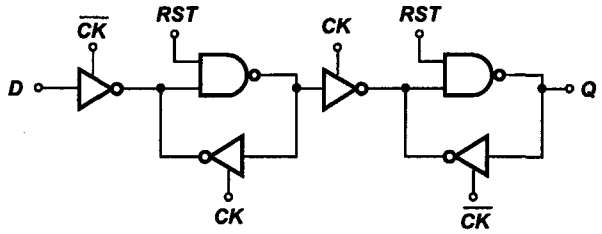
5.5 Serial Interface Bus

The calibration control signals for the ADC was provided from outside. A 4 wire serial interface bus (SIB) was designed to minimize the number of pins and yet provide all the control signals to the prototype. As the name suggests, the data is taken in a serial fashion and is loaded on the configuration register which is 30 bit wide. Figure 5.13(a) shows the implementation details of the bus. Implementation of flip-flop is shown in Fig. 5.13(b). It consists of two pairs of shift registers each 30-bit wide. The data is loaded in a serial fashion to the first shift-register. When the LCLK signal goes high data from the first shift register is loaded to the second shift register in a parallel fashion. This is done so that all the control signals to the prototype are updated at the same time. The four input control signals are the following:

1. SDATA: Serial data input,
2. SCLK: Serial clock input,
3. RST: Reset for the shift register, and



(a)



(b)

Figure 5.13: (a) Serial interface bus and (b) Flip-flop implemenation.

4. LCLK: Load clock.

The output of the SIB is 30 bit wide, and the different fields (from bit 1-30) are the following:

1. SIB<1>: This signal determines whether to choose the calibration reference voltage or the normal reference voltage.
2. SIB<2:10>: This is 9-bit thermometer code input for the reference DAC.
3. SIB<11:20>: This is 10-bit control signals and decides which stage is under calibration in normal mode. (Normal mode is D/A conversion, subtraction and residue amplification.)
4. SIB<21:30>: This 10-bit wide control signal that puts a given stage under calibration in multiply-by-2 mode.

5.6 Clock Generator

Figure 5.14 shows the block diagram of the clock generator system in the ADC. The input to the system is a 1 GHz frequency clock with at least 100 mV peak-

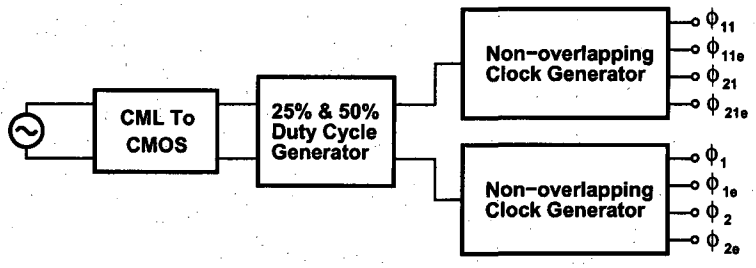


Figure 5.14: Block diagram of the clock generator system.

to-peak swing at a common-mode level of $V_{DD}/2$. This type of waveform is often

called a current-mode-logic (CML) clock. For driving the MOS switches in the MDAC an input clock with rail-to-rail swing is needed. Therefore, it requires a converter that takes a CML input and converts that to CMOS levels, or a CML to CMOS converter block.

Figure 5.15 shows the implementation of the converter. It first amplifies the input signal with a two-stage amplifier. First stage consists of an NMOS input

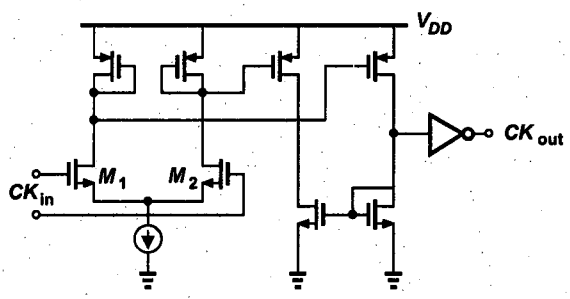


Figure 5.15: CML to CMOS converter.

pair with a diode-connected PMOS loads and in the second stage a push-pull configuration is used. The small-signal gain of the amplifier is about 30 dB. Output of the amplifier is buffered using inverters.

Non-overlapping clocks are required for the switched-capacitor circuits. Figure 5.16 shows the schematic of a circuit that generates such clocks. The output

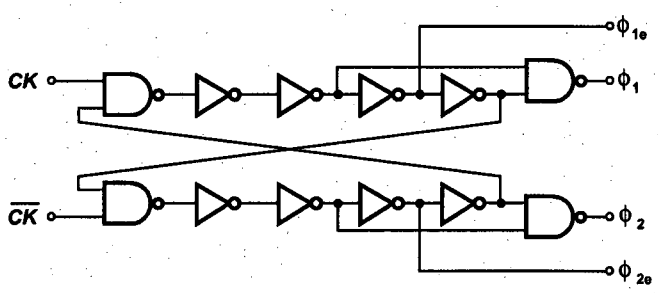


Figure 5.16: Non-overlapping clock generator

waveforms for the clock generator system are as shown in the Fig. 5.17.

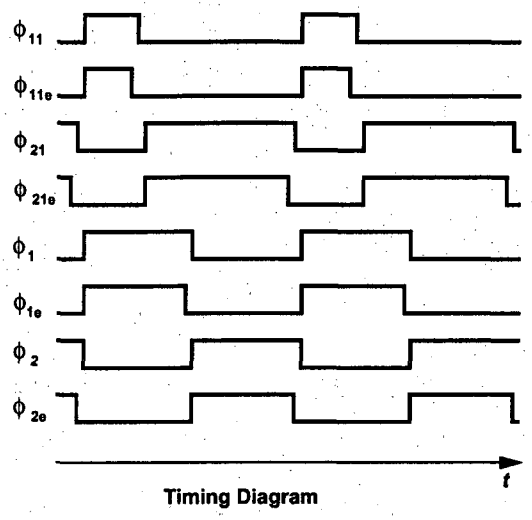
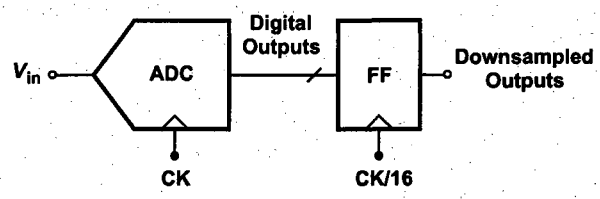


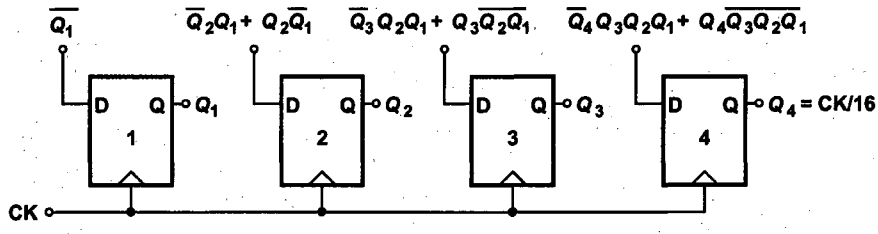
Figure 5.17: Timing diagram.

5.7 Downsampling Circuit

Digital outputs of the ADC are downsampled by a factor of 16. A conceptual block diagram of the downsampling circuit is shown in Fig. 5.18(a), where outputs of the ADC are stored in flip-flops clocked by a divide-by-16 clock. This divide-by-16 clock is generated using a synchronus binary counter implemented using four D-flip-flops (DFFs) and combination logic. The circuit diagram is shown in Fig. 5.18(b). Output of each DFF is denoted by Q_j (j=1$\cdots$4). Input to each DFF is then generated by a combination logic which performs the logical operation shown in Fig. 5.18(b). The output clock is taken from the fourth DFF or Q_4.



(a)



(b)

Figure 5.18: (a) Block diagram of the downsampling circuit and (b) Divide-by-16 clock generator.

5.8 Conclusion

Design of an ADC is a complex process. Many of the blocks mentioned above require multiple iterations to achieve the desired performance. In our approach, we followed a top-down design methodology. We first emulated the entire system in Matlab and used models for different blocks such as op amp (for gain error and non linearity), comparator (for offsets) etc. This helped us in deriving the specifications for the blocks. (E.g., what is the minimum value of gain for the op amp?) After that, we tried different topology for that particular block and picked the one that gave the best results. Final aspect was to simulate the entire design (from PAD to PAD) to see the system performance that required significant amount of time due to the complexity of the system. After the fabrication the prototype was tested and the experimental results are presented in the next chapter.

CHAPTER 6

Experimental Results

The prototype ADC has been fabricated in 90-nm digital CMOS technology. Shown in Fig. 6.1 is the die, whose active area measures 700 μm x 200 μm. MOS

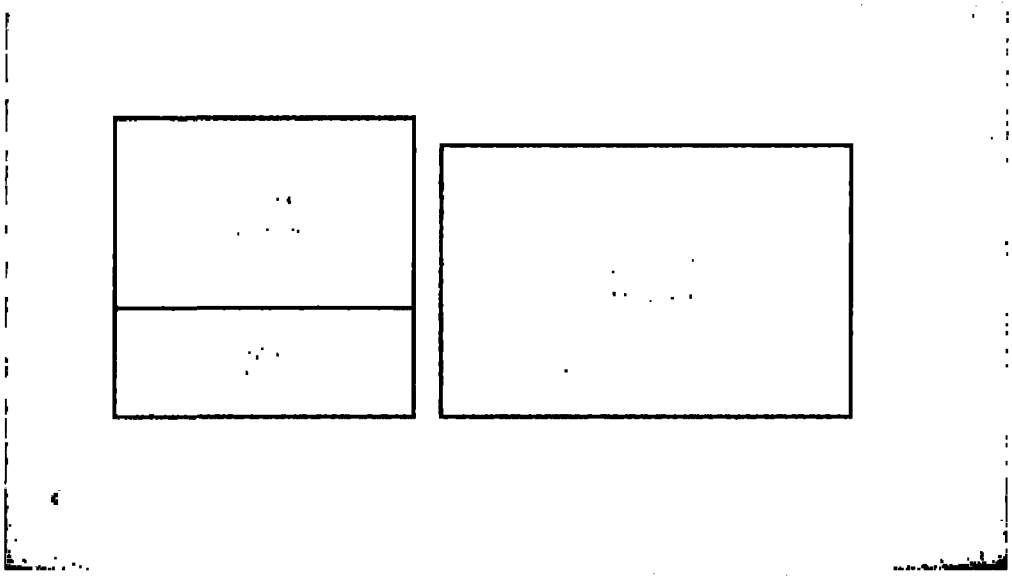


Figure 6.1: Die photograph.

capacitors used for bypassing the reference and the supply lines occupy 700 μm x 500 μm. It is a pad-limited design comprising of 64 pads, of which 27 are digital output pads, two are analog input pads, and the rest are supply, reference, bias, clock and ground pads. The total area of the chip is 2.5 mm x 1.4 mm.

The die has been mounted directly on a printed-circuit board (PCB) to minimize the bond-wire inductance and its associated ringing at high clock frequen-

cies. The PCB design is critical in achieving the performance and a six-layer PCB with four internal plane layers was used. The internal layers are used for the reference and supply lines. A set of four capacitors (0.1 nF, 1 nF, 10 nF, and 100 nF) on these lines are used for high frequency decoupling. The analog input is derived from a low-noise RF generator, band-pass filtered and converted to a differential form using on board RF transformers. A differential clock for the system is also generated in a similar fashion. The open-drain digital outputs are pulled-up using 500 Ω on-board resistors. To simplify testing, the outputs are downsampled by a factor of 16 and captured by the logic analyzer. The data is then transferred to the computer using a general-purpose-interface-bus (GPIB) interface and analyzed in MATLAB [37]. The calibration control signals are also generated on computer and transferred using the parallel-port interface. Operating with a 1.2-V supply, the ADC draws 55 mW, of which 40 mW is consumed by the op amps and 15 mW by the comparators and the clock buffer.

The calibration is run off-chip, but a detailed gate-level synthesis of the calibration logic is performed to estimate the associated power dissipation. Figure 6.2 shows a block diagram of the synthesized system. The complexity is about 20,000 gates. The nonlinearity correction requires the function $y = \alpha_3 x^3$, which, if implemented directly, incurs a considerable area and power penalty. However, the logic can be greatly simplified by observing that the correction term ($\alpha_3 x^3$) is only a few LSBs wide. The adder output (shown as input x) is also truncated to 6 bits and the coefficient α_3 is represented by only 4 bits. The output of this block is truncated to 6 bits. With a clock frequency of 500 MHz in 90-nm CMOS technology, the total power dissipation of the logic is about 8 mW with $V_{DD} = 1.2$ V and 5.6 mW with $V_{DD} = 1$ V.

At the system startup, calibration control signals are applied and data is

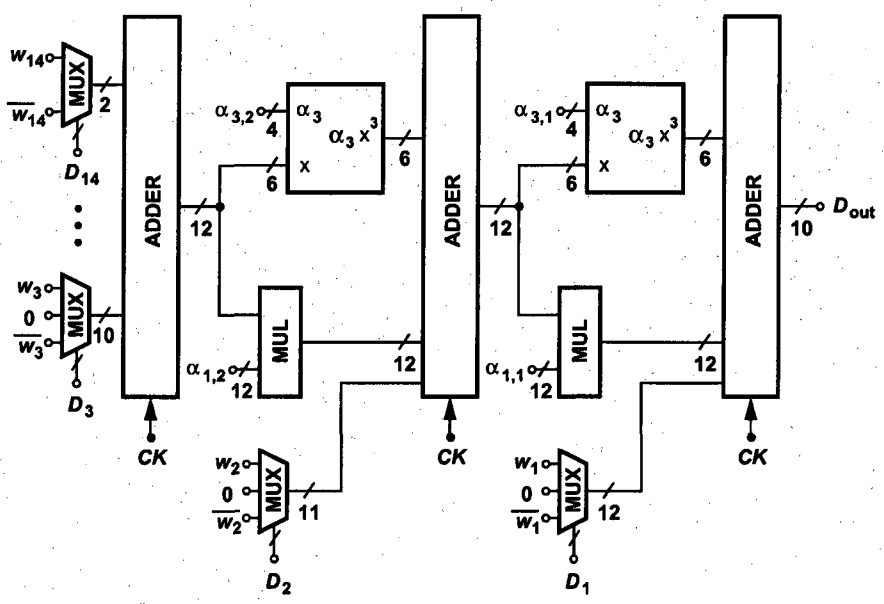


Figure 6.2: Block diagram of synthesized calibration logic.

captured and transferred to the computer. The calibration algorithm (described in Chapter 3) is run and the $\alpha_{1,j}$, $\alpha_{3,j}$, and w_j coefficients are determined.

To characterize the static performance of the ADC, the histogram or code density test was performed. It has been shown in [38], that the minimum number of samples, N_t needed for β-bit precision with 100(1-α) percent confidence is given by

$$N_t \geq \frac{Z^2_{\alpha/2}\pi 2^{n-1}}{\beta}, \tag{6.1}$$

where, $Z_{\alpha/2}$ is the number of standard-deviations for 100(1-α) confidence. In our system, this results in 1 million samples required for 99% confidence with 0.1-bit precision. Since the logic analyzer depth is 512 KSamples, two data sets are needed to get the required 1 million samples. To ensure that the data is not repeated within samples, the input frequency is chosen so that it is not harmonically related to the clock frequency.

The captured data is processed by the computer using the already determined calibration coefficients to get the correct output value. To compare the ADC performance, with and without calibration, first the calibration coefficients are assumed to be ideal (i.e., no correction and $\alpha_{1,j} = 0.5$, $\alpha_{3,j} = 0$ and $w_j = 0.5$), then with real values for $\alpha_{1,j}$ and w_j (i.e., gain error and DAC error correction), and finally with real values for $\alpha_{1,j}$, $\alpha_{3,j}$, and w_j (i.e., gain error, DAC error and nonlinearity correction). Figure 6.3 shows the measured DNL and INL at a sampling rate of 500 MHz for the three cases. The uncalibrated prototype suffers

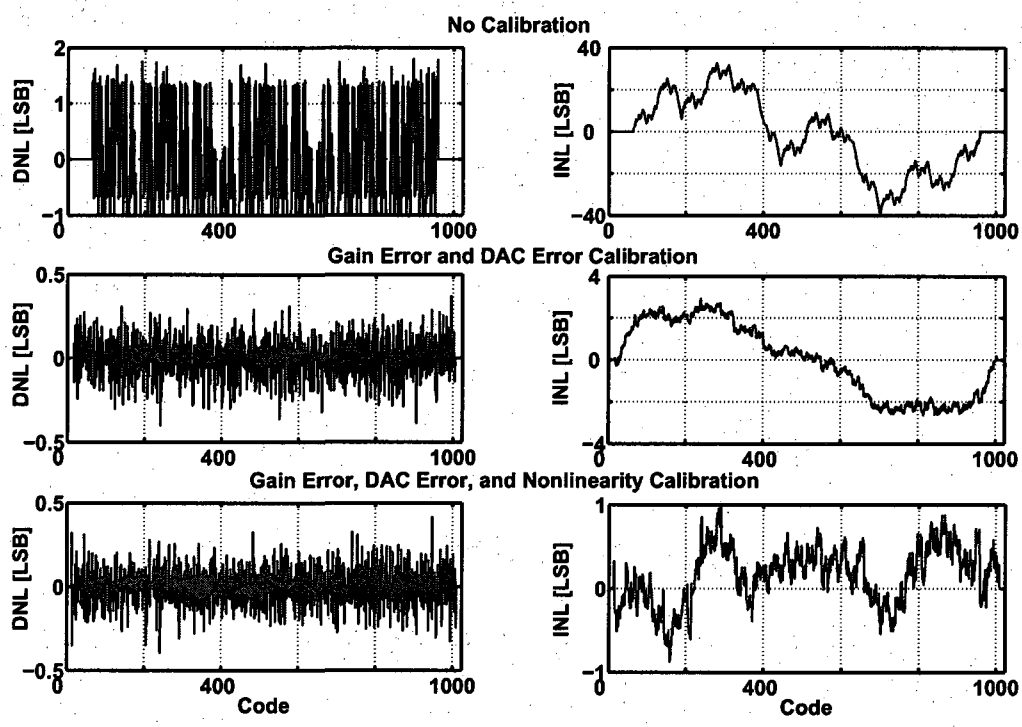


Figure 6.3: Measured differential and integral nonlinearity at a sampling rate of 500 MHz.

from a large number of missing codes and an INL of 40 LSB. After the gain error and the DAC error correction the INL falls below 4 LSB. The shape of INL plots indicates uncorrected third-order nonlinearity of the ADC. After full calibration,

the DNL and INL fall below 0.4 LSB and 1 LSB, respectively.

To measure the dynamic performance of the ADC, the FFT test was performed. The calibrated data is processed by the Hanning window to suppress the spectral leakage [39]. Figure 6.4 shows the measured output spectrum for an input frequency of 10.7 MHz and a sampling rate of 500 MHz. (Due to the

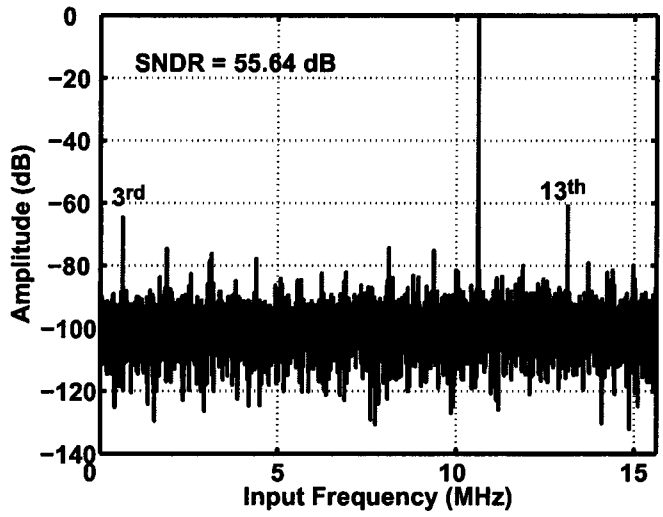


Figure 6.4: Output spectrum for 10.7 MHz input frequency at a sampling rate of 500 MHz.

downsampling factor of 16, the spectrum is shown up to half of 500 MHz/16 = 31.25 MHz.) Since the foreground calibration is performed at a sampling rate of 100 MHz, operation at 500 MHz suffers slightly from uncorrected gain error and nonlinearity. Also, the fifth-order harmonic remains uncorrected and relatively significant.

Figure 6.5 shows the output spectrum for an input frequency of 233 MHz. The SNDR is equal to 52.8 dB, yielding a figure-of-merit (FOM) of 0.3 pJ/conversion. The degradation is partially attributed to the ringing on the external reference lines that feed the sampling capacitors of all of the MDAC stages. Even though

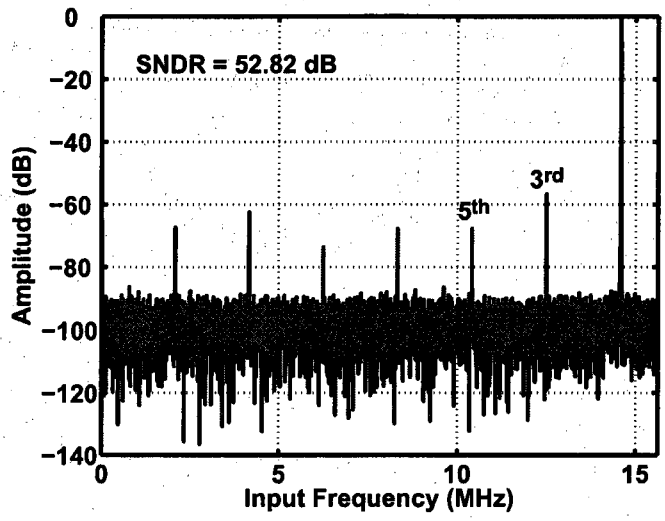


Figure 6.5: Output spectrum for 233 MHz input frequency at a sampling rate of 500 MHz.

a bypass capacitance of 500 pF is tied on-chip between $+V_{REF}$ and $-V_{REF}$, the total capacitance that MDACs switch to these reference reaches 500 fF, creating considerable ringing for a bond wire inductance of greater than 2 nH. It is expected that an on-chip reference buffer improves the dynamic performance.

Figure 6.6 plots the measured SNDR as a function of the analog input frequency at a sampling rate of 500 MHz. The SNDR starts at 56 db for low input frequencies and decreases gradually to 53 dB near nyquist frequencies.

Table I compares the performance of this ADC with that of prior art.

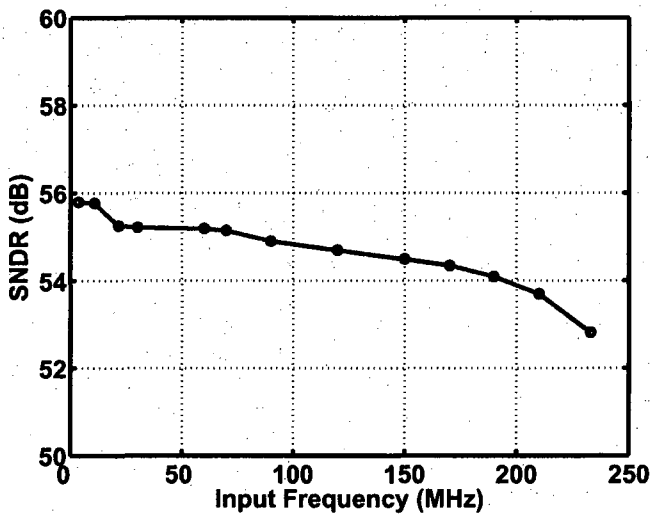


Figure 6.6: Measured SNDR as a function of input frequency at a sampling rate of 500 MHz.

Table 6.1: Comparison with prior art

	This Work	[3]	[2]	[5]	[1]
Resolution	10 bits	10 bits	11 bits	10 bits	11 bits
Conversion Rate	500 MHz	205 MHz	800 MHz	1.35 GHz	1 GHz
Supply Voltage	1.2 V	1.0 V	1.3/1.5 V	1.2/1.6 V	1.2/2.5 V
Input Voltage	1.2 Vpp	1 Vpp	NA	NA	NA
Power (mW)	55	61	350	175	250
SNDR (dB)	52.8	53.9	54	48.1	52
@Frequency (MHz)	@233	@102.5	@400	@675	@500
INL (LSB)	1	0.5	1.6	NA	2
DNL (LSB)	0.4	0.5	0.5	NA	0.7
FOM (pJ/Conv)	0.31	0.65	1.07	0.6	0.77
Technology	90 nm	90 nm	90 nm	0.13 μm	0.13 μm
Active Area	0.5 mm^2	1 mm^2	1.4 mm^2	1.6 mm^2	3.5 mm^2

CHAPTER 7

Conclusion and Future Work

As each generation of CMOS technology continues to further limit the performance of op amps, calibration techniques that deal with not only gain error but also nonlinearity become essential. This dissertation has introduced a pipelined ADC calibration method and an accurate resistor ladder topology that can remove residue gain error, DAC error, and op amp nonlinearity. Owing to a high-speed low-power op amp design, the ADC achieves the highest SNDR reported for a power consumption of 55 mW.

Calibration is performed at the startup and is implemented off-chip in the prototype. The power consumption of the calibration logic (plus the digital correction) is approximately 8 mW at a clock frequency of 500 MHz in 90-nm CMOS technology. The complexity is about 20,000 gates. It is expected that in future generations of CMOS technology the power consumption will reduce further.

The fabricated prototype delivered the performance mentioned here. However, some aspects of the system have room for improvement.

First, the closed-loop gain of the op amp drifts with temperature, degrading the performance if calibration is performed at a different temperature. It is observed in simulations, that a constant overdrive-voltage biasing scheme [32] maintains the gain relatively constant and should be used in the next prototype. Second, the high resistance of the reference DAC limits the speed (100 MHz) at

which calibration is performed. However, due to second-order effects the calibration coefficients are frequency dependent. Therefore, the resistance of the DAC should be made smaller to run the calibration at the system speed (500 MHz). Third, the bond-wire inductance results in considerable ringing on the reference lines at higher speeds even with a 500 pF on-chip bypass capacitor. It could be significantly reduced by using an on-chip reference buffer, although at a considerable power penalty. Finally, the op amp sharing technique can be employed to further reduce the power consumption of the system.

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