A Noise Reduction 12-bit 125-MSPS SAR ADC With Asynchronous Logic Regulation Technique

Daiguo Xu, Hequan Jiang, Dongbing Fu, Guangbing Chen, Shiliu Xu, Jianan Wang, Xiaoquan Yu and Liang Li

***Abstract*—This brief presents a noise reduction 12-bit 125-MSPS successive approximation register (SAR) analog-to-digital converter (ADC) with asynchronous logic regulation technique. With a gain-boosted structure, noise reduction technique is provided in the design of dynamic comparator. Further, an additional positive feedback loop is introduced to reduce the regeneration delay of the comparator. Therefore, the contradiction of equivalent input-referred noise and regeneration delay of dynamic comparator is solved. In addition, an asynchronous logic regulation technique is exhibited to provide long and short delay clocks to enable comparator in the MSB and LSB cycles, respectively. Consequently, the settling time of DAC is enough and the conversion speed of SAR ADC is increased without any redundant cycles. To demonstrate the proposed techniques, a design of SAR ADC is fabricated in 65-nm CMOS technology, consuming 4 mW from 1.2 V power supply with a SNDR >66.7 dB and SFDR >82.1 dB. The proposed ADC core occupies an active area of 0.048 mm^2, and the corresponding FoM is 27.2 fJ/conversion-step at Nyquist rate.**

***Index Terms*—Analog-to-digital converter (ADC); Noise reduction comparator; Asynchronous logic regulation; Successive-approximation-register (SAR) ADC.**

I. Introduction

In recent years, with the feature sizes of CMOS devices scaled down, 10 to 12-bit SAR ADCs could reach sampling rates of tens or hundreds MS/s with excellent power efficiency and small area and provide compact area [1]-[8]. Further, because the SAR ADC does not need residue amplification and the KT/C noise is small with large capacitive DAC array, the equivalent input-referred noise of comparator is the bottleneck in the design of medium and high resolution SAR ADCs. A high-speed dynamic comparator is introduced in [9], but static current is dissipated in the reset/regeneration phases and static power is inevitable. A low power structure is exhibited in [10], which brings no static current. But the regeneration delay is increased. A low regeneration delay with low-power dynamic comparator is provided in [11]. A g_m-boosted StrongARM comparator is provided in [12], which improves the transconductance of comparator to increase the regeneration speed. A low-noise dynamic comparator for high-speed SAR ADCs is shown in [13], the gain of second stage is improved to depress noise. The bandwidth of the comparator is reduced and the regeneration delay will increase. However, the contradiction of equivalent input-referred noise and regeneration delay in dynamic comparator is not solved in [9]-[13]. To avoid generating high frequency clock, asynchronous successive approximation logic is used in the design of SAR ADCs, the delay of asynchronous logic and the settling time of weighted capacitors should match. In order to get enough accuracy, the enable of comparator should after the settling of weighted capacitors. The setting time of MSB capacitors are longer than those of LSB ones. Consequently, the settling time of MSB capacitors and the delay of asynchronous successive approximation logic are the speed bottlenecks in the MSB and LSB cycles, respectively. To increase the conversion speed of SAR ADC loop, short delay of asynchronous successive approximation logic is selected, and several redundant techniques are introduced to calibrate the errors of settling insufficient in MSB cycles [14-15]. Redundant capacitors should be inserted to the capacitive DAC array, that means the bandwidth of sampling net will decrease and the difficulty of DAC layout arrangement is increased. In addition, the calibration methods will increase the complexity and power consumption of SAR ADCs.

This brief proposes a high-speed dynamic comparator with noise reduction technique, the input-referred noise and regeneration delay of dynamic comparator are both reduced by double-positive-feedback and gain-boosted structures, respectively. Moreover, an asynchronous logic regulation technique is also proposed, we provide slow and fast asynchronous logic paths in this design. The slow asynchronous logic is selected in the MSB cycles to satisfy the settling of MSB weighted capacitors, the fast asynchronous logic is chose in the LSB cycles to realize the speed improvement of whole SAR ADC. Without any redundant bit techniques, the performance of the SAR ADC is improved and the complexity and power consumption is also reduced.

The remainder of the work is divided into four sections. In Section II, the proposed SAR ADC architecture and design considerations are introduced. Section III provides the key techniques and detailed circuit blocks. Finally, Section IV and V give the measurement results and conclusions, respectively.

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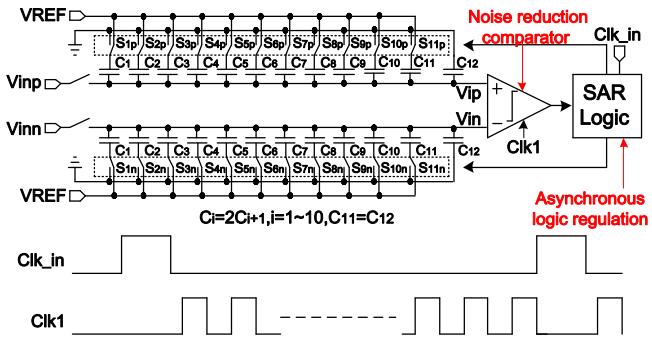

Fig. 1. The proposed 12-bit 125-MSPS SAR architecture and time sequence.

II. Proposed SAR ADC Architecture and Design Considerations

The 12-bit 125-MSPS SAR architecture and time sequence are presented in Fig. 1. When Clks is 1(sampling phase), the sampling switch will turn on to sample differential input signals Vip/Vin. Clk1 will trigger the noise reduction comparator to generate 12 bit digital output codes in serial when Clks is 0 (conversion phase). As shown in Fig. 1, to avoid using an accurate common mode voltage and provide better common-mode rejection ratio, the weight capacitors C_i (i=1 to 10) are split into two equal sub-capacitors, the sub-capacitors are connected to negative (GND) and positive (VREF) references in sampling phase. For 12 bit SAR ADCs, larger unit capacitor could improve the match of DAC array, the unit capacitor is set to 2 fF by using MOM capacitor from the mismatch table of foundry. In order to achieve higher linearity, the differential $V_{p\text{-}p}$ of input signal is set to 1.6 V. To minimize the parasitic capacitance of sampling plate to ground, the weighted capacitors C_i (i=1 to 12) are designed by metals of M5~M7. Because of the parasitic capacitance from sampling plate to ground, the real LSB is about 0.36 mV. To achieve fast sampling speed (~125 MS/s) with charge injection and clock feedthrough effects depression, boosting sampling switch with moderate area (45 μm/60nm) is used. The kT/C noise is about 0.04 mV *rms*, it indicates that the input-referred noise of dynamic comparator should smaller than 0.16 mV *rms*.

III. Key Techniques of SAR ADC and Design Implementation

A. *High-speed dynamic comparator with noise reduction technique*

A high-speed dynamic comparator with noise reduction technique is illustrated in Fig. 2 (a). Firstly, PMOS input pairs are used in the 1st stage to reduce the 1/f noise and a gain is provided to improve the noise performance. Secondly, we keep the main structure of [11] in the design of 2nd stage, M18 in Fig. 2 (a) is triggered by enabled signal clk directly to eliminate the intended delay in [11]. The fast positive feedback path (feedback loop1) could provide a high-speed regeneration. Moreover, unlike only one positive feedback loop (feedback loop1) in conventional dynamic comparators, another positive feedback loop (feedback loop2) is provided by M14-M17 in

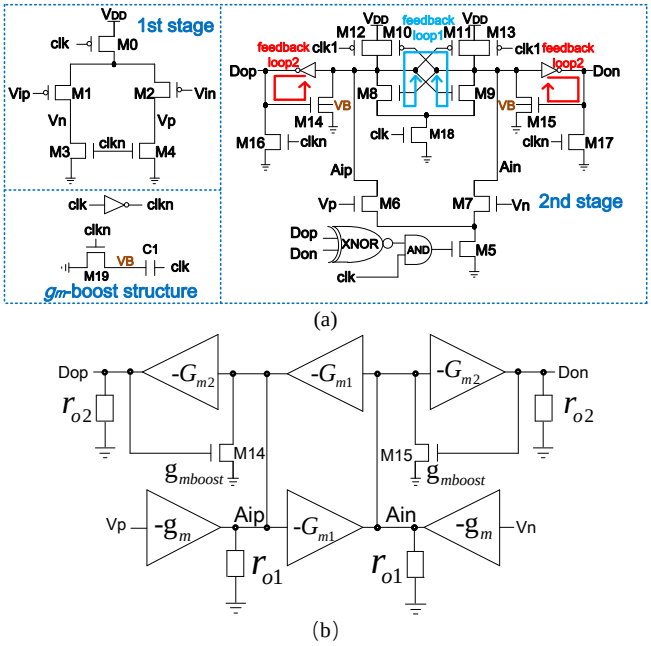

Fig. 2. (a) Proposed high-speed dynamic comparator with noise reduction technique and (b) small-signal mode in saturation region of the 2nd stage.

this structure. When clk is 0 and clkn is 1, the comparator is in reset phase, M5, M14, M15 are turned off and M16, M17 are turned on, there is no static power consumption in the proposed comparator. When clk changes from 0 to, the comparator enters regeneration phase, the proposed positive loops (feedback loop1 and loop2) are both enabled. Unlike the pull-down NMOS in [12], the operation of feedback loop2 is closely related to input differential signals Vip and Vin. With meta-stability depression compared to [12], regeneration delay of the proposed comparator is reduced obviously by the double-positive-feedback structure. Although this proposed positive feedback enhanced technique will increase the parasitic capacitance of Aip/Ain slightly, the regeneration speed of the proposed comparator is increased obviously compared to [9]-[13]. Small-signal mode in saturation region of the 2nd stage is illustrated in Fig. 2 (b). Because of the symmetrical structure, r_{o1} and r_{o2} are the impedances of Aip/Ain and Dop/Don, respectively. $-g_m$ and $-G_{m1}$ are the transconductances of M6/M7 and inverters (M8/M10 and M9/M11), g_{mboost} and $-G_{m2}$ are the transconductances of M14/M16 and inverters. We could obtain four equations by Kirchhoff's current law as

$$[\Delta Vp(-g_m)+\Delta Ain(-G_{m1})+\Delta Dop(-g_{mboost})]r_{o1}=-\Delta Aip\,, \quad (1)$$

$$[\Delta Vn(-g_m)-\Delta Aip(-G_{m1})-\Delta Don(-g_{mboost})]r_{o1}=\Delta Ain\,, \quad (2)$$

$$-\Delta Aip(-G_{m2})r_{o2}=\Delta Dop\,, \quad (3)$$

$$\Delta Ain(-G_{m2})r_{o2}=-\Delta Don\,, \quad (4)$$

The small-signal gain of the 2nd stage (A) can be approximately expressed as

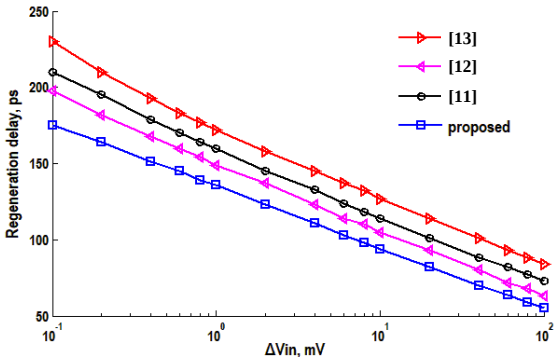

Fig. 3 The comparisons of regeneration delay versus different inputs

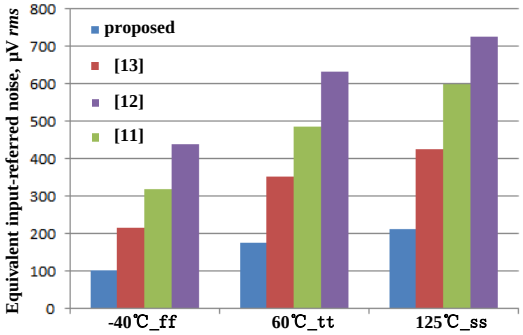

Fig. 4 Equivalent input-referred noises against temperature with transient noise analysis

$$A = \frac{g_m r_{o1}}{\frac{G_{m1} r_{o1}}{G_{m2} r_{o2}} - g_{mboost} r_{o1}}, \quad (5)$$

We could know that the small-signal gain of the 2nd stage (A) will increase as the increase of g_{mboost} from equation (5). Consequently, the input-referred noise of the comparator could be reduced. Meanwhile, the bandwidth of the proposed comparator is not reduced. We use the substrate voltage coupled technique in [16] to increase the g_{mboost} in equation (5). The transconductance of NMOS could be expressed as

$$g_m = \mu_n C_{OX} \frac{W}{L} [V_{GS} - (V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}))], \quad (6)$$

Where μ_n and C_{OX} are mobility ratio of electron and oxide layer capacitance of NMOS, W/L is the width to length ratio, V_{GS} is the gate-source voltage of NMOS. γ and Φ_F are constants, V_{SB} is the source-substrate voltage of NMOS, V_{TH0} is the threshold voltage when V_{SB} is 0. The g_m boost structure is also shown in Fig. 6 (a), clk is 0 and clkn is 1 when the comparator is in reset phase, M19 is turned on, the substrate voltages of M14/M16 (VB) are set to 0. When the comparator enters regeneration phase, clk changes from 0 to 1, M19 is turned off by clkn and VB is coupled to a higher voltage by $C1$. The g_{mboost} is increased 35% as $C1$ changes from 0 to 3fF and VB changes from 0 to 0.4V. As the variation of PVT, the leakage current of M14/M16 caused by the g_m boosted structure is smaller than 1.5 nA with $C1$ is smaller than 3fF. The gain of the proposed comparator is improved by the gain-boost structure, the equivalent input-referred noise of comparator is obviously reduced compared to conventional structures.

To evaluate the performance of the proposed high-speed and noise reduction dynamic comparator, four types of comparators

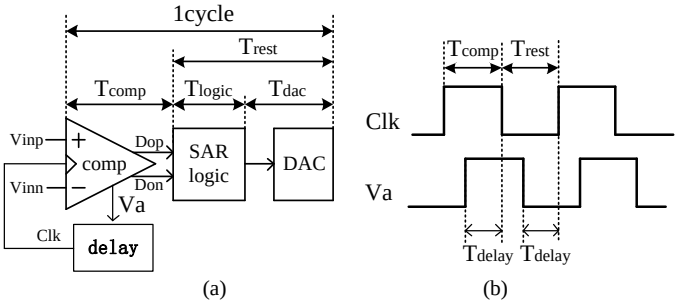

Fig. 5 (a) The delay distribution of asynchronous SAR and (b) timing diagram

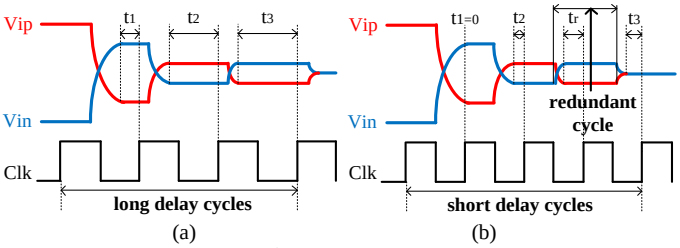

Fig. 6 Approximation examples of Vip and Vin. (a) With long delay cycles and (b) with short delay cycles

are designed in a 65 nm CMOS technology under the same values of input/output parasitic capacitance and latch size, post-simulation based comparison to [11]-[13] and the proposed one is done. The comparisons of regeneration delay versus different inputs are shown in Fig. 3. Because of double-positive-feedback technique, the proposed comparator provides shorter regeneration delay which is reduced about 16.3% that of [11] and 10% that of [12]. Fig. 4 shows the simulation results of the comparator noise obtained with Spectre transient noise simulation with supply voltage changing of 3%. With the proposed noise reduction technique, the equivalent input-referred noise of proposed comparator is about 175 μV *rms* at 60°C (typical corner), which is smaller than those of [11] (487 μV *rms*) and [13] (352 μV *rms*). The equivalent input-referred noise reductions in -40°C (ff corner) and 125°C (ss corner) are more than 22.4% and 30.5%, respectively. After 200 runs Monte Carlo simulations, the maximum variation of offset is smaller than 4 LSB, only a DC error is introduced for single channel SAR ADC.

B. Asynchronous logic regulation technique

The delay distribution of asynchronous SAR is exhibited in Fig. 5 (a), the comparator (comp) is in reset and regeneration phase when Clk is 0 and 1, respectively. When Dop and Don are reset to the same voltage in the reset phase, Va is set to 0. When Dop and Don are with different voltages in the regeneration phase, Va is set to 1. Because of the delay block in Fig. 5 (a), there is a T_{delay} between the rising/falling edges of Va and the falling/rising edges of Clk in Fig.5 (b). In order to ensure the accuracy of SAR ADC, the triggering of comparator should after the settling of weighted capacitors, that means long delay cycles of Clk is selected. Approximation examples of Vip and Vin with long delay cycle is shown in Fig. 6 (a), the settling time of weighted capacitors will decrease as the going of approximation. It indicates that the settling time of Vip/Vin will decrease as the progress of approximation and the delays between settling of DAC and rising edge of Clk (t1, t2 and t3) will increase, extra time is wasted in the LSB cycles and the

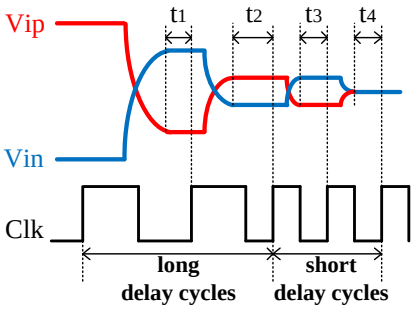

Fig. 7 Approximation examples of Vip and Vin with asynchronous logic regulation technique.

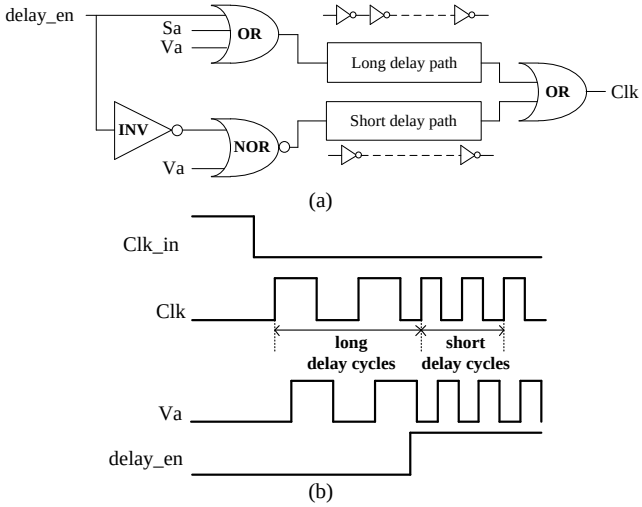

Fig. 8 (a) The schematic and (b) timing diagram of the asynchronous logic regulation technique

conversion speed of SAR ADC is reduced. Redundant bit is introduced in [14]-[15] and short delay cycles of Clk is provided in Fig. 6 (b). A redundant cycle is provided to calibrate the incomplete settling of Vip/Vin in MSB cycles. Further, the short delay cycles of Clk could reduce the unnecessary waiting time of comparator obviously. However, there are some drawbacks of redundant technique. Firstly, the additional redundant weighted capacitors will deteriorate the matching of DAC layout and reduce the bandwidth of sampling net. Moreover, extra calibration technique should be introduced, the complexity and power consumption of design will increase and the redundant cycles will increase the number of whole cycles, the improvement of conversion speed is limited.

Approximation examples of Vip and Vin with asynchronous logic regulation technique is shown in Fig. 7, in order to improve the accuracy of SAR ADC, we provide long delay cycles of Clk in the settling of MSB weighted capacitors to make the triggering of comparator after the settling of weighted capacitors. Meanwhile, to improve the conversion speed of SAR ADC, we provide short delay cycles of Clk in the settling of LSB weighted capacitors to reduce the unnecessary waiting time of comparator. No redundant weighted capacitor is added to DAC array, the match of weighted capacitors will improved and the complexity and power consumption will also decrease. The schematic and timing diagram of the asynchronous logic regulation technique are shown in Fig. 8 (a) and Fig. 8 (b), respectively. As exhibited in Fig. 8 (a), the input/output of the

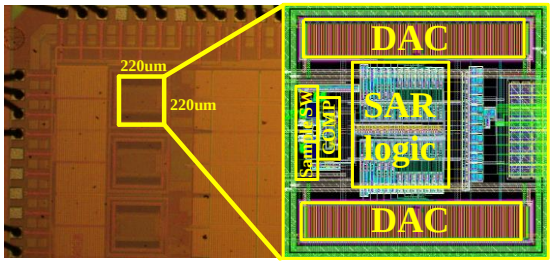

Fig. 9. The die micrograph of proposed SAR ADC

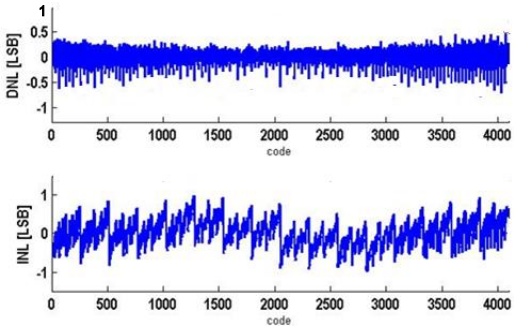

Fig. 10. Measured DNL and INL

TABLE I
THE PERFORMANCE COMPARISONS

	[3]	[5]	[7]	[8]	**This Work**
Technology (nm)	40	65	90	65	**65**
Supply (V)	0.9	1.2	1.2	1.2	**1.2**
Sampling rate (MS/s)	100	100	120	120	**125**
SNDR (dB)	67.3	61.5	64.3	63.3	**66.7**
ENOB (bit)	10.9	9.9	10.4	10.2	**10.8**
SFDR (dB)	82	81	81	74.6	**82.1**
Power (mW)	2.6	1.9	3.2	3.2	**4**
FoM (fJ/conv)	14.6	21.3	28	28	**27.2**
Area (mm^2)	0.014	0.03	0.04	0.42	**0.048**

long delay path are opposite and the input/output of the short delay path are identical. The long/short delay paths will provide long/short delays, respectively. SAR ADC is in sampling phase when Clk_in is 1, the asynchronous approximation phase will begin when Clk_in changes from 1 to 0. The corresponding rising edges will be provided one by one from the SAR logic technique in [16], we choose the 2nd rising edge as delay_en in Fig. 8 (b). The long delay path is selected before the rising edge of delay_en and the short delay path is selected after the rising edge of delay_en. Consequently, the delay of Clk could be regulated with the asynchronous logic regulation technique, the contradiction of accuracy and speed is relieved without redundant bit technique. In addition, the matching of DAC layout is improved and the complexity and power consumption of SAR ADC are also reduced. The average conversion speed is increased 29% with the variation of PVT compared to conventional structures.

IV. MEASUREMENT RESULTS

The proposed SAR ADC is designed in 1P9M 65nm CMOS technology. The die micrograph of proposed SAR ADC is shown in Fig. 9. The core area is 220 μm×220 μm. The

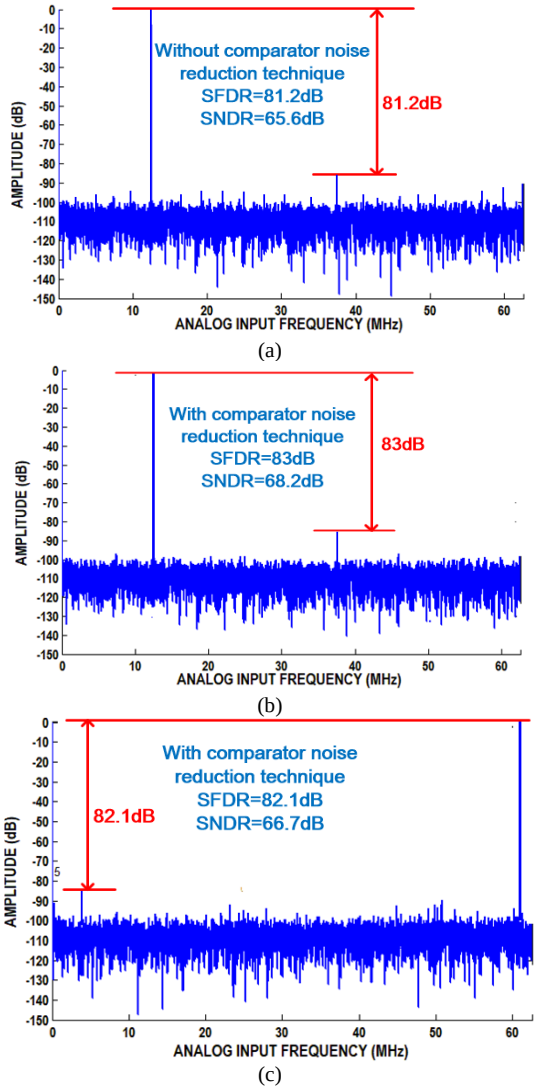

Fig. 11. Measured FFT spectrums with sampling rate 125 MS/s. (a) 12 MHz input without the proposed comparator noise reduction technique, (b) 12 MHz input with the proposed comparator noise reduction technique, (c) 61 MHz input with the proposed comparator noise reduction technique.

measurements of DNL and INL of the proposed ADC are shown in Fig. 10. The peak DNL and INL are -0.75/+0.47 LSB and -0.97/+0.95 LSB. The measurement results with 12 MHz input without and with proposed techniques are shown in Fig. 11 (a) and Fig. 11 (b), respectively. Without the presence of the comparator noise reduction technique, the signal to noise and distortion ratio (SNDR) is 65.6 dB, which is limited by the noise of comparator. By using the proposed comparator noise reduction technique, the SNDR improves from 65.6 dB to 68.2 dB. In addition, the ENOB is increased from 10.6 to 11, the improvement of spurious free dynamic range (SFDR) is around 1.8 dB. The measured FFT spectrum at 61 MHz input with comparator noise reduction technique is shown in Fig. 12 (c), which achieves a SFDR of 82.1 dB and a SNDR of 66.7 dB. Table I shows the performance comparisons of the 12b SAR ADCs with sampling rates from 100 MS/s to 125 MS/s. The proposed SAR ADC achieves an area of 0.048 mm^2 and a figure-of-merit (FoM) of 27.2 fJ/conversion step at Nyquist rate.

V. Conclusions

A 12-bit 125-MSPS 4 mW SAR ADC with comparator noise reduction and asynchronous logic regulation techniques is proposed. The equivalent input-referred noise and regeneration delay of proposed comparator are both reduced by gain-boosted and double-positive-feedback structures, respectively. Further, the cycle delay could be regulated to make the settling time of MSB cycles sufficient and improve the conversion speed of LSB cycles. The proposed SAR ADC gives a > 66.7 dB SNDR and achieves SFDR > 81.2 dB with a FoM of 27.2 fJ/conv-step at Nyquist rate.

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