A 12-b 1-GS/s 31.5-mW Time-Interleaved SAR ADC With Analog HPF-Assisted Skew Calibration and Randomly Sampling Reference ADC

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***Abstract*— This paper presents a 12-b, 1-GS/s ADC array, realized by time-interleaving four 250-MS/s pipelined SAR ADCs, with integrated on-chip reference voltage buffers. A reference ADC-based calibration algorithm treats static nonlinearity, gain, and offset errors in the array. Timing-skew errors between the sub-ADCs are distinguished from those of the gain mismatches by the assistance of an analog high-pass filter (HPF) for input slope information and subsequently corrected by digitally controlled delay lines (DCDLs). Directly driven off the on-chip 50-Ω termination resistors without any dedicated input buffer, the 65-nm CMOS prototype ADC array also employs a frequency-hopped, randomly-sampling scheme for the ref. ADC, eliminating the spectral effect of its interference to the main array. The core ADC consumes 31.5 mW and occupies an area of 0.27 mm^2, including nine on-chip reference voltage buffers, the ref. ADC, and the HPF path. The measured peak signal to noise and distortion ratio of the array is 65.3 dB, and the measured spurious-free dynamic range is >70 dB from dc to 500 MHz at 1 GS/s with calibration. The prototype ADC chip achieves an figure of merit of 20.9 and 59.7 fJ/step (the latter is limited by the jitter of an off-chip clock source) for a low-frequency input and a Nyquist input, respectively.**

***Index Terms*— Pipelined SAR ADC, random frequency-hopped sampling, reference ADC interference, skew calibration, time-interleaved ADC array.**

I. Introduction

TIME-INTERLEAVING (TI) successive-approximation-register (SAR) ADCs presents a tempting solution to achieving low-power, 12- to 14-b, giga-sample-per-second+ ADCs for direct-sampling applications in advanced CMOS nodes. However, as in any TI-ADC array, the approach suffers from the path-mismatch errors (e.g., gain, offset, and timing-skew mismatch errors) that can severely limit the spectral performance of the array. In practice, calibration is often applied to a TI-ADC array to treat the interleaving artifacts. A reference ADC-based calibration technique was reported in [1], in which a slow-but-accurate ref. ADC digitizes the same input signal along with the interleaved sub-ADC array. By equalizing the decimated digital outputs of the sub-ADCs to those of the ref. ADC, the inter-sub-ADC mismatch errors and the intra-sub-ADC linearity errors can all be corrected. Later works extended the technique to treating the timing-skew errors [2]–[4]. In [2], the input derivative information is extracted by two slow-but-accurate ref. ADCs; the skew is then estimated by dividing the skew error by the input derivative. In [3] and [4], a full-speed, low-resolution ref. ADC, which is free of any timing error, is used as the timing reference for the main array.

One key issue of the ref. ADC-based calibration approach is the interference between the ref. ADC and the main ADC array, coupled through the input network, when separate input drivers are absent at the chip front end [5]–[7]. In general, as the ref. ADC is an accurate ADC running at a decimated sample rate to calibrate all sub-ADCs in turns, its loading on the input network and kickback interference to the sub-ADCs are time-variant in nature, which can lead to spurious tones (as a function of the ref. sample rate) in the array spectrum. Employing a separate input buffer for the ref. ADC is an obvious remedy to this issue. However, the extra power and the high-linearity specs of the buffer are nontrivial design challenges. In this paper, we propose a frequency-hopped, randomly-sampling scheme for the ref. paths, thus eliminating the spurious tones due to the ref. interference. While capable of being deployed as a stand-alone treatment, the technique can also function effectively when the ADC input buffers are employed, as is often done in commercial parts.

This paper is organized as follows. Section II describes the architecture of the prototype ADC array. Section III introduces the calibration algorithm that corrects the interleaving errors. Section IV covers the sample-point randomization technique for the ref. paths. Section V presents the circuit implementation detail of the prototype chip, followed by the experimental results of both the foreground (FG) and background (BG)

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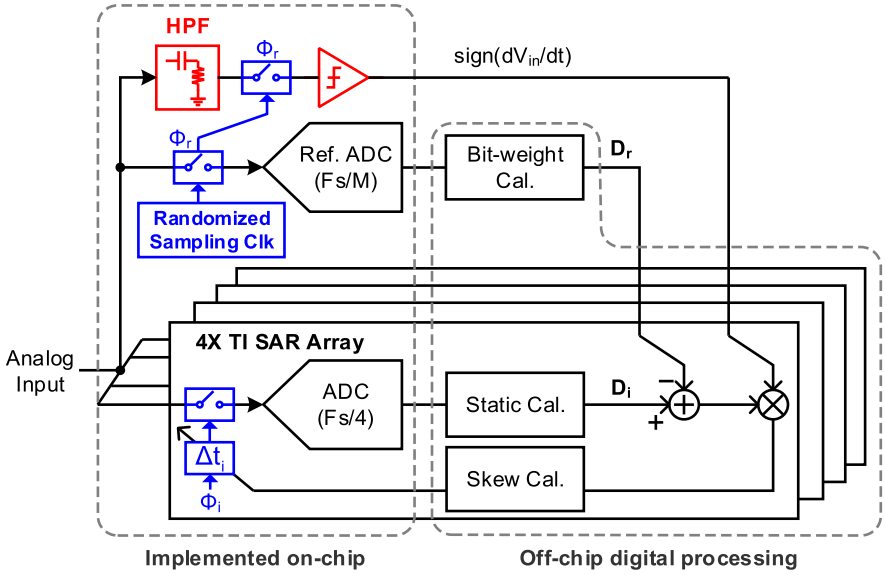


Fig. 1. Block diagram of the TI-ADC array with analog HPF-assisted timing-skew calibration.

calibrations in Section VI. Finally, Section VII concludes this paper.

II. ADC Architecture

The block diagram of the four-way TI-ADC array is shown in Fig. 1. The sub-ADCs employ a power-efficient pipelined SAR architecture with on-chip reference buffers and asynchronous SAR logic to achieve a 250-MS/s sample rate and a 12-b resolution. Besides a slow ref. ADC, a high-pass filter (HPF) trailed by a single comparator (i.e., a 1-bit ADC) is also implemented on-chip for input slope detection. A decimated split-ADC configuration, consisting of the slow ref. ADC and one sub-ADC, is employed to correct the static errors in the array [8], including the first-stage DAC mismatch and the inter-stage gain errors within the sub-ADCs, as well as the offset and gain mismatch errors between the sub-ADCs. The static errors are corrected in the digital domain by adjusting five bit-weight (radix) and one-offset taps for each sub-ADC. The timing-skew errors are identified by jointly examining the outputs of the ref. ADC, the HPF path, and the sub-ADCs, a.k.a. the direct-derivative-information (DDI) method [9]. Four digitally controlled delay lines (DCDLs) are implemented on-chip, each for fine-tuning the sample clock timing of one sub-ADC. The ref. ADC, which is a single-stage SAR, employs a small sample capacitor of 30 fF to minimize its kickback to the ADC input. Furthermore, a frequency-hopping scheme is implemented on-chip to randomize the ref. ADC sample points to eliminate any spectral spurs due to the time-varying loading effect and kickback noise of the ref. path.

In the prototype reported in this paper, the SAR control logic and the ref. sample-randomization logic are all integrated on-chip. The calibration functions of the sub-ADC bit weight, inter-sub-ADC gain, and offset extraction and correction, as well as the DCDL control code update, are realized in a desktop PC; the communication between the PC and the chip is facilitated by an on-chip scan chain.

III. Calibration of Time-Interleaved ADC Array

A. Calibration of Static Mismatch

The split ADC [10] is a popular way to improve ADC linearity, in which the quantization is done via two parallel ADCs with different transfer functions. The nonlinearity information is extracted from the difference between the two digital outputs and is used to linearize both ADCs. Only when both ADCs are linearized, their outputs will be consistent for different input values. Usually, a one-bit pseudorandom noise (PN) can be injected into one of the ADCs to result in a differing quantization trajectory [8]. In this paper, a decimated split-ADC configuration is utilized to calibrate not only the static mismatches between various sub-ADCs in the array but also the capacitor mismatch and inter-stage gain errors within each sub-ADC. In the conventional split-ADC configuration, every input sample is processed by the two ADCs, and the outputs are averaged between the two with a 3-dB SNR benefit. However, in our configuration, since the ref. ADC is clocked at a much lower rate, it cannot be paired with each sub-ADC for all the samples; the pairing instead happens in a decimated fashion. The term "decimated split-ADC" specifically indicates that the "split" is enabled only when the ref. ADC samples together with one sub-ADC for the calibration purpose, in contrast to the conventional sense, reported in [10].

In this paper, as shown in Fig. 2, the ref. ADC is clocked at F_s/M on average, and the sub-ADCs are clocked at $F_s/4$. When the two paths are aligned to sample the input, the split-ADC calibration is enabled to update the bit weights of the two ADCs in the digital domain. The ref. ADC rotates across all sub-ADCs and all conversion paths including the ref. ADC itself that will eventually get linearized. Because the ref. ADC is unique, all sub-ADC characteristics are automatically equalized upon this round-robin treatment.

One key difference between the decimated split-ADC array calibration and the ref. ADC-based calibration [1], [9] is that

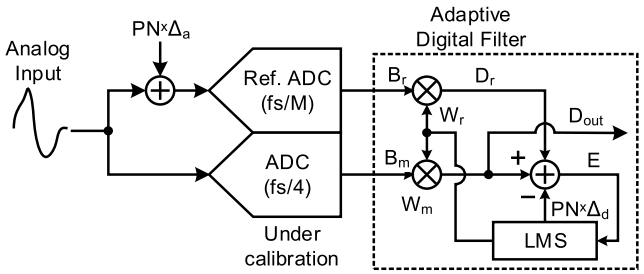


Fig. 2. Decimated split-ADC calibration of the ref. ADC and the sub-ADCs.

in the latter, the ref. ADC is linear to begin with, whereas in the decimated split-ADC array calibration, both the ref. ADC and the sub-ADCs in the array are calibrated at the same time. As a result, the linearity specs and, thus, the design complexity of the ref. ADC is relaxed.

The sub-ADCs employ a 5-bit first stage and an 8-bit second stage; both are SARs. The corresponding radix calibration equation is

$$D_m = \sum_{i=0}^{4} B_{m,i} W_{m,i} + D_{m,R} W_{m,5} + W_{m,\mathrm{OS}} \tag{1}$$

where $B_{m,i} (i = 0 \ldots 4)$ are the five raw output bits of the first stage starting from the MSB. $D_{m,R}$ is the combined digital output of the second stage without calibration. $W_{m,i} (i = 0 \ldots 4)$ are the bit weights associated with the DAC capacitors of the first stage. $W_{m,5}$ is the bit weight associated with the interstage gain. $W_{m,\mathrm{OS}}$ stands for the offset voltage between the ref. ADC and the sub-ADC under calibration. The subscript m in (1) ranges from 0 to 3 for the four sub-ADCs.

The radix calibration equation for the ref. ADC is

$$D_r = \sum_{i=0}^{4} B_{r,i} W_{r,i} + D_{r,R} W_{r,5} - PN \times W_{r,PN} \tag{2}$$

where $B_{r,i} (i = 0 \ldots 4)$ are the first five raw output bits of the ref. ADC, starting from the MSB. $D_{r,R}$ is the combined digital output of the remaining bits, which are not calibrated. PN is a pseudorandom bit sequence, which sets the perturbation in the split-ADC calibration [8]. $W_{r,i} (i = 0 \ldots 4)$ are the bit weights corresponding to the first five DAC capacitors. $W_{r,PN}$ is the bit weight associated with the capacitor used for the PN injection. $W_{r,5}$ is the lumped bit weight associated with the remaining capacitors of the ref. SAR ADC.

In the above-mentioned configuration, there are 14-bit weights, 7 for the ref. ADC and 7 for the sub-ADC, to be determined. We can write them in two vectors $\mathbf{W}_r$ and $\mathbf{W_m}$. The split-ADC calibration will enforce $D_r - D_m = 0$, which leads to

$$\begin{aligned}&[B_{r,0} \quad B_{r,1} \quad B_{r,2} \quad B_{r,3} \quad B_{r,4} \quad D_{r,R} \quad -PN \\ &\quad -B_{m,0} \quad -B_{m,1} \quad -B_{m,2} \quad -B_{m,3} \quad -B_{m,4} \quad -D_{m,R} \quad -1] \\ &\quad \times \begin{bmatrix} \mathbf{W_r} \\ \mathbf{W_m} \end{bmatrix} = 0.\end{aligned} \tag{3}$$

In (3), one bit weight needs to be fixed to avoid an underdetermined system. To match the gain of each sub-ADC to that of the ref. ADC, the fixed bit weight is assigned to the ref. ADC.

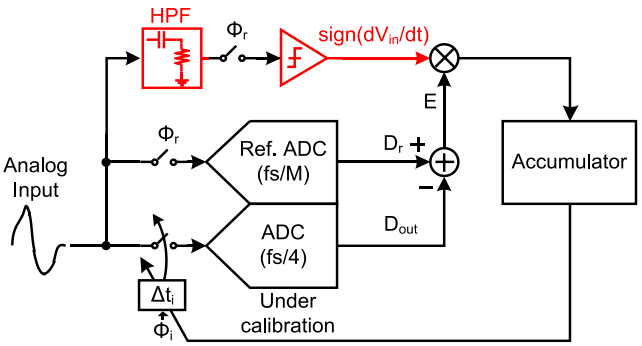


Fig. 3. Analog HPF-assisted skew calibration of the TI-ADC array.

We choose to fix the MSB bit weight of the ref. ADC at its ideal value of 2048, which leads to

$$\begin{aligned}&[B_{r,1} \quad B_{r,2} \quad B_{r,3} \quad B_{r,4} \quad D_{r,R} \quad -PN \\ &\quad -B_{m,0} \quad -B_{m,1} \quad -B_{m,2} \quad -B_{m,3} \quad -B_{m,4} \quad -D_{m,R} \quad -1] \\ &\quad \times \begin{bmatrix} \mathbf{W'_r} \\ \mathbf{W_m} \end{bmatrix} \\ &= -2048 \times B_{r,0}.\end{aligned} \tag{4}$$

$\mathbf{W}'_r$ are the remaining bit weights of the ref. ADC. In this paper, we use the LMS algorithm to iteratively solve (4).

B. Calibration of Timing Skew

The timing skew calibration is derived from the DDI calibration technique [9]. Assuming that the clock skew is relatively small, the skew error can be approximated as

$$E_{\mathrm{skew}} = D_r - D_{\mathrm{out}} \approx \frac{dV_{\mathrm{in}}}{dt} \times \Delta t_i \tag{5}$$

where D_{out} is the digital output of one sub-ADC and Δt_i is the sample clock skew between the ref. ADC and the sub-ADC. As shown in Fig. 3, an HPF is employed to detect the input slope dV_{in}/dt. The transfer function of the capacitor-resistor high-pass filter (C-R HPF) can be approximated as

$$H_{\mathrm{HPF}}(j\omega) = \frac{j\omega}{j\omega + (\mathrm{RC})^{-1}} \approx j\omega \mathrm{RC} \tag{6}$$

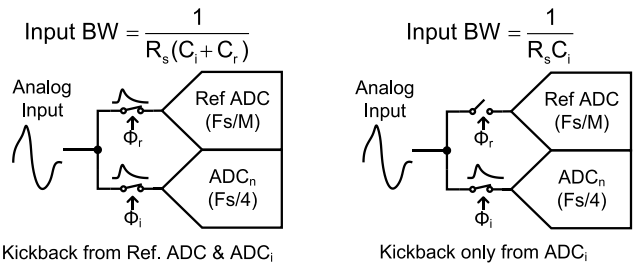
for an input frequency much lower than the HPF corner frequency. The time-domain equivalence of (6) is

$$V_{\mathrm{HPF}}(V_{\mathrm{in}}) \approx \frac{dV_{\mathrm{in}}}{dt} \times \mathrm{RC} \tag{7}$$

where $V_{\mathrm{HPF}}(V_{\mathrm{in}})$ is the analog output of the HPF. Since only the sign of the skew is necessary to update the DCDL codes, a zero-crossing comparator trailing the HPF serves the purpose. The sign of the timing skew can be estimated by

$$\begin{aligned}\mathrm{sign}(\Delta t_i) &= \frac{\mathrm{sign}(D_r - D_{\mathrm{out}})}{\mathrm{sign}(dV_{\mathrm{in}}/dt)} \\ &= \mathrm{sign}(D_r - D_{\mathrm{out}}) \times \mathrm{sign}(V_{\mathrm{HPF}}).\end{aligned} \tag{8}$$

In this paper, an accumulator block is used to obtain the average value of (8), $\overline{\mathrm{sign}(D_r - D_{\mathrm{out}}) \times \mathrm{sign}(V_{\mathrm{HPF}})}$, and to direct the update of the DCDL.



(a) (b)

Fig. 4. Ref. ADC-related kickback noise and input bandwidth variation. (a) Ref. ADC is sampling. (b) Ref. ADC is idle.

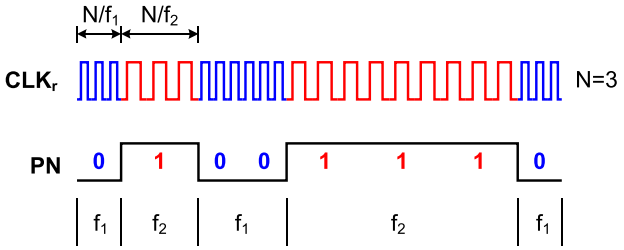
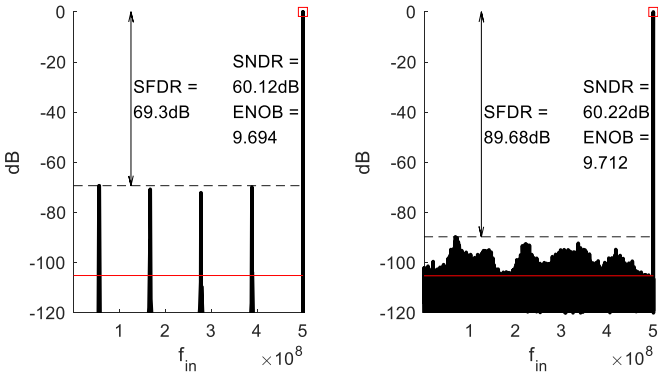


Fig. 5. Sample clock of the ref. ADC with randomization.

IV. Reference ADC Interference

One subtle issue of TI-ADC design is the interference between the various sub-ADCs through the input network. An input buffer with low output impedance is usually needed to absorb the kickback produced by the sub-ADC S/H circuits. This problem is exacerbated when a reference path is introduced. Suppose that the ADC array is clocked at a sample rate of F_s, each sub-ADC runs at F_s/L, and the ref. ADC operates at a different frequency F_s/M, where M and L are the co-prime integers. For example, if the sub-ADCs run at $F_s/4$, the reference can operate at $F_s/5$ to enable the calibration of each sub-ADC. As shown in Fig. 4, any kickback from the ref. ADC can generate a spur at its sample frequency of $F_s/5$. In addition, the bandwidth of the sample network with the ref. ADC varies from time to time, as shown in Fig. 4; for most of the time, only the sample capacitor of one sub-ADC loads the input. When the ref. ADC samples, the input bandwidth is reduced due to the extra loading presented by the ref. path. Let R_s be the effective source resistance, C_i and C_r be the sample capacitances of the sub-ADC and the ref. ADC, respectively. For an input frequency much lower than the -3-dB bandwidth of the input network, the effect of the bandwidth variation can be approximated by a constant delay, i.e., the ADC sample point is slightly delayed every M sample, resulting in spurs in the array spectrum at $F_s/M \times i \pm F_{\text{in}}$, $i = 1, 2, \ldots, (M-1)/2$.

To remedy the reference interference problem, a randomization technique reported for the dc–dc converter [11] is adopted here to randomize the sample frequency of the ref. path. In this scheme, the sample frequency of the ref. ADC randomly hops between multiple frequencies; for each frequency, the sample clock lasts for an integer number of clock periods of that frequency. Fig. 5 shows a simple example, in which two frequencies f_1 and f_2 are used, and for each frequency, the sample clock lasts for three clock periods. One key feature



(a) (b)

Fig. 6. MATLAB simulated spectra of the ADC array when the ref. ADC operates (a) with a fixed and (b) with a randomly frequency-hopped sample rate.

of this frequency-hopping scheme is that the hopping period varies with the selection of the hopping frequencies. In the example, the hopping period is either $3/f_1$ or $3/f_2$. A pseudo-random bit sequence PN selects the sample frequency between f_1 and f_2. The spurs due to the interference are eliminated if f_1 and f_2 are non-commensurate.

Behavioral simulation is performed to verify the randomization technique. Let $R_s = 25\ \Omega$ and $C_r = 40$ fF, i.e., a 1-ps delay is introduced whenever the ref. path samples. As shown in Fig. 6, for an input near the Nyquist frequency, the spurs are located at $\pm F_s/18$, $\pm 3F_s/18$, $\pm 5F_s/18$, and $\pm 7F_s/18$ and are as large as -69.3 dBc when the ref. ADC operates at a fixed frequency of $F_s/9$ while the array operates at $F_s = 1$GS/s. When the ref. ADC sample rate randomly hops between four frequencies, $F_s/5$, $F_s/7$, $F_s/11$, and $F_s/14$, and for each frequency, the ref. ADC operates for one clock cycle (i.e., $N = 1$), the spurs are all suppressed below -89.6 dBc.

Finally, we note that the ref. ADC interference is not eliminated by randomization, and it is simply spread across the spectrum. The total error power it generates is proportional to its sample rate. For example, in the above-mentioned random frequency-hopping case, the average sample rate of the ref. ADC is lower than $F_s/5$ (because it varies between four frequencies, $F_s/5$, $F_s/7$, $F_s/11$, and $F_s/14$). As a result, less error is introduced to the main ADC array, and the resulting array signal to noise and distortion ratio (SNDR) is about 2 dB higher relative to the case with a fixed ref. sample rate of $F_s/5$.

V. Circuit Implementation

A. Pipelined SAR Sub-ADC

The two-stage pipelined SAR sub-ADC is shown in Fig. 7. The first stage resolves 5 bits, and the second stage resolves 8 bits with 1-bit inter-stage redundancy. The sub-ADC implementation is based on [12]. The inter-stage gain is $8\times$. The ratio of the residue-sampling capacitance to the DAC capacitance in the second stage is set to 2, which effectively halves the reference voltage. Several circuit techniques are adopted to achieve a 12-bit, 250-MS/s operation with low power in a 65-nm process. An asynchronous SAR logic is adopted for both the first- and second-stage SARs. In addition, two reference voltage buffers are included on-chip to eliminate the

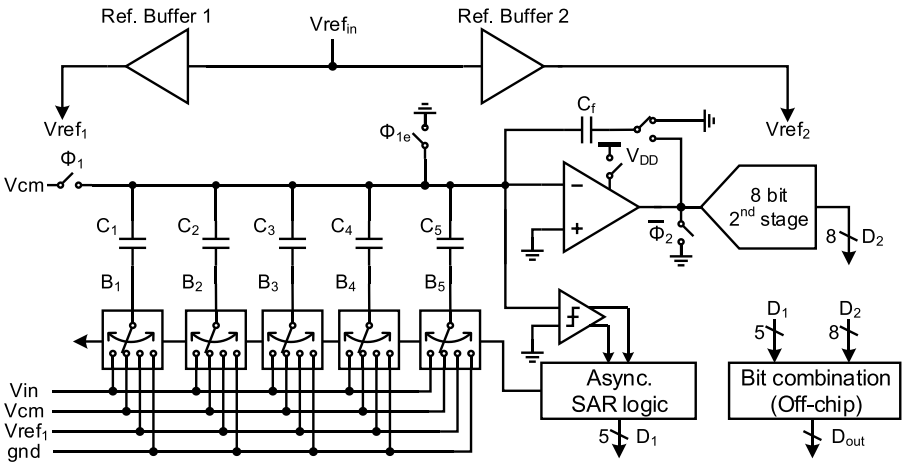


Fig. 7. Block diagram of the 12-b, 250-MS/s pipelined SAR sub-ADC.

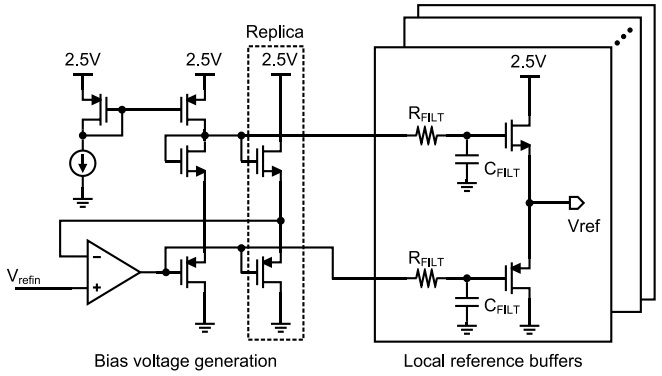


Fig. 8. On-chip reference voltage buffers and the bias generation circuit.

need for large reference-decoupling capacitors. Fig. 8 shows the reference buffer of the sub-ADCs. Two push–pull source followers generate the reference voltages for the first- and second-stage SARs separately. Since the reference voltage is 1.2 V in this design, the supply voltage of the reference buffer is set to 2.5 V. The NMOS transistor on the top side is a 2.5-V thick-oxide transistor, whereas the PMOS transistor is a thin-oxide transistor. The gate voltages of the PMOS and NMOS transistors are generated by a replica circuit (see Fig. 8) [13]. The negative feedback guarantees that the reference buffer output is identical to V_{refin}. In each sub-ADC, separate buffers are used in the first and second stages for isolation, while V_{refin} is the same for the two stages. There are nine on-chip buffers in total (two buffers per sub-ADC and one for the ref. ADC). Since the bias circuit is shared by all on-chip buffers, an low-pass filter is inserted in between the bias circuit and the buffers for isolation (see Fig. 8).

B. Ref. SAR ADC

A 12-bit SAR ADC functions as the ref. ADC, which adopts a synchronous design driven by a 1-GHz external clock. The architecture of the ref. ADC is shown in Fig. 9. Considering input loading, suppose the unit DAC capacitor is 1 fF, and then, the total DAC capacitance is around 2 pF. As a result, the reference kickback would be 4× larger than that of the sub-ADC, which has a sample capacitor of 450 fF. To reduce the ref. DAC capacitance, first, a bridge structure is used; the bridge capacitance can be calculated as follows:

$$C_B = \frac{C_{\text{low,tot}}}{2^L - 1} \tag{9}$$

where L and $C_{\text{low,tot}}$ are the resolution and total capacitance of the lower segment of the DAC, respectively. Second, the input signal is sampled on a separate capacitor of 30 unit cells. The scheme will reduce the SNR of the SAR ADC. However, in this paper, only the linearity of the ref. ADC is critical, not the SNR (the SNR of the ref. ADC mainly affects the calibration speed). As shown in Fig. 9, the ref. ADC has a total input capacitance of around 30 fF, and it produces 14 raw bits. A separate reference buffer is used for the ref. ADC. A pre-amplifier is employed to reduce the comparator kickback.

In Fig. 9, if the sum of the bit weights of the lower segment of the DAC is smaller than the LSB weight of the upper segment, the digital-domain calibration will fail. This scenario can be avoided by intentionally sizing up C_B, forcing a sub-binary weighting even in the presence of parasitic capacitance and mismatch. In this prototype, however, the mismatch was too large due to a layout error, resulting in an spurious-free dynamic range (SFDR) of ∼70 dB of the ref. ADC even with weight calibration.

As described in Section IV, the sample rate of the ref. ADC is randomized. The implementation of the sample clock generation circuit is shown in Fig. 10. The 7-bit digital counter counts from 0 to 127. The counter output is connected to a digital comparator. Once the comparator output is high, the counter is reset to zero, and the comparator output becomes low. The other input of the comparator takes on a value of 54, 96, 83, or 113 randomly. The digital comparator output is sampled by a flip-flop to generate the ref. ADC sample clock. Since the system clock is 1 GHz, the sample period of the ref. ADC varies randomly between 54, 96, 83, and 113 ns.

C. Multiphase Clock Generator

A shift register is used to generate the multiphase clock signals that drive the four sub-ADCs [14]. Since the input clock is 1 GHz, each output clock signal has a frequency

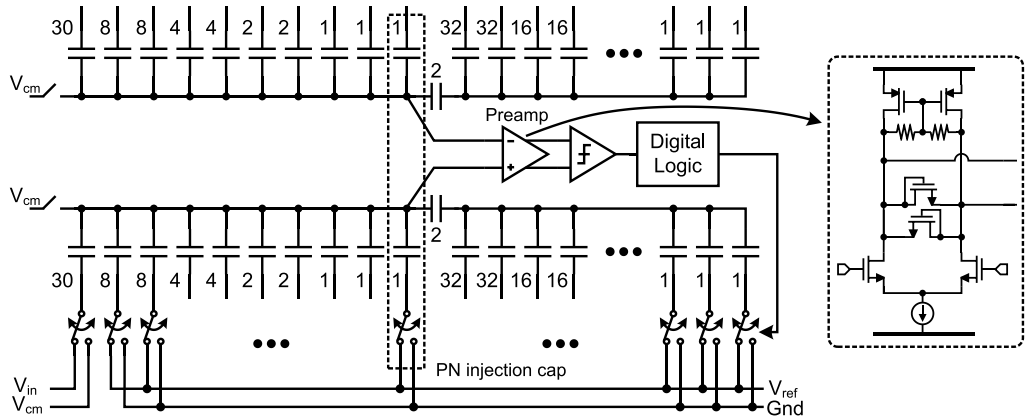


Fig. 9. Ref. SAR ADC architecture.

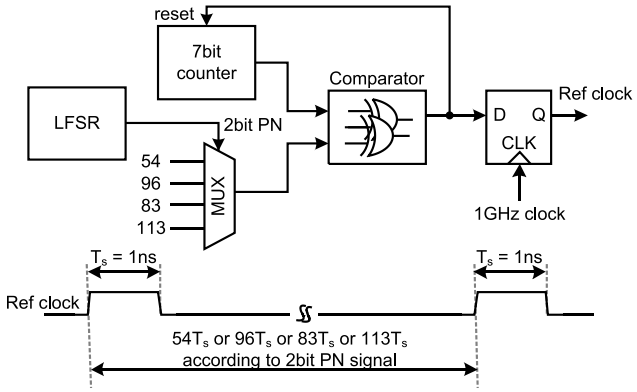


Fig. 10. Sample clock generation circuit for the ref. ADC.

of 250 MHz and a duty cycle of 25%, with a phase of 0°, 90°, 180°, or 270°. The four clock phases are fed into four DCDLs for skew calibrations. As shown in Fig. 11, the DCDL consists of three sections of variable capacitors [15] with a tuning range of 13.7 ps and an LSB size of 70 fs. Each pipelined SAR ADC needs two input clock phases: one defines the sample phase and the other defines the amplification phase. The phase difference between the two is 270°. As shown in Fig. 11, a set of dummy delay lines fixed at the minimum delay is used to generate the clock phase of 270°. In this paper, since the S/H networks of the ref. ADC and the sub-ADCs are different and physically separated by approximately 800 μm, a coarse DCDL is utilized in the ref. ADC to set its sample point to within the range of those of the sub-ADCs, as shown in Fig. 12. The coarse DCDL achieves a tuning range of 100 ps and an LSB size of 1 ps. Most collective skew between the array and the ref. ADC is eliminated by the coarse DCDL.

D. HPF and Comparator

As shown in Fig. 13, a passive C-R HPF followed by a comparator is used to detect the sign of the input signal slope. The sample point of the HPF path is synchronized to that of the ref. ADC. One option in this paper is to use the sample clock (CLKIN in Fig. 12) to directly drive the comparator which samples the HPF output. In this case, the kickback from resetting the comparator can directly contaminate the following ref. ADC sample. To fix this, a self-timing technique is adopted to reset the comparator immediately after the regeneration is completed. The schematic and the timing diagram of the self-timing loop are shown in Fig. 13. A separate static latch is used to store the comparator output. The common-mode voltage of the HPF output is set to be equal to the input common-mode voltage.

The HPF can only be considered as a derivative filter when its corner frequency is higher than the input frequency of interest. Since only the sign of the slope is needed, the 1-b large quantization noise will randomize the estimation error from the HPF when its corner frequency is close to the input frequency. A similar argument can be made in terms of the HPF group delay [9]. In contrast, a high HPF corner frequency will slow down the convergence. In [9], the corner frequency is set to 1.2× of the Nyquist frequency; in this paper, the corner frequency of the HPF is designed to be around 800 MHz, which is 1.6× of the Nyquist.

The offset of the comparator and the relative timing skew between the ref. ADC and the HPF path is also potential error sources for the skew calibration, whose effects are fully analyzed in [9] and excerpted in the Appendix. In short, as can be seen in Section VI, they produce no noticeable effect on the skew calibration and the array linearity performance when the input frequency is on the high side relative to the dead-band frequency (with or without comparator offset treatment).

E. Input Sampling Network

Fig. 14 shows a simplified schematic of the input network of the ADC array. During the sample phase, the input signal is acquired on the DAC capacitors of a sub-ADC. In the presence of an input bond-wire inductance, the kickback from the S/H circuit can hardly settle to the 12-bit level within the 1-ns tracking time. The issue is alleviated by the on-chip 58-Ω termination resistors, i.e., the three polysilicon resistors shown in Fig. 14.

One problem of on-chip termination is the nonlinearity of the polysilicon resistor induced by self-heating, which can be minimized by increasing the total area of the resistor. However, it would also increase the associated parasitic capacitance and reduce the ADC input bandwidth. Another solution is to choose a zero-temperature-coefficient (ZTC) resistor. In the 65-nm process we used, there are two kinds

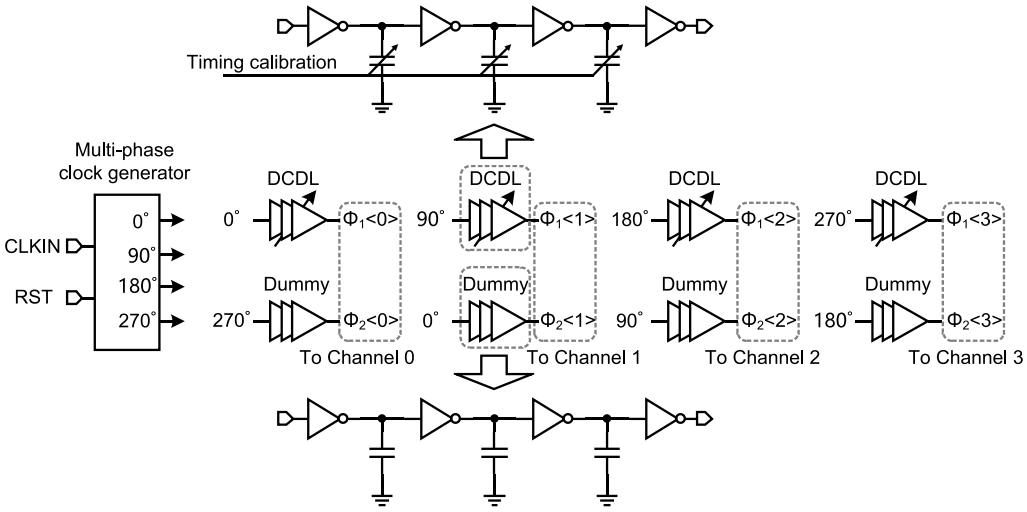


Fig. 11. Timing calibration circuit for the main ADC array.

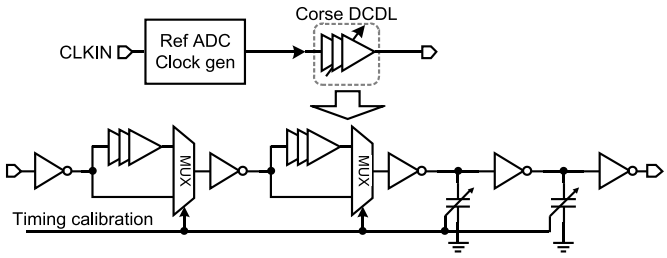


Fig. 12. Timing calibration circuit for the ref. ADC.

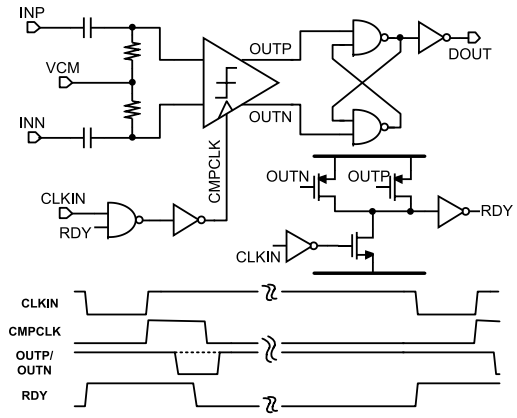


Fig. 13. HPF and comparator with a self-timing circuit.

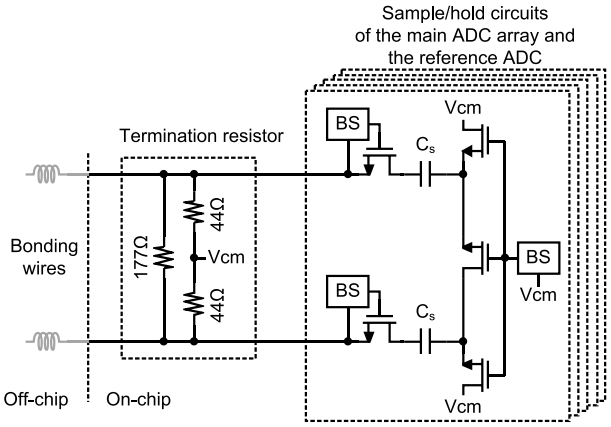


Fig. 14. Input network of the TI-ADC array.

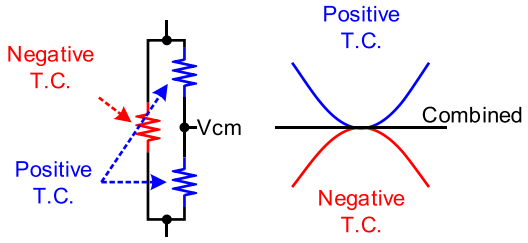


Fig. 15. ZTC input-termination resistors.

of polysilicon resistors that have opposite temperature coefficients. As shown in Fig. 15, they are connected in parallel to achieve a near-ZTC. Monte Carlo simulations show that the input network can achieve a linearity of over 90 dB.

VI. Measurement Results

The prototype TI-ADC array was fabricated in a 65-nm CMOS process. A die photograph is shown in Fig. 16. The active area of the ADC core is 0.27 mm^2. Including the on-chip bypass capacitors, the total chip area is 0.84 mm^2 (0.7 mm $\times$ 1.2 mm). At 1 GS/s, the chip (excluding digital output buffers) consumes a total power of 31.5 mW from three voltage supplies of 1.2, 2.5, and 1.4 V. The residue amplifiers, the non-overlapping clock-generation circuits, and the reference switch buffers of the main ADC array are powered by a 1.2-V supply. The nine reference voltage buffers of the main ADC array and the ref. ADC are powered by a 2.5-V supply. The multi-phase clock generator and the DCDLs in the main ADC array are powered by a 1.2-V supply. The reference switch buffers and the preamplifier of the ref. ADC are powered by a 1.4-V supply.[1] The clock-generation circuit

[1]The ref. ADC was designed for a 1.2-V operation. It turns out that we need to raise the supply to 1.4 V to partially compensate for the performance loss due to a layout error in the ref. ADC.

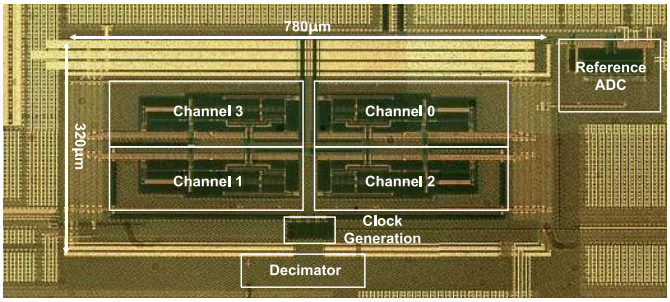


Fig. 16. Die photograph.

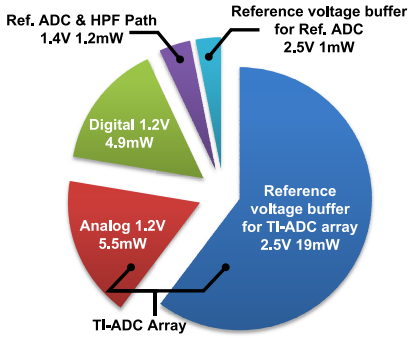


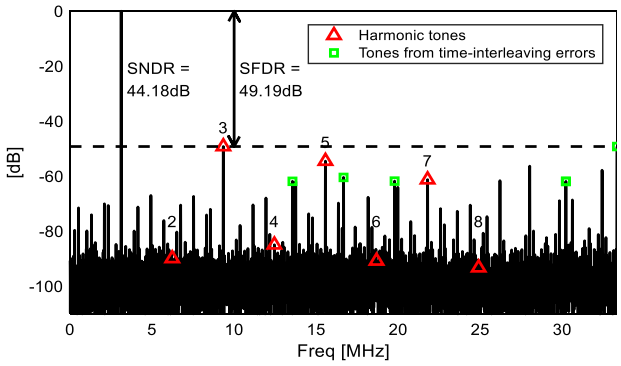
Fig. 17. Breakdown of power consumption.

for the ref. ADC is supplied by another 1.2-V supply. All on-chip digital logics share one 1.2-V supply. A detailed power breakdown of the prototype chip is shown in Fig. 17, wherein the ref. ADC power includes those of both the frequency-hopped ref. ADC and the HPF path. The digital outputs of the main ADC array are decimated by 15× before being sent off-chip.

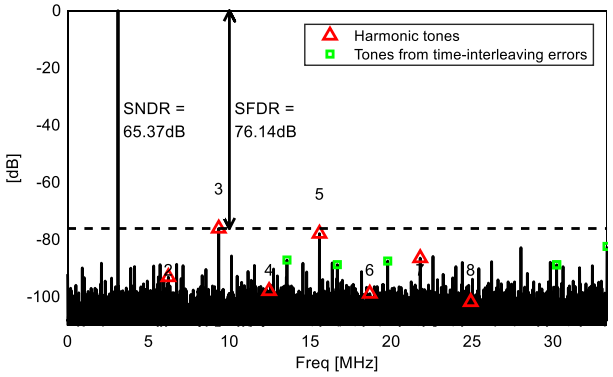
In testing, both BG and FG calibrations were applied to treat the static and dynamic mismatch errors of the TI-ADC array. While the chip was designed to be capable of a full BG operation, the ref. ADC error limited the achievable array SFDR in the BG mode, as detailed in Sections VI-A–VI-E. Both the FG and BG results are reported in this paper for completeness and comparison.

A. Background Static and Skew Calibrations

A calibration is performed to correct the static conversion errors due to the capacitor mismatch, inter-stage gain, and inter-sub-ADC gain and offset errors. For the pipelined SAR ADCs in the main array, only the five leading bits are calibrated. The bit-weight extraction is performed using the decimated split-ADC technique described in Section II. Due to the layout error in the ref. ADC, its measured SFDR is limited to 70.6 dB (with an SNDR of 50.8 dB), which in turn limits the post-calibration linearity of the TI-ADC array. Fig. 18(a) and (b) shows the output spectra of the ADC array before and after BG calibration, respectively. An improvement of 21 dB in SNDR and 27 dB in SFDR is observed. Fig. 19 plots the learning curves of the BG calibration; an SFDR of over 70 dB and an SNDR of around 65 dB are consistently achieved after 200 ksamples of adaptation. The DCDL control codes are fixed at the default values during this measurement.



(a)



(b)

Fig. 18. Measured prototype ADC array output spectra at 1 GS/s with a 3-MHz sine-wave input. (a) Before and (b) after calibration.

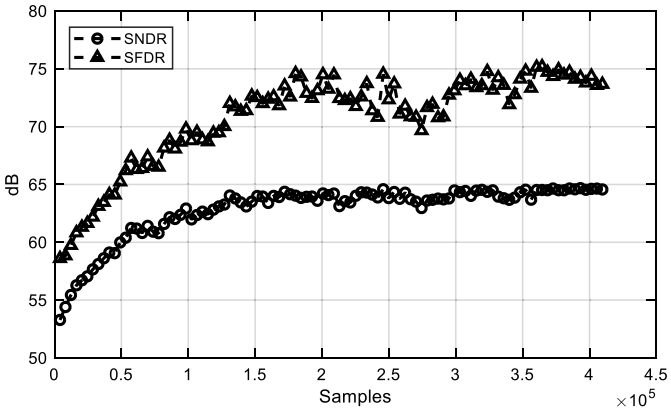


Fig. 19. Measured SNDR and SFDR learning curves of the ADC array during the BG static calibration.

The BG skew calibration is then performed with a 300-MHz sinusoidal input. The radix, gain, and offset coefficients are frozen during this measurement. Fig. 20 shows the convergence curves of the DCDL control codes for the four sub-ADCs during the calibration; all the timing-skew spurs fall below −75 dBc after 300 ksamples. As discussed in Section V-D, the presence of a small comparator offset in the HPF path is of no concern to the skew calibration for an input frequency of 300 MHz [9]. In the prototype, we implemented an offset trimming circuit for the comparator (with an adjustment range of [−20 20] mV and a 4-b digital control). In testing, the trimming circuit was manually adjusted, leaving

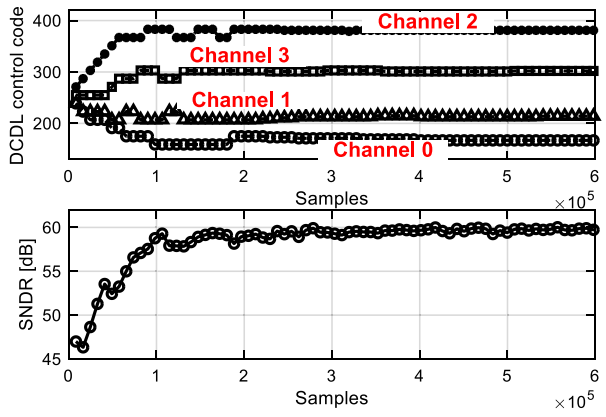


Fig. 20. Measured convergence curves of the ADC array during the BG timing-skew calibration.

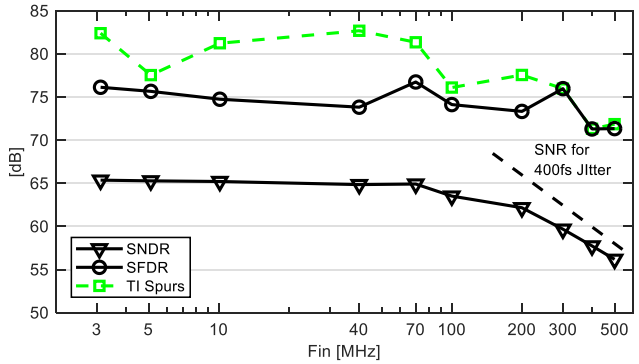


Fig. 21. Measured SNDR and SFDR of the ADC array vs. the input frequency at an aggregate sample rate of 1 GS/s.

a residual offset of ~2.5 mV. The skew calibration results confirm that this offset produces no noticeable effect on the array SNDR and SFDR performance.

B. Dynamic Performance With Frozen Coefficients

To simplify and speed up the lab measurement process, the coefficients extracted from the BG static and skew calibrations described in Section VI-A are used in evaluating the ADC performance that is reported in this section. Specifically, the radix, gain, and offset coefficients were extracted with a low-frequency (3 MHz) input; and the DCDL control codes were obtained with a high-frequency (300 MHz) input. The ref. ADC was kept running for all the measurements.

The calibration results vs. the input frequency with frozen coefficients are plotted in Fig. 21. The low-frequency SFDR and SNDR stay above 75 and 65 dB, respectively, until around 100 MHz. The measured SNDR at high frequency is limited by the 400-fs rms jitter of our lab instrument producing the master clock for the chip. Fig. 22 plots the TI-ADC output spectra with a Nyquist input frequency of 500 MHz. The calibration consistently suppresses all skew-related spurs to below −70 dBc.

C. Foreground Radix Calibration

As mentioned before, due to the layout error in the ref. ADC, the measured SFDR of the TI-ADC array in the BG mode is limited to 75 dB even at low input frequencies. To unveil the true performance of the array sub-ADCs, an FG radix calibration has also experimented as follows.

In the FG method, a filtered sinusoidal signal is applied to the input of the ADC, and the optimum bit weights are extracted using a sine-fit algorithm. As shown in Fig. 23, the FG calibration results show a 6-dB higher SFDR compared with the BG result shown in Fig. 18(b) at low input frequencies.

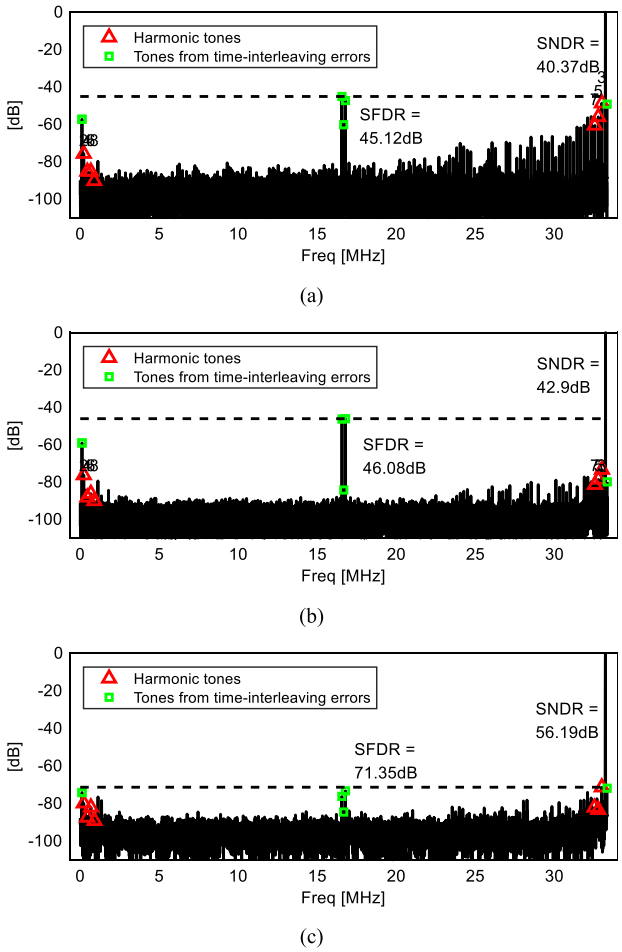


Fig. 22. Measured ADC array output spectra at 1 GS/s for a 500-MHz input with (a) no calibration, (b) static calibration only, and (c) both static and skew calibrations. The red triangle annotates the harmonics, and the green square denotes the interleaving tones.

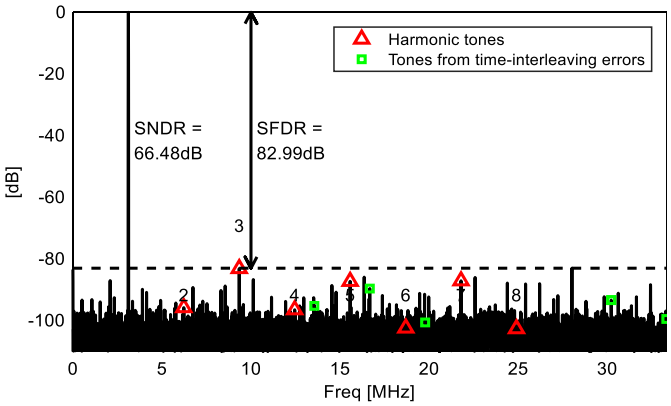


Fig. 23. Measured ADC array output spectrum with FG radix calibration.

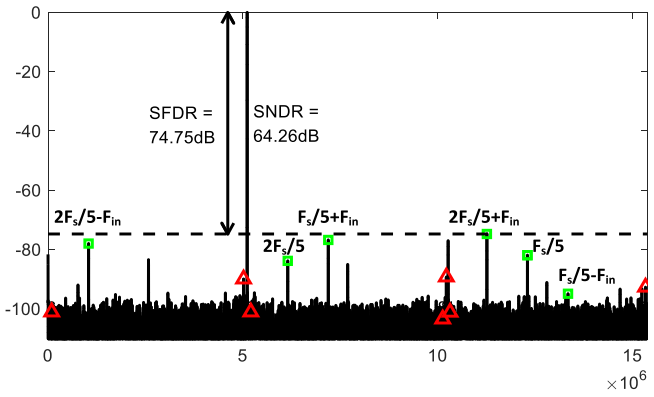


Fig. 24. Measured ADC array output spectrum without ref. sample randomization (experimental result from an earlier prototype).

TABLE I
MEASURED PERFORMANCE COMPARISON

		Payne ISSCC 2011[16]	Ali JSSC 2014[17]	Mulder ISSCC 2015[18]	Nam JSSC 2018[19]	This work
Fs [GS/s]		1	1	0.8	1.6	1
Interleaving (Factor)		Yes (2×)	No	Yes (2×)	Yes (8×)	Yes (4×)
Sub-ADC Architecture		Pipeline	Pipeline	Pipeline	SAR	Pipeline SAR
Technology		BiCMOS 180nm	CMOS 65nm	CMOS 28nm	CMOS 65nm	CMOS 65nm
TI-Calibration Type	Offset	BG	N/A	BG	FG	BG, FG
	Gain	N/A	N/A	BG	FG	BG, FG
	Timing	Analog BG	N/A	Analog BG	Analog FG	Analog BG, FG
SNDR @LF [dB]		62	69	54.7	72.1	65.3
SNDR @HF [dB]		59	68	57.1	65.0	56.2
On-Chip Ref. Buffer		Yes	Yes	Yes	No	Yes
Power [mW]		575	1200	76.4	37.7	31.5
Area [mm^2]		2.35	18	0.23	0.9	0.27
FoM$_W$ @LF [fJ/c-s]		558.9	521.0	215.1	7.2	20.9
FoM$_W$ @HF [fJ/c-s]		789.6	584.6	163.2	16.2	59.7
FoM$_S$ @HF [dB]		148	154	154	168	158

D. Effectiveness of Ref. Sample Randomization

An earlier version of the chip without incorporating the ref. sample randomization technique was also measured. When the ref. ADC is clocked at $F_s/5$, multiple spurs at $n \cdot F_s/5$ and $n \cdot F_s/5 \pm F_{\text{in}}$ can be observed in the array spectrum shown in Fig. 24, wherein the input frequency is 5 MHz, the aggregate sample rate is 400 MS/s, and the digital outputs are decimated by 13×.

E. Measurement Summary

Table I summarizes the measurement results of the prototype and compares them with those of several state-of-the-art parts.

VII. CONCLUSION

A 12-b, 1-GS/s ADC array with FG and BG calibrations is reported in a 65-nm CMOS process by interleaving four 12-b, 250-MS/s pipelined SAR sub-ADCs. A ref. ADC and an analog HPF path followed by a comparator are implemented on-chip to enable the calibration that treats timing skews, static gain, and offset mismatch errors in this prototype. The ref. ADC sample points are further randomized using a frequency-hopping scheme to mitigate its interference to the main ADC array. The prototype ADC achieves a more than 70-dB SFDR at Nyquist input and a peak SNDR of 65.3 dB in measurement with Walden and Schreier figure of merits on par with or exceeding a few state-of-the-art parts of similar sample rates and resolutions.

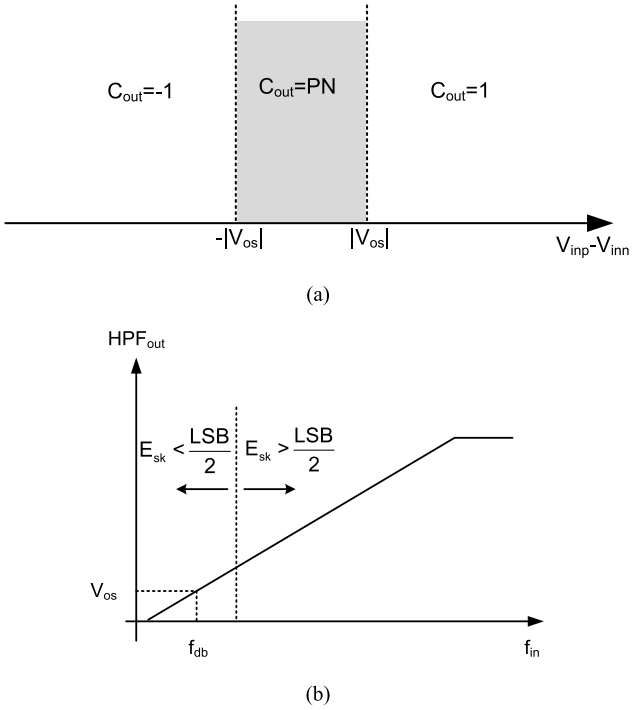


Fig. 25. Comparator in the HPF path with offset chopping. (a) Illustration of the voltage-domain dead band. (b) Frequency-domain illustration.

APPENDIX
HPF-PATH NON-IDEAL EFFECTS

Some circuit non-idealities, i.e., the offset of the comparator trailing the HPF and the timing skew among the two ref. paths, their impact on the derivative-path performance, and potential circuit solutions, are discussed in the Appendix, which is an excerpt adapted from [9].

A. Comparator Offset in HPF Path

Comparator offset can potentially bias the sign detection of the derivative circuit. While calibration or auto-zeroing can be performed on the comparator, chopping serves as a more efficient remedy here and is described as follows.

The basic idea is to implement a pair of choppers, directed by a one-bit PN, around the comparator. The randomization effect of chopping will destroy any consistent bias in the sign detection, thus eliminating the wrongful updates of the calibration circuit. The benefit can be analyzed in more detail with the help of Fig. 25(a), where we assume an offset voltage V_{os}. When the differential input of the comparator is larger than V_{os} or smaller than $-V_{\text{os}}$, chopping will yield no effect on the comparator decision; in contrast, when the input is bounded between these values, the outcome is identical

to the PN, i.e., when the HPF output is small for low input frequencies, the sign of the derivative is totally determined by the PN

$$\text{sign}(\Delta t_i) = \overline{\text{sign}(D_r - D_{\text{out}}) \cdot PN} \tag{A1}$$

which must converge to zero, as the PN is independent of any error in the ADC. In contrast, for high input frequencies, neither the PN nor the comparator offset will influence the sign of the derivative. Effectively, the random chopping introduces a dead band for low input frequencies of the skew calibration, which is shown in Fig. 25(b). Given the value of V_{os} and the *RC* time constant of the HPF, the upper frequency bound of the dead band f_{db} can be determined. The derivative estimation is free of any offset bias beyond this frequency, whereas below it, the skew adjustment just halts. This does not introduce any problem in practice, as for low-frequency inputs, the skew error is also small; thus, as long as the upper frequency bound of the dead band is lower than the critical frequency (i.e., the skew-insensitive frequency, at which the skew-induced conversion error is less than 1/2 LSB), the dead band is of no concern.

To derive an expression for f_{db}, we assume that the corner frequency of the HPF is f_c, the ADC array resolution is N, and $V_{\text{os}} = k \cdot \text{LSB}$. A sinusoidal input of amplitude A and frequency f_{db} will fall into the dead band, which means

$$\frac{f_{db}}{\sqrt{f_{db}^2 + f_c^2}} \cdot A = V_{\text{os}}. \tag{A2}$$

Substituting A by 2^{N-1} LSB (assuming a full-scale input) and V_{os} by $k \cdot$LSB in (A2), the upper frequency bound of the dead band can be determined as

$$f_{db} = \frac{k}{\sqrt{2^{2N-2} - k^2}} \cdot f_c. \tag{A3}$$

At the meantime, the maximum skew error can be expressed as

$$E_{\text{skew}} = \frac{dV_{\text{in}}}{dt} \cdot (\Delta t_{\max} - \Delta t_{\min}) \le \pi f_{\text{in}} V_{\text{FS}} \times (\Delta t_{\max} - \Delta t_{\min}) \tag{A4}$$

where $\Delta t_{\max}$ and $\Delta t_{\min}$ are the max and min timing skews of the array, respectively. When the input frequency is less than a certain value, the maximum skew error is less than 1/2 LSB, and the ADC array output is insensitive to the skew error. This skew-insensitive frequency is given by

$$f_{\text{si}} = \frac{1}{2^{N+1}\pi \cdot (\Delta t_{\max} - \Delta t_{\min})} = \frac{1}{2^{N+1}\pi \cdot \Delta t_{pp}}. \tag{A5}$$

In summary, as long as $f_{db} \le f_{\text{si}}$ holds, the comparator offset of the HPF path will not introduce any noticeable error. It can be guaranteed by choosing the corner frequency of the HPF.

B. Timing Skew Between Two Ref. Paths

In Fig. 1, albeit the ref. ADC and the HPF-trailing comparator are driven by the same clock, skew exists inevitably between them due to layout and device mismatch. Thus, (8) becomes

$$\text{sign}(\Delta t_i) = \overline{\text{sign}\left(\frac{dV_{\text{in}}}{dt} \cdot \Delta t_i\right) \cdot \text{sign}\left(\frac{dV_{\text{in}}}{dt} + \frac{d^2V_{\text{in}}}{dt^2} \cdot \Delta t_d\right)} \tag{A6}$$

where Δt_d is the timing skew between the two ref. paths. The extra term in (A5) can be approximated as

$$\overline{\left(\Delta t_i \frac{dV_{\text{in}}}{dt}\right) \cdot \left(\frac{d^2V_{\text{in}}}{dt^2} \cdot \Delta t_d\right)} = \overline{\Delta t_i \left(\frac{dV_{\text{in}}}{dt} \cdot \frac{d^2V_{\text{in}}}{dt^2}\right) \Delta t_d} \tag{A7}$$

in which we dropped the sign(.) argument for simplicity. Since a signal is orthogonal to its derivative [20], (A7) must evaluate to zero for constants Δt_i and Δt_d. Thus, the ref.-path skew would be averaged out by the adaptive calibration loop.

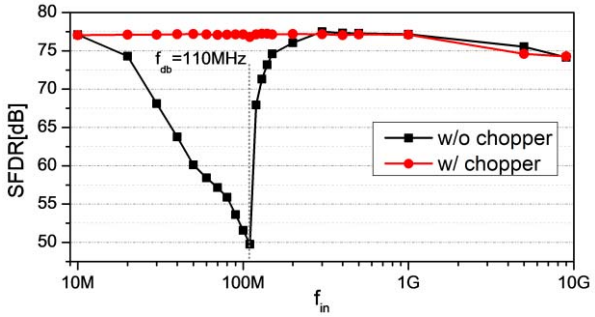


Fig. 26. Simulated array SFDR versus input frequency with and without chopping.

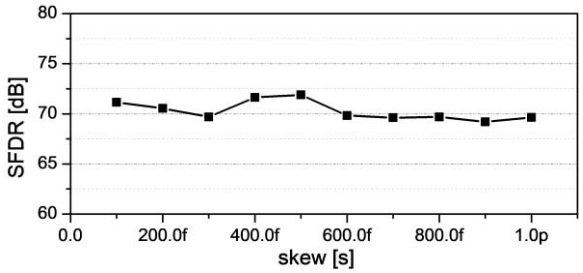


Fig. 27. Simulated array SFDR versus the clock skew between the two ref. paths.

C. Simulation Results

Behavioral simulations are performed for a 20-GS/s, 8-b, ten-way TI-ADC array to verify the effects of the ref. path non-idealities. With a 10-mV comparator offset, $f_{\text{db}} = 110$ MHz is determined from (A3). Also, with a max skew span of 2 ps, $f_{\text{si}} = 310$ MHz is calculated from (A5). The HPF corner frequency is set to 12 GHz or 1.2× of the Nyquist frequency.

First, the simulated SFDR of the TI-ADC array with and without chopping is shown in Fig. 26. Without chopping, the linearity after calibration exhibits a significant dip around 110 MHz, revealing the bias problem caused by the 10-mV offset at low input frequencies as analyzed before. In contrast, when chopping is enabled, the SFDR performance is nearly constant over all input frequencies. It is noteworthy that the SFDR results are nearly indistinguishable with or

without chopping once the input frequency exceeds the deadband frequency.

Second, the timing skew between the HPF path and the ref. ADC is varied from 100 fs to 1 ps in the simulation. The resulting array SFDR is plotted in Fig. 27, which is nearly constant over all skew values. The input frequency is set to 9.7 GHz in this simulation.

ACKNOWLEDGMENT

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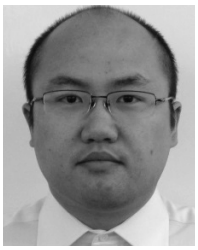

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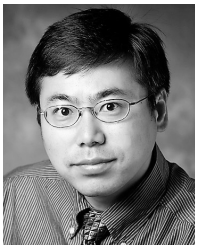

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