Design of Database Systems with DRAM-only Heterogeneous Memory Architecture

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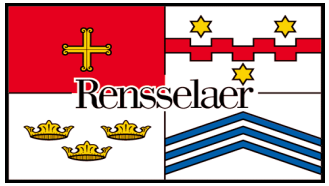
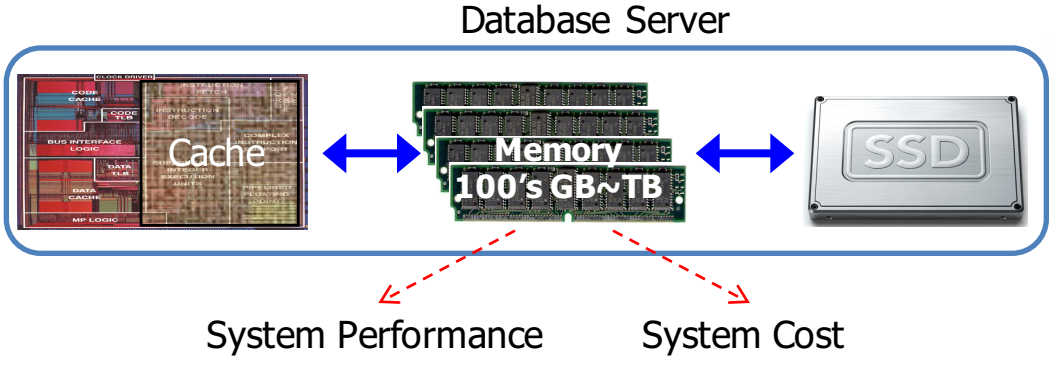
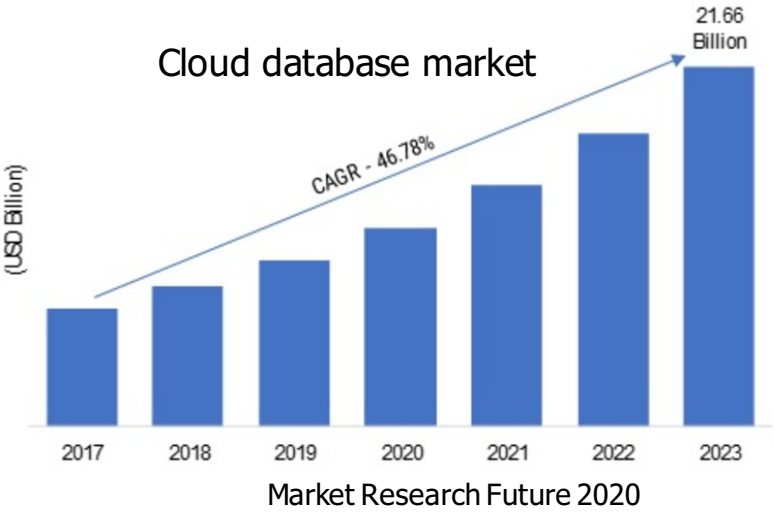


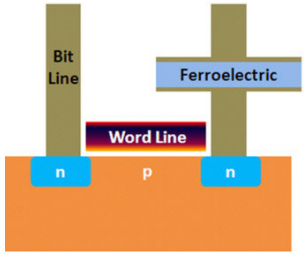
Database: Driver for Larger Memory

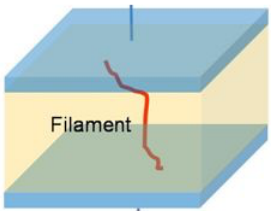
- Database: Cornerstone of modern information technology infrastructure

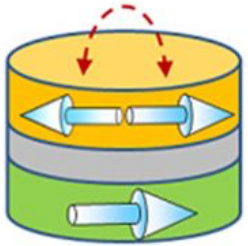


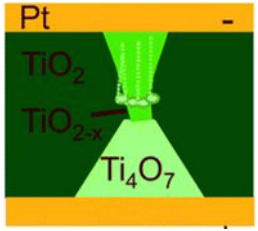


Search for new memory technologies

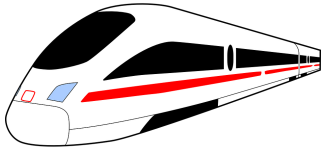




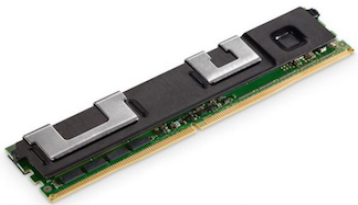




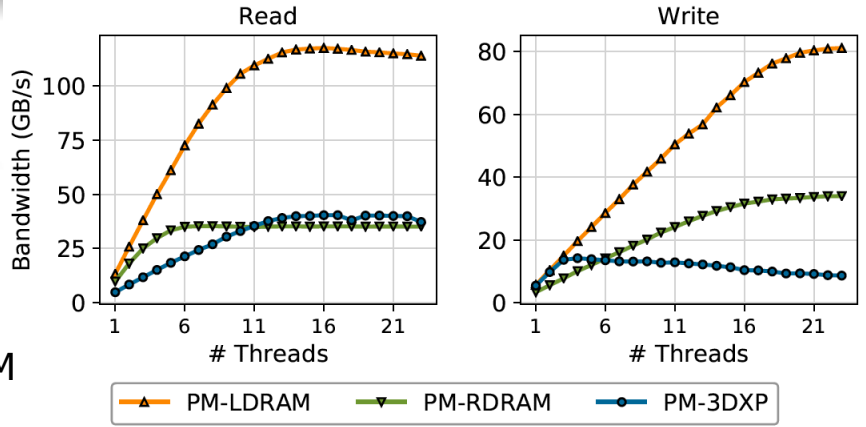
Search for New Memory Technologies



BIT COST **RAW RELIABILITY** **LATENCY** **BANDWIDTH** **ENDURANCE**



Intel 3DXP Optane DIMM



- x significantly slower than DRAM
- x Only 10^6 cycling endurance vs. $>10^{12}$ DRAM cycling endurance
- x Only ~50% cheaper than today's DRAM

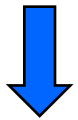
"Basic Performance Measurements of the Intel Optane DC Persistent Memory Module" 2019

DRAM-only Memory Hierarchy

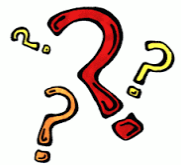
NVM is widely portrayed as the *only hope* to tackle the memory wall challenge

This thesis: DRAM-only paradigm to innovate/improve future memory systems

1. Very long maturity cycle for any memory technology
   - Little real-world success after 20-years of intensive research on NVM
   - Huge uncertainty on NVM scalability in terms of speed, cost, and endurance

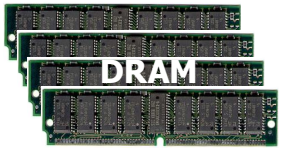


Have we already exploited the full potential of DRAM?



DRAM-only Memory Hierarchy: Motivation

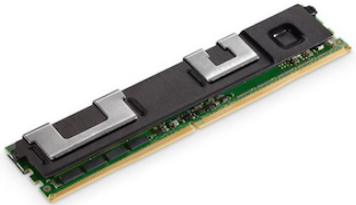
2. Over-hyped NVM cost advantage
   - All the claims on NVM cost advantage *conveniently* use today's byte-accessible DRAM as the baseline ➔ misleading conclusion
   - A simple fact: Any memory technology is fundamentally subject to a trade-off between raw reliability and cost



Today's DRAM DIMM

No ECC or weak 8-byte ECC

Unfair comparison



Intel 3DXP Optane DIMM

Strong 256-byte ECC

- High raw reliability ➔ high cost
- Low data access latency

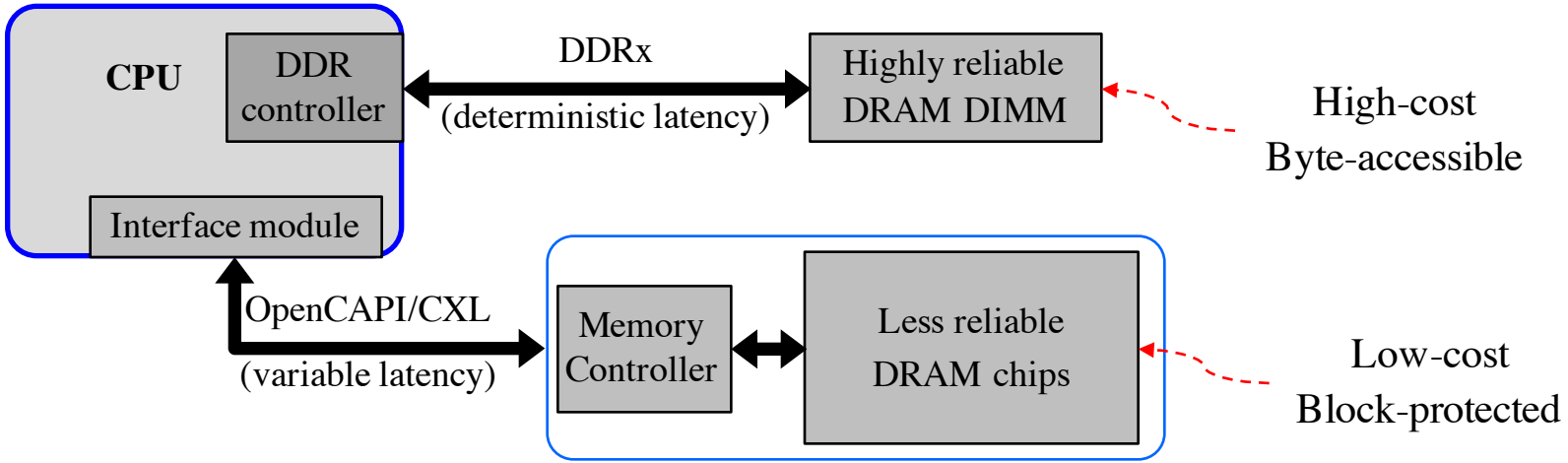
- Low raw reliability ➔ low cost
- Long data access latency

DRAM-only Memory Hierarchy: Motivation

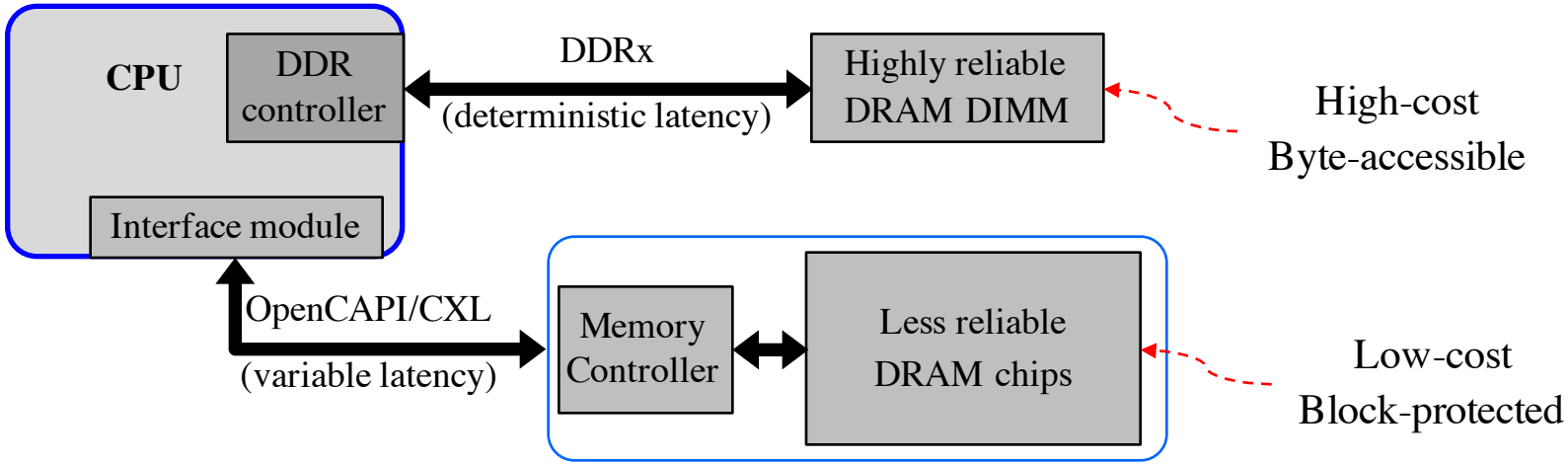
3. Media-agnostic, latency-oblivious CPU-memory interfaces

OpenCAPI™ CXL Compute Express Link GEN Z

This thesis: DRAM-only heterogeneous memory hierarchy



DRAM-only Heterogeneous Memory Hierarchy



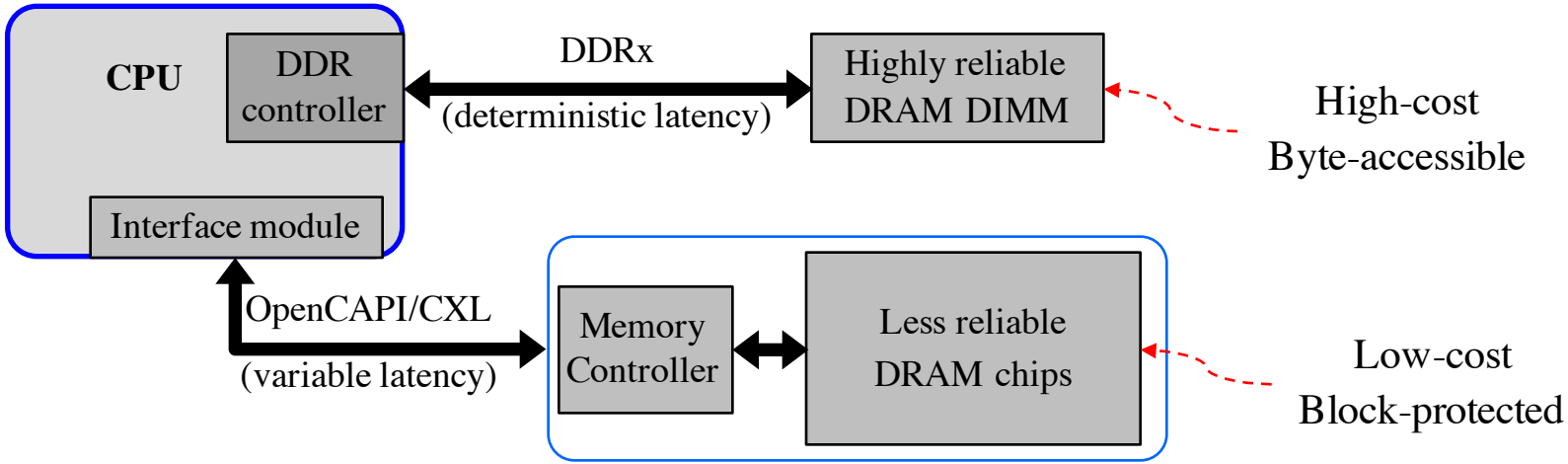
✓ Lower memory cost

✓ Truly DRAM-grade speed/endurance

✓ Zero technology-level uncertainty

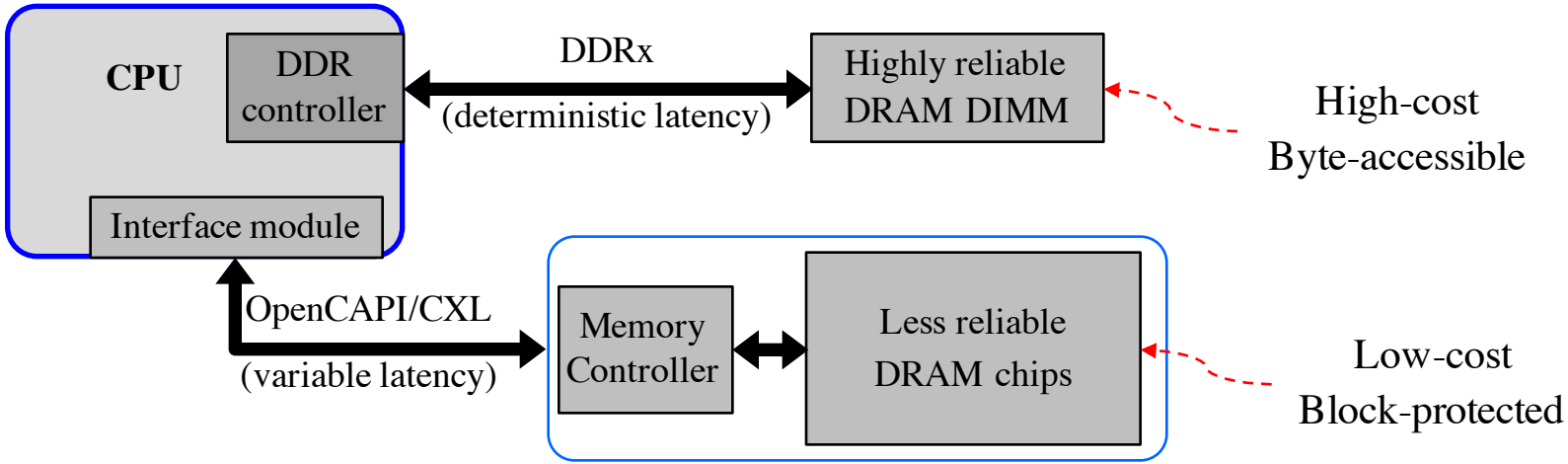
✓ Mature manufacturing infrastructure

DRAM-only Heterogeneous Memory Hierarchy



- Cross-layer research: Hardware-level
  - Develop ECC/compression-centric techniques for block-protected DRAM
  - Investigate practical implementation of block-protected DRAM controller
  - Implement an FPGA-based OpenCAPI-compliant experimental hardware prototyping platform

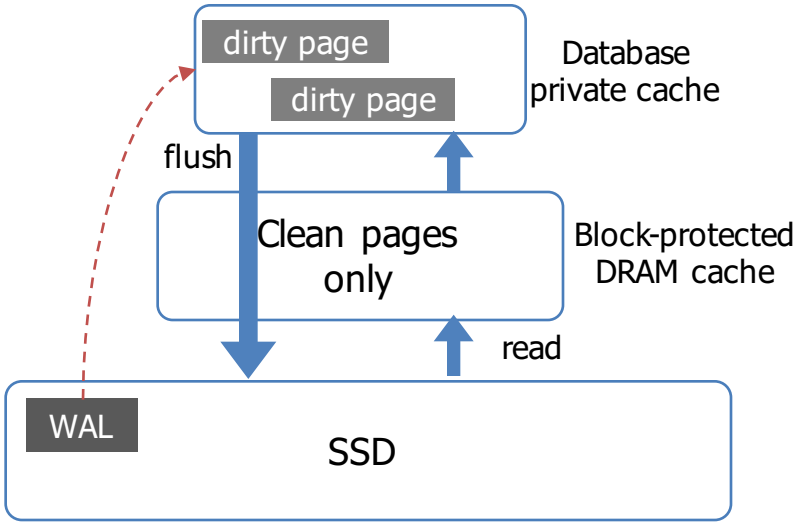
DRAM-only Heterogeneous Memory Hierarchy

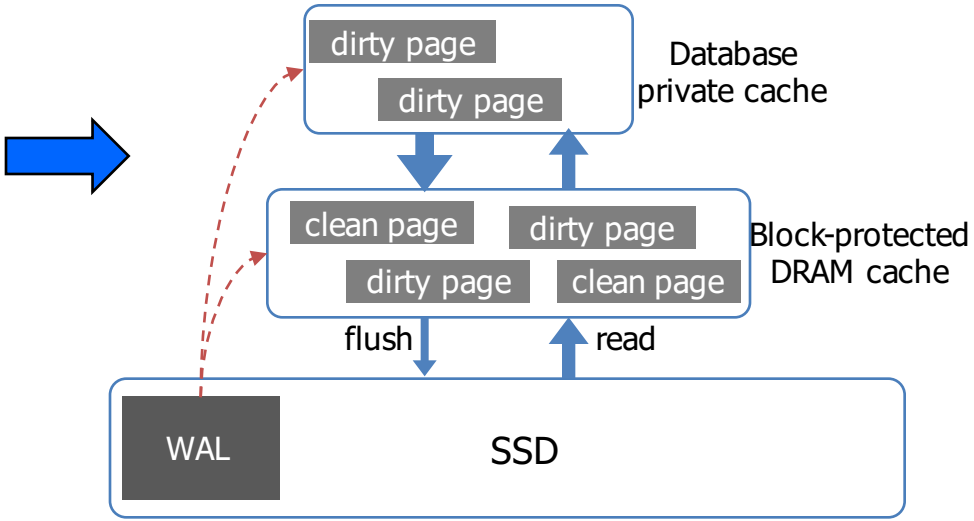


- Cross-layer research: Software-level
  - Study how existing relational database (e.g., MySQL) and NoSQL (e.g., Redis) can effectively utilize the heterogeneous DRAM-only memory system
  - Develop a new in-memory key-value (KV) store that can fully take advantage of the heterogeneous DRAM-only memory system

Initial Research Accomplishment

DRAM-only heterogeneous tiered caching for relational database





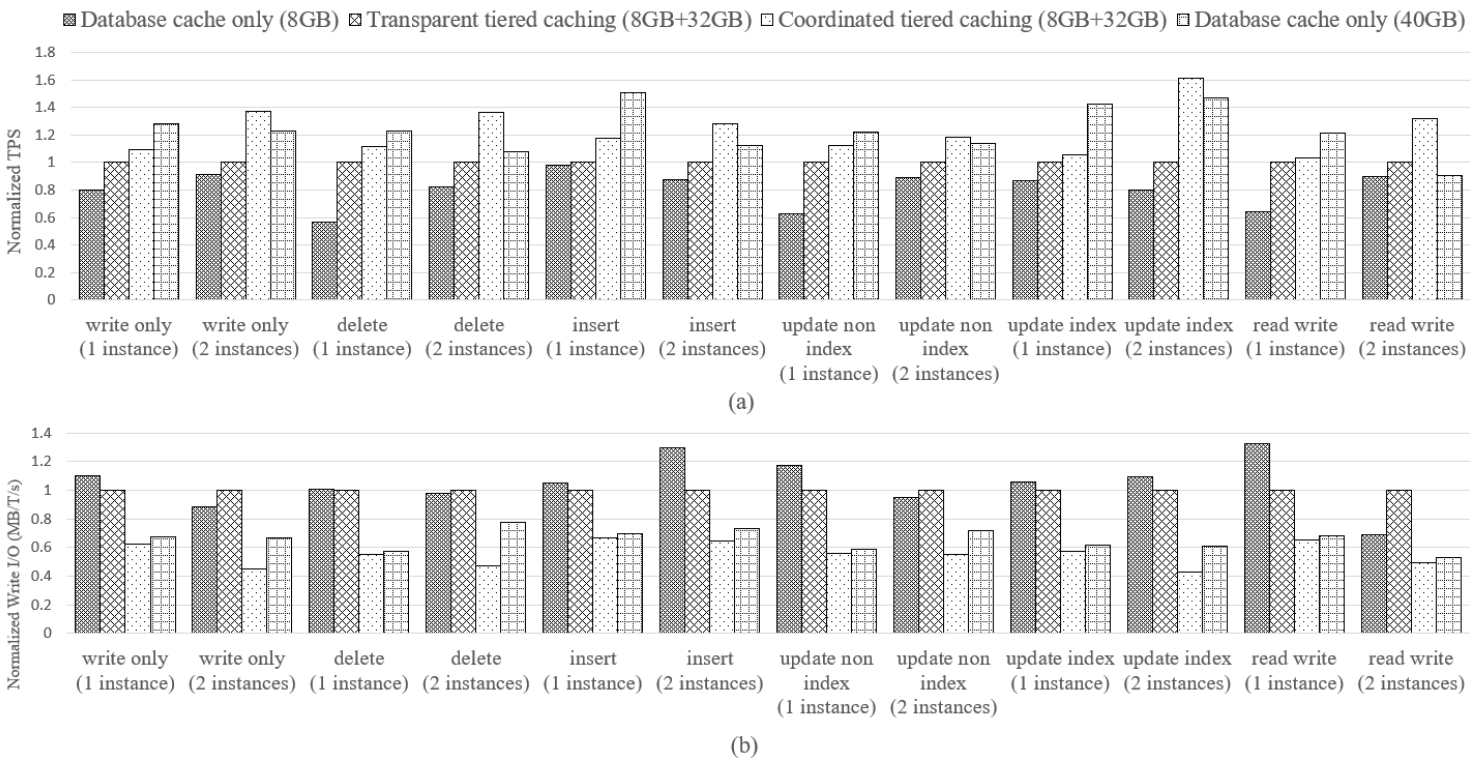
Transparent tiered caching

High write IO traffic ➔ lower performance

Proposed coordinated tiered caching

Low write IO traffic ➔ higher performance

Evaluation: MySQL



(a) Normalized TPS performance, and (b) normalized write throughput