CSci 402 - Operating Systems

Quiz 8

Fall 2023

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(This exam is open book and open notes.
Remember what you have promised when you signed your
Academic Integrity Honor Code Pledge.)

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Time: (N/A) minutes

_____-
Name (please print)

Total: 10 points

_____-
Signature

Instructions

1. This is the first page of your exam. The previous page is a title page and does not have a page number. Since this is a take-home exam, no need to sign above since you won't submit this file.
2. Read problem descriptions carefully. You may not receive any credit if you answer the wrong question. Furthermore, if a problem says *"in N words or less"*, use that as a hint that N words or less are expected in the answer (your answer can be longer if you want). Please note that points may get *deducted* if you put in wrong stuff in your answer.
3. If a question doesn't say `weenix`, please do not give `weenix`-specific answers.
4. Write answers to all problems in the **answers text file**.
5. For non-multiple-choice and non-fill-in-the blank questions, please show all work (if applicable and appropriate). If you cannot finish a problem, your written work may help us to give you partial credit. We may not give full credit for answers only (i.e., for answers that do not show any work). Grading can only be based on what you wrote and cannot be based on what's on your mind when you wrote your answers.
6. Please do *not* just draw pictures to answer questions (unless you are specifically asked to draw pictures). Pictures will not be considered for grading unless they are clearly explained with words, equations, and/or formulas. It's very difficult to draw pictures in a text file and you are not permitted to submit additional files other than the answers text file.
7. For problems that have multiple parts, please clearly *label* which part you are providing answers for.
8. Please ignore minor spelling and grammatical errors. They do not make an answer invalid or incorrect.
9. During the exam, please only ask questions to *clarify* problems. Questions such as "would it be okay if I answer it this way" will not be answered (unless it can be answered to the whole class). Also, you are suppose to know the definitions and abbreviations/acronyms of *all technical terms*. We cannot "clarify" them for you. We also will **not** answer any clarification-type question for multiple choice problems since that would often give answers away.
10. Unless otherwise specified and stated explicitly, multiple choice questions have one or more correct answers. You will get points for selecting correct ones and you will lose points for selecting wrong ones.
11. When we grade your exam, we must assume that you wrote what you meant and you meant what you wrote. So, please write your answers accordingly.

(Q1) (2 points) Which of the following statements are correct about the **basic two-level page table for a 32-bit CPU**?

(1) while performing address translation, virtual page number can be thought of as an array index while the offset cannot be thought of as array index
(2) while performing address translation, virtual page number cannot be thought of as an array index while the offset can be thought of as array index
(3) while performing address translation, virtual page number and the offset in a virtual address can both be thought of as array indices
(4) while performing address translation, if the M bit inside a page table entry is 0, it means that the corresponding physical page number is invalid
(5) none of the above is a correct answer

Answer (just give numbers): _____

(Q2) (2 points) Which of the following statements are correct about **page tables**?

(1) the x86 CPU uses a hashed page table
(2) the CR3 register inside the x86 CPU contains a virtual address
(3) for the x86 CPU, a page directory entry contains a virtual page number while a page table entry contains a physical page number
(4) the inverted page table is usually faster than the basic two level page table
(5) none of the above is a correct answer

Answer (just give numbers): _____

(Q3) (2 points) Which of the following statements are correct about **translation lookaside table (TLB)**?

(1) just like the page table, the TLB is a kernel data structure
(2) in the x86 CPU, the TLB is "flushed" when you change the CR3 register
(3) if a 4-way set associative cache is used to implement a TLB, the bucket size in each line in the TLB is 16 because $2^4 = 16$
(4) in implementing a TLB, fully associative cache is more "expensive" to implement than direct mapping cache
(5) none of the above is a correct answer

Answer (just give numbers): _____

(Q4) (2 points) Which of the following statements are correct about the **storage hierarchy in today's systems**?

(1) the L2 cache is typically faster than RAM
(2) SSD access time is about the same as the RAM access time
(3) the L3 cache is typically faster than the L2 cache
(4) hard drives are typically faster than SSDs
(5) none of the above is a correct answer

Answer (just give numbers): _____

(Q5) (2 points) Let's say that you have just created a new user process, which of the following statements are correct about **demand paging**?

(1) when you get the first page fault in the stack segment and the corresponding page table entry has V = 0, the kernel needs to set up a backing store for the corresponding page in the swap space
(2) with demand paging, you would initialize the page table with V = 1 in every page table entry
(3) when you get the first page fault in the text segment and the corresponding page table entry has V = 0, the kernel would get the missing page from the swap space
(4) when you get the first page fault in the data segment and the corresponding page table entry has V = 0, the kernel would get the missing page from the executable file
(5) none of the above is a correct answer

Answer (just give numbers): _____