Makefile and Git activity

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1 Step 1 – Basic Target Definition

Basic definition of a target with a recipe and dependency

```
bkochuna.o: bkochuna.c

ceho gcc -c bkochuna.c -o bkochuna.o

cp bkochuna.c bkochuna.o
```

2 Step 2 — Definition of a clean target

```
bkochuna.o: bkochuna.c
cecho gcc -c bkochuna.c -o bkochuna.o
cp bkochuna.c bkochuna.o

clean:
frm -rf *.o
```

3 Step 3 — Two targets

```
bkochuna.o: bkochuna.c

echo gcc -c bkochuna.c -o bkochuna.o

pkochuna.c bkochuna.o

kcvaughn.o: kcvaughn.c

echo gcc -c kcvaughn.c -o kcvaughn.o

cp kcvaughn.c kcvaughn.o

rm -rf *.o
```

4 Step 4 — all target

How to make all the things

```
all: bkochuna.o kcvaughn.o

bkochuna.o: bkochuna.c

echo gcc -c bkochuna.c -o bkochuna.o

cp bkochuna.c bkochuna.o

kcvaughn.o: kcvaughn.c

echo gcc -c kcvaughn.c -o kcvaughn.o

cp kcvaughn.c kcvaughn.o

rm -rf *.o
```

5 Step 5 — Using Variables

Use variables; helpful for linking step.

```
1 CC = gcc
3 OBJ = bkochuna.o kcvaughn.o
5 all: main
  bkochuna.o: bkochuna.c
     echo $(CC) -c bkochuna.c -o bkochuna.o
     cp bkochuna.c bkochuna.o
kcvaughn.o: kcvaughn.c
   echo $(CC) -c kcvaughn.c -o kcvaughn.o
     cp kcvaughn.c kcvaughn.o
13
14
15 main: $(OBJ)
  echo $(CC) $(OBJ) -o main.exe
16
17
18 clean:
19 rm -rf *.o
```

6 Step 6 — Multiline input

```
1 CC = gcc
3 OBJ = bkochuna.o \
4 kcvaughn.o
6 all: main
8 bkochuna.o: bkochuna.c
    echo $(CC) -c bkochuna.c -o bkochuna.o
10
    cp bkochuna.c bkochuna.o
11
kcvaughn.o: kcvaughn.c
echo $(CC) -c kcvaughn.c -o kcvaughn.o
    cp kcvaughn.c kcvaughn.o
14
15
16 main: $(OBJ)
echo $(CC) $(OBJ) -o main.exe
19 clean:
20 rm -rf *.o
```

7 Step 7 — Implicit Rules

Suffix substitution