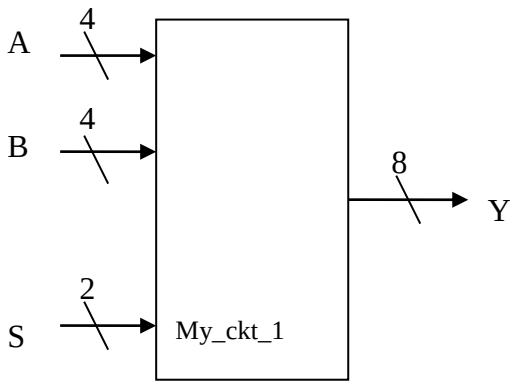
Homework 1
Due Day: 11/5

Consider a system consisting of 3 input ports and 1 output port as shown below.



In the system, the 3 input ports are denoted by A, B, and S, respectively. Let A={Ai, i=0,…,3}, B={Bi, i=0,…,3}, and S={S0,S1}. The output port is denoted by Y={Yi, i=0,…,7}. The input port S determines the mode of the operations. There are 4 modes in the system. The following table shows the operations of each mode.

Mode	Operations
Mode 1 (S={S1,S0}={0,0})	Yi=Ai AND Bi, i=0,…,3.
Mode 2 (S={S1,S0}={0,1})	Y= A*B
Mode 3 (S={S1,S0}={1,0})	Y= A+B
Mode 4 (S={S1,S0}={1,1})	Y=A/B

For modes 2, 3 and 4, inputs A and B are treated as unsigned integers.

Write a VHDL code to implement the system using Quartus II. Your project report should include the following items.

1. the Quartus II project file containing the VHDL code of the system,
2. the word files containing the simulation results and the corresponding discussions.

Hint: Data type UNSIGNED may be useful for signals A, B, S and Y.

Reference output:

(此為範例測資，同學可自行調整輸入內容)