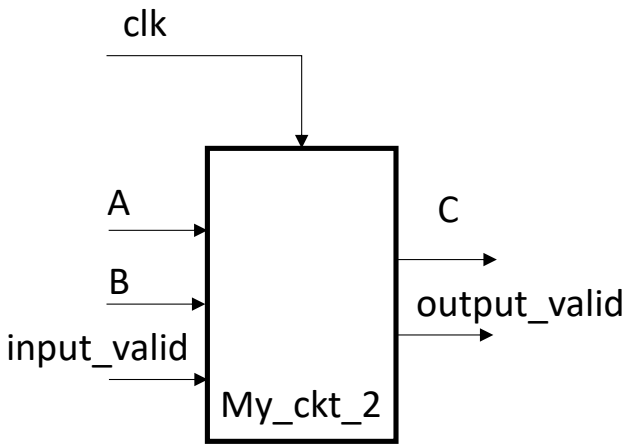
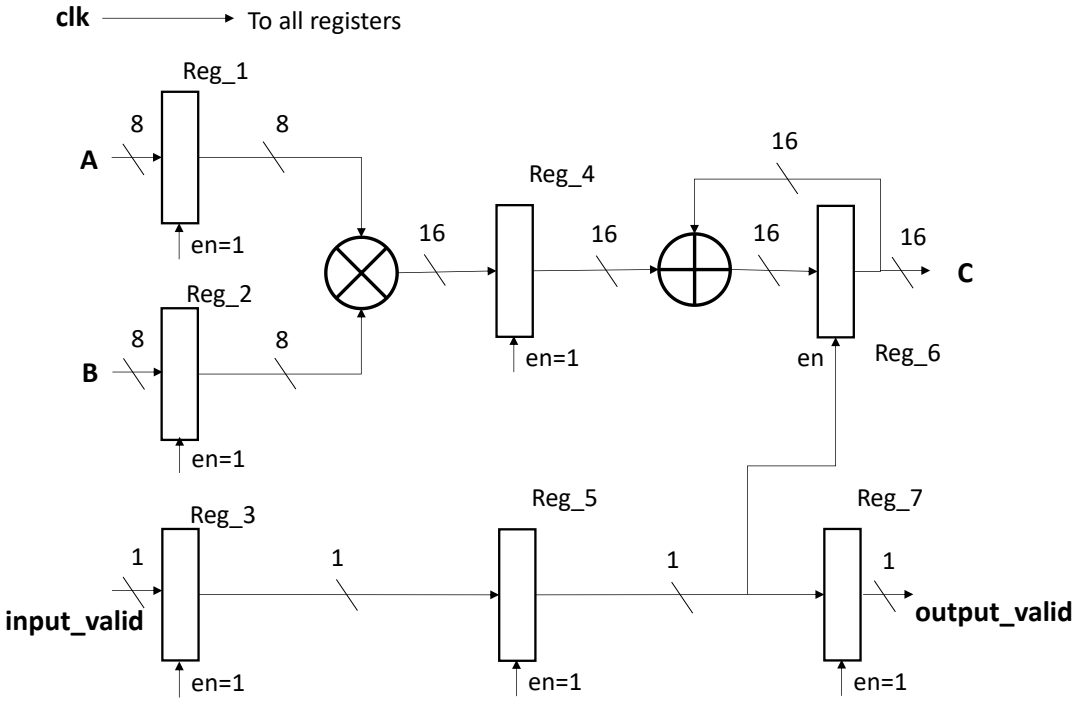
Homework 2
Due Day: 12/3

Consider a system consisting of 4 input ports and 2 output port as shown below.



In the system, the 4 input ports are denoted by clk, A, B, and input_valid, respectively. The output ports are denoted by C and output_valid. The system provides the multiplication and accumulation operations, as shown below.



There are 7 registers (Reg_1, Reg_2, Reg_3, Reg_4, Reg_5, Reg_6, Reg_7) in the circuit. These registers can be implemented by D_FF. There are also an unsigned integer multiplier, and an unsigned integer adder,

Write a VHDL code to implement the system using Quartus II. Your project report should include the following items.

1. the Quartus II project file containing the VHDL code of the system,
2. the word files containing the simulation results and the corresponding discussions.

*作業繳交格式:

請繳交一個壓縮檔，檔名:學號_hwX (e.g. 60947001S_hw2)

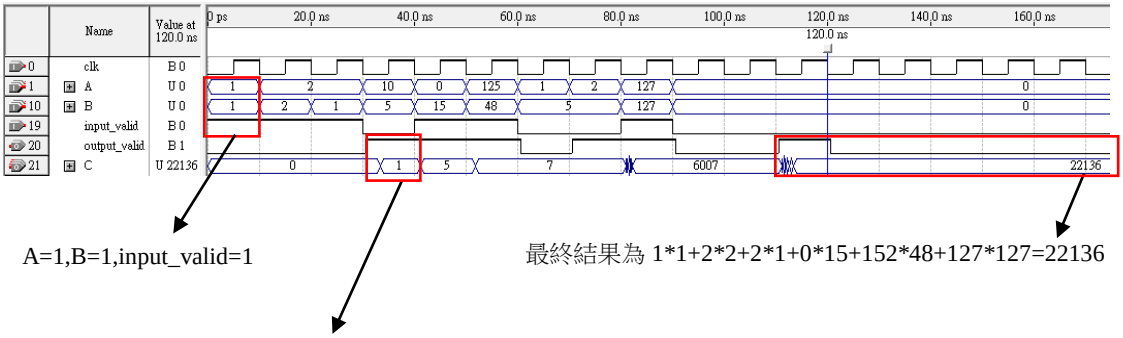
壓縮檔內容包含:

1.心得報告(word/pdf)

2.完整可執行的 quartus project

Reference output:
(此為範例測資，同學可自行調整輸入內容)

測資 1



因此 output_valid 間隔 2 clocks 會有 input_valid 的值 1

C(initial=0)間隔 2 clocks 會有 A*B+C 的值 1。

測資 2