FWC RTL Assignment 2

Due by 10/12/2022

The purpose of this assignment is to enable you to use Xilinx IPs instantiation in Vivado, generate bitstream and run it on the board. The documents required will be more or less the same as the ones mentioned in the last assignment. If you need more info related to the IPs, Google! This is a substantial assignment, so the specification is kept flexible, but you still need to achieve the functionality. I'll list down the basic steps that you can take to get started.

1. *Read the overview of all the three Xilinx IPs mentioned below.*
2. *Plan out the design of your module keeping in mind the ports and working of the above three IPs.*
3. *Write the code of your module and instantiate the IPs appropriately in the code.*

Instantiate 3 Xilinx IPs mentioned below and write a Verilog module to interface with it to achieve the following specification.

The assignment is to generate Fibonacci sequence using addition and store it in a true dual port standalone block memory generator IP from Xilinx. The flow should be such that you generate an entry in the Fibonacci sequence and then you store it in the memory one after another. The memory can be treated as cyclic, i.e., once you have used the entire memory, you can wrap around and start writing from 0^{th} address again. Use appropriate clock (using Xilinx clocking wizard IP, and use the clock available on the FPGA as source clock for the clocking wizard) frequency so that the memory doesn't get filled too quickly. Try to implement a pipelined module. Simulate and verify the functionality. Now, connect system ILA IP to the block memory generator ports to observe the working on the board. Synthesise, implement and generate the bitstream for a board that is available for use (discuss with Praneeth about the availability of the board). Run it on the board and see if you're able to observe data being written to the memory.

Submit your module and tb code, along with a screenshot of the working simulation, timing report as seen at the bottom of Vivado window, and a screenshot of the ILA showing the working, in a single PDF file.