

RTL-Assignment 1

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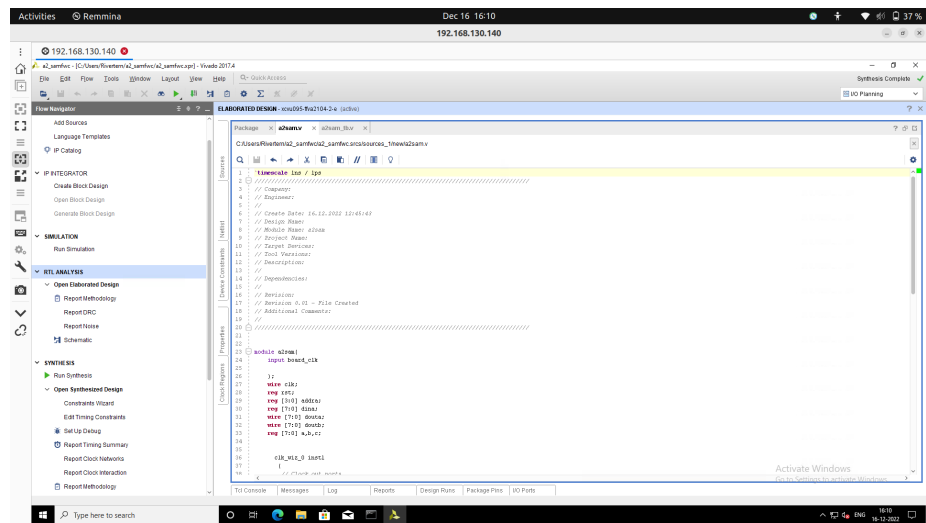


Figure 1: module code

1 Module Code

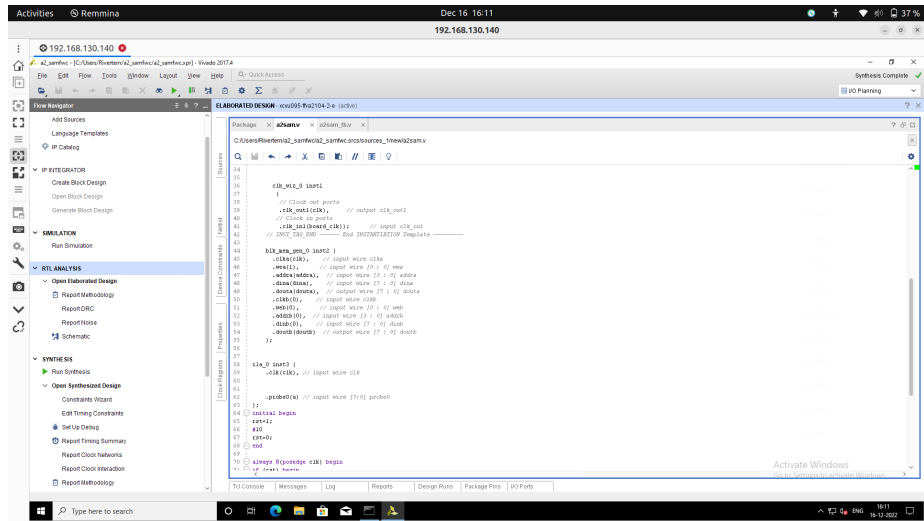


Figure 2: module code

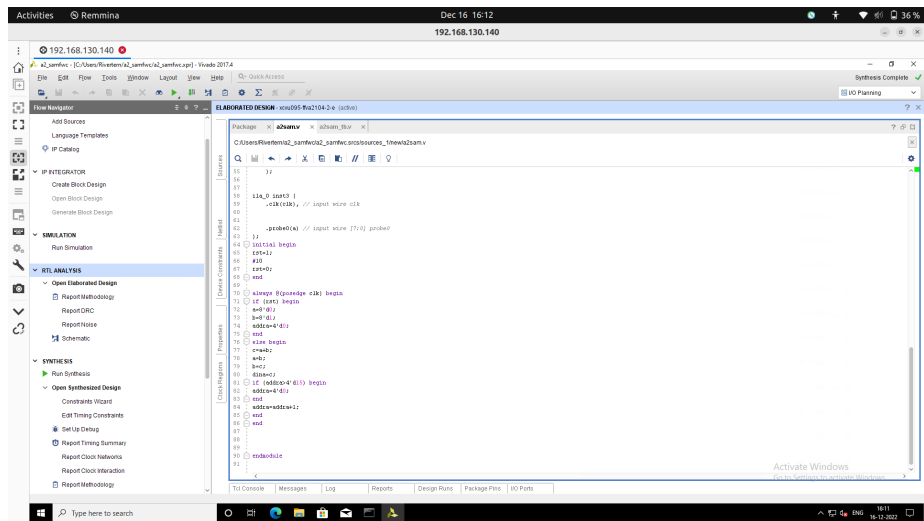


Figure 3: module code

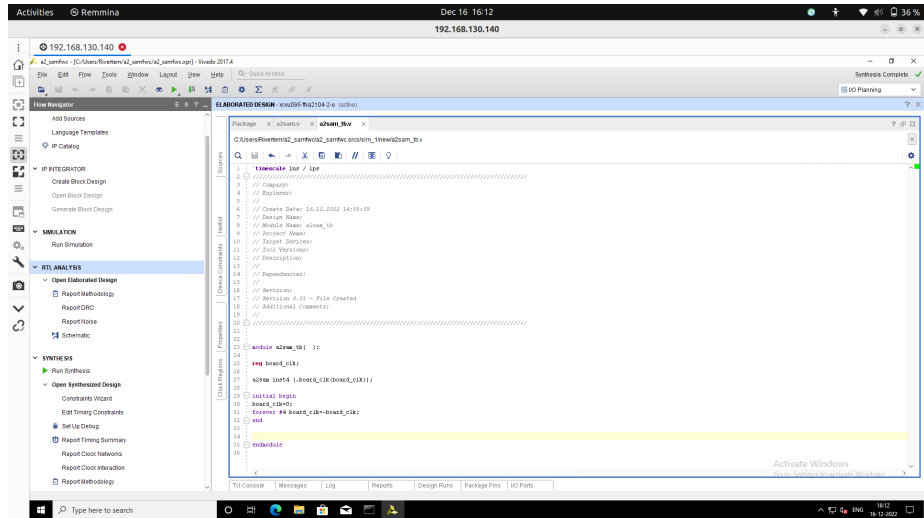


Figure 4: testbench code

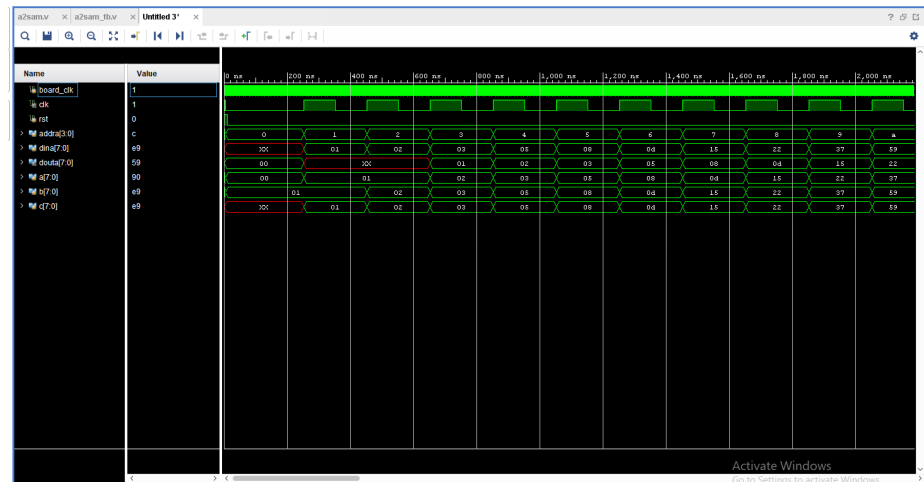


Figure 5: Timing diagram

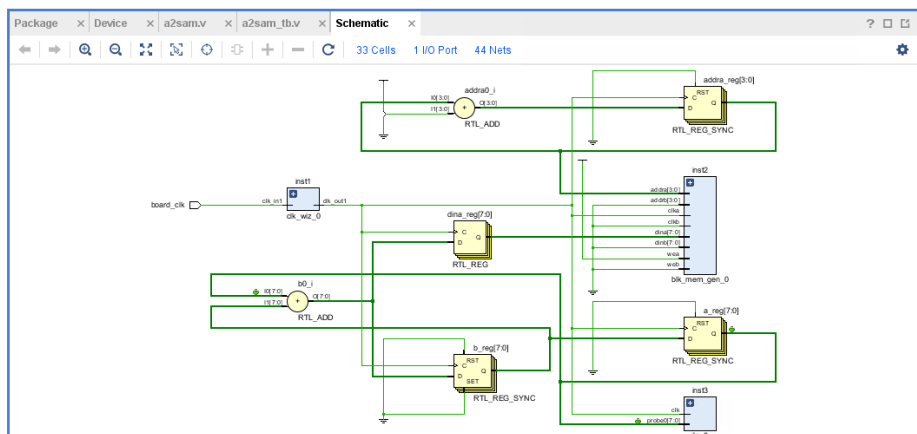


Figure 6: Schematic diagram

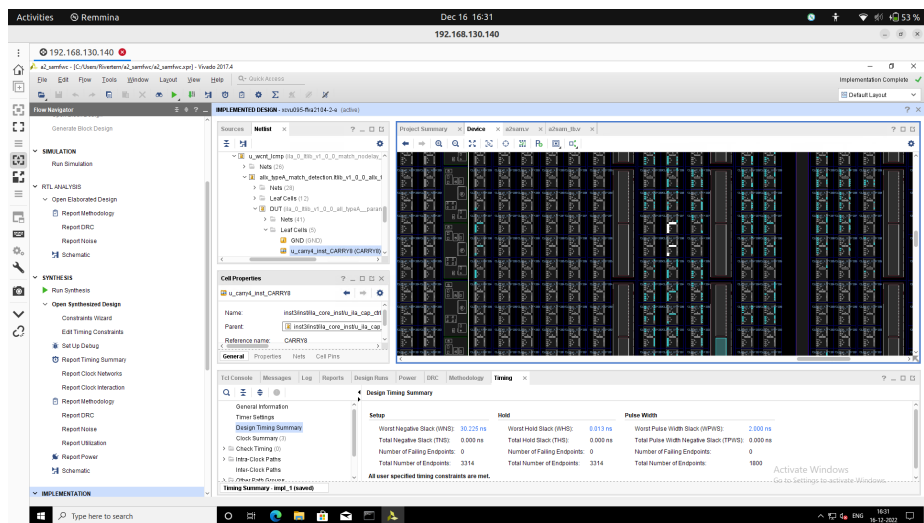


Figure 7: Timing Report