FWC RTL Assignment 1

Due by 27/11/2022

The purpose of this assignment is to enable you to start using the simulation and synthesis tools in Vivado. It requires a substantial amount of work on your part as you need to learn the basics of the Vivado tool before implementing the assignment. Chapters 1 and 2 from UG893 document and chapters 1, 3, and 4 from UG910 document from Xilinx will help in learning the basics of the tool. These documents are available on Google.

Design an 8-bit down counter. The count value is loaded from ‘in’ input on a positive clock edge when ‘latch’ input is high. Count value is decremented by 1 on a positive clock edge while ‘dec’ input is high. Stop decrementing at 0 and raise ‘zero’ flag output active high whenever count value is 0. ‘latch’ input has priority over ‘dec’ input. Whenever ‘divide-by-two’ input is high and ‘latch’ input is low and ‘dec’ input is low (both dec and divide-by-two will never be high at the same time), divide the current contents of the counter by 2.

1. Write a hardware synthesisable Verilog code for the module design.
2. Simulate the design in Vivado by writing a Verilog testbench and reproducing the timing diagram given below.
3. Synthesise the design in Vivado and create a netlist.
4. Submit your design diagram, any FSM that you used, timing diagram, test bench code and module code, etc., as a single PDF file.