4.20.25 - 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM SO-DIMM Design Specification

DDR4 SDRAM SO-DIMM Design Specification

Revision 1.31

August 2019

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1 Product Description

This specification defines the electrical and mechanical requirements for 260 pin, 1.2 V (VDD), Small Outline, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM SO-DIMMs). These DDR4 SO-DIMMs are intended for use as main memory when installed in PCs, laptops and other systems.

Reference design examples are included which provide an initial basis for DDR4 SO-DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666 and PC4-3200 support. All DDR4 SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

Table 1 — Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (nominal)	69.6 mm x 30.0 mm	Refer to MO-310 2 mm wider than DDR3
Pin Count and Pitch	260 on 0.5 mm centers	
DDR4 SDRAMs Supported	4 Gb, 8 Gb, 12 Gb, 16 Gb, 24 Gb, 32 Gb, 64 Gb	78/106-ball FBGA package for x8 and 96/112-ball FBGA for x16 devices. Refer to MO-207: x8 variations DT-z, DW-z x16 variations DU-z, DY-z
Capacity	2 GB - 256 GB	SDP - 32 GB max, 3DS -256 GB max
DDR4 SDRAM width	x8, x16	
Serial Presence Detect, Thermal Sensor (SPD-TSE/SPD)	512 byte	See EE1004-v and TSE2004av specifications
Voltage Options	PC4 - 1.2 V for VDD	All DDR4 modules use a common VDD–VDDQ power plane. They are tied together on the DIMM, but by standard definition are supported on the pinout to accommodate future enhancements.
	PC4 - 0.6 V for VTT	Termination voltage for Address, Command, and Control.
	2.5 V for VPP	This supply has VSS as its return path. On DIMM It is treated as a separate supply from VDDSPD.
	2.5 V or 3.3 V for VDDSPD	SPD supply is operable with 2.5 V or 3.3 V.
Interface	1.2 V signaling	

2 Environmental Requirements

DDR4 SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation. These will typically be non-ECC SO-DIMMs.

DDR4 SO-DIMMs that have ECC support are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature	-50 to +100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Note 2 Up to 9850 ft.
Note 3 The component maximum case temperature (T_{CASE}) shall not exceed the value specified in the DDR4 DRAM component specification.

3 Connector Pinout and Signal Description

Table 3 — Connector Pin Definition

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I^2C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

Note 1 RAS_n is a multiplexed function with A16.
Note 2 CAS_n is a multiplexed function with A15.
Note 3 WE_n is a multiplexed function with A14.

3 Connector Pinout and Signal Description (cont'd)

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Level	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	VDD	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	VDD	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	VDD	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	VDD	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	VDD	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	VDD	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	VDD	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	VDD	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	VDD	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	VDD	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	VDD	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

Table 4 — Input/Output Functional Description (Cont'd)

Symbol	Type	I/O Level	Function
RESET_n	CMOS Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.
PARITY	Input	VDD	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	VDD	ALERT: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. Using this signal or not is dependent on the system. This is an open drain signal. It requires a pullup resistor on the system.
EVENT_n	Output	VDDSPD	I2C thermal event indicator. Open drain, requires a pullup resistor on the system.
SAVE_n	Input/ Output	-	Not used on SODIMMs. SODIMMs will have no connection to this pin. See specifications of NVDIMMs for signal description.
SCL	Input	VDDSPD	Bus clock used to strobe data into and out of I2C devices. Open drain and requires a pullup resistor on the system.
SDA	Input/ Output	VDDSPD	I2C data. Open drain and requires a pullup resistor on the system.
SA0-SA2	Input	VDDSPD	Device address for the SPD.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.
NC			No Connect: No on DIMM electrical connection is present.
VDD[1]	Supply		Power Supply: 1.2 V +/- 0.06 V
VSS	Supply		Ground
VTT[2]	Supply		Power Supply: 0.6 V
VPP	Supply		DRAM Activating Power Supply: 2.5 V (2.375 V min, 2.75 V max)
VREFCA	Supply		Reference voltage for CA
VDDSPD	Supply		Power supply used to power the I2C bus on the SPD.

3.1 DDR4 SO-DIMM Connector Pin Assignments

Table 5 — DDR4 SO-DIMM 260 Pin Connector Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	1	2	VSS	A3	131	132	A2
DQ5	3	4	DQ4	A1	133	134	EVENT_n
VSS	5	6	VSS	VDD	135	136	VDD
DQ1	7	8	DQ0	CK0_t	137	138	CK1_t
VSS	9	10	VSS	CK0_c	139	140	CK1_c
DQS0_c	11	12	DM0_n, DBI0_n, NC	VDD	141	142	VDD
DQS0_t	13	14	VSS	PARITY	143	144	A0
VSS	15	16	DQ6		KEY		
DQ7	17	18	VSS				
VSS	19	20	DQ2	BA1	145	146	A10/AP
DQ3	21	22	VSS	VDD	147	148	VDD
VSS	23	24	DQ12	CS0_n	149	150	BA0
DQ13	25	26	VSS	A14/WE_n	151	152	A16/RAS_n
VSS	27	28	DQ8	VDD	153	154	VDD
DQ9	29	30	VSS	ODT0	155	156	A15/CAS_n
VSS	31	32	DQS1_c	CS1_n	157	158	A13
DM1_n, DBI1_n, NC	33	34	DQS1_t	VDD	159	160	VDD
VSS	35	36	VSS	ODT1	161	162	C0, CS2_n, NC
DQ15	37	38	DQ14	VDD	163	164	VREFCA
VSS	39	40	VSS	C1, CS3_n, NC	165	166	SA2
DQ10	41	42	DQ11	VSS	167	168	VSS
VSS	43	44	VSS	DQ37	169	170	DQ36
DQ21	45	46	DQ20	VSS	171	172	VSS
VSS	47	48	VSS	DQ33	173	174	DQ32
DQ17	49	50	DQ16	VSS	175	176	VSS
VSS	51	52	VSS	DQS4_c	177	178	DM4_n, DBI4_n, NC
DQS2_c	53	54	DM2_n, DBI2_n, NC	DQS4_t	179	180	VSS
DQS2_t	55	56	VSS	VSS	181	182	DQ39
VSS	57	58	DQ22	DQ38	183	184	VSS
DQ23	59	60	VSS	VSS	185	186	DQ35
VSS	61	62	DQ18	DQ34	187	188	VSS
DQ19	63	64	VSS	VSS	189	190	DQ45
VSS	65	66	DQ28	DQ44	191	192	VSS
DQ29	67	68	VSS	VSS	193	194	DQ41
VSS	69	70	DQ24	DQ40	195	196	VSS
DQ25	71	72	VSS	VSS	197	198	DQS5_c
VSS	73	74	DQS3_c	DM5_n, DBI5_n, NC	199	200	DQS5_t
DM3_n, DBI3_n, NC	75	76	DQS3_t	VSS	201	202	VSS
VSS	77	78	VSS	DQ46	203	204	DQ47
DQ30	79	80	DQ31	VSS	205	206	VSS
VSS	81	82	VSS	DQ42	207	208	DQ43

Table 5 — DDR4 SO-DIMM 260 Pin Connector Pin Wiring Assignments (Cont'd)

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
DQ26	83	84	DQ27	VSS	209	210	VSS
VSS	85	86	VSS	DQ52	211	212	DQ53
CB5, NC	87	88	CB4, NC	VSS	213	214	VSS
VSS	89	90	VSS	DQ49	215	216	DQ48
CB1, NC	91	92	CB0, NC	VSS	217	218	VSS
VSS	93	94	VSS	DQS6_c	219	220	DM6_n, DBI6_n, *NC*
DQS8_c	95	96	DM8_n, DBI8_n, *NC*	DQS6_t	221	222	VSS
DQS8_t	97	98	VSS	VSS	223	224	DQ54
VSS	99	100	CB6, NC	DQ55	225	226	VSS
CB2, NC	101	102	VSS	VSS	227	228	DQ50
VSS	103	104	CB7, NC	DQ51	229	230	VSS
CB3, NC	105	106	VSS	VSS	231	232	DQ60
VSS	107	108	RESET_n	DQ61	233	234	VSS
CKE0	109	110	CKE1	VSS	235	236	DQ57
VDD	111	112	VDD	DQ56	237	238	VSS
BG1	113	114	ACT_n	VSS	239	240	DQS7_c
BG0	115	116	ALERT_n	DM7_n, DBI7_n, *NC*	241	242	DQS7_t
VDD	117	118	VDD	VSS	243	244	VSS
A12	119	120	A11	DQ62	245	246	DQ63
A9	121	122	A7	VSS	247	248	VSS
VDD	123	124	VDD	DQ58	249	250	DQ59
A8	125	126	A5	VSS	251	252	VSS
A6	127	128	A4	SCL	253	254	SDA
VDD	129	130	VDD	VDDSPD	255	256	SA0
				VPP	257	258	VTT
				VPP	259	260	SA1

4 Power Details

4.1 DIMM Voltage Requirements

The DIMM voltage requirements and the SDRAM voltage requirements are not identical. There must be some allowance for a small voltage drop across the DIMM. Table 6 defines the requirements for the Host at the DIMM socket.

Some modules have lower current requirements. Any specific module must meet the SDRAM voltage requirements for its worst case supply currents.

Table 6 — DDR4 SO-DIMM DC Operating Voltage[1,2,3] - 1.2 V operation

Symbol	Parameter	Voltage Rating (V)			Maximum Expected Current (AMPs)	Power State
		Minimum	Typical[4]	Maximum		
VDD	Supply Voltage	1.16	1.21	1.26	5.0	Operational
VPP	Activation Supply Voltage	2.41	2.50	2.75	1.5	Operational
VTT[5]	Termination Voltage	0.565	0.605	0.64	0.5	Operational
VDDSPD	SPD Supply Voltage	2.41	2.5	2.75	0.1	Operational

Note 1 20 MHz bandwidth limited measurement for all voltages in the table.
Note 2 Voltages are measured at the DIMM gold fingers.
Note 3 The SDRAM specification must be met and take precedence over this document.
Note 4 Typical voltage is platform dependent, suggested value only.
Note 5 At the DIMM interface VTT is the only voltage during normal operating conditions that can both source and sink current.
Note 6 SDRAM VDD specification range.

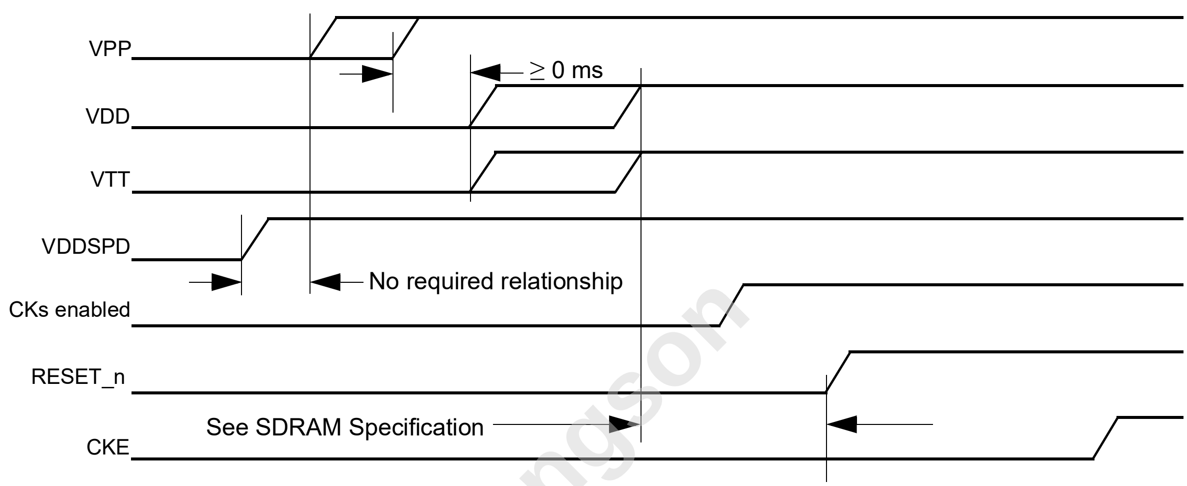
4.2 Rules for Power-Up Sequence

The timing characteristics are illustrated in Figure 1.

VPP is the point of reference for the power on sequence. Note the following points of interest:

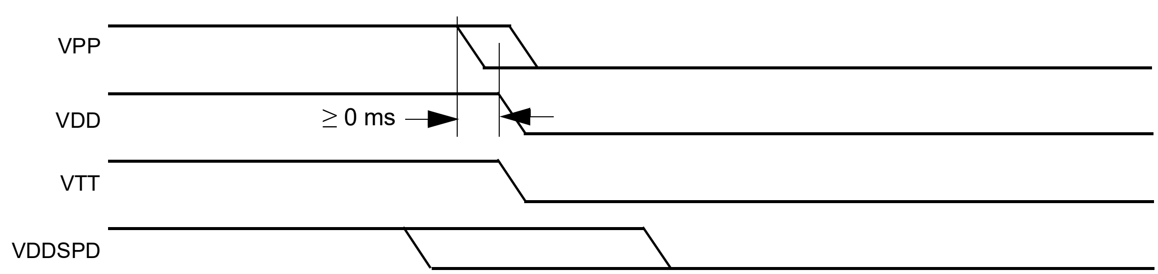
1. VDDSPD is an independent power source which has no specific relationship to the other power sources.
2. VTT has a specific relationship to VDD: VTT = VDD/2.

The CK_t/CK_c input signals must be driven LOW throughout the VDD power ramp at least until the VDD supply voltage has settled to its final value.



Note Start of ramp reference is 300 mV, as per the SDRAM specification.

Figure 1 — Graphical View of Recommended Power Sequence



Note It is permissible for VPP to start ramping off prior to VDD starting to ramp off. VPP must remain ≥ VDD.

Figure 2 — Graphical View of Recommended Power Down Sequence

4.3 Feed Through Voltage (VFT)

The normal power down sequence requires the voltage relationships established during power on be maintained. VFT is defined as the voltage delta between VSS and the associated power plane with no power applied to that plane. The absolute value of this voltage must remain less than 200 mV (|VFT| ≤ 0.20 V), which is less than the 300 mV DRAM ramp reference level for start or end of voltage ramp.

5 Component Details

MO-207 allows a maximum DRAM package height of 21.0 mm. The maximum package size is not required for DDR4 SO-DIMMs. The larger the DRAM package, the farther it must be placed from the edge connector and the longer the DQ bus must be. Minimizing the DRAM package size to what is actually required improves signal integrity. Decoupling is improved if the capacitors are placed closer to the DRAM balls. Power delivery is improved with a reduction in width of the DRAMs to what is actually required.

See section 6.7.3 for target DRAM package size.

Figure 3 shows the mechanical information for the DDR4 SDRAM components. To use a smaller SDRAM component some or all of the mechanical support balls may be omitted.

Figure 3 — DIMM Ball Patterns for DDR4 SDRAM Components

5 Component Details (Cont'd)

Table 7 — DDR4 x8 SDRAM DIMM Pad Array

Top view

MO-207 variation DW-z

	1	2	3	4	8	9	10	11	
A	NC[8]	NC[8]		NC[8]	NC[8]		NC[8]	NC[8]	
B									
C	NC[8]	NC[8]		NC[8]	NC[8]		NC[8]	NC[8]	
D									
E									
F	NC[8]	VDD	VSSQ	NC[1]	DM_n, DBI_n, NC[2]	VSSQ	VSS	NC[8]	A
G		VPP	VDDQ	DQS_c	DQ1	VDDQ	ZQ		B
H		VDDQ	DQ0	DQS_t	VDD	VSS	VDDQ		C
J		VSSQ	DQ4	DQ2	DQ3	DQ5	VSSQ		D
K		VSS	VDDQ	DQ6	DQ7	VDDQ	VSS		E
L		VDD	NC, ODT1[3]	ODT	CK_t	CK_c	VDD		F
M		VSS	NC, CKE1, C0[4]	CKE	CS_n	NC, CS1_n, C1[5]	TEN[9]		G
N		VDD	A14/WE_n	ACT_n	A15/CAS_n	A16/RAS_n	VSS		H
P		VREFCA	BG0	A10/AP	A12/BC_n	BG1	VDD		J
R		VSS	BA0	A4	A3	BA1	VSS		K
T		RESET_n	A6	A0	A1	A5	ALERT_n		L
U		VDD	A8	A2	A9	A7	VPP		M
V	NC[8]	VSS	A11	PAR[6]	A17[7]	A13	VDD	NC[8]	N
W									
Y									
AA	NC[8]	NC[8]		NC[8]	NC[8]		NC[8]	NC[8]	
AB									
AC	NC[8]	NC[8]		NC[8]	NC[8]		NC[8]	NC[8]	
		1	2	3	7	8	9		

MO-207 variation DT-z

Note 1 TDQS_c is not a valid function for DDR4 SDRAMs on SO-DIMMs
Note 2 TDQS_t is not a valid function for DDR4 SDRAMs on SO-DIMMs.
Note 3 C2 is not valid functions for DDR4 SDRAMs on SO-DIMMs. ODT1 will be valid for DDR4 DDP SDRAMs only.
Note 4 CKE1 is valid functions for DDR4 DDP SDRAMs on SO-DIMMs.
Note 5 This pin is NC for SDP SDRAM packages. For DDP SDRAM packages, CS1_n will be valid. For 3DS SDRAM packages, C1 will be valid only for a four die stack.
Note 6 Parity input for address parity.
Note 7 A17 is not valid for x8 and x16 SDRAMs of 16G bits or less.
Note 8 These balls are mechanical support balls for large DRAM packages. A pad array to support MO-207 variation DT-z will not include these balls.
Note 9 TEN, Test Enable is not intended to be used on SO-DIMM modules and must be tied low.

5 Component Details (Cont'd)

Table 8 — DDR4 x16 SDRAM DIMM Pad Array

Top view

MO-207 variation DY-z

	1	2	3	4	8	9	10	11	
A	NC[4]	NC[4]		NC[4]	NC[4]		NC[4]	NC[4]	
B									
C									
D	NC[4]	VDDQ	VSSQ	DQ8	UDQS_c	VSSQ	VDDQ	NC[4]	A
E		VPP	VSS	VDD	UDQS_t	DQ9	VDD		B
F		VDDQ	DQ12	DQ10	DQ11	DQ13	VSSQ		C
G		VDD	VSSQ	DQ14	DQ15	VSSQ	VDDQ		D
H		VSS	UDM_n, UDBI_n[1]	VSSQ	LDM_n, LDBI_n[1]	VSSQ	VSS		E
J		VSSQ	VDDQ	LDQS_c	DQ1	VDDQ	ZQ		F
K		VDDQ	DQ0	LDQS_t	VDD	VSS	VDDQ		G
L		VSSQ	DQ4	DQ2	DQ3	DQ5	VSSQ		H
M		VDD	VDDQ	DQ6	DQ7	VDDQ	VDD		J
N		VSS	CKE	ODT	CK_t	CK_c	VSS		K
P		VDD	A14/WE_n	ACT_n	CS_n	A16/RAS_n	VDD		L
R		VREFCA	BG0	A10/AP	A12/BC_n	A15/CAS_n	VSS		M
T		VSS	BA0	A4	A3	BA1	TEN[5]		N
U		RESET_n	A6	A0	A1	A5	ALERT_n		P
V		VDD	A8	A2	A9	A7	VPP		R
W	NC[4]	VSS	A11	PAR[2]	NC[3]	A13	VDD	NC[4]	T
Y									
AA									
AB	NC[4]	NC[4]		NC[4]	NC[4]		NC[4]	NC[4]	
		1	2	3	7	8	9		

MO-207 variation DU-z

Note 1 TDQS_t and TDQS_c are not valid functions for DDR4 SDRAMs on SO-DIMMs.
Note 2 Parity input for address parity.
Note 3 A17 is not valid for x8 and x16 SDRAMs of 16G bits or less.
Note 4 These balls are mechanical support balls for large DRAM packages. A pad array to support MO-207 variation DU-z will not include these balls.
Note 5 TEN, Test Enable is not intended to be used on SO-DIMM modules and must be tied low.

5.1 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR4 SDRAM signals.

Bypass capacitors for DDR4 SDRAM devices must be located near the device power pins.

5.2 Decoupling Guidelines

Table 9 — DDR4 SO-DIMM Decoupling Capacitor Guidelines

	Guideline	Notes
VDD	Minimum of two decoupling capacitors to VSS per SDRAM	Should be placed as close as possible to the DRAM VDD ball
	Minimum of four bulk decoupling capacitors to VSS per module	
VTT	Minimum of one decoupling capacitor to VDD per every two termination resistors or a decoupling capacitor at both ends of each resistor network	Should be placed as close as possible to the termination resistors
	Minimum of one decoupling capacitor to VDD (located near the card edge VTT pin) or a decoupling capacitor at both ends of each resistor network	
VPP	Minimum of one decoupling capacitor to VSS per DRAM ball	Should be placed as close as possible to the DRAM VPP ball
	Minimum of one decoupling capacitor to VSS (located near the card edge VPP pin)	
VREFCA	Minimum of one decoupling capacitor to VDD per DRAM	Should be placed as close as possible to the DRAM VREFCA ball
	Minimum of one decoupling capacitor to VDD (located near the card edge VREFCA pin)	

Note 1 Decoupling capacitor values vary by module and may be staggered to achieve best overall impedance vs. frequency response.
Note 2 Recommended values for decoupling are 0.01 µF, 0.1 µF, and 1.0 µF.
Note 3 Recommended value for bulk decoupling is 4.7 µF.
Note 4 Depending on the DRAM package size, all placements may not be possible.

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into four groups:
1. Data and Strobe (DQ)
2. Address and Command (ADD/CMD)
3. Control (CTRL)
4. Clock (CK)

The following table summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. They sweep from the left side of the module to the right.

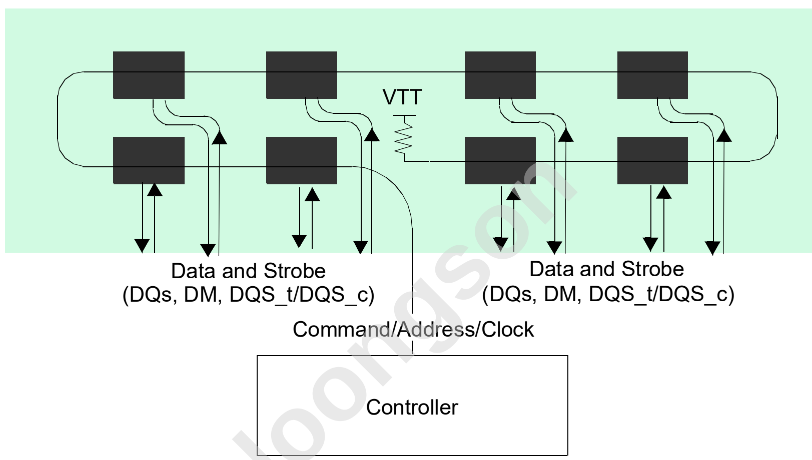


Figure 4 — Example SO-DIMM Fly-By Topology

6.2 Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for SO-DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. A typical data net structure is shown in the Figure 5.

6.2 Explanation of Net Structure Diagrams (Cont'd)

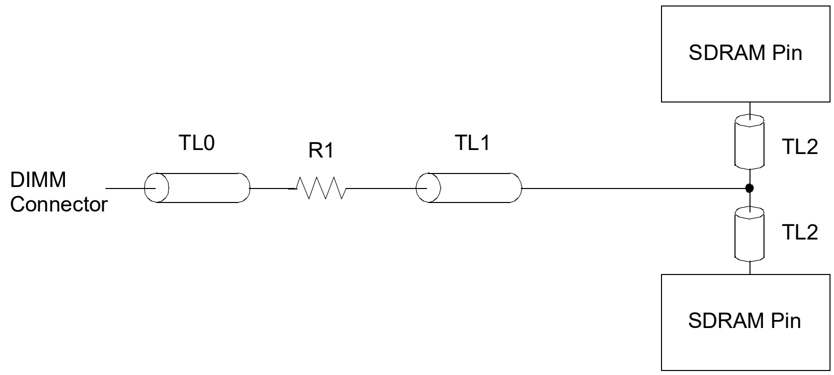


Figure 5 — Net Structure Example

6.3 General Net Structure Routing Rules

Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace segment length table that summarizes the minimum and maximum length for each trace segment in each signal group.

6.3.1 Clock, Control, and Address/Command Groups

DDR4 modules implement a fly-by topology for routing CK, CTRL, and ADD/CMD signal groups. CTRL and ADD/CMD groups on DDR4 modules are length/delay matched to CK, between the connector and each SDRAM, resulting in a significantly reduced timing skew across these groups. Table 10 contains length/delay matching rules associated with these signal groups.

For the length tables in the Annexes where there is not a specified tolerance and the tolerance is not covered by Table 10 a value of ± 1.0 mm shall be used.

Table 10 — CK, CTRL, and ADD/CMD Group Length Matching Rules

Signal Group	Matching Rules
CK_t-to-CK_c Matching	Match TLx segment by TLx segment to within 0.1 mm. See Figure 6 for naming.
CK Pair-to-CK Pair Matching (Pair-to-Pair: Average Length)	Match total compensated length from connector to each SDRAM to within 0.25 mm
CTRL Group Matching	Match total compensated length from connector to each SDRAM to within 1.0 mm
CTRL-to-CK Matching	Match total compensated length of all CTRL signals from connector to each SDRAM to within CK ± 0.5 mm
ADD/CMD Group Matching	Match total compensated length from connector to each SDRAM to within 1.0 mm
ADD/CMD-to-CK Matching	For one rank modules the ADD/CMD group must be matched to the CK to within ± 0.5 mm. For two rank modules, simulations (or calculations) are required to establish what lengths are required to match timing between CK and ADD/CMD.
TL2 Stub Length Matching	Match TL2 stub length at each SDRAM, on a given signal, to within ± 1.5 mm. Where there is a difference in TL2 segments between a TOP and BOTTOM SDRAM, the length for the TOP SDRAM will be used. See Figure 6 for naming.

Table 10 — CK, CTRL, and ADD/CMD Group Length Matching Rules (Cont'd)

Signal Group	Matching Rules
TL2 MAX Stub Length Limits ADD/CMD	TL2 ≤ 4.0 mm. See Figure 6 for naming. Compensation is not applied for this measurement.
TL2 MAX Stub Length Limits Clock	TL2 ≤ 2.0 mm. See Figure 6 for naming. Compensation is not applied for this measurement.
TL2 MAX Stub Length Limits CTRL	TL2 ≤ 3.7mm. See Figure 6 for naming. Compensation is not applied for this measurement.
CK First-to-Last Length	Maximum length from first SDRAM and last SDRAM = 205 mm
Neck down Length	5.0 mm ≤ length ≤10.0 mm; match to within ± 1.0 mm if there is a long lead-in section.

Note 1 All length matching is done using velocity compensated stripline equivalent lengths.
Note 2 A velocity compensation ratio of 1.1 will be used (MS length/1.1 = SL equivalent length).
Note 3 Neck down length is the trailing portion of the TL1 segment, which is routed at the standard 0.1 mm width.
Note 4 Maximum first-to-last length can be calculated by subtracting length to first SDRAM from length to last SDRAM.
Note 5 Via compensation is required. For via equivalent length see section 6.3.8 on page 23.

6.3.2 Lead-in vs. Loaded Sections

See Figure 6 for transmission line name designations. The CK, CTRL, and ADD/CMD topologies are conceptually divided into two topology sections. The segments between the connector and the first SDRAM node via (TL0 + TL1) are collectively termed the lead-in section, while the segments that run between SDRAM node vias (TL3), as well as the SDRAM load stubs (TL2), are collectively termed the loaded section. The loaded section also contains the segments between the last SDRAM and the termination (TL4).

For DDR4, there are 2 basic placements for DRAM on SO-DIMMs. One case is as in Figure 4 with DRAMs placed in two rows. For this placement the lead-in section is short and will not have a trace impedance difference from the other traces on the bus.

For the placement where there is only a single row, the lead-in section will be much longer. This would normally cause a greater impedance discontinuity. In order to reduce the impedance discontinuity seen at the first load, the lead-in section is routed at a lower nominal impedance than the loaded section, typically with the lead-in section routed at 40 Ω nominal, and the loaded section routed at 55 Ω nominal, although some modules may vary. The transition from the wider lead-in trace width to the standard width of the loaded section must occur within a length window preceding the first SDRAM node via, which is termed the neck down length. The first DRAM is the one on the extreme left.

6.3.3 Length/Delay Matching to SDRAM Devices

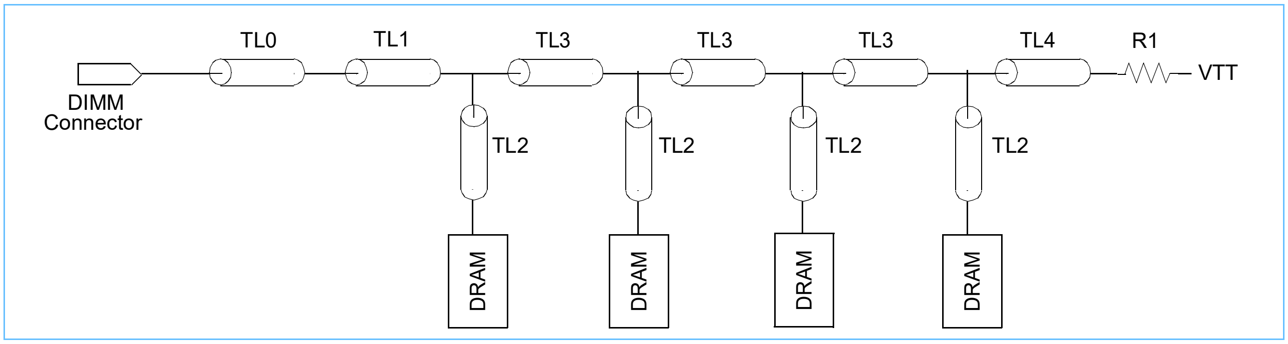


Figure 6 — Example Address routing topology

As mentioned previously, length/delay matching is required between the connector and each SDRAM individually. The length/delay matching process is iterative in nature, and there is no single-best method defined. It is generally recommended that the path from the connector to the first SDRAM (TL0 + TL1 + TL2) be matched across the CK group, and then across the CTRL and ADD/CMD groups—as per the length matching guidelines—adjusting the CK length as needed to reach the length window of the CTRL and ADD/CMD groups. It is important to note that matching is done from connector to the SDRAM ball, and includes the TL2 segment. It is during this process that the breakout pattern dependent length variance in the TL2 stub on each signal will be tuned out.

Once length/delay matching to the first device is complete, the length matching to the remaining devices is straightforward and can be accomplished by simply length-matching the intra-node segments (TL3), assuming the TL2 stub length for a given signal does not vary from SDRAM to SDRAM.

The total compensated length from the connector to the first and last SDRAM is documented in the segment length tables for each module type, in the net structure definitions sections; however, it is assumed that the length matching rules are met at all SDRAM devices.

6.3.4 Velocity Compensation

Since the lead-in section can have a wide variation in the proportion of its length routed as microstrip (MS) and stripline (SL), the length/delay matching process includes a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the stripline equivalent length. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

6.3.5 Load/Delay Compensation

The concept of load/delay compensation refers to the technique whereby the segment lengths between SDRAMS, on the CLK and CTRL signal groups, are purposely lengthened in order to add additional flight time delay, as required to compensate for the fact that the ADD/CMD topology for 2 rank modules has 2 loads (1 top + 1 bottom) for each fly-by node, whereas the CLK and CTRL topologies have only one load per node. Where implemented, the CLK and CTRL segments between SDRAMs shall be routed approximately 4.5mm longer than the corresponding segment on ADD/CMD group. A specific number can be identified using simulation or calculation. The net result of this compensation is less overall ADD/CMD to CLK skew across the module, thereby improving the ability of the controller to correctly center the CLK within the ADD/CMD and CTRL valid windows.

6.3.6 Data and Strobe Group

The DDR4 modules treat each byte lane as a separate signal sub-group, with each byte lane group length/delay matched with velocity compensation as previously described. The length of the individual byte lanes may vary substantially across the module, with the controller providing timing realignment circuitry. A summary table of the length/delay matching rules associated with the data signal group is provided below.

Two DIMMs per channel (2DPC) may have a sensitivity to SO-DIMM DQ stub length for motherboard topologies using a TEE configuration. To support this topology at higher speeds it is recommended that SO-DIMM designs have a minimum uncompensated DQ length of 15 mm.

Table 11 — Data and Strobe Group Length Matching Rules

Signal Group	Matching Rules
DQS_t-to-DQS_c Matching	Match total compensated length to within 0.1 mm
DQ/DM to DQS within Byte Lane	Match total compensated length from the connector to each SDRAM of all DQ and DM signals within a byte lane to within DQS ± 1.0 mm
Minimum Byte Lane Length	Minimum uncompensated length from the connector to the SDRAM shall not be less than 11.0 mm. A minimum of 15.0 mm is recommended for future designs to support motherboard topologies using a TEE configuration.
Maximum Byte Lane Length	Maximum uncompensated length from the connector to the SDRAM shall not be greater than 30.5 mm

Note 1 All length matching is done using velocity compensated stripline equivalent lengths.
Note 2 A velocity compensation ratio of 1.1 will be used (MS length/1.1 = SL equivalent length).
Note 3 Via compensation is required. For via equivalent length see the section on Via compensation.

6.3.7 ALERT_n Wiring

See Figure 7. Wiring for the ALERT_n signal shall be from the first DRAM that the clock connects with where a pullup resistor will also be located, to the last DRAM the clock connects with. ALERT_n wiring will continue from this last DRAM to the edge connector. Any controller termination on the main board is not shown.

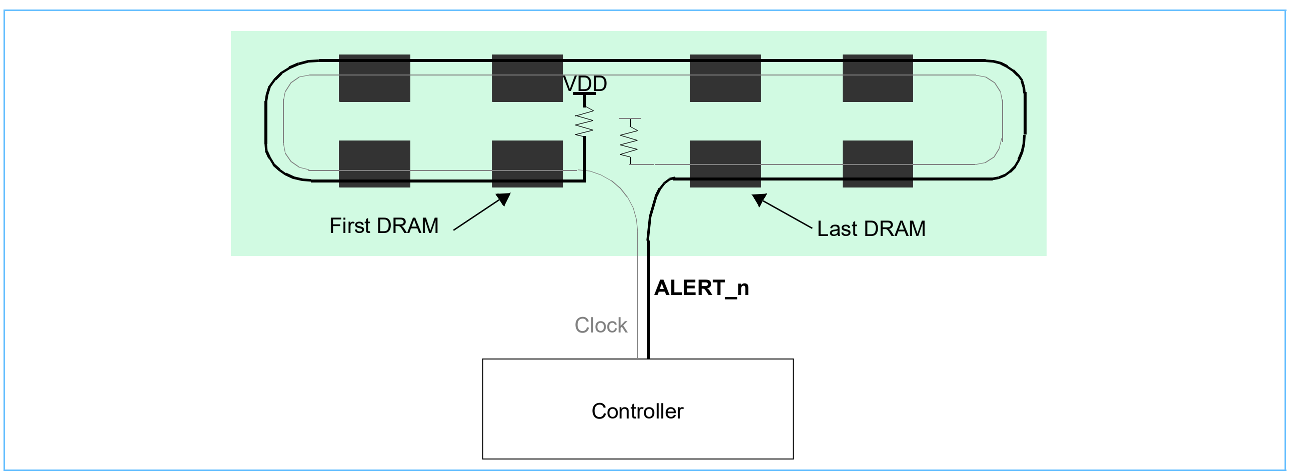


Figure 7 — ALERT_n Wiring Illustration

6.3.8 Via Compensation

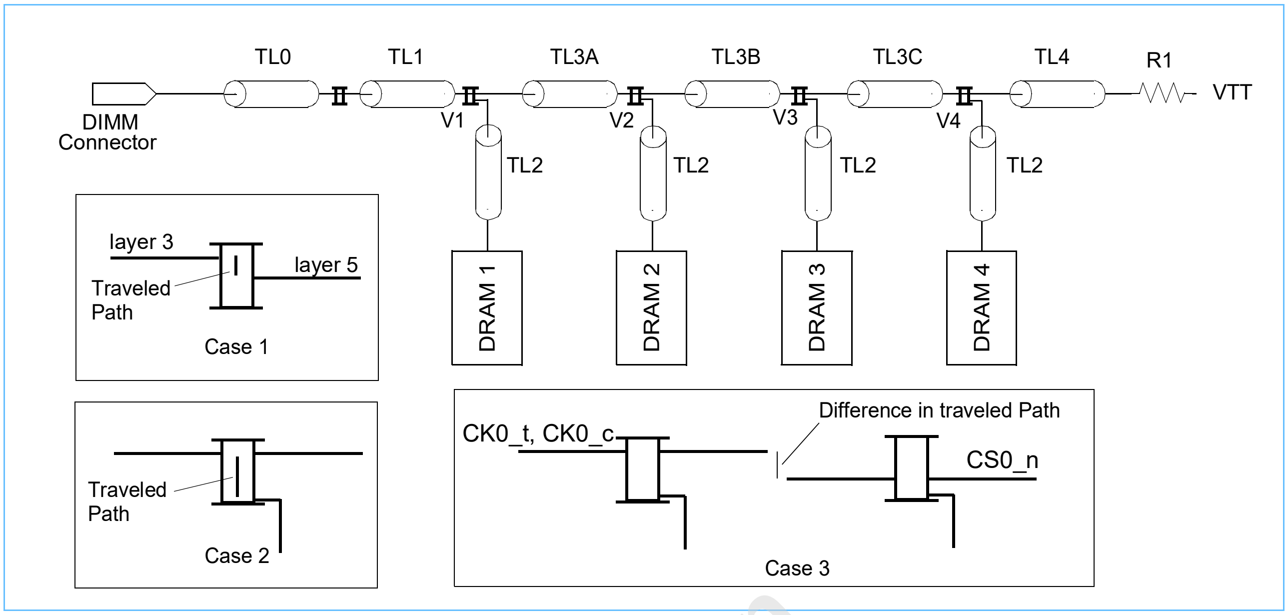


Figure 8 — Via Compensation Diagram

Refer to Figure 8. Via compensation on the CK, CTRL, and ADD/CMD signal groups is recommended but not required. There are several cases to consider:

1. If any of the segments TL0, TL1, TL3A, TL3B, and TL3C are on different layers, the via transitions should be included for any calculations for DRAMs farther down the daisy chain.
2. For the calculation to a specific DRAM, the via at the SDRAM location being calculated should also be included in the calculation (layer to surface). This can be thought of as additional TL2 length.
3. Where Control and CK nets for a single rank are routed on different layers, DRAM to DRAM via compensation should be applied to account for the difference in the layer to surface. The TL3 length traces may be increased for the traces routed closer to the DRAM surface as 1.4 x difference in the via traveled length. For single rank designs, this compensation may also be applied to the Address nets. This may be documented by adding additional rows in the length table to record the lengths per layer. The compensated values for the first and last DRAM would only include the nets routed on the layer that is farthest from the surface with the DRAM. This compensation is optional for the Raw Card Sponsor. The compensation may be applied by individual manufacturers whether employed by the sponsor or not. If Via compensation is applied by the manufacturer and not by the sponsor, a tolerance of ± 2.0 mm may be added to the values in the length tables of the Annex. In this case, the values for the compensated length to the first and last DRAMs do not need to be met and do not have a tolerance.

Via compensation is required on the DQ/DQS byte lanes, where the via count varies within a byte lane.

Consider the additional length as compensated length.

Only the difference in vias needs to be considered. If all signals in a group make exactly the same transition then the vias are not adding additional skew and can be ignored. There are several methods that may be used for via compensation.

6.3.8 Via Compensation (Cont'd)

Method 1:

Z axis. This method just adds the vertical length that the signal travels along the via barrel. This is the simplest approach and is available as a feature in the Cadence layout tool.

Method 2:

Z axis scaling. This method uses the travel distance in the via barrel with a multiplier of 2. This is based on the experience of a 2.5 mm via compensation value for board thickness of 1.27 mm from DDR3. For DDR4, a value of 2.2 mm may be used for signals transition between outer layers. PCB thickness is 1.20 mm. Outer layer copper is 0.045 mm. Remove both outer layers from the overall thickness, 1.110 mm. Multiply by 2, 2.220 mm. Round the result to 2.2 mm. Another example: if a signal transitions from an outer layer to the closest internal layer and the dielectric thickness is 0.100 mm then the value for the via compensation is 0.2 mm.

Method 3:

Fixed constant. This simplifies as 2 choices for vias. 2.2 mm for those that travel all the way through the board and 1.1 mm for any vias where the signal does not travel the full length of the via barrel.

Any method may be used for defining the reference designs. The method used must be identified in the respective annex. If more than one method is used, each case must be identified in the respective annex.

6.3.9 Plane Referencing

Table 12 — Plane Referencing

Signals	Reference	Notes
DQ, DQS	Ground	
Address, Command, Control and VREFCA	VDD	
Clock	VDD	

6.4 Rules for Higher Speed (2666 Mb/s or higher)

With higher speeds DIMM designs are more sensitive to component variations. To allow manufactured designs to remain compliant to a JEDEC reference design Annex but still operate at the intended speed some additional variation in the rules is allowed. The following list summarizes the rules.

Rules for Higher Speeds:

1. Placement configuration must match the reference design (Vertical and Horizontal DRAM orientation).
2. Physical placement may be changed. There is no specific limit.
3. All routing topologies must be maintained. The lengths may be adjusted as defined below.
4. Clock routing lengths may be adjusted as needed to maintain timing to the address.
5. Control routing lengths may be adjusted as needed to maintain timing to the clock.
6. The address routing lengths between the DRAMs may be adjusted by ± 5 mm relative to the reference design. The segment between the via and the DRAM ball may also be changed as needed.
7. The address routing lengths between the first and the second DRAMs may be adjusted by ± 10 mm.
8. The address routing lengths between the byte 3 and byte 4 for non-ECC DIMMs and the ECC byte and byte 4 for ECC DIMMs may be adjusted by ± 20 mm.
9. DQ routing lengths may bae adjusted by ± 0.80 mm.
10. Termination (Rtt) values may be changed if supported by testing or simulation.

6.5 Address Mirroring

DDR4 two-rank SO-DIMMs will use address mirroring. DRAMs for even ranks will be placed on the front side of the module. DRAMs for odd ranks will be placed on the back side of the module. Wiring of the address bus will be as defined in Table 13.

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a “load mode” operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR4 SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the odd ranks.

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Table 13 — DIMM Wiring Definition for Address Mirroring

Signal Name	DRAM Ball Label		Comment
Connector	Even Rank	Odd Rank	
A0	A0	A0	
A1	A1	A1	
A2	A2	A2	
A3	A3	**A4**	
A4	A4	**A3**	
A5	A5	**A6**	
A6	A6	**A5**	
A7	A7	**A8**	
A8	A8	**A7**	
A9	A9	A9	
A10/AP	A10/AP	A10/AP	
A11	A11	**A13**	
A12/BC_n	A12/BC_n	A12/BC_n	
A13	A13	**A11**	
A14/WE_n	A14/WE_n	A14/WE_n	
A15/CAS_n	A15/CAS_n	A15/CAS_n	
A16/RAS_n	A16/RAS_n	A16/RAS_n	
A17	A17	A17	A17 is only valid for x4 based DIMM with SDRAM components greater than 8 Gb.
BA0	BA0	**BA1**	
BA1	BA1	**BA0**	
BG0	BG0	**BG1**	BG1 is not valid for x16 DRAM components. For x16 DRAM components signal BG0 will be wired to DRAM ball BG0 for both ranks.
BG1	BG1	**BG0**	BG1 is not valid for x16 DRAM components. For x16 DRAM components signal BG0 will be wired to DRAM ball BG0 for both ranks.

6.6 DIMM Routing Space Constraints

These are the physical rules for traces and space including keepout requirements.

Preferred rules are to be used whenever possible. Exceptional rules are only to be used when necessary. Exceptional rules, when applied, are to only be used in the area of the board where they are required and preferred rules used in all other areas. Where preferred rules cannot be used it is encouraged that the most conservative rules be used up to the exceptional rules. Rules falling between preferred and exceptional are considered exceptional.

When exceptional rules are used it must be noted in the annex for each specific raw card. It is preferred that additional details be included to identify the areas of the card that use exceptional rules.

These rules are for design of the reference card only. It is not required that these rules be met by individual manufacturers building from the reference designs.

Table 14 — Routing Space Constraints

Feature	Preferred (mm)	Exceptional (mm)	Comment
Via Size Large - Drill	0.250	0.250	To be used where possible
Via Size Large - Pad	0.450	0.450	
Via Size Large - Anti-pad	0.700	0.700	
Via Size Large - Solder mask	Designer preference	Designer preference	Solder mask openings are easy to change.
Via Size Small - Drill	0.200	0.200	To be used if larger via cannot be used.
Via Size Small - Pad	0.400	0.400	
Via Size Small - Anti-pad	0.600	0.600	
Via Size Small - Solder mask	Designer preference	Designer preference	Solder mask openings are easy to change.
Solder mask opening (for pad)	Designer preference	Designer preference	Solder mask openings are easy to change.
Solder mask opening (cover adjacent trace)	Designer preference	Designer preference	Solder mask openings are easy to change.
Pad to pad spacing for pads of different components that are soldered down	0.250	0.200	Concern is solder bridging
Line to pad spacing	0.125	0.100	
Line to line spacing (single ended)	0.100	0.100	
Line to line spacing (differential)	0.100	0.090	
Line to shape spacing	0.200	0.125	
Shape to shape spacing	0.200	0.100	
Via to BGA pad	0.175	0.150	Copper to copper
Via to non-BGA pad	0.150	0.125	Copper to copper
Via to Via	0.200	0.150	Copper to copper
Drill wall to drill wall (nominal)	0.400		
Drill wall (nominal) to board edge (nominal)	0.500		

Table 14 — Routing Space Constraints (Cont'd)

Feature	Preferred (mm)	Exceptional (mm)	Comment
DRAM (nominal) to DRAM (nominal)	0.350	0.300	
DRAM (nominal) to board edge (nominal)	0.400	0.300	
Copper to board edge (nominal)	0.300	0.250	
Component pad to board edge (nominal)	0.400	0.400	
Lower board edge to passive pad or component of less than 0.80 mm height	4.150	4.000	
Lower board edge to component body (nominal) of greater than 0.80 mm height	4.200	4.000	For SO-DIMMs this is not likely required.
Minimum trace width on outer layers	0.090	0.075	Related to cross section shape
Minimum trace width on inner layers	0.075	0.075	Related to cross section shape

6.7 DIMM Physical Requirements

Any exceptions to the following requirements will be noted in the specific annex associated with the specific design.

6.7.1 Via Size

Use larger via (0.250 drill) where possible. Smaller via (0.200 mm drill) allowed if needed. There is a preference not to mix via sizes on a design.

6.7.2 Component Pad Sizes and Geometry

Where 0201 size passive components are used, the pad will be 0.4 mm square with a 0.2 mm space between the pads for each component.

Pads for all other components are left to the reference card designer to define.

Manufacturers of these SO-DIMM reference designs may adjust pad sizes and geometry.

6.7.3 DRAM Package Size

Maximum DRAM package size affects the DQ trace length and placement of decoupling capacitors.

For DDR4 SO-DIMMs using x8 based components, the reference designs will use a maximum package size of 11.0 mm nominal width and 13.0 mm nominal height.

For SO-DIMMs using x16 based components, a 11.0 mm nominal width and 14.0 mm nominal height will be used.

Some designs may only support a smaller SDRAM package size.

6.7.4 Clock Termination

Termination for differential clocks will use two resistors, one connected to each side, the true signal (_t) and the complementary signal (_c), of the differential pair. The other side of each resistor will be connected together and to a capacitor. The other side of the capacitor will be connected to the reference plane for the differential pair. This will be VDD. The capacitor value will be 0.01 µF.

6.7.5 ZQ Calibration Wiring

The DDR4 SDRAMs have a ZQ pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All SO-DIMMs must connect a 240 Ω ± 1% resistor from this pin of the SDRAM to ground (VSS). Every SDRAM package must have its own ZQ resistor. Sharing is not allowed.

6.7.6 DQ Stub Resistor

DQ stub resistor will be 15 Ω for all SO-DIMMs. See Figure 5.

6.7.7 TEN Wiring

TEN is a Test Enable pin. It is not intended to be used on SO-DIMM modules and must be tied low.

6.8 Reference Stackups

The section defines the preferred stackup for 6, 8 and 10 layer SO-DIMMs. Stackup for specific cards may be different from the preferred stackup in the tables below.

Table 15 — Preferred 10 Layer Stackup for SO-DIMMs

Layers				
	Solder Mask	15 µm		
1	Cu	45 µm	Signal	3/8 oz + Plating
	Prepreg	70 µm		
2	Cu	15 µm	VDD/VSS	1/2 oz
	Core	100 µm		
3	Cu	15 µm	Signal	1/2 oz
	Prepreg	150 µm		
4	Cu	15 µm	VDD/VSS	1/2 oz
	Core	80 µm		
5	Cu	15 µm	Signal	1/2 oz
	Prepreg	180 µm		
6	Cu	15 µm	Signal	1/2 oz
	Core	80 µm		
7	Cu	15 µm	VDD/VSS	1/2 oz
	Prepreg	150 µm		
8	Cu	15 µm	Signal	1/2 oz
	Core	100 µm		
9	Cu	15 µm	VDD/VSS	1/2 oz
	Prepreg	70 µm		
10	Cu	45 µm	Signal	3/8 oz + Plating
	Solder Mask	15 µm		

Total thickness 1200 ± 100 µm as measured across connector contact fingers (without solder mask)

6.8 Reference Stackups (Cont'd)

Table 16 — Preferred 8 Layer Stackup for SO-DIMMs

Layers				
	Solder Mask	15 µm		
1	Cu	45 µm	Signal	3/8 oz + Plating
	Prepreg	70 µm		
2	Cu	15 µm	VDD/VSS	1/2 oz
	Core	80 µm		
3	Cu	15 µm	Signal	1/2 oz
	Prepreg	320 µm		
4	Cu	15 µm	VDD/VSS	1/2 oz
	Core	80 µm		
5	Cu	15 µm	Signal	1/2 oz
	Prepreg	320 µm		
6	Cu	15 µm	Signal	1/2 oz
	Core	80 µm		
7	Cu	15 µm	VDD/VSS	1/2 oz
	Prepreg	70 µm		
8	Cu	45 µm	Signal	3/8 oz + Plating
	Solder Mask	15 µm		

Total thickness 1200 ± 100 µm as measured across connector contact fingers (without solder mask)

Table 17 — Preferred 6 Layer Stackup for SO-DIMMs

Layers				
	Solder Mask	15 µm		
1	Cu	45 µm	Signal	3/8 oz + Plating
	Prepreg	70 µm		
2	Cu	30 µm	VDD/VSS	1 oz
	Core	80 µm		
3	Cu	30 µm	Signal	1 oz
	Prepreg	700 µm		
4	Cu	30 µm	Signal	1 oz
	Core	80 µm		
5	Cu	30 µm	VDD/VSS	1 oz
	Prepreg	70 µm		
6	Cu	45 µm	Signal	3/8 oz + Plating
	Solder Mask	15 µm		

Total thickness 1200 ± 100 um as measured across connector contact fingers (without solder mask)

6.9 Impedance Targets

Three impedances are defined for DDR4 SO-DIMMs.

1. 55 Ω ± 10% (typically achieved with 0.075 mm trace widths)
2. 50 Ω ± 10% (typically achieved with 0.10 mm trace widths)
3. 40 Ω ± 10% (typically achieved with 0.15 mm trace widths)

These trace widths are valid for internal and external layers for the stackups given in section 6.8. Some variation in trace width may be required to reach the impedance targets if the stackup is modified from those in section 6.8.

One variation that may be considered is using 0.09 mm trace widths on the outer layers. It is suggested this be restricted to short traces only and the dielectric thickness not be modified but accept 52 Ω as the target impedance.

Three differential impedances are defined for DDR4 SO-DIMMs.

1. 93 Ω ± 15% (typically achieved with 0.075 mm trace widths with a 0.10 mm space)
2. 83 Ω ± 15% (typically achieved with 0.10 mm trace widths with a 0.10 mm space)
3. 70 Ω ± 15% (typically achieved with 0.15 mm trace widths with a 0.10 mm space)

These trace widths are valid for internal and external traces for the stackups given in section 6.8. Some variation in trace width may be required to reach the impedance targets if the stackup is modified from those in section 6.8.

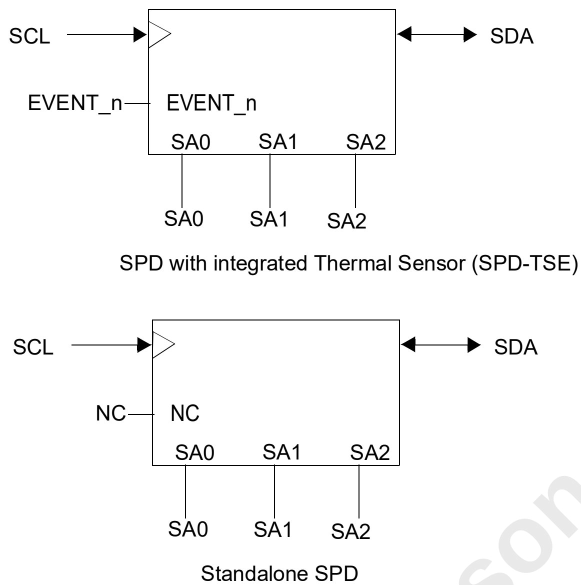
Table 18 — Impedance Assignments by Signal Type

Signal Type	Lead-in Section[1]	Loaded Section
CLOCK	70 Ω differential	93 Ω differential
ADD/CMD	40 Ω	55 Ω
CTRL	40 Ω	55 Ω
DQ	50 Ω	
DQS	83 Ω differential	

Note 1 SO-DIMMs with SDRAM components in two rows will use impedances defined for the loaded section throughout the design.

6.10 SPD Wiring and Placement

An optional on-DIMM thermal sensor may provide DIMM temperature readout through an integrated thermal sensor. See Figure 9.



Notes:
1. One footprint exists for an SPD/thermal sensor placement. It can be a SPD-only device or it can be a combination device containing both an SPD and a thermal sensor. For designs only allowing for the SPD only component, EVENT_n is not wired.

Figure 9 — Block Diagram: SPD-TSE/ SPD

TDFN packages are used for the thermal sensor and the serial presence-detect. MO-229C, variations W2030D-3, V2030D-3, and U2030D will be referenced for the thermal sensor and serial presence-detect part.

SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT_n not wired.

SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT_n wired.

6.11 DQ Mapping to Support CRC

For DDR4, a CRC feature has been added to support higher speeds. Generally, when using CRC, the bit order is 1:1 between the source and the destination. This is not true for DIMMs where the bit order is somewhat random based on minimizing routing to maximize signal integrity. The CRC computation is based on a byte. For x4 based SDRAMs the computation is truncated to 4 bits, a nibble. See the DDR4 SDRAM specification JESD79-4 for a more complete explanation of how CRC is implemented. To fix the mapping issue, the host must understand the bit order at the SDRAM to map the DQ bits into the CRC generator for WRITE commands so that the SDRAM will decode the CRC correctly. The same is true for READs.

When there is more than one rank on a DIMM, the even ranks are on the front and the odd ranks are on the back. When DRAMs are placed back to back and are of a different package rank, the DQ relationship between the even ranks and the odd ranks are fixed. To reduce the number of variations in the DQ mapping, the following rules are defined.

Rule 1: Bits within a nibble must stay together.

Rule 2: Nibbles may be swapped within a byte.

Rule 3: Definition of mapping is for rank 0 only. All even ranks have the same DQ mapping. Even rank to odd rank mapping is to swap bit 0 with 1, swap bit 2 with 3, swap bit 4 with 5 and swap bit 6 with 7.

For DIMMs that use 3DS components, the rank definition applies to package ranks. The additional die within a 3DS component are logical ranks and are part of one package rank. Another way of looking at this is that each chip select (CSx_n) used is one package rank. Where there is only one package rank, that rank may be placed on the front or the back or split between the front or back. Table 19 defines rank 0 mapping and therefore fully defines all DIMMs with one package rank.

18 bytes of the SPD are allocated for holding the DQ mapping information, one byte for each nibble of the DIMM connector. See Table 19. The table exactly specifies which DQ bits are in each nibble. The DQ Map Index refers to the specific map that is defined in Table 20.

Use of CRC is an optional feature. If a DIMM does not support CRC, values of 0x00 must fill the table.

It is required that all reference designs support CRC.

Table 19 — SPD DQ Nibble Map for CRC

SPD Content - 18 bytes allocated (Example values)										
SPD Address	DQ Bits	DQ Map Index (Hex)[1]		SPD Address	DQ Bits	DQ Map Index (Hex)		SPD Address	DQ Bits	DQ Map Index (Hex)
60	DQ[0-3]	0x2B		66	DQ[24-27]	TBD		72	DQ[40-43]	TBD
61	DQ[4-7]	0x15		67	DQ[28-31]	TBD		73	DQ[44-47]	TBD
62	DQ[8-11]	0x0C		68	CB[0-3]	TBD		74	DQ[48-51]	TBD
63	DQ[12-15]	0x35		69	CB[4-7]	TBD		75	DQ[52-55]	TBD
64	DQ[16-19]	TBD		70	DQ[32-35]	TBD		76	DQ[56-59]	TBD
65	DQ[20-23]	TBD		71	DQ[36-39]	TBD		77	DQ[60-63]	TBD

Note 1 This column illustrates the values that the SPD might hold. These values are an example but do correlate with the values in the additional tables and figures.

6.11 DQ Mapping to Support CRC (Cont'd)

The DQ Map table defines all possible mappings following Rule 1 and Rule 2. For x4 based DIMMs there are 24 mappings. These are represented by DQ Map Index values 0x01 through 0x18. Offsetting by 1 allows 0x00 to be used to indicate that mapping using the table is not supported. For x8 based DIMMs, there are 48 mappings and the entire table is used. Note that the there is a gap between the left side of the table and the right side (0x19 to 0x20). These DQ Map Index values are invalid. All the values above 0x38 are invalid.

CRC is defined for x8 based components and x4 based components. For the purpose of CRC, x16 components are treated as 2 separate x8 components. Similarly a x32 component would be treated as 4 separate x8 based components. The definition for CRC can be found in the JESD79-4 specification for DDR4 SDRAMs.

Table 20 — Nibble/Byte DQ Map Patterns for CRC

DQ Map Index (Hex)	Connector - bit within nibble				DQ Map Index (Hex)	Connector - bit within nibble			
	0	1	2	3		0	1	2	3
	SDRAM bit					SDRAM bit			
0x01	0	1	2	3	0x21	4	5	6	7
0x02	0	1	3	2	0x22	4	5	7	6
0x03	0	2	1	3	0x23	4	6	5	7
0x04	0	2	3	1	0x24	4	6	7	5
0x05	0	3	1	2	0x25	4	7	5	6
0x06	0	3	2	1	0x26	4	7	6	5
0x07	1	0	2	3	0x27	5	4	6	7
0x08	1	0	3	2	0x28	5	4	7	6
0x09	1	2	0	3	0x29	5	6	4	7
0x0A	1	2	3	0	0x2A	5	6	7	4
0x0B	1	3	0	2	0x2B	5	7	4	6
0x0C	1	3	2	0	0x2C	5	7	6	4
0x0D	2	0	1	3	0x2D	6	4	5	7
0x0E	2	0	3	1	0x2E	6	4	7	5
0x0F	2	1	0	3	0x2F	6	5	4	7
0x10	2	1	3	0	0x30	6	5	7	4
0x11	2	3	0	1	0x31	6	7	4	5
0x12	2	3	1	0	0x32	6	7	5	4
0x13	3	0	1	2	0x33	7	4	5	6
0x14	3	0	2	1	0x34	7	4	6	5
0x15	3	1	0	2	0x35	7	5	4	6
0x16	3	1	2	0	0x36	7	5	6	4
0x17	3	2	0	1	0x37	7	6	4	5
0x18	3	2	1	0	0x38	7	6	5	4

6.11 DQ Mapping to Support CRC (Cont'd)

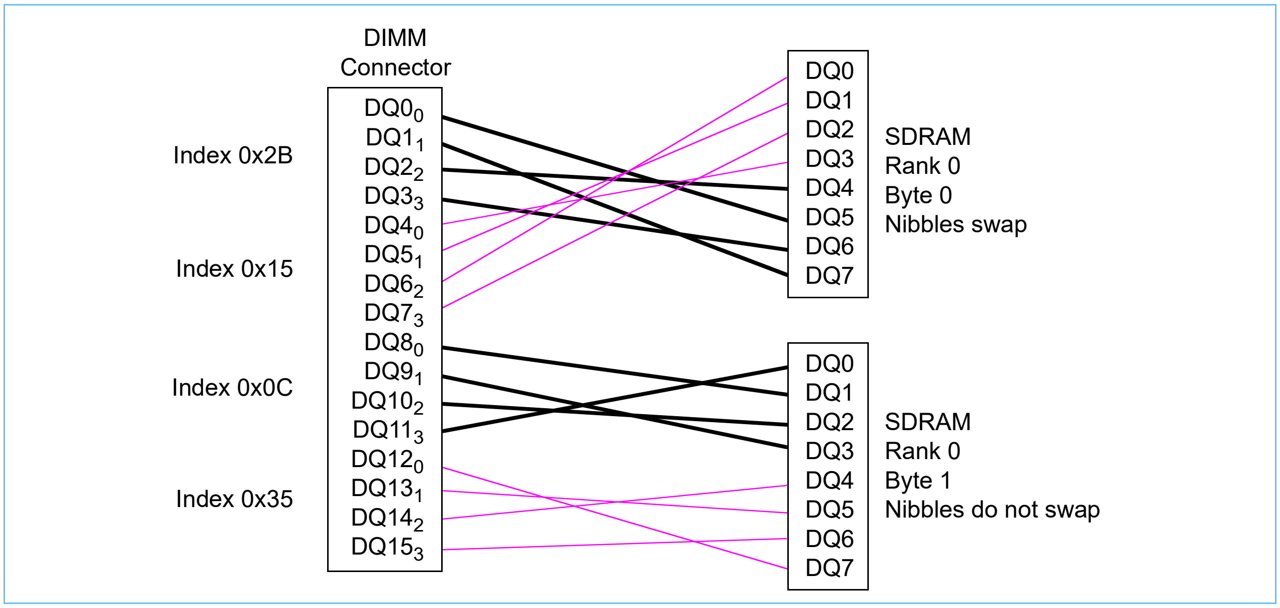


Figure 10 — Example of DQ Wiring with Mapping for CRC

Table 21 — Example of DQ Mapping for CRC

DQ bit of DIMM Connector

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
First x8 SDRAM								Second x8 SDRAM											
5	7	4	6																
				3	1	0	2												
								1	3	2	0								
												7	5	4	6				

DQ mapping for first nibble matches index 0x2B.
0x2B would be stored in the SPD table for the first nibble.

DQ mapping of second nibble matches index 0x15.
0x15 would be stored in the SPD table for the second nibble.

0x0C for the 3rd nibble.

0x35 for the fourth nibble.

7 Serial Presence Detect Component Specification

This section is included for convenience. Please refer to the DDR4 SPD Contents Master Specification for the most up to date specification.

7.1 Serial Presence Detect Definition

The Serial Presence Detect function must be implemented on the DDR4 SDRAM SO-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR4 Module Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices.

The following is the SPD address map for all DDR4 modules. It describes where the individual lookup table entries will be held in the serial EEPROM. Consistent with the definition of DDR4 generation SPD devices which have four individual write protection blocks of 128 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 22 — SPD Address Map

Block	Range		Description
0	0-127	0x000-0x07F	Base Configuration and DRAM Parameters
1	128-255	0x080-0x0FF	Module Specific Parameters -- See annexes for details
2	256-319	0x100-0x13F	Reserved -- must be coded as 0x00
	320-383	0x140-0x17F	Manufacturing Information
3	384-511	0x180-0x1FF	End User Programmable

Table 23 — Block 0: Base Configuration and DRAM Parameters

Byte Number		Function Described
0	0x000	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage
1	0x001	SPD Revision
2	0x002	Key Byte / DRAM Device Type
3	0x003	Key Byte / Module Type
4	0x004	SDRAM Density and Banks
5	0x005	SDRAM Addressing
6	0x006	SDRAM Package Type
7	0x007	SDRAM Optional Features
8	0x008	SDRAM Thermal and Refresh Options
9	0x009	Other DRAM optional features
10	0x00A	Reserved -- must be coded as 0x00
11	0x00B	Module Nominal Voltage, VDD
12	0x00C	Module Organization
13	0x00D	Module Memory Bus Width
14	0x00E	Module Thermal Sensor
15-16	0x00F-0x010	Reserved -- must be coded as 0x00
17	0x011	Timebase
18	0x012	SDRAM Minimum Cycle Time (tCKAVGmin)

Table 23 — Block 0: Base Configuration and DRAM Parameters (Cont'd)

Byte Number		Function Described
19	0x013	SDRAM Maximum Cycle Time (tCKAVGmax)
20	0x014	CAS Latencies Supported, First Byte
21	0x015	CAS Latencies Supported, Second Byte
22	0x016	CAS Latencies Supported, Third Byte
23	0x017	CAS Latencies Supported, Fourth Byte
24	0x018	Minimum CAS Latency Time (tAAmin)
25	0x019	Minimum RAS to CAS Delay Time (tRCDmin)
26	0x01A	Minimum Row Precharge Delay Time (tRPmin)
27	0x01B	Upper Nibbles for tRASmin and tRCmin
28	0x01C	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte
29	0x01D	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte
30	0x01E	Minimum Refresh Recovery Delay Time (tRFC1min), LSB
31	0x01F	Minimum Refresh Recovery Delay Time (tRFC1min), MSB
32	0x020	Minimum Refresh Recovery Delay Time (tRFC2min), LSB
33	0x021	Minimum Refresh Recovery Delay Time (tRFC2min), MSB
34	0x022	Minimum Refresh Recovery Delay Time (tRFC4min), LSB
35	0x023	Minimum Refresh Recovery Delay Time (tRFC4min), MSB
36	0x024	Minimum Four Activate Window Time (tFAWmin), Most Significant Nibble
37	0x025	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte
38	0x026	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group
39	0x027	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group
40	0x028	Minimum CAS to CAS Delay Time (t_{CCD_L}min), same as bank group
41-59	0x028-0x03B	Reserved -- must be coded as 0x00
60-77	0x03C-0x04D	Connector to SDRAM Bit Mapping
78-116	0x04E-0x075	Reserved -- must be coded as 0x00
117	0x075	Fine Offset for Minimum CAS to CAS Delay Time (t_{CCD_L}min), same bank group
118	0x76	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group
119	0x77	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group
120	0x078	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (tRCmin)
121	0x079	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)
122	0x07A	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)
123	0x07B	Fine Offset for Minimum CAS Latency Time (tAAmin)
124	0x07C	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)
125	0x07D	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)
126	0x07E	CRC for Base Configuration Section, Least Significant Byte
127	0x07F	CRC for Base Configuration Section, Most Significant Byte

8 Product Label

This section is included for convenience. Please refer to Section 4.19.4 for the most up-to-date specification.

The following labels shall be applied to all DDR4 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggg, are to be omitted when not needed.

8.1 DDR4 DIMM Label Format for DRAM-only module types

ggg**GB** phe**Rx**ff **PC4**s**-**wwwwaa**-**mccd**-**bb

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted)
1GB, 2GB, 4GB, etc. (no space between digits and units)

phe**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.
p =
1 = 1 package rank of SDRAMs per DIMM
2 = 2 package ranks of SDRAMs per DIMM
3 = 3 package ranks of SDRAMs per DIMM
4 = 4 package ranks of SDRAMs per DIMM

h = blank for monolithic DRAMs (SDP), else for modules using stacked DRAM:
h = DRAM package type
D = Dual die multi-load DRAM stack (DDP)
Q = Quad die multi-load DRAM stack (QDP)
S = Single load DRAM stacking (3DS)

e = blank for SDP, DDP, or QDP, else for modules using 3DS stacks, logical ranks per package rank
2 = 2 logical ranks in each package rank
4 = 4 logical ranks in each package rank
8 = 8 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

s = SDRAM operational scaling
blank = DDR4
E = DDR4E with operational scaling

wwww = Module speed in Mb/s/data pin
1600
1866
2133
2400
2666
2933
3200

aa = SDRAM speed grade
aa = Speed grade, i.e., J, K, L, etc. (See JESD79-4 and 3DS Addendum specifications for details)

8.1 DDR4 DIMM Label Format for DRAM-only module types (Cont'd)

Examples:

DDR4 Monolithic Components				
Letter	Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
J	All	10	10	10
K	All	11	11	11
L	All	12	12	12
M	All	13	13	13
N	All	14	14	14
P	All	15	15	15
R	All	16	16	16
T	All	17	17	17
U	All	18	18	18
V	All	19	19	19
W	All	20	20	20
Y	All	21	21	21
AA	All	22	22	22
AC	All	24	24	24

DDR4 3DS Stacked Single-Load Components				
Letter	Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
J	All	12	11	10
K	All	13	12	11
L	All	14	13	12
M	All	15	14	13
N	All	16	15	14
P	2133P-3DS2A	17	15	15
P	2133P-D 3DS2A	17	15	15
P	2133P-3DS3A	18	15	15
P	2400P-3DS3B	18	16	15
R	All	20	16	16
T	2400T-3DS2A	19	17	17
T	2666T-3DS3A	20	17	17
U	2400U-3DS2A	20	18	18
U	2400U-3DS4A	22	18	18

DDR4 3DS Stacked Single-Load Components (Cont'd)				
Letter	Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
U	2400U-D 3DS4A	22	18	18
V	All	22	19	19
W	All	24	20	20
AA	All	26	22	22
AC	All	28	24	24

m = Module Type
- A = Unbuffered 16-bit Small Outline DIMM ("16b-SO-DIMM"), x16 data bus (*placeholder*)
- B = Unbuffered 32-bit Small Outline DIMM ("32b-SO-DIMM"), x32 data bus (*placeholder*)
- C = Registered 72-bit Small Outline DIMM ("72b-SO-RDIMM"), x64 primary + 8 bit ECC module data bus (*placeholder*)
- E = Unbuffered DIMM ("UDIMM"), x64 primary + 8 bit ECC module data bus
- L = Load Reduced DIMM ("LRDIMM"), x64 primary + 8 bit ECC module data bus
- N = Mini registered DIMM ("Mini-RDIMM"), x64 primary + 8 bit ECC module data bus
- R = Registered DIMM ("RDIMM"), x64 primary + 8 bit ECC module data bus
- S = Small Outline DIMM ("SO-DIMM"), no ECC (x64 bit module data bus)
- T = Unbuffered 72-bit Small Outline DIMM ("72b-SO-DIMM"), x64 primary + 8 bit ECC module data bus
- U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- W = Mini unbuffered DIMM ("Mini-UDIMM"), x64 primary + 8 bit ECC module data bus

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases (new method -- preferred)
- P = Pre-release or Engineering sample (for legacy modules; new modules should use A~K)
- Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. Legacy DIMM labels allowed for a single pre-production indicator 'P' in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first letter in the cc field to indicate which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level:

Production Levels		
DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1

Production Levels (Cont'd)		
DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
P	-	Legacy pre-production indicator; production revision documented in module SPD
Z	Z	Non-standard design

Legacy DIMM labels allowed for a single pre-production indicator in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first character in the cc field to indicate which raw card revision the pre-production module represents.

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0

ccd = F0 Production F0 module

ccd = FB Pre-production sample of raw card F1

ccd = F1 Production F1 module

Examples:

16GB 2Rx4 PC4-2133N-RA2-11
16 GB DDR4 RDIMM (72 bit data bus)
2 package ranks per DIMM
using SDP DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file A revision 2 used for the assembly
DDR4 SPD revision 1.1

16GB 2DRx4 PC4-2133N-RJ0-10
16 GB DDR4 RDIMM (72 bit data bus)
2 package ranks per DIMM
using DDP multi-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file J revision 0 used for the assembly
DDR4 SPD revision 1.0

8.1 DDR4 DIMM Label Format for DRAM-only module types (Cont'd)

16GB 1S2Rx4 PC4-2133N-RF1-10

16 GB DDR4 VLP RDIMM (72 bit data bus)
1 package rank per DIMM
with 2 logical ranks per package rank
using 2H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file F revision 1 used for the assembly
DDR4 SPD revision 1.0

32GB 2DRx8 PC4-2400U-UZZZ-11

32 GB DDR4 UDIMM (64 bit data bus)
2 package ranks per DIMM
using DDP multi-load stacked DDR4 SDRAMs
x8 data organization per SDRAM
DDR4-2400 performance
Speed grade U: CAS Latency = 18
Non-JEDEC standard design used for the assembly
DDR4 SPD revision 1.1

16GB 1S4Rx4 PC4-2133R-LZZZ-10

16 GB DDR4 LRDIMM
1 package rank per DIMM
with 4 logical ranks per package rank
using 4H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade R: CAS Latency = 16
Non-JEDEC design used for the assembly
DDR4 SPD revision 1.0

16GB 1S2Rx4 PC4-2133N-RFC-10

16 GB DDR4 VLP RDIMM (72 bit data bus)
1 package rank per DIMM
with 2 logical ranks per package rank
using 2H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Pre-production engineering sample of raw card reference design file F revision 2 used for the assembly
DDR4 SPD revision 1.0

32GB 2DRx8 PC4E-2400U-UZZZ-11

32 GB DDR4E UDIMM (64 bit data bus)
2 package ranks per DIMM
using DDP multi-load stacked DDR4 SDRAMs
x8 data organization per SDRAM
DDR4E-2400 performance with operational scaling
Speed grade U: CAS Latency = 18
Non-JEDEC standard design used for the assembly
DDR4 SPD revision 1.1

8.1 DDR4 DIMM Label Format for DRAM-only module types (Cont'd)

16GB 1S4Rx4 PC4E-2133R-LZZZ-10
16 GB DDR4E LRDIMM
1 package rank per DIMM
with 4 logical ranks per package rank
using 4H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4E-2133 performance with operational scaling
Speed grade R: CAS Latency = 16
Non-JEDEC design used for the assembly
DDR4 SPD revision 1.0

8.2 DDR4 DIMM Label Format for Hybrid memory module types

"System accessible memory" refers to media that is available for use by the system. For NVDIMM-N this refers to the DRAM capacity. For NVDIMM-H, this refers to the usable Flash capacity. For NVDIMM-P, this refers to the guaranteed Host accessible volatile or non-volatile capacity.

Hybrid modules appear to the system with a "base module type" compatible interface. For example, an NVDIMM-N may be constructed with an RDIMM-style interface or an LRDIMM-style interface. What specific functions the module provides are described in an "Hybrid Media Type" field ('n'), essentially a functional overlay on the base module type.

DDR4 DIMM labels for Hybrid memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

Legacy hybrid memory module labels required the technical detail section only.

8.2.1 Module Type Section

DDR4 dimm_type

Where:

dimm_type = one of:

NVUDIMM-N			
NVRDIMM-N	NVRDIMM-H	NVRDIMM-P	NVRDIMM-PL
NVLRDIMM-N	NVLRDIMM-H	NVLRDIMM-P	NVLRDIMM-PL

8.2.2 Technical Detail Section

ggg**GB** phe**R**x**ff** **N**nn**4**s**-**wwwwaa**-**mccd**-**bb

Where:

ggg = Module total capacity, in gigabytes, for system accessible DRAM on primary bus (ECC not counted)
ggg: natural numbers

GB = Gigabytes of module capacity; may be **TB** for terabytes

phe**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.
p =
1 = 1 package rank of SDRAMs per DIMM
2 = 2 package ranks of SDRAMs per DIMM
3 = 3 package ranks of SDRAMs per DIMM
4 = 4 package ranks of SDRAMs per DIMM

8.2.2 Technical Detail Section (Cont'd)

h = blank for monolithic DRAMs (SDP), else for modules using stacked DRAM:

h = DRAM package type

D = Dual die multi-load DRAM stack (DDP)

Q = Quad die multi-load DRAM stack (QDP)

S = Single load DRAM stacking (3DS)

e = blank for SDP, DDP, or QDP, else for modules using 3DS stacks, logical ranks per package rank

2 = 2 logical ranks in each package rank

4 = 4 logical ranks in each package rank

8 = 8 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly

x4 = x4 organization (4 DQ lines per SDRAM)

x8 = x8 organization

x16 = x16 organization

N = NVDIMM

nn = NVDIMM type

N = persistent DRAM using NAND flash

H = NAND flash accessed as a block cached, byte addressable device

P = transactional credit based device

PL = transactional credit based device, lightweight protocol

s = SDRAM operational scaling

blank = DDR4

E = DDR4E with operational scaling

wwww = Module speed in Mb/s/data pin

1600

1866

2133

2400

2666

2933

3200

aa = SDRAM speed grade

aa = Speed grade, i.e., J, K, L, etc.

Examples:

DDR4 Monolithic Components				
Letter	Speed Grade	CAS (SEND) Latency	tRCD in nCK	tRP in nCK
J	All	10	10	10
K	All	11	11	11
L	All	12	12	12
M	All	13	13	13
N	All	14	14	14
P	All	15	15	15
R	All	16	16	16
T	All	17	17	17
U	All	18	18	18

DDR4 Monolithic Components (Cont'd)				
Letter	Speed Grade	CAS (SEND) Latency	tRCD in nCK	tRP in nCK
V	All	19	19	19
W	All	20	20	20
Y	All	21	21	21
AA	All	22	22	22
AC	All	24	24	24
Note: For NVDIMM-P and NVDIMM-PL, SEND latency is defined; tRCD and tRP are not				

DDR4 3DS Stacked Single-Load Components				
Letter	Speed Grade	CAS (SEND) Latency	tRCD in nCK	tRP in nCK
J	All	12	11	10
K	All	13	12	11
L	All	14	13	12
M	All	15	14	13
N	All	16	15	14
P	2133P-3DS2A	17	15	15
P	2133P-D 3DS2A	17	15	15
P	2133P-3DS3A	18	15	15
P	2400P-3DS3B	18	16	15
R	All	20	16	16
T	2400T-3DS2A	19	17	17
T	2666T-3DS3A	20	17	17
U	2400U-3DS2A	20	18	18
U	2400U-3DS4A	22	18	18
U	2400U-D 3DS4A	22	18	18
V	All	22	19	19
W	All	24	20	20
AA	All	26	22	22
AC	All	28	24	24
Note: For NVDIMM-P and NVDIMM-PL, SEND latency is defined; tRCD and tRP are not				

8.2.2 Technical Detail Section (Cont'd)

m = Base Module Type
- A = Unbuffered 16-bit Small Outline DIMM ("16b-SO-DIMM"), x16 data bus (*placeholder*)
- B = Unbuffered 32-bit Small Outline DIMM ("32b-SO-DIMM"), x32 data bus (*placeholder*)
- C = Registered 72-bit Small Outline DIMM ("72b-SO-RDIMM"), x64 primary + 8 bit ECC module data bus (*placeholder*)
- E = Unbuffered DIMM ("UDIMM"), x64 primary + 8 bit ECC module data bus
- L = Load Reduced DIMM ("LRDIMM"), x64 primary + 8 bit ECC module data bus
- N = Mini registered DIMM ("Mini-RDIMM"), x64 primary + 8 bit ECC module data bus
- R = Registered DIMM ("RDIMM"), x64 primary + 8 bit ECC module data bus
- S = Small Outline DIMM ("SO-DIMM"), no ECC (x64 bit module data bus)
- T = Unbuffered 72-bit Small Outline DIMM ("72b-SO-DIMM"), x64 primary + 8 bit ECC module data bus
- U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- W = Mini unbuffered DIMM ("Mini-UDIMM"), x64 primary + 8 bit ECC module data bus

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases (new method -- preferred)
- P = Pre-release or Engineering sample (for legacy modules; new modules should use A~K)
- Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. Legacy DIMM labels allowed for a single pre-production indicator 'P' in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first letter in the cc field to indicate which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level
:

Production Levels		
DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9

Production Levels (Cont'd)		
DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
P	-	Legacy pre-production indicator; production revision documented in module SPD
Z	Z	Non-standard design

Legacy DIMM labels allowed for a single pre-production indicator in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first character in the cc field to indicate which raw card revision the pre-production module represents.

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0

ccd = F0 Production F0 module

ccd = FB Pre-production sample of raw card F1

ccd = F1 Production F1 module

8.2.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> (Format %02x%02x%02x%02x%02x%02x%02x%02x%02x)
where

<vid> = DIMM Vendor ID, 4 characters (SPD bytes 320, 321)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 322)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 323),
2 characters for week (SPD byte 324)
<serial> = Unique serial number assigned by manufacturer, 8 characters (SPD bytes 325~328)

8.2.4 Part Number Section

PN:partnumber

Where:

partnumber = module part number (SPD bytes 329~348)

8.2.5 Physical Presence Security Identifier Section

PSID:psid

Where:

psid = Physical Presence Security ID, exactly 32 printable characters
as defined by the Trusted Computing Group Storage Opal SSC Feature Set: PSID specification; see trustedcomputinggroup.org for details

This field is required for hybrid modules that incorporate self-encryption to allow data recovery.

8.2.6 Machine Readable Section

2d_barcode

Where:

2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails(S)serialnumber(P)partnumber or

(L)technicaldetails(S)serialnumber(P)partnumber(K)psid for modules supporting self-encryption

Where:

technicaldetails, serialnumber, partnumber, and psid are as defined in the above specification sections.

The serialnumber field is exactly 18 characters long.

The partnumber field must include all 20 characters from SPD bytes 329~348 including leading or trailing space characters.

The psid field, when included, is exactly 32 characters long.

No whitespace characters (space, newline, etc.) are permitted in the barcode in the required JEDEC fields except as described above for the partnumber field.

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x) where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition, lower case characters (a-z) may be used for supplier specific information.

Delineated sections of the barcode may be in any order.

Examples:

DDR4 NVRDIMM-N
16GB 2Rx4 NN4-2133N-RA2-12
SN:802C26160112345678
PN:MTA12ASF2G72PA-4H4A0

16 GB DDR4 SDRAM with no system accessible Flash
DDR4 RDIMM-compatible interface NVDIMM-N
2 package ranks per DIMM
using SDP DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file A revision 2 used for the assembly
DDR4 SPD revision 1.2
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2016 week 01
Unique product serial number 12345678
Part number MTA12ASF2G72PA-4H4A0
No PSID key
Barcode text
(L)16GB 2Rx4 NN4-2133N-RA2-12(S)802C-1601-26-12345678(P)MTA12ASF2G72PA-4H4A0

8.2.6 Machine Readable Section (Cont'd)

DDR4 NVLRDIMM-H
1TB 1Rx4 NH4-1866M-LB1-12
SN:078501171678123456
PN:DTINF4-1TF18Z2A

1 TB NAND Flash-only, no system accessible DRAM
DDR4 LRDIMM-compatible interface NVDIMM-H
Appears as 1 package rank per DIMM
of SDP DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-1866 performance
Speed grade M: CAS Latency = 12
Raw card reference design file B revision 1 used for the assembly
DDR4 SPD revision 1.2
Manufacturer code 07 85
Manufacturing location 01 (vendor specific)
Manufacturing date 2017 week 16
Unique product serial number 78123456
Part number DTINF4-1TF18Z2A
No PSID key
Barcode text
(L)1TB 1Rx4 NH4-1866M-LB1-12(S)0785-01-1716-78123456(P)DTINF4-1TF18Z2A*(+5 spaces)*

DDR4 NVRDIMM-P
16GB 1Rx4 NP4-2133N-RA2-12
SN:80CE03172256781234
PN:XIT16G32GPR4A1

16 GB mounted as a transactional oriented device
DDR4 RDIMM-compatible interface NVDIMM-P
1 chip select signal used
x4 data organization
DDR4-2133 performance
Speed grade N: SEND Latency = 14
Raw card reference design file A revision 2 used for the assembly
DDR4 SPD revision 1.2
Manufacturer code 80 CE
Manufacturing location 03 (vendor specific)
Manufacturing date 2017 week 22
Unique product serial number 56781234
Part number XIT16G32GPR4A1
No PSID key
Barcode text
(L)16GB 1Rx4 NP4-2133N-RA2-12(S)80CE-03-1722-56781234(P)XIT16G32GPR4A1

9 JEDEC Process

JEDEC provides PCB reference designs for DIMM modules. The designs are divided into families, one of which is Small Outline DIMMs (SO-DIMMs). Letters (A, B, C etc.) are used to define specific configurations (raw cards) of modules such as 2 rank with x8 based SDRAMs. Additional characteristics may further refine cards into specific raw card (R/C) letters. Letter assignments are arbitrary and usually chronological. There is no other association to the letter assignments.

R/Cs are reviewed and balloted by JEDEC members before being placed on the JEDEC website as reference designs. This is called registration. The initial registration is 0. A specific card may be the registration of R/C A0. Subsequent design updates to the reference design go through the same balloting process and increment the registration number from 0 to 1 or the next highest number.