

PXI™-5

PXI Express Hardware Specification

PCI EXPRESS eXtensions for Instrumentation

An Implementation of ***CompactPCI® Express***



Revision 1.0
August 22, 2005





PXI Express 硬件规格

PCI EXPRESS 仪器仪表

实现

紧凑型 PCI Express

PXI Express 硬件规范修订版 1.0 08/22/2005

修订版 1.0
八月 22, 2005



IMPORTANT INFORMATION

Copyright

© Copyright 1997-2005 PXI Systems Alliance. All rights reserved.

This document is copyrighted by the PXI Systems Alliance. Permission is granted to reproduce and distribute this document in its entirety and without modification.

NOTICE

The *PXI Express Hardware Specification* is authored and copyrighted by the PXI Systems Alliance. The intent of the PXI Systems Alliance is for the *PXI Express Hardware Specification* to be an open industry standard supported by a wide variety of vendors and products. Vendors and users who are interested in developing PXI-compatible products or services, as well as parties who are interested in working with the PXI Systems Alliance to further promote PXI as an open industry standard are invited to contact the PXI Systems Alliance for further information.

The PXI Systems Alliance wants to receive your comments on this specification. Visit the PXI Systems Alliance web site at <http://www.pxisa.org/> for contact information and to learn more about the PXI Systems Alliance.

The attention of adopters is directed to the possibility that compliance with or adoption of the PXI Systems Alliance specifications may require use of an invention covered by patent rights. The PXI Systems Alliance shall not be responsible for identifying patents for which a license may be required by any PXI Systems Alliance specification, or for conducting legal inquiries into the legal validity or scope of those patents that are brought to its attention. PXI Systems Alliance specifications are prospective and advisory only. Prospective users are responsible for protecting themselves against liability for infringement of patents.

The information contained in this document is subject to change without notice. The material in this document details a PXI Systems Alliance specification in accordance with the license and notices set forth on this page. This document does not represent a commitment to implement any portion of this specification in any company's products.

The PXI Systems Alliance makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The PXI Systems Alliance shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Compliance with this specification does not absolve manufacturers of PXI equipment from the requirements of safety and regulatory agencies (UL, CSA, FCC, IEC, etc.).



Trademarks

PXI™ is a trademark of the PXI Systems Alliance.

PICMG™ and CompactPCI® are trademarks of the PCI Industrial Computation Manufacturers Group.

Product and company names are trademarks or trade names of their respective companies.

重要信息

版权

© 版权所有 1997-2005 PXI 系统联盟。保留所有权利。

本文档的版权归 PXI 系统联盟所有。允许完整复制和分发本文档，不加修改。

通知

PXI Express 硬件规范由 PXI 系统联盟编写并拥有版权。PXI 系统联盟的目的是使 PXI Express 硬件规范成为由各种供应商和支持的产品支持的开放行业标准。欢迎有兴趣开发 PXI 兼容产品或服务的供应商和用户，以及有兴趣与 PXI 系统联盟合作以进一步推广 PXI 作为开放行业标准的各方，以获取更多信息。

PXI 系统联盟希望收到您对本规范的意见。请访问 PXI 系统联盟网站，网址为 <http://www.pxisa.org/>，了解联系信息并了解有关 PXI 系统联盟的更多信息。

采用者的注意是，遵守或采用 PXI 系统联盟规范可能需要使用专利权所涵盖的发明。PXI 系统联盟不负责识别任何 PXI 系统联盟规范可能需要许可的专利，也不负责对引起其注意的专利的法律有效性或范围进行法律调查。PXI 系统联盟规范仅供参考。潜在用户有责任保护自己免受专利侵权的责任。

本文档中包含的信息如有更改，恕不另行通知。本文档中的材料根据本页规定的许可证和通知详细介绍了 PXI 系统联盟规范。本文档并不代表在任何公司的产品中实施本规范的任何部分的承诺。

PXI 系统联盟对本材料不作任何形式的保证，包括但不限于对适销性和特定用途适用性的默示保证。PXI 系统联盟不对此处包含的错误或与提供、性能或使用本材料相关的偶然或间接损害负责。

遵守本规范并不能免除 PXI 设备制造商对安全和监管机构（UL、CSA、FCC、IEC 等）的要求。



商标

PXI 是 PXI 系统联盟的商标。

PICMG 和 CompactPCI 是 PCI 工业计算制造商集团的商标。

产品名称和公司名称是其各自公司的商标或商品名称。

PXI Express Hardware Specification Revision History

This section is an overview of the revision history of the PXI Express Hardware Specification.

Revision 1.0, August 22, 2005

This is the first public revision of the PXI Express specification.



PXI Express 硬件规格修订历史

本节概述了 PXI Express 硬件规范的修订历史。

修订版 1.0,2005 年 8 月 22 日

这是 PXI Express 规范的首次公开修订版。



This Page Intentionally Left Blank



此页面故意留空



Contents

1. Introduction

1.1	Objectives.....	11
1.2	Intended Audience and Scope.....	13
1.3	Background and Terminology.....	13
1.4	Applicable Documents	14
1.5	Useful Web Sites.....	14

2. PXI Express Architecture Overview

2.1	Mechanical Architecture Overview	17
2.1.1	Module and Slot Types	17
2.1.1.1	3U and 6U PXI Express System Module and Slot	17
2.1.1.2	3U and 6U PXI Express Peripheral Module and Slot.....	20
2.1.1.3	3U and 6U PXI Express Hybrid Peripheral Slot	23
2.1.1.4	3U and 6U PXI Express System Timing Module and Slot	25
2.1.1.5	PXI-1 Slot.....	28
2.1.1.6	3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module.....	28
2.1.2	System Slot and System Timing Module Location.....	29
2.1.3	Additional Mechanical Features.....	30
2.1.4	Interoperability with CompactPCI Express.....	30
2.1.5	Typical System Components.....	30
2.1.6	Chassis Supporting Stacking 3U Modules in a 6U Slot.....	31
2.2	Electrical Architecture Overview.....	32
2.2.1	Features Leveraged from CompactPCI Express	33
2.2.2	Features Leveraged from the PXI Hardware Specification	34
2.2.3	New Instrumentation Features	34
2.2.3.1	High-Frequency System Reference Clock.....	36
2.2.3.2	Differential Synchronization Signal	36
2.2.3.3	Differential Triggers	37
2.2.3.4	System Timing Module	37
2.2.4	Slot Identification.....	37
2.2.4.1	Module Drivers and the GA Pins.....	37
2.2.4.2	Determining the Chassis Number.....	37
2.2.5	Controller Identification.....	38
2.2.6	Chassis Identification	38
2.2.7	Power Requirements	38
2.3	Software Architecture Overview.....	38



3. Mechanical Requirements

3.1	Drawing Standard.....	41
3.2	Dimensional Units.....	41
3.3	Chassis Subrack Mechanical Requirements.....	41
3.4	Minimum Slot Requirements to be a PXI Express Chassis	41
3.5	Features Leveraged from PXI-1: PXI Hardware Specification	41
3.5.1	Maximum Number of Slots.....	41
3.5.2	System Slot Location and Rules.....	41
3.5.3	Slot Numbering and Orientation	42
3.5.4	PXI-1 Slot.....	42
3.5.5	Hybrid Slot-Compatible PXI-1 Peripheral Modules	43
3.6	Features Leveraged from CompactPCI Express Specification	43
3.6.1	Module Connector Requirements.....	43
3.6.1.1	Advanced Differential Fabric (ADF) Connector	43
3.6.1.2	Enriched Hard-Metric (eHM) Connector	43
3.6.1.3	Universal Power (UPM) Connector.....	43

内容

1. 介绍

- 1.1 目标 11
- 1.2 目标受众和范围 13
- 1.3 背景和术语 13
- 1.4 适用文件 14
- 1.5 有用的网站 14

2. PXI Express 架构概述

- 2.1 机械架构概述 17
 - 2.1.1 模块和插槽类型 17
 - 2.1.1.1 3U 和 6U PXI Express 系统模块和插槽 17
 - 2.1.1.2 3U 和 6U PXI Express 外设模块和插槽 20
 - 2.1.1.3 3U 和 6U PXI Express 混合外设插槽 23
 - 2.1.1.4 3U 和 6U PXI Express 系统定时模块和插槽 25
 - 2.1.1.5 PXI-1 插槽 28
 - 2.1.1.6 兼容 3U 和 6U 混合插槽的 PXI-1 外设模块 28
 - 2.1.2 系统插槽和系统定时模块位置 29
 - 2.1.3 附加机械功能 30
 - 2.1.4 与 CompactPCI Express 30 的互作性
 - 2.1.5 典型系统组件 30
 - 2.1.6 机箱支持在 6U 插槽中堆叠 3U 模块 31
- 2.2 电气架构概述 32
 - 2.2.1 CompactPCI Express 33 利用的功能
 - 2.2.2 PXI 硬件规范 34 中利用的功能
 - 2.2.3 新的仪器功能 34
 - 2.2.3.1 高频系统参考时钟 36
 - 2.2.3.2 差分同步信号 36
 - 2.2.3.3 差动触发器 37
 - 2.2.3.4 系统定时模块 37
 - 2.2.4 槽识别 37
 - 2.2.4.1 模块驱动器和 GA 引脚 37
 - 2.2.4.2 确定底盘编号 37
 - 2.2.5 控制器识别 38
 - 2.2.6 底盘识别 38
 - 2.2.7 电源要求 38
- 2.3 软件架构概述 38

3. 机械要求

- 3.1 图纸标准 41
- 3.2 尺寸单位 41
- 3.3 机箱子机架机械要求 41
- 3.4 PXI Express 机箱的最低插槽要求 41
- 3.5 PXI-1 的特性: PXI 硬件规范 41
 - 3.5.1 最大插槽数 41
 - 3.5.2 系统插槽位置和规则 41
 - 3.5.3 槽编号和方向 42
 - 3.5.4 PXI-1 插槽 42
 - 3.5.5 混合插槽兼容 PXI-1 外设模块 43
- 3.6 CompactPCI Express 规范 43 中利用的功能
 - 3.6.1 模块连接器要求 43
 - 3.6.1.1 高级差分结构 (ADF) 连接器 43
 - 3.6.1.2 强化硬公制 (eHM) 连接器 43
 - 3.6.1.3 通用电源 (UPM) 连接器 43



3.6.2	Backplane Connector Requirements	43
3.6.2.1	Advanced Differential Fabric (ADF) Connector.....	43
3.6.2.2	Enriched Hard-Metric (eHM) Connector	43
3.6.2.3	Universal Power (UPM) Connector.....	43
3.6.3	3U and 6U Module Requirements.....	44
3.6.3.1	System Module	44
3.6.3.2	PXI Express Peripheral Module	44
3.6.4	Backplane Requirements.....	46
3.6.4.1	System Slot	46
3.6.4.2	Peripheral Slot	46
3.6.4.3	PXI Express Hybrid Peripheral Slot	47
3.7	New Module and Slot Types.....	48
3.7.1	PXI Express System Timing Module Requirements.....	48
3.7.2	Backplane Requirements for New Slot Types	50
3.7.2.1	PXI Express System Timing Slot Requirements	50
3.8	Requirements for Stacking 3U Modules in 6U Slots	54
3.9	PXI Logo.....	54
3.10	Chassis with Built-In System Modules	55
3.11	Cooling Requirements	56
3.11.1	Module Cooling Requirements	56
3.11.2	Chassis Cooling Requirements.....	56
3.12	Environmental Specifications	57
3.12.1	Temperature Specifications.....	57
3.12.2	Humidity Specifications.....	57
3.12.3	Vibration Specifications.....	57
3.12.4	Acoustic Noise Specifications.....	57
3.13	PXI Express Compatibility Glyphs	57
3.13.1	Module Glyphs	57
3.13.2	Chassis Slot Glyphs.....	58



4. Electrical Requirements

4.1	PCI Signals.....	59
4.1.1	Hybrid Slot Requirements	59
4.1.2	PXI-1 Slot Requirements	59
4.2	CPCI Express Signals	59
4.2.1	System Module/Slot Requirements	59
4.2.2	PXI Express Peripheral Module / Slot Requirements	61
4.2.3	System Timing Module/Slot Requirements	62
4.2.4	Hybrid Slot Requirements	63
4.3	PXI-1 Instrumentation Signals.....	64
4.3.1	Reference Clock: PXI_CLK10.....	64
4.3.2	Trigger Bus.....	64
4.3.3	Star Trigger	65
4.3.4	Local Bus.....	65
4.4	PXI Express Timing References	66
4.4.1	Backplane Requirements	66
4.4.1.1	PXIE_CLK100	66
4.4.1.2	PXI_CLK10.....	66
4.4.1.3	PXIE_SYNC100	67
4.4.1.4	Timing, Switching, and PXIE_SYNC_CTRL	67
4.4.2	System Timing Module Requirements.....	71
4.4.3	Peripheral Module Requirements.....	71
4.4.3.1	PXIE_CLK100	71

3.6.2	背板连接器要求 43
3.6.2.1	高级差分结构 (ADF) 连接器 43
3.6.2.2	强化硬公制 (eHM) 连接器 43
3.6.2.3	通用电源 (UPM) 连接器 43
3.6.3	3U 和 6U 模块要求 44
3.6.3.1	系统模块 44
3.6.3.2	PXI Express 外设模块 44
3.6.4	背板要求 46
3.6.4.1	系统插槽 46
3.6.4.2	外围插槽 46
3.6.4.3	PXI Express 混合外设插槽 47
3.7	新模块和插槽类型 48
3.7.1	PXI Express 系统定时模块要求 48
3.7.2	新插槽类型 50 的背板要求
3.7.2.1	PXI Express 系统时序时隙要求 50
3.8	在 6U 插槽中堆叠 3U 模块的要求 54
3.9	PXI 徽标 54
3.10	内置系统模块的机箱 55
3.11	冷却要求 56
3.11.1	模块冷却要求 56
3.11.2	机箱冷却要求 56
3.12	环境规范 57
3.12.1	温度规格 57
3.12.2	湿度规格 57
3.12.3	振动规格 57
3.12.4	声学噪声规格 57
3.13	PXI Express 兼容性字形 57
3.13.1	模块字形 57
3.13.2	机箱插槽字形 58



4. 电气要求

4.1	PCI 信号 59
4.1.1	混合槽要求 59
4.1.2	PXI-1 插槽要求 59
4.2	CPCI Express 信号 59
4.2.1	系统模块/插槽要求 59
4.2.2	PXI Express 外设模块/插槽要求 61
4.2.3	系统时序模块/插槽要求 62
4.2.4	混合槽要求 63
4.3	PXI-1 仪器信号 64
4.3.1	参考时钟: PXI_CLK10 64
4.3.2	触发总线 64
4.3.3	星际扳机 65
4.3.4	65 路公交车
4.4	PXI Express 时序参考 66
4.4.1	背板要求 66
4.4.1.1	PXIe_CLK100 66
4.4.1.2	PXI_CLK10 66
4.4.1.3	PXIe_SYNC100 67
4.4.1.4	定时、开关和 PXIe_SYNC_CTRL 67
4.4.2	系统时序模块要求 71
4.4.3	外围模块要求 71
4.4.3.1	PXIe_CLK100 71

	4.4.3.2	PXI_CLK10.....	72
	4.4.3.3	PXIe_SYNC100	72
4.5	Differential Triggers.....	74	
4.5.1	Chassis Requirements	74	
4.5.2	PXIe Peripheral Module / Slot Requirements	75	
4.5.2.1	PXIe_DSTARA	75	
4.5.2.2	PXIe_DSTARB	76	
4.5.2.3	PXIe_DSTARC	76	
4.5.3	System Timing Module/Slot Requirements	77	
4.5.3.1	PXIe_DSTARA	77	
4.5.3.2	PXIe_DSTARB	77	
4.5.3.3	PXIe_DSTARC	78	
4.6	Slot Identification.....	78	
4.7	Backplane Identification	78	
4.8	SMBus Address Reservation.....	79	
4.9	Electrical Guidelines for 6U.....	79	
4.9.1	6U Chassis that Support Stacking 3U Modules	80	
4.10	Connector Pin Assignments	80	
4.10.1	PXI Express Peripheral Slots and Modules.....	80	
4.10.2	PXI Express System Slot and Modules.....	80	
4.10.2.1	4 Link Configuration	81	
4.10.2.2	2 Link Configuration	82	
4.10.3	PXI Express Hybrid Peripheral Slot.....	83	
4.10.4	PXI-1 Slot.....	83	
4.10.5	System Timing Slot.....	84	
4.11	POWER.....	84	
4.11.1	Power Requirements from CompactPCI Express	85	
4.11.2	Chassis Requirements	85	
4.11.2.1	Minimum Required Continuous Current.....	85	
4.11.2.2	Low-Power Chassis Power Supply Specifications	87	
4.11.3	Module Requirements	87	
4.11.3.1	Maximum Continuous Current Draw	88	
4.12	Chassis Grounding	88	



5. Regulatory Requirements

5.1	Requirements for EMC	89
5.2	Requirements for Electrical Safety	89
5.3	Additional Requirements for Chassis.....	89

6. PXI Express Software Specification Compliance

Figures

Figure 1-1.	PXI Express Hardware Specification Architectures	12
Figure 1-2.	PXI Express Software Specification Architecture	12
Figure 2-1.	3U PXI Express System Module.....	18
Figure 2-2.	6U PXI Express System Module.....	18
Figure 2-3.	3U PXI Express System Slot.....	19
Figure 2-4.	6U PXI Express System Slot.....	20
Figure 2-5.	3U PXI Express Peripheral Module	21
Figure 2-6.	6U PXI Express Peripheral Module	21
Figure 2-7.	3U PXI Express Peripheral Slot	22
Figure 2-8.	6U PXI Express Peripheral Slot	23
Figure 2-9.	3U PXI Express Hybrid Peripheral Slot.....	24

	4.4.3.2	PXI_CLK10 72
	4.4.3.3	PXIe_SYNC100 72
4.5	差动触发器 74	
4.5.1	底盘要求 74	
4.5.2	PXIe 外设模块/插槽要求 75	
4.5.2.1	PXIe_DSTARA 75	
4.5.2.2	PXIe_DSTARB 76	
4.5.2.3	PXIe_DSTARC 76	
4.5.3	系统时序模块/插槽要求 77	
4.5.3.1	PXIe_DSTARA 77	
4.5.3.2	PXIe_DSTARB 77	
4.5.3.3	PXIe_DSTARC 78	
4.6	插槽识别 78	
4.7	背板识别 78	
4.8	SMBus 地址预订 79	
4.9	6U 79 电气指南	
4.9.1	支持堆叠的 6U 机箱 3U 模块 80	
4.10	连接器引脚分配 80	
4.10.1	PXI Express 外设插槽和模块 80	
4.10.2	PXI Express 系统插槽和模块 80	
4.10.2.1	4 链路配置 81	
4.10.2.2	2 链路配置 82	
4.10.3	PXI Express 混合外设插槽 83	
4.10.4	PXI-1 插槽 83	
4.10.5	系统定时插槽 84	
4.11	功率 84	
4.11.1	CompactPCI Express 85 的电源要求	
4.11.2	底盘要求 85	
4.11.2.1	所需的最小连续电流 85	
4.11.2.2	低功耗机箱电源规格 87	
4.11.3	模块要求 87	
4.11.3.1	最大连续电流消耗 88	
4.12	机箱接地 88	



5. 监管要求

- 5.1 EMC 89 的要求
- 5.2 电气安全要求 89
- 5.3 机箱 89 的附加要求

6. PXI Express 软件规范合规性

数字

图 1-1.PXI Express 硬件规范架构 12 图 1-2.PXI Express 软件规范架构 12 图 2-1.3U PXI Express 系统模块 18 图 2-2.6U PXI Express 系统模块 18 图 2-3.3U PXI Express 系统插槽 19 图 2-4.6U PXI Express 系统插槽 20 图 2-5.3U PXI Express 外设模块 21 图 2-6.6U PXI Express 外设模块 21 图 2-7.3U PXI Express 外设插槽 22 图 2-8.6U PXI Express 外设插槽 23 图 2-9.3U PXI Express 混合外设插槽 24

Figure 2-10.	6U PXI Express Hybrid Peripheral Slot.....	25
Figure 2-11.	6U PXI Express System Timing Module.....	26
Figure 2-12.	3U PXI Express System Timing Slot.....	27
Figure 2-13.	6U PXI Express System Timing Slot.....	27
Figure 2-14.	6U PXI Express System Timing Slot with Stacked 3U Support	28
Figure 2-15.	3U Hybrid Peripheral Slot Compatible PXI-1 Module	29
Figure 2-16.	6U Hybrid Peripheral Slot Compatible PXI-1 Module	29
Figure 2-17.	Typical System Components.....	31
Figure 2-18.	Example of a PXI Express Chassis that Supports 3U Stacking	32
Figure 2-19.	Instrumentation Signal Implementation Example.....	35
Figure 2-20.	Instrumentation Signals Connector Mapping.....	36
Figure 3-1.	6U PXI Express Peripheral Module PCB	45
Figure 3-2.	6U PXI Express Peripheral Module	46
Figure 3-3.	6U PXI Express Peripheral Slot	47
Figure 3-4.	6U PXI Express Hybrid Slot	48
Figure 3-5.	3U PXI Express System Timing Module PCB	49
Figure 3-6.	6U PXI Express System Timing Module PCB	50
Figure 3-7.	3U PXI Express System Timing Slot Backplane Dimensions	51
Figure 3-8.	6U PXI Express System Timing Slot Backplane Dimensions.....	52
Figure 3-9.	6U PXI Express System Timing Slot with Stacked Support Backplane Dimensions	53
Figure 3-10.	PXI Logo.....	55
Figure 3-11.	PXI Express Logo	55
Figure 3-12.	Cooling Airflow Direction in a PXI Express System	56
Figure 3-13.	Module Glyphs.....	58
Figure 3-14.	Slot Glyphs.....	58
Figure 4-1.	PXI Trigger Bus Termination	64
Figure 4-2.	Timing relationship of PXI_CLK10 to PXIe_CLK100	68
Figure 4-3.	Timing Relationship of PXIe_SYNC100 to PXI_CLK10 and PXIe_CLK100	68
Figure 4-4.	PXIe_SYNC100 Default Behavior	69
Figure 4-5.	PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart	70
Figure 4-6.	PXIe_SYNC100 Using PXIe_SYNC_CTRL as Enable.....	70
Figure 4-7.	Timing Relationship between SYNC_CTRL and PXI_CLK10	71
Figure 4-8.	Peripheral Module Circuit for Terminating PXIe_CLK100 Signal.....	72
Figure 4-9.	Peripheral Module Circuit for Terminating PXIe_SYNC100 Circuit	73
Figure 4-10.	Circuit to recreate PXI_CLK10 Internally as MyCLK10	73
Figure 4-11.	Peripheral Module Circuit for Terminating PXIe_DSTARA	76
Figure 4-12.	Text Required for Low-Power Chassis	87



Tables

Table 2-1.	PXI Express and CompactPCI Express Specification Names	17
Table 2-2.	PXI and PXI Express Module Interoperability	33
Table 3-1.	Upper and Lower 3U Slot Implementation	54
Table 4-1.	System Module and Slot Requirements	59
Table 4-2.	PXI Express Peripheral Module and Slot Requirements	61
Table 4-3.	System Timing Module and Slot Requirements	62
Table 4-4.	Hybrid Slot Requirements.....	63
Table 4-5.	Timing relationship of PXI_CLK10 to PXIe_CLK100	68
Table 4-6.	Timing Relationship of PXIe_SYNC100 to PXI_CLK10 and PXIe_CLK100	69
Table 4-7.	Timing Relationship between SYNC_CTRL and PXI_CLK10	71
Table 4-8.	PXIe_DSTAR Set Mapping	74
Table 4-9.	PXI Express Peripheral Slot and Module Pin Assignments.....	80
Table 4-10.	Pin Assignments for 4 Link Operation.....	81
Table 4-11.	Pin Assignments for 2 Link Operation.....	82

图 2-10.6U PXI Express 混合外设插槽 25 图 2-11.6U PXI Express 系统时序模块 26 图 2-12.3U PXI Express 系统时序插槽 27 图 2-13.6U PXI Express 系统时序插槽 27 图 2-14.6U PXI Express 系统时序插槽, 带堆叠 3U 支架 28 图 2-15.3U 混合外设插槽兼容 PXI-1 模块 29 图 2-16.6U 混合外设插槽兼容 PXI-1 模块 29 图 2-17.典型系统组件 31 图 2-18.支持 3U 堆叠的 PXI Express 机箱示例 32 图 2-19.仪器信号实现示例 35 图 2-20.仪器信号连接器映射 36 图 3-1.6U PXI Express 外设模块 PCB 45 图 3-2.6U PXI Express 外设模块 46 图 3-3.6U PXI Express 外设插槽 47 图 3-4.6U PXI Express 混合插槽 48 图 3-5.3U PXI Express 系统定时模块 PCB 49 图 3-6.6U PXI Express 系统定时模块 PCB 50 图 3-7.3U PXI Express 系统定时插槽背板尺寸 51 图 3-8.6U PXI Express 系统定时插槽背板尺寸 52 图 3-9.带堆叠支撑背板的 6U PXI Express 系统定时插槽 53 图 3-10.PXI 徽标 55 图 3-11.PXI Express 徽标 55 图 3-12.PXI Express 系统中的冷却气流方向 56 图 3-13.模块字形 58 图 3-14.插槽字形 58 图 4-1.PXI 触发总线终端 64 图 4-2.PXI_CLK10 与 PXIE_CLK100 68 的时序关系 图 4-3.PXIE_SYNC100 与 PXI_CLK10 和 PXIE_CLK100 的时序关系 68 图 4-4. PXIE_SYNC100 默认行为 69 图 4-5.在 3.33 MHz 时 PXIE_SYNC100 使用 PXIE_SYNC_CTRL 作为重启 70 图 4-6.PXIE_SYNC100 使用 PXIE_SYNC_CTRL 作为使能 70 图 4-7.SYNC_CTRL 与 PXI_CLK10 之间的时序关系 71 图 4-8.用于终止 PXIE_CLK100 信号的外围模块电路 72 图 4-9.用于终止 PXIE_SYNC100 电路的外围模块电路 73 图 4-10.在内部重新创建 PXI_CLK10 为 MyCLK10 的电路 73 图 4-11.用于端接 PXIE_DSTARA 76 的外围模块电路 图 4-12.低功耗机箱所需的文本 87



表

表 2-1.PXI Express 和 CompactPCI Express 规范名称 17 表 2-2.PXI 和 PXI Express 模块互作性 33 表 3-1.上 3U 插槽和下 3U 插槽实现 54 表 4-1.系统模块和插槽要求 59 表 4-2.PXI Express 外设模块和插槽要求 61 表 4-3.系统时序模块和插槽要求 62 表 4-4.混合插槽要求 63 表 4-5.PXI_CLK10 与 PXIE_CLK100 的时序关系 68 表 4-6.PXIE_SYNC100 与 PXI_CLK10 和 PXIE_CLK100 的时序关系 69 表 4-7.SYNC_CTRL 和 PXI_CLK10 之间的时序关系 71 表 4-8.PXIE_DSTARA 集映射 74 表 4-9.PXI Express 外设插槽和模块引脚分配 80 表 4-10.4 链路工作的引脚分配 81 表 4-11.2 链路工作的引脚分配 82

Table 4-12.	Hybrid Peripheral Slot Pin Assignments.....	83
Table 4-13.	PXI Express System Timing Slot/Module Pinout.....	84
Table 4-14.	PXI Express Chassis Minimum Required Continuous Current	85
Table 4-15.	PXI Express Backplane Continuous Current Capability	87



表 4-12.混合外设插槽引脚分配 83 表 4-13.PXI Express 系统时序插槽/模块引脚排列 84 表 4-14.PXI Express 机箱所需的最小连续电流 85 表 4-15.PXI Express 背板连续电流能力 87



This Page Intentionally Left Blank



此页面故意留空



1. Introduction

This section describes the primary objectives and scope of the PXI-5: PCI Express eXtensions for Instrumentation specification. It also defines the intended audience and lists relevant terminology and documents.

1.1 Objectives

PXI Express was created to build on the successful PXI-1: PXI Hardware Specification and the new CompactPCI Express standard to make new levels of performance possible in modular instrumentation and automation Systems. Similar to the PXI-1 standard, existing industry standards are leveraged by PXI Express to benefit from high component availability at lower costs. PXI Express also continues to maintain software compatibility with industry-standard personal computers, allowing customers to use the same software tools and environments with which they are familiar. Not only does PXI Express provide a giant leap in measurement and automation performance, but it also provides a high level of compatibility with PXI-1, so customers can preserve their investment in PXI-1 Modules.

PXI Express leverages the electrical features defined by the widely adopted PCI Express specification for data movement. This is accomplished by PXI Express Modules complying with the CompactPCI Express specification, which combines the PCI Express electrical specification with rugged Eurocard mechanical packaging and high-performance differential connectors. This allows measurement and automation Systems based on PXI Express to have a data throughput of 6 GBytes/sec in each direction. PXI Express also offers two-way interoperability with CompactPCI Express products.

Instrumentation capabilities within PXI Express can reach a new level of performance by providing point-to-point differential triggers, point-to-point differential variable clocks, and a 100 MHz differential System clock. The highly used bussed triggers, point-to-point triggers, and 10 MHz clock defined in the PXI-1 specification are maintained. This allows PXI Express Module designers to make optimized cost versus performance tradeoffs when implementing instrumentation features.



PXI Express maintains compatibility with Modules designed to be compliant with the PXI-1 specification in two ways. First, PXI Express allows Chassis to have slots that are defined in the PXI-1 specification. Second, PXI Express defines a slot that accepts either a high-performance Module that uses PCI Express for data transfer or a Module designed to the PXI-1 specification that has had a connector change. Of course, this also means PXI Express allows for the compatibility with Modules designed to the CompactPCI specification.

By implementing PCI Express, PXI Express Systems can leverage the large base of existing industry-standard software. Desktop PC users have access to different levels of software, from operating systems to low-level device drivers to high-level instrument drivers to complete graphical APIs. All of these software levels can be used in PXI Express Systems. The PXI Systems Alliance maintains a separate Software Specification for PXI Express Modules, Chassis, and Systems. By having a separate Software Specification, the PXI Systems Alliance can more quickly adopt the latest operating Systems and software standards. PXI Express Modules, Chassis, and Systems developed to comply with this PXI Hardware Specification must also comply with the PXI-6: *PXI Express Software Specification*.

1. 介绍

本节介绍 PXI-5: PCI Express eXtensions for Instrumentation 规范的主要目标和范围。它还定义了目标受众，并列出了相关术语和文档。

1.1 目标

PXI Express 的创建基于成功的 PXI-1: PXI 硬件规范和新的 CompactPCI Express 标准，使模块化仪器仪表和自动化系统的性能达到新的水平。与 PXI-1 标准类似，PXI Express 利用现有的行业标准，以更低的成本从高组件可用性中受益。PXI Express 还继续保持与行业标准个人计算机的软件兼容性，使客户能够使用他们熟悉的相同软件工具和环境。PXI Express 不仅在测量和自动化性能方面实现了巨大飞跃，而且还与 PXI-1 提供了高水平的兼容性，因此客户可以保留对 PXI-1 模块的投资。

PXI Express 利用广泛采用的 PCI Express 规范定义的电气特性进行数据移动。这是通过符合 CompactPCI Express 规范的 PXI Express 模块实现的，该规范将 PCI Express 电气规范与坚固的 Eurocard 机械封装和高性能差分连接器相结合。这使得基于 PXI Express 的测量和自动化系统在每个方向上的数据吞吐量为 6 GBytes/sec。PXI Express 还提供与 CompactPCI Express 产品的双向互作性。

PXI Express 中的仪器仪表功能可以通过提供点对点差分触发器、点对点差分可变时钟和 100 MHz 差分系统时钟，将性能提升到一个新的水平。PXI-1 规范中定义的高度使用的总线触发器、点对点触发器和 10 MHz 时钟将得到保留。这使得 PXI Express 模块设计人员在实现仪器功能时能够在成本与性能之间进行优化的权衡。

PXI Express 通过两种方式保持与设计为符合 PXI-1 规范的模块的兼容性。首先，PXI Express 允许机箱具有 PXI-1 规范中定义的插槽。其次，PXI Express 定义了一个插槽，该插槽可以接受使用 PCI Express 进行数据传输的高性能模块，也可以接受根据 PXI-1 规范设计但已更改连接器的模块。当然，这也意味着 PXI Express 允许与按照 CompactPCI 规范设计的模块兼容。

通过实施 PCI Express，PXI Express 系统可以利用现有行业标准软件的庞大基础。台式 PC 用户可以访问不同级别的软件，从作系统到低级设备驱动程序，再到高级仪器驱动程序，再到完整的图形 API。所有这些软件级别都可以在 PXI Express 系统中使用。PXI 系统联盟为 PXI Express 模块、机箱和系统维护了单独的软件规范。通过拥有单独的软件规范，PXI 系统联盟可以更快地采用最新的作系统和软件标准。为符合本 PXI 硬件规范而开发的 PXI Express 模块、机箱和系统也必须符合 PXI-6: PXI Express 软件规范。



1. Introduction

Figure 1-1 summarizes the scope of the *PXI Express Hardware Specification* by depicting its mechanical and electrical architectures.

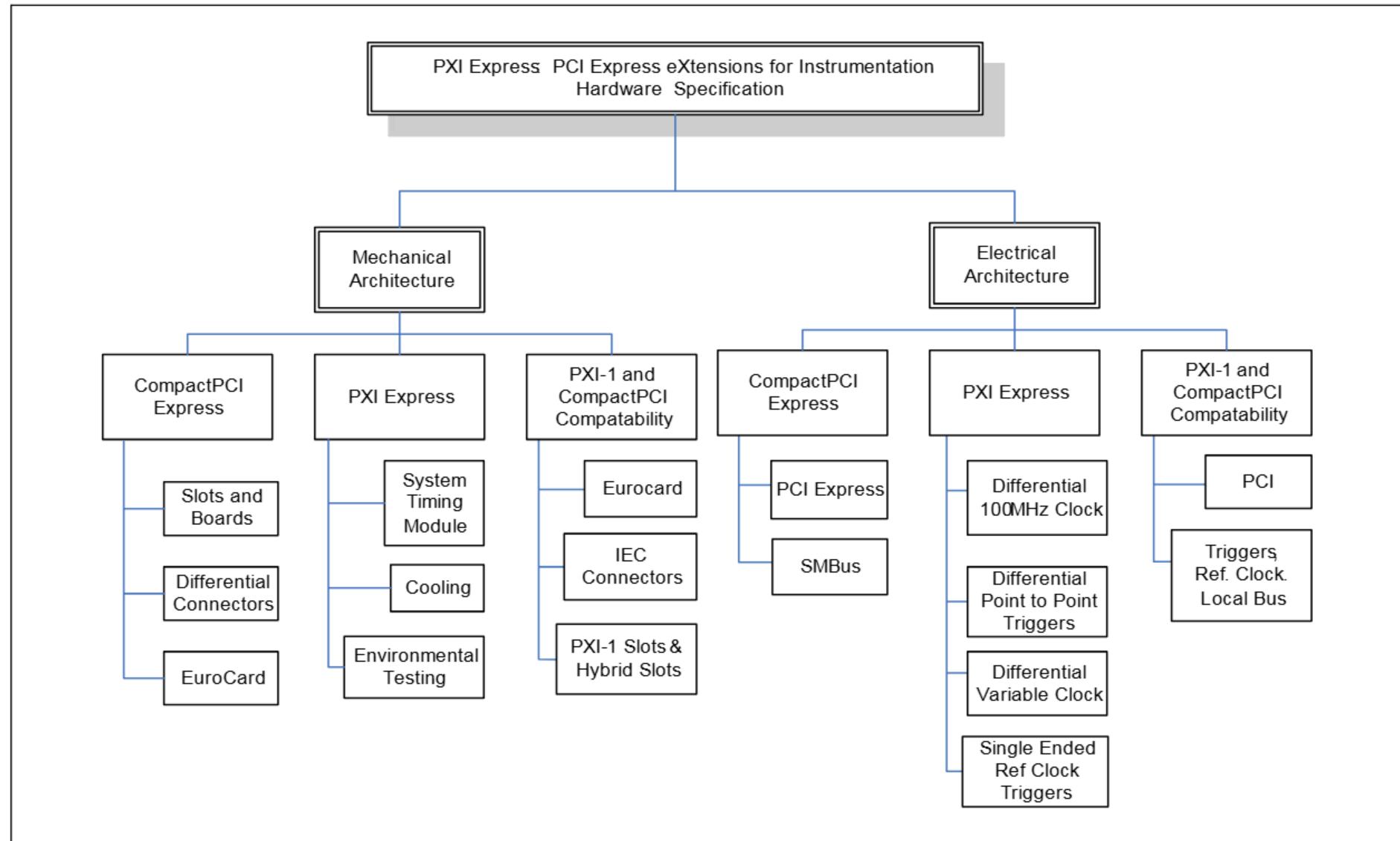


Figure 1-1. *PXI Express Hardware Specification Architectures*



Figure 1-2 summarizes the scope of the PXI-6: *PXI Express Software Specification* by depicting its architecture.

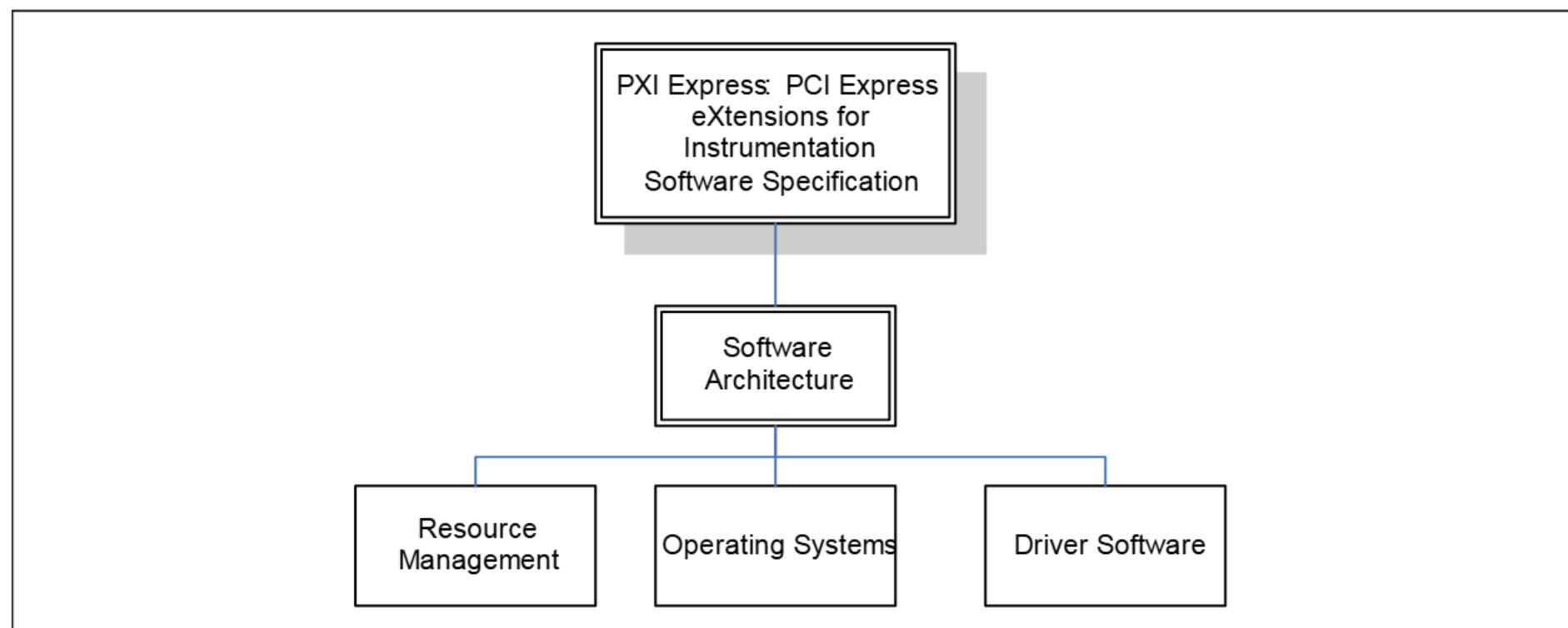


Figure 1-2. *PXI Express Software Specification Architecture*

1. 介绍

图 1-1 通过描述 PXI Express 硬件规范的机械和电气架构，总结了 PXI Express 硬件规范的范围。

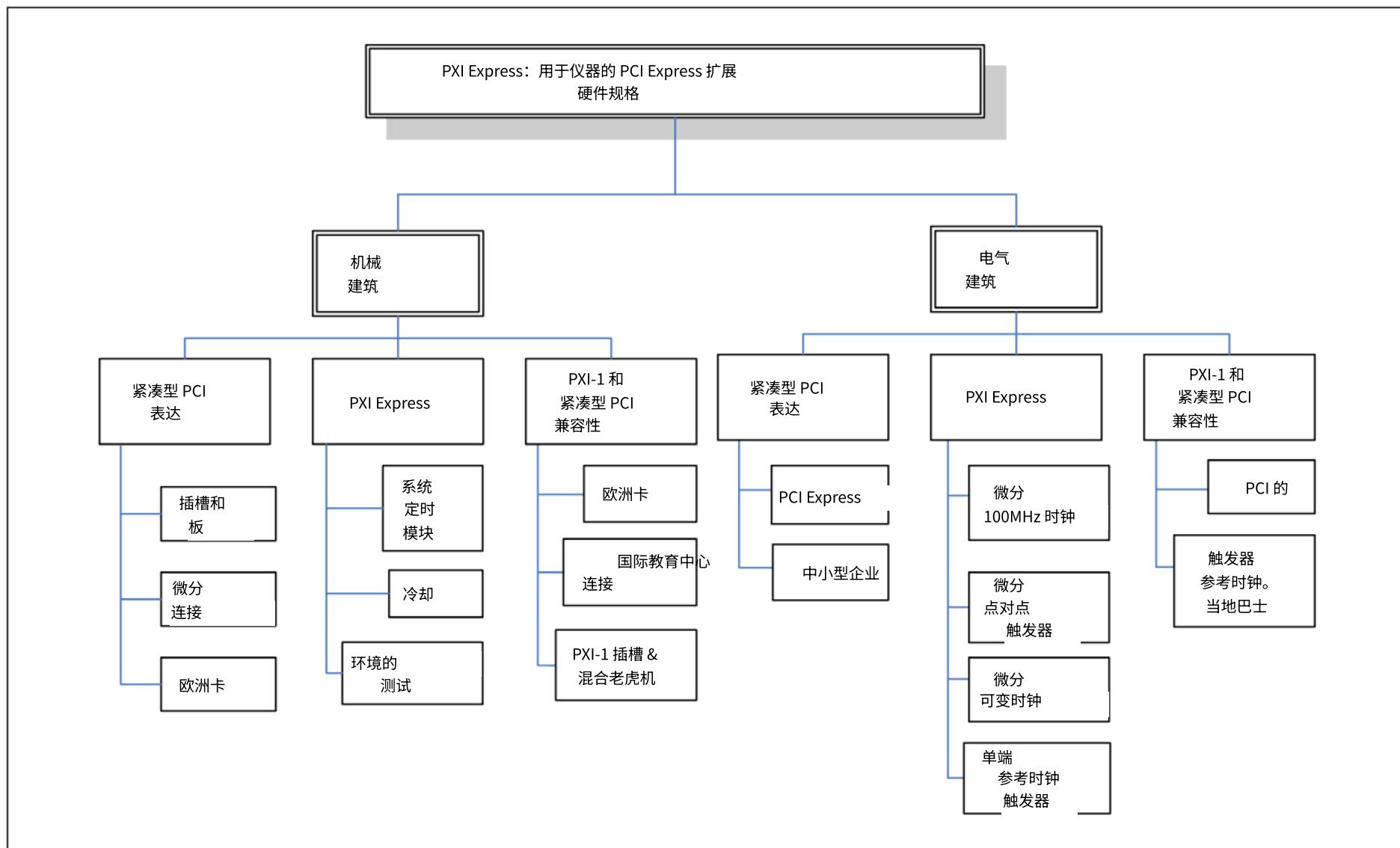


图 1-1.PXI Express 硬件规格架构



图 1-2 通过描述其架构总结了 PXI-6: PXI Express 软件规范的范围。

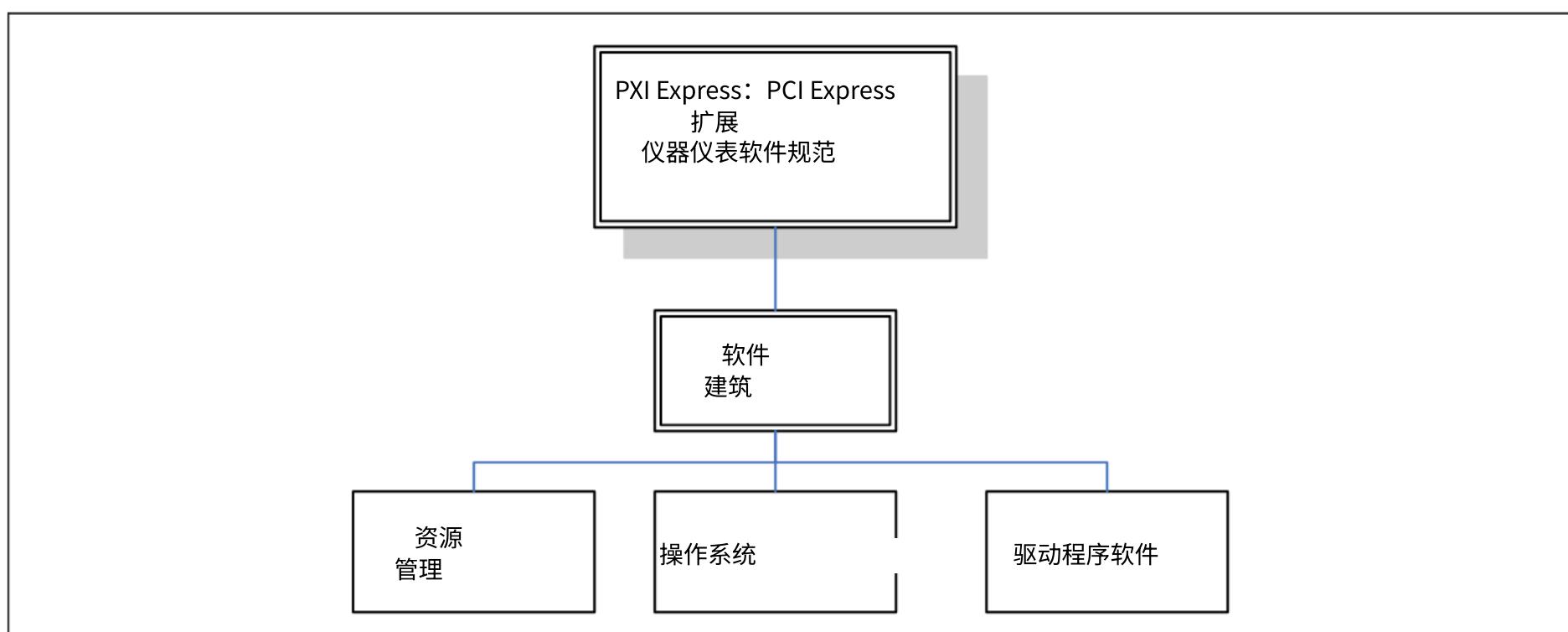


图 1-2.PXI Express 软件规范架构

1.2 Intended Audience and Scope

This specification is organized with a top-down approach whereby general descriptions precede the more detailed specifications found deeper in the subsections. This structure is intended to serve the needs of a variety of audiences from product developers to System integrators to end-users. Product developers may want to become familiar with all portions of this specification, while end users may be interested in only the feature set description and perhaps the summaries of how these features are implemented. The goal of this specification is to serve as the highest level document relevant to all users and providers of PXI Express compatible Systems, but in many cases this specification references other specifications such as CompactPCI Express and PXI-1 for certain details. These specifications and the specifications they in turn refer to may be needed to fully implement PXI Express products.

The first section of this specification describes the features that PXI Express Systems can offer and how these features can be applied to instrumentation. The subsequent sections cover the mechanical, electrical, and software requirements specific to implementing PXI Express features.

1.3 Background and Terminology

This section defines the acronyms and key words that are referred to throughout this specification. This specification uses the following acronyms:

- **API**—Application Programming Interface
- **CompactPCI**—PICMG 2.0 Specification
- **Eurocard**—European Packaging Specifications (IEC 60297, IEEE 1101.1, IEEE 1101.10, IEEE 1101.11)
- **GPIB**—General Purpose Interface Bus, IEEE 488
- **ISA**—Industry Standard Architecture; desktop PC adapter board specification
- **PCI**—Peripheral Component Interconnect; electrical specification defined by PCISIG
- **PCI Express**—Serialized evolution of PCI
- **PCI-SIG**—PCI Special Interest Group
- **PICMG**—PCI Industrial Computer Manufacturers Group
- **PXI**—PCI eXtensions for Instrumentation
- **PXI Express**—PCI Express eXtensions for Instrumentation
- **VISA**—Virtual Instrument Software Architecture
- **VITA**—VMEbus International Trade Association
- **VME**—Versa Module Europe; VMEbus specification governed by the VSO
- **VPP**—VXI*plug&play* Specification
- **VSO**—VITA Standards Organization
- **VXI**—VME Extensions for Instrumentation



This specification uses several key words, which are defined as follows:

RULE: Rules SHALL be followed to ensure compatibility. A rule is characterized by the use of the words SHALL and SHALL NOT.

RECOMMENDATION: Recommendations consist of advice to implementers that will affect the usability of the final Module. A recommendation is characterized by the use of the words SHOULD and SHOULD NOT.

1.2 目标受众和范围

本规范采用自上而下的方法进行组织，其中一般描述在小节中更详细的规范之前。这种结构旨在满足从产品开发人员到系统集成商再到最终用户等各种受众的需求。产品开发人员可能希望熟悉本规范的所有部分，而最终用户可能只对功能集描述感兴趣，也许对这些功能如何实现的摘要感兴趣。本规范的目标是作为与 PXI Express 兼容系统的所有用户和提供商相关的最高级别文档，但在许多情况下，本规范引用了其他规范，例如 CompactPCI Express 和 PXI-1，以了解某些细节。这些规范及其所引用的规范可能需要完全实现 PXI Express 产品。

本规范的第一部分介绍了 PXI Express 系统可以提供的功能以及如何将这些功能应用于仪器。后续部分介绍了实现 PXI Express 功能的特定机械、电气和软件要求。

1.3 背景和术语

本节定义了整个规范中引用的首字母缩略词和关键字。本规范使用以下首字母缩略词：

- API - 应用程序编程接口
- CompactPCI—PICMG 2.0 规范
- Eurocard - 欧洲封装规范 (IEC 60297、IEEE 1101.1、IEEE 1101.10、IEEE 1101.11)
- GPIB — 通用接口总线, IEEE 488
- ISA—行业标准架构;台式电脑适配器板规格
- PCI—外围组件互连;PCISIG 定义的电气规范
- PCI Express — PCI 的序列化演进
- PCI-SIG—PCI 特别兴趣小组
- PICMG—PCI 工业计算机制造商集团
- PXI—用于仪器的 PCI 扩展
- PXI Express — PCI Express 仪器仪表扩展
- VISA—虚拟仪器软件架构
- VITA—VMEbus 国际贸易协会
- VME—Versa Module Europe;由 VSO 管理的 VMEbus 规范
- VPP—VXI 即插即用规范
- VSO — VITA 标准组织
- VXI—用于仪表的 VME 扩展



本规范使用了几个关键词，定义如下：

规则：应遵守规则以确保兼容性。规则的特点是使用 SHALL 和 SHALL NOT 这两个词。

建议：建议包括对实施者的建议，这些建议将影响最终模块的可用性。建议的特点是使用了“应该”和“不应该”这两个词。

PERMISSION: Permissions clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. A permission is characterized by the use of the word MAY.

OBSERVATION: Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

MAY: A key word indicating flexibility of choice with no implied preference. This word is usually associated with a permission.

SHALL: A key word indicating a mandatory requirement. Designers SHALL implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification. This word is usually associated with a rule.

SHOULD: A key word indicating flexibility of choice with a strongly preferred implementation. This word is usually associated with a recommendation.

1.4 Applicable Documents

This specification defines extensions to the base PCI Express and CompactPCI Express specifications referenced in this section. It is assumed that the reader has a thorough understanding of PCI Express and CompactPCI Express. The CompactPCI Express specification refers to several other applicable documents with which the reader may wish to become familiar. This specification refers to the following documents directly:

- PXI Software Specification (Latest Revision)
- PXI Hardware Specification (Latest Revision)
- *PCI Local Bus Specification*, Rev. 2.3
- *PCI Express Base Specification 1.1*
- *PCI Express Card Electromechanical (CEM) Specification 1.1*
- *PICMG 2.0 R3.0 CompactPCI Specification*
- *PICMG EXP.0 CompactPCI Express Specification*
- *System Management Bus (SMBus) Specification, Version 2.0*
- *VXIplug&play Specifications* (VPP-3.x and VPP-7)
- IEC 61326-1:1998, *Electrical equipment for measurement, control, and laboratory use—EMC requirements—Part I, General requirements*, International Electrotechnical Commission
- IEC 1010-1:1990 + A1:1992, *Safety requirements for electrical equipment for measurement, control, and laboratory use—Part 1, General requirements*, International Electrotechnical Commission
- IEC 60068-1, *Environmental testing*, International Electrotechnical Commission



1.5 Useful Web Sites

Below is a list of Web site links that at the time of publication of this specification point to sites with information useful in the understanding and design of PXI products:

- <http://www.pxisa.org/>—PXI specifications
- <http://www.picmg.org/>—PICMG specifications
- <http://www.ieee.org/>—IEEE specifications
- <http://www.iec.org/>—IEC specifications
- <http://www.pcisig.com/>—PCI and PCI Express specifications

1. 介绍

权限：权限阐明了规范中未明确禁止的领域。权限让读者放心，某种方法是可以接受的，并且不会造成任何问题。权限的特点是使用“可能”一词。

观察：观察阐明了规则的含义，并引起了人们对可能被忽视的事情的关注。它们还给出了某些规则背后的基本原理，以便读者理解为什么必须遵守该规则。

MAY：一个关键词，表示选择的灵活性，没有隐含的偏好。这个词通常与权限相关联。

SHALL：表示强制性要求的关键词。设计人员应实施此类强制性要求，以确保可互换性并声称符合规范。这个词通常与规则相关联。

SHOULD：一个关键词，表示选择的灵活性和强烈首选的实现。这个词通常与建议相关联。

1.4 适用文件

本规范定义了本节中引用的基本 PCI Express 和 CompactPCI Express 规范的扩展。假定读者对 PCI Express 和 CompactPCI Express 有透彻的了解。CompactPCI Express 规范是指读者可能希望熟悉的其他几个适用文档。本规范直接引用以下文档：

- PXI 软件规范（最新版本）
- PXI 硬件规格（最新版本）
- PCI 本地总线规范，修订版 2.3
- PCI Express 基本规范 1.1
- PCI Express 卡机电（CEM）规范 1.1
- PICMG 2.0 R3.0 CompactPCI 规范
- PICMG EXP.0 CompactPCI Express 规范
- 系统管理总线（SMBus）规范，版本 2.0
- VXI 即插即用规格（VPP-3.x 和 VPP-7）
- IEC 61326-1: 1998, 测量、控制和实验室用电气设备 EMC 要求——第一部分，一般要求，国际电工委员会
- IEC 1010-1: 1990 + A1: 1992, 测量、控制和实验室用电气设备的安全要求——第 1 部分，一般要求，国际电工委员会
- IEC 60068-1, 环境测试，国际电工委员会



1.5 有用的网站

以下是在本规范发布时指向的网站链接列表，这些链接指向包含对理解和设计 PXI 产品有用的信息的网站：

- <http://www.pxisa.org/> — PXI 规格
- <http://www.picmg.org/> — PICMG 规格
- <http://www.ieee.org/> — IEEE 规范
- <http://www.iec.org/> — IEC 规范
- <http://www.pcisig.com/> — PCI 和 PCI Express 规范

- <http://www.vita.com/>—VME specifications
- <http://www.vxi.org/>—VXI specifications
- <http://www.vxipnp.org/>—VISA specifications
- <http://www.smbus.org/>—SMBus specification



- <http://www.vita.com/> - VME 规格
- <http://www.vxi.org/> - VXI 规范
- <http://www.vxipnp.org/> - VISA 规格
- <http://www.smbus.org/> - SMBus 规范



This Page Intentionally Left Blank



此页面故意留空



2. PXI Express Architecture Overview

This section presents an overview of PXI Express System features and capabilities by summarizing the mechanical, electrical, and software architectures defined by this specification.

2.1 Mechanical Architecture Overview

PXI Express supports 3U and 6U Module form factors just like PXI-1. Several new connectors have been added to support PCI-Express and are defined by the CompactPCI Express specification. This specification uses different names for the Module and slot types as compared to CompactPCI Express and introduces some new types as well. Table 2-1 shows the PXI Express component name and the equivalent CompactPCI Express component name.

Table 2-1. PXI Express and CompactPCI Express Specification Names

PXI Express Specification Name	CompactPCI Express Specification Name
PXI Express System Slot	System Slot
PXI Express System Module	System Board
PXI Express Peripheral Slot	Type 2 Peripheral Slot
PXI Express Peripheral Module	Type 2 Peripheral Board
PXI Express Hybrid Slot	Hybrid Slot
Hybrid Slot Compatible PXI-1 Module	N/A
PXI Express System Timing Slot	N/A
PXI Express System Timing Module	N/A
PXI-1 Slot	Legacy Slot
PXI-1 Module	CompactPCI Peripheral Board



The Module and slot types used from the CompactPCI Express specification as well as the new ones introduced by this specification are described in the following sections.

2.1.1 Module and Slot Types

PXI Express Module and slot types include a 3U and 6U PXI Express System Module and Slot, a 3U and 6U PXI Express Peripheral Module and Slot, a PXI Express 3U and 6U Hybrid Peripheral Slot, a 3U and 6U PXI Express System Timing Module and Slot, a 3U and 6U Hybrid Slot, and a 3U and 6U Hybrid Slot compatible PXI-1 Module. In addition to these Module and slot types, 3U and 6U PXI Peripheral Slots defined in the PXI-1 specification are allowed in PXI Express Chassis to support PXI-1 Peripheral Modules.

2.1.1.1 3U and 6U PXI Express System Module and Slot

PXI Express System Modules have four required connectors, XP1/XJ2/XJ3/XJ4, as defined by the CompactPCI Express specification. A simplified description of the connector functionality is XP1/XJ1 is for power, XP2/XJ2 and XP3/XJ3 are for PCI Express, and XP4/XJ4 is for instrumentation signals defined in the PXI-1 specification. The 6U System Module may use J3/J4/J5 for rear I/O applications.

2. PXI Express 架构概述

本节通过总结本规范定义的机械、电气和软件架构，概述了 PXI Express 系统的特性和功能。

2.1 机械架构概述

PXI Express 支持 3U 和 6U 模块外形规格，就像 PXI-1 一样。添加了几个新的连接器来支持 PCI-Express，并由 CompactPCI Express 规范定义。与 CompactPCI Express 相比，该规范对模块和插槽类型使用不同的名称，并引入了一些新类型。表 2-1 显示了 PXI Express 组件名称和等效的 CompactPCI Express 组件名称。

表 2-1.PXI Express 和 CompactPCI Express 规范名称

PXI Express 规范名称	CompactPCI Express 规范名称
PXI Express 系统插槽	系统插槽
PXI Express 系统模块	系统板
PXI Express 外设插槽	2 型外设插槽
PXI Express 外设模块	2 型外围板
PXI Express 混合插槽	混合老虎机
混合插槽兼容 PXI-1 模块	不适用
PXI Express 系统时序插槽	不适用
PXI Express 系统时序模块	不适用
PXI-1 插槽	旧版老虎机
PXI-1 模块	CompactPCI 外设板

以下部分介绍了 CompactPCI Express 规范中使用的模块和插槽类型以及本规范引入的新模块和插槽类型。

2.1.1 模块和插槽类型

PXI Express 模块和插槽类型包括 3U 和 6U PXI Express 系统模块和插槽、3U 和 6U PXI Express 外设模块和插槽、PXI Express 3U 和 6U 混合外设插槽、3U 和 6U PXI Express 系统定时模块和插槽、3U 和 6U 混合插槽以及 3U 和 6U 混合插槽兼容 PXI-1 模块。除了这些模块和插槽类型外，PXI Express 机箱中还允许 PXI-1 规范中定义的 3U 和 6U PXI 外设插槽支持 PXI-1 外设模块。

2.1.1.1 3U 和 6U PXI Express 系统模块和插槽

PXI Express 系统模块有四个必需的连接器，即 XP1/XJ2/XJ3/XJ4，如 CompactPCI Express 规范所定义。连接器功能的简化描述是，XP1/XJ1 用于电源，XP2/XJ2 和 XP3/XJ3 用于 PCI Express，XP4/XJ4 用于 PXI-1 规范中定义的仪器信号。6U 系统模块可将 J3/J4/J5 用于后置 I/O 应用。

2. PXI Express Architecture Overview

Figures 2-1 and 2-2 show the 3U and 6U PXI Express System Modules, respectively.

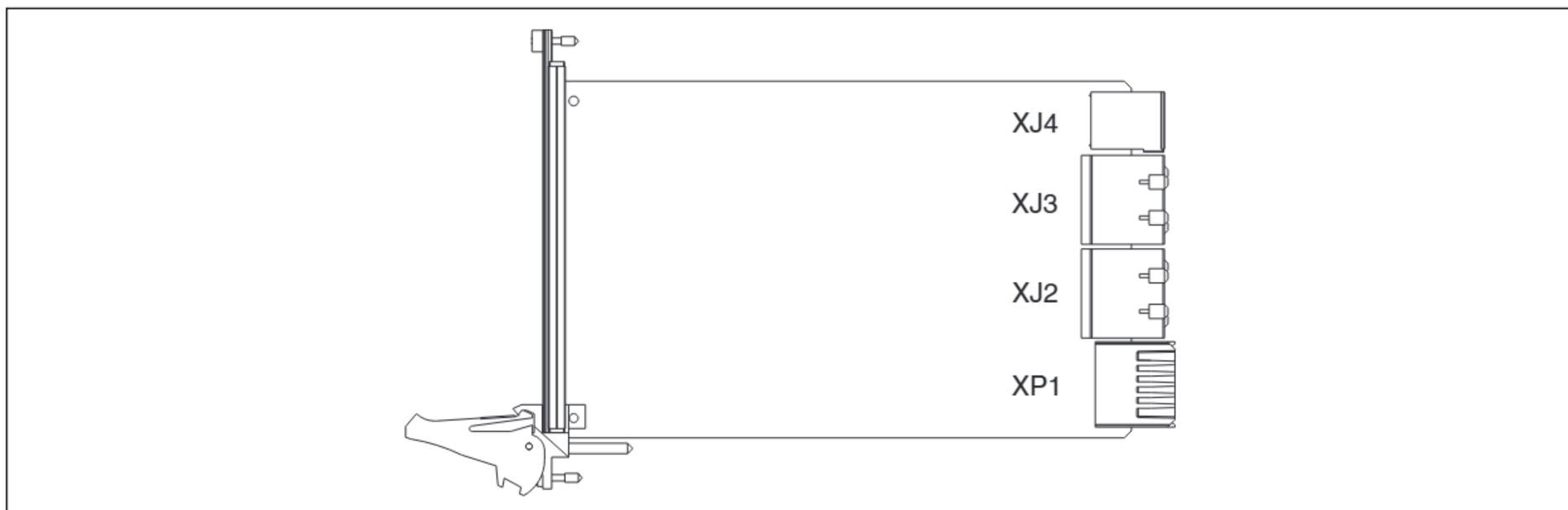


Figure 2-1. 3U PXI Express System Module

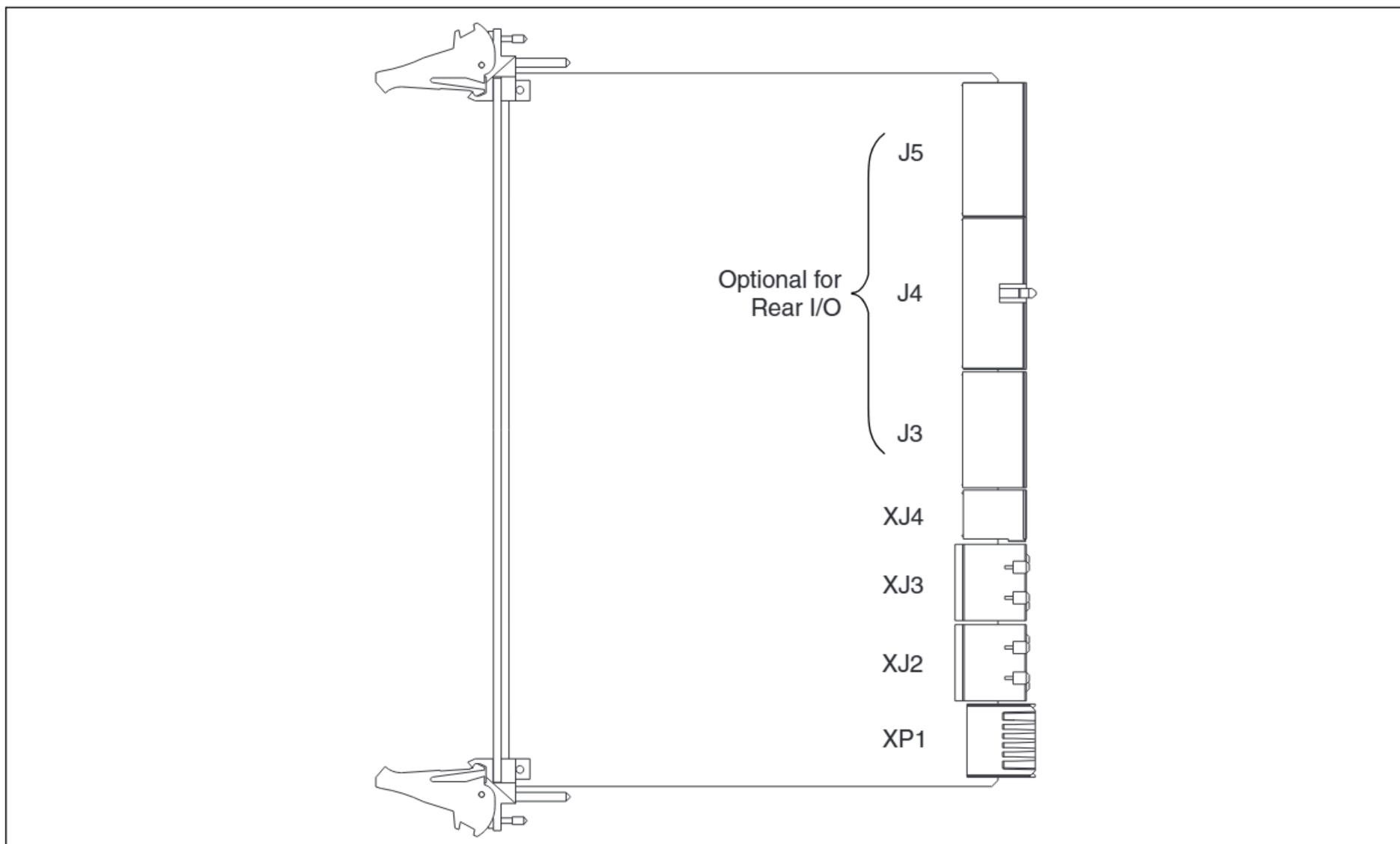


Figure 2-2. 6U PXI Express System Module

2. PXI Express 架构概述

图 2-1 和 2-2 分别显示了 3U 和 6U PXI Express 系统模块。

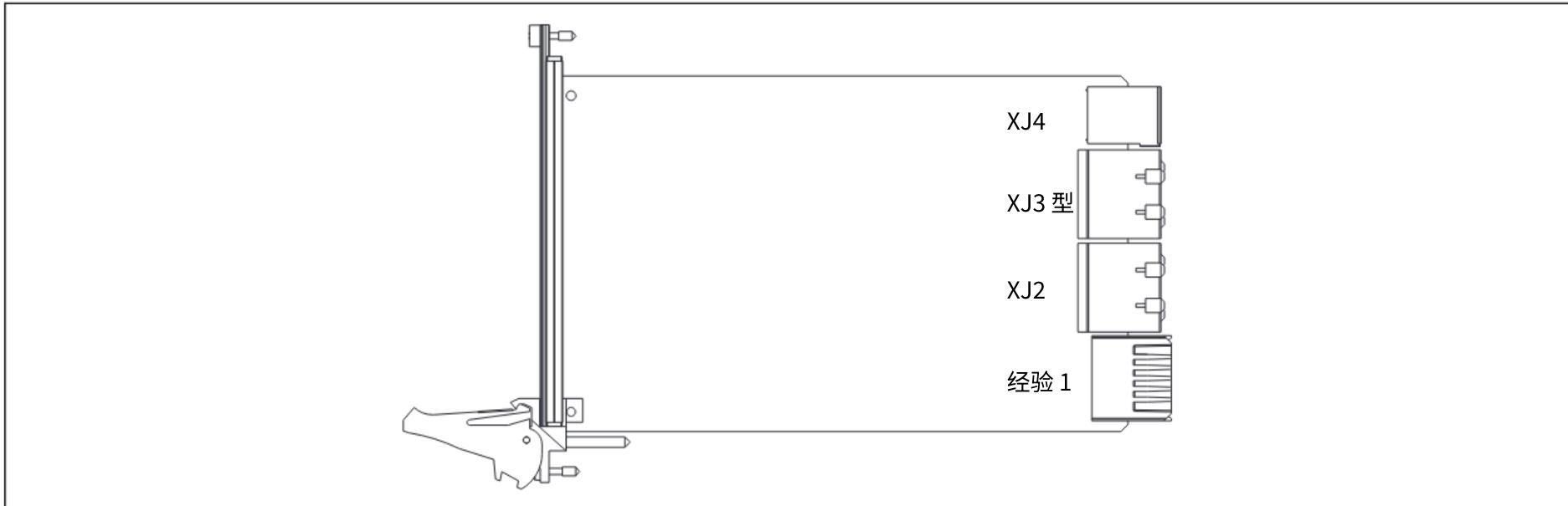


图 2-1.3U PXI Express 系统模块

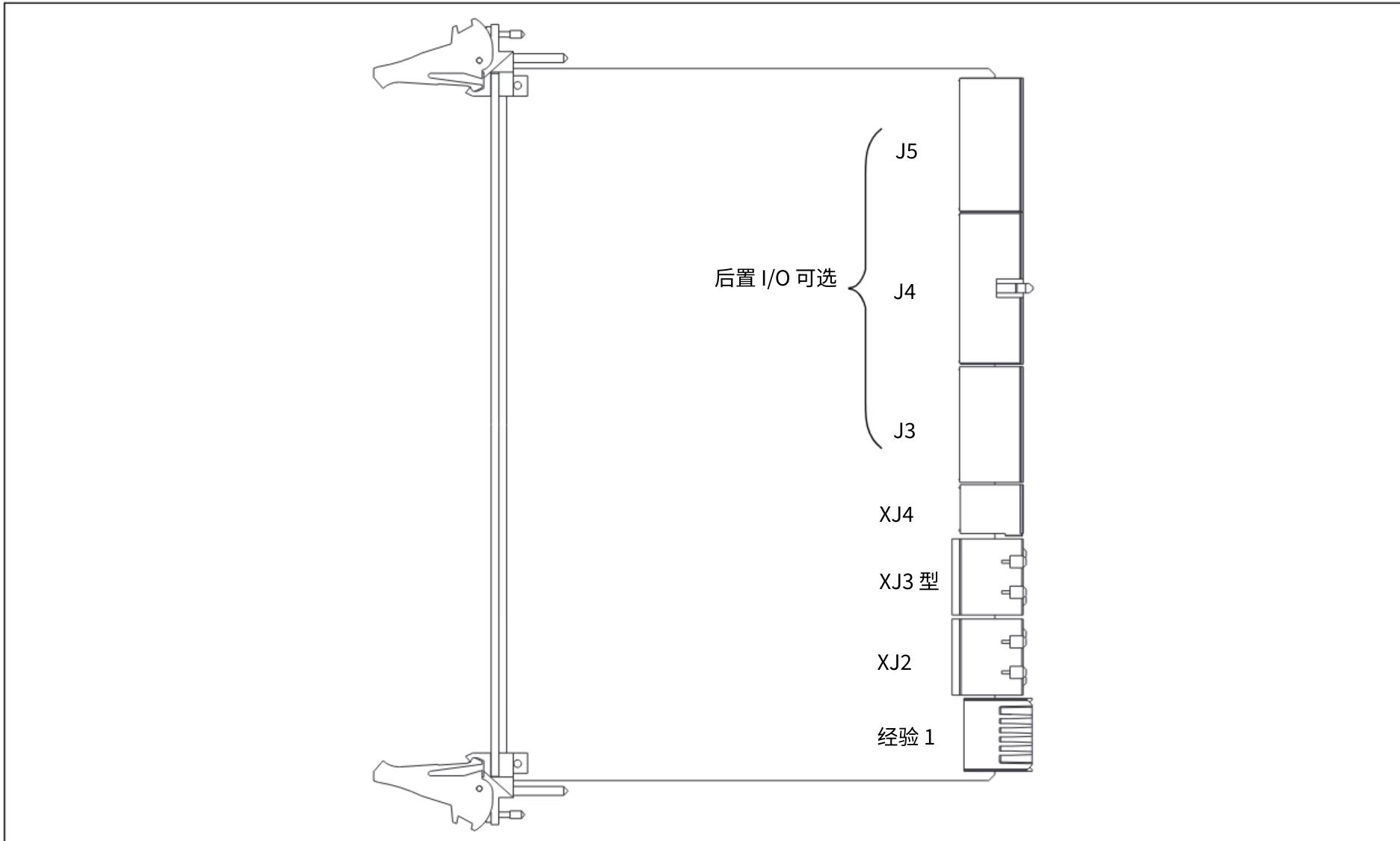


图 2-2.6U PXI Express 系统模块

Figures 2-3 and 2-4 show the 3U and 6U PXI Express System Slots, respectively.

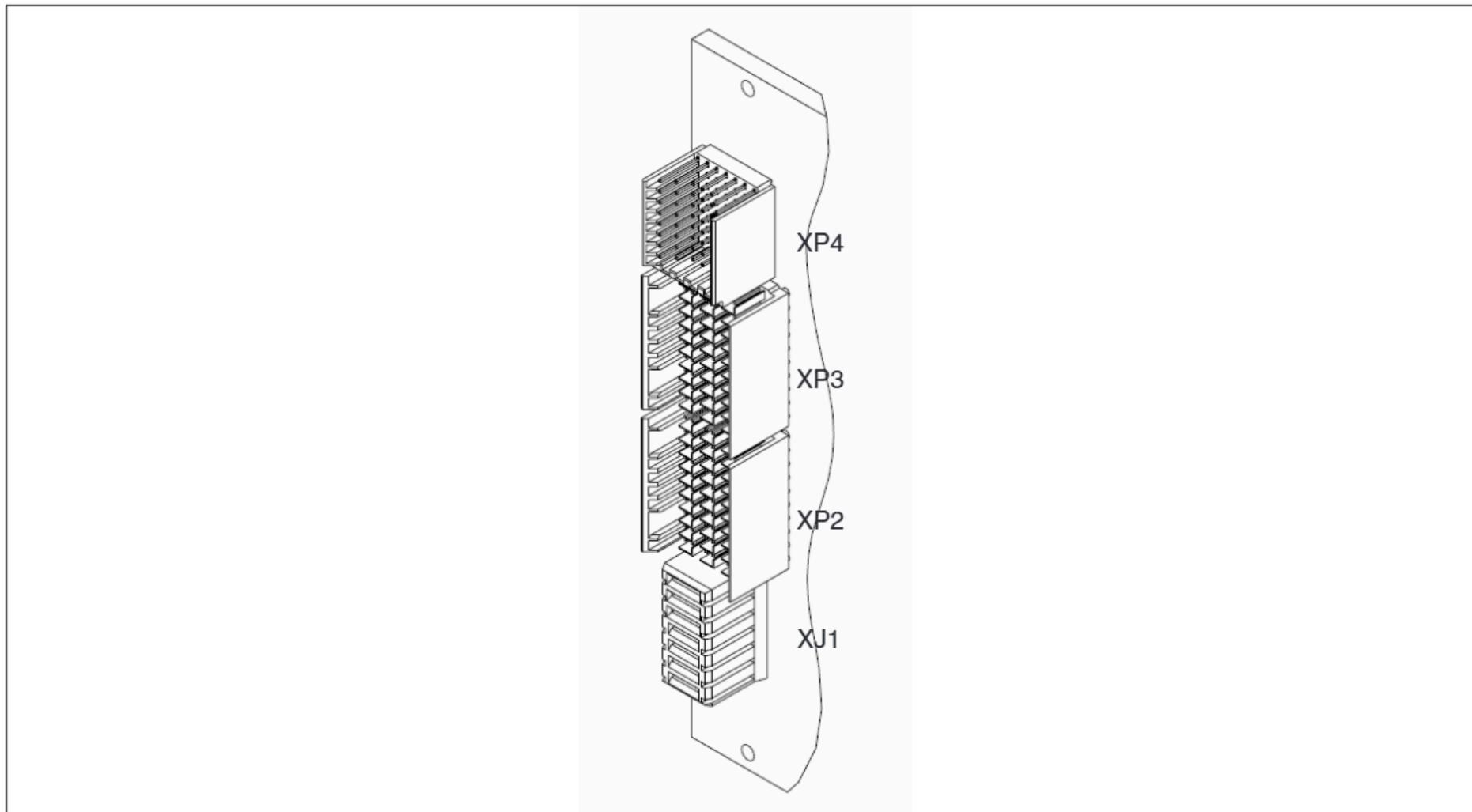


Figure 2-3. 3U PXI Express System Slot



图 2-3 和 2-4 分别显示了 3U 和 6U PXI Express 系统插槽。

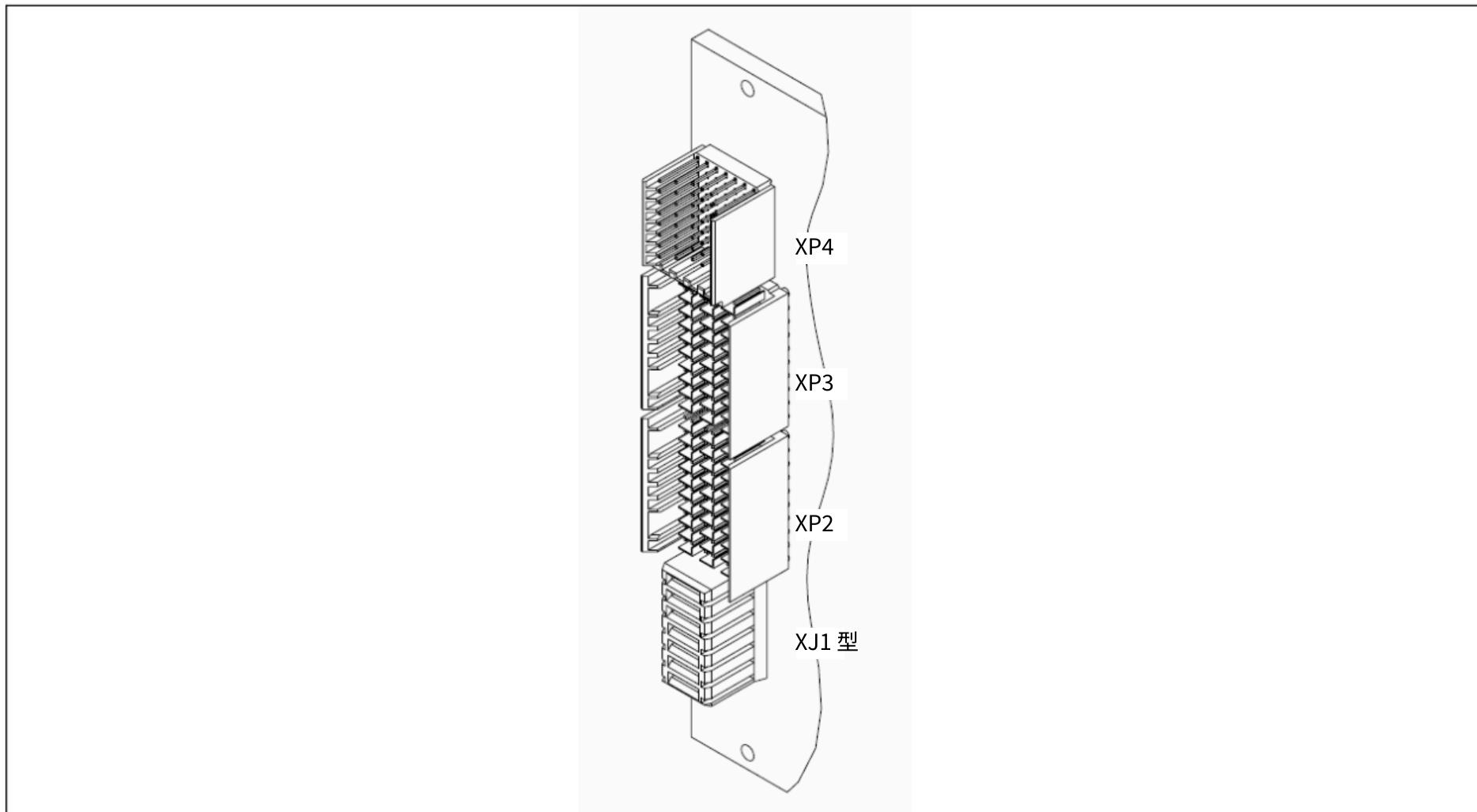


图 2-3.3U PXI Express 系统插槽



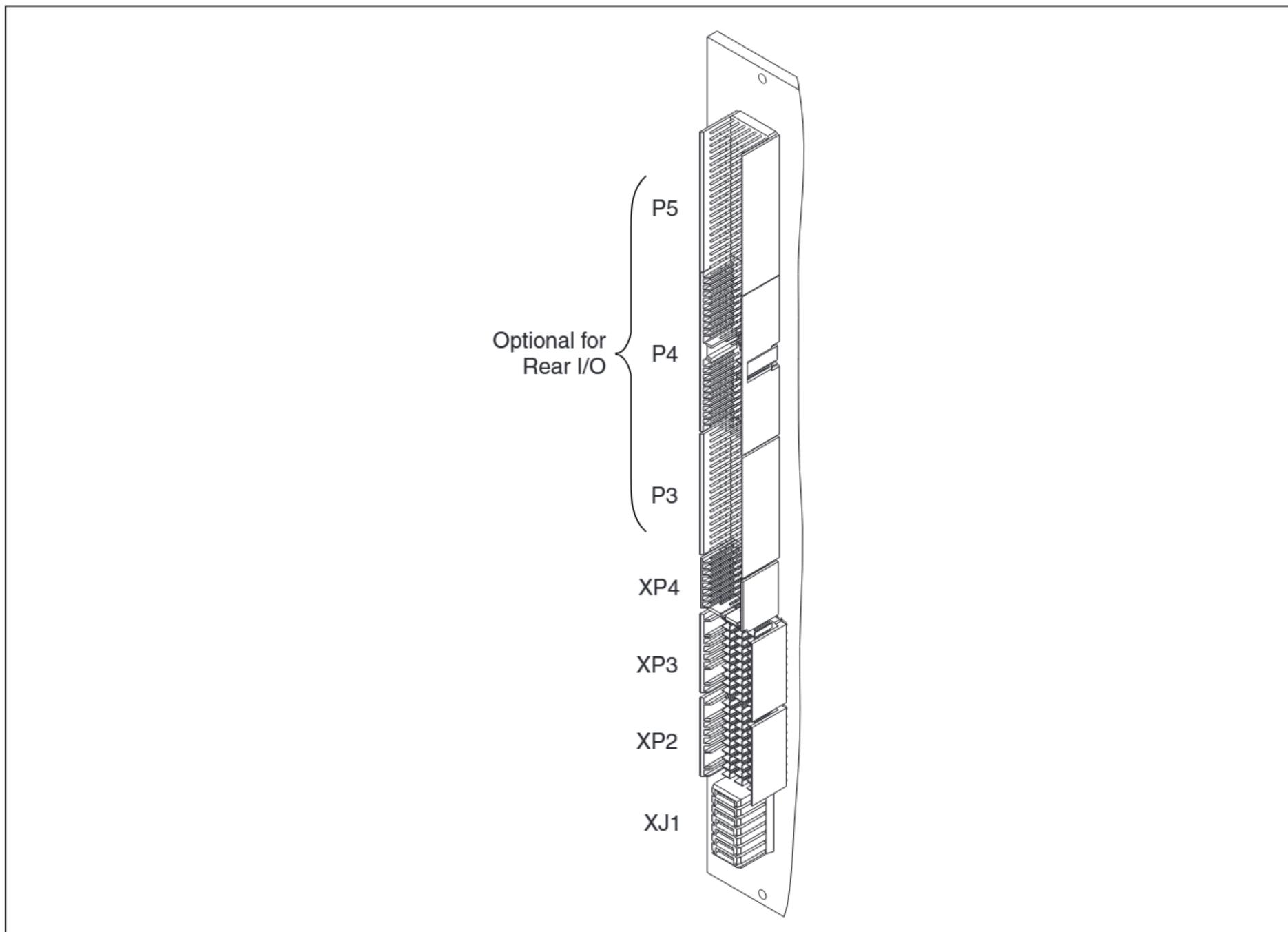


Figure 2-4. 6U PXI Express System Slot

2.1.1.2 3U and 6U PXI Express Peripheral Module and Slot

The 3U PXI Express Peripheral Module has two connectors, XJ3 and XJ4. A simplified description of the connector functionality is that XP3/XJ3 are for PCI Express and Differential Triggers and Timing, and XP4/XJ4 is for instrumentation signals that are defined in the PXI-1 specification. The 6U PXI Express Peripheral Module has an Optional eHM connector (required for backplanes), XJ8, that is populated in the upper columns of the legacy J5 location to provide additional power to the 6U Module. The PXI Express specification does not support the use of J3/J4/J5 on 6U Peripheral Modules.

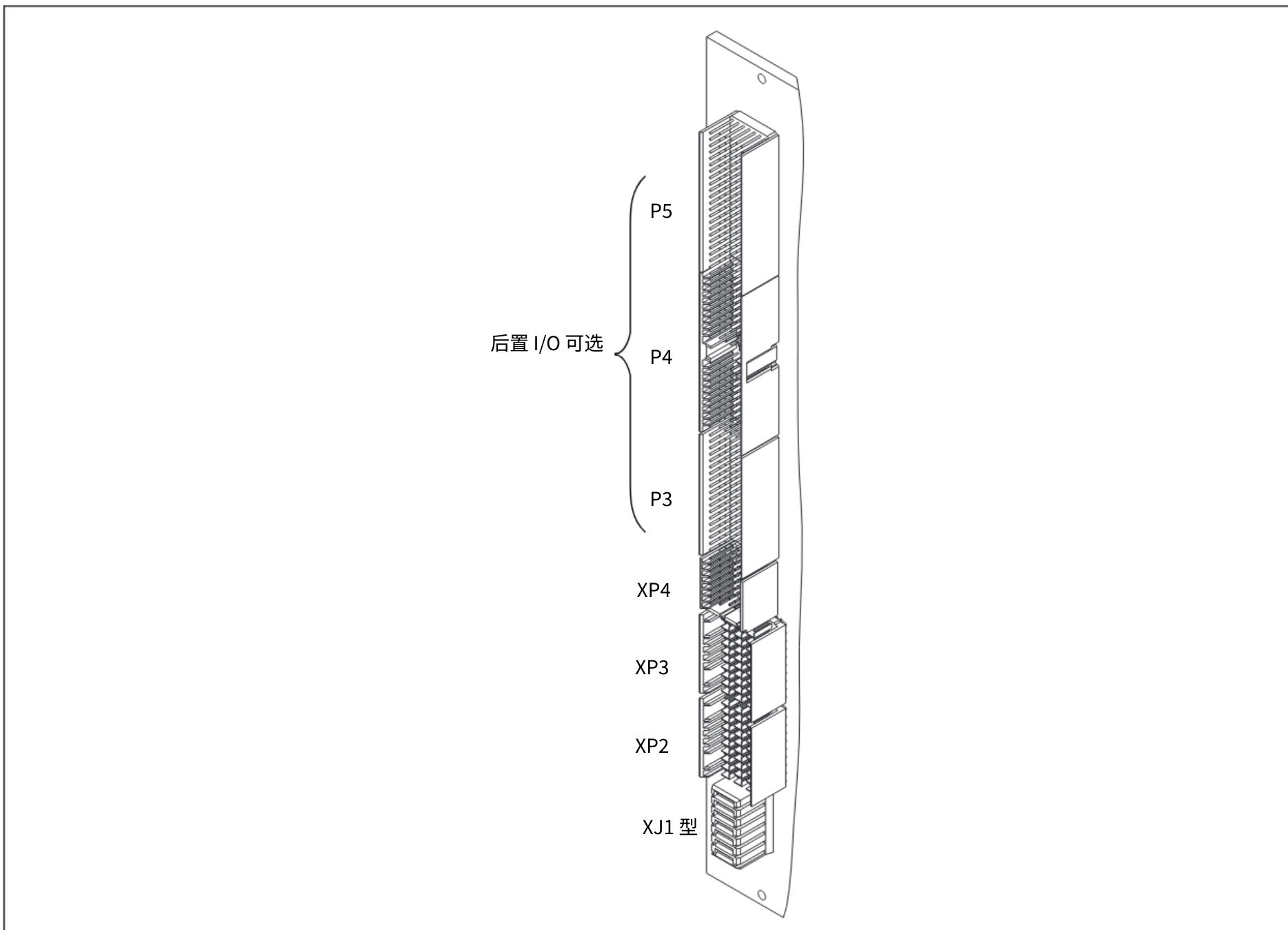


图 2-4.6U PXI Express 系统插槽

2.1.1.2 3U 和 6U PXI Express 外设模块和插槽

3U PXI Express 外设模块有两个连接器，XJ3 和 XJ4。连接器功能的简化描述是，XP3/XJ3 用于 PCI Express 和差分触发器和定时，XP4/XJ4 用于 PXI-1 规范中定义的仪器信号。6U PXI Express 外设模块有一个可选的 eHM 连接器（背板必需），XJ8，该连接器填充在传统 J5 位置的上列中，为 6U 模块提供额外的电源。PXI Express 规范不支持在 6U 外设模块上使用 J3/J4/J5。

Figures 2-5 and 2-6 show the 3U and 6U PXI Express Peripheral Modules, respectively.

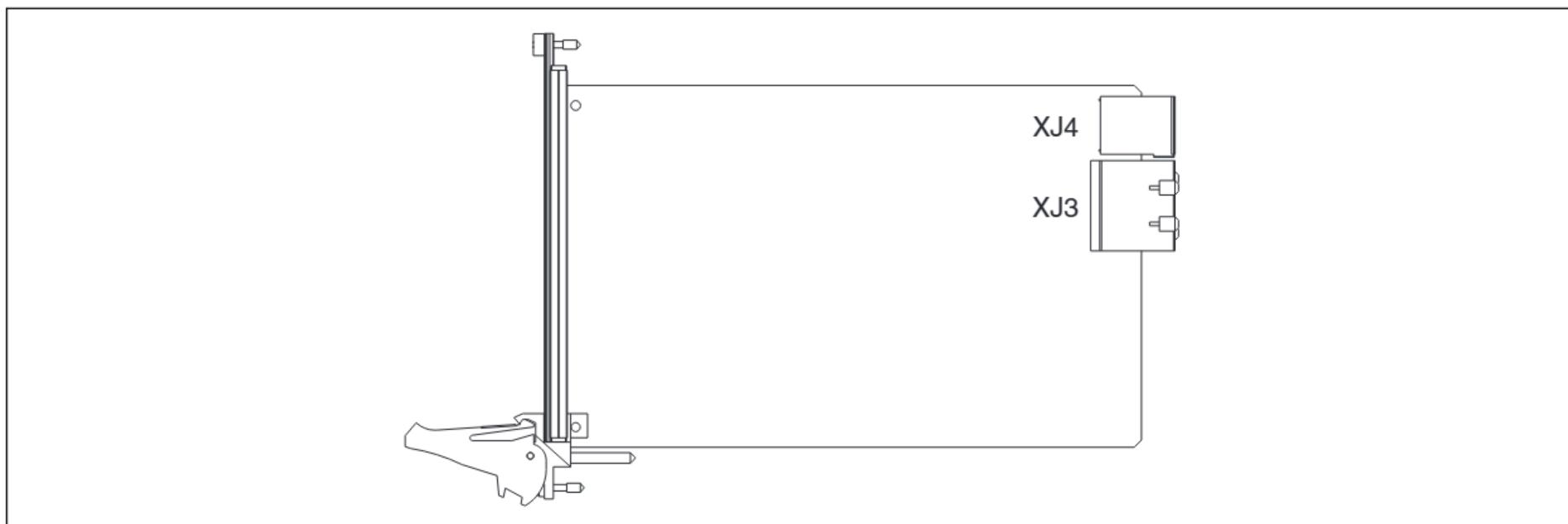


Figure 2-5. 3U PXI Express Peripheral Module

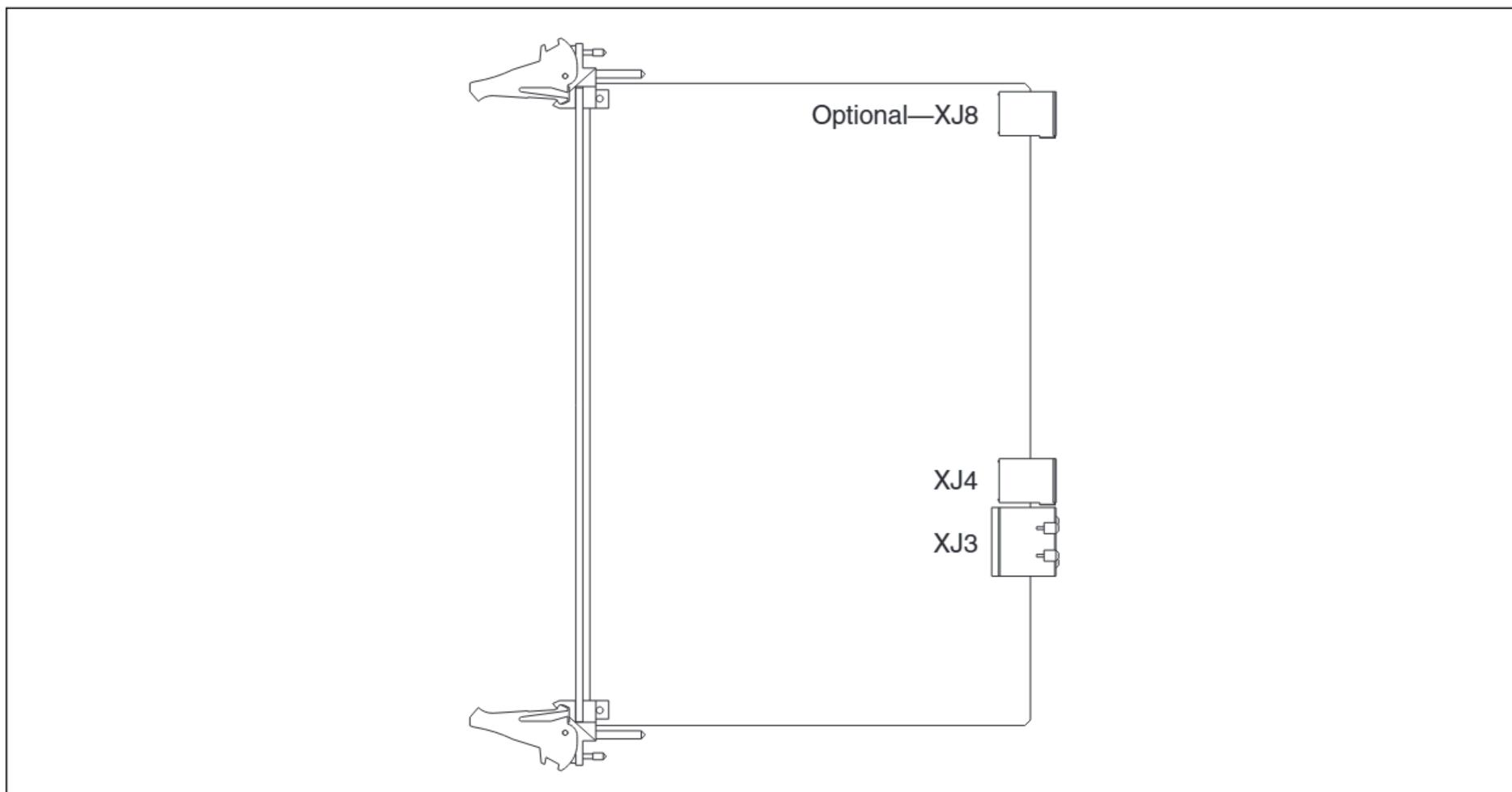


Figure 2-6. 6U PXI Express Peripheral Module



图 2-5 和 2-6 分别显示了 3U 和 6U PXI Express 外设模块。

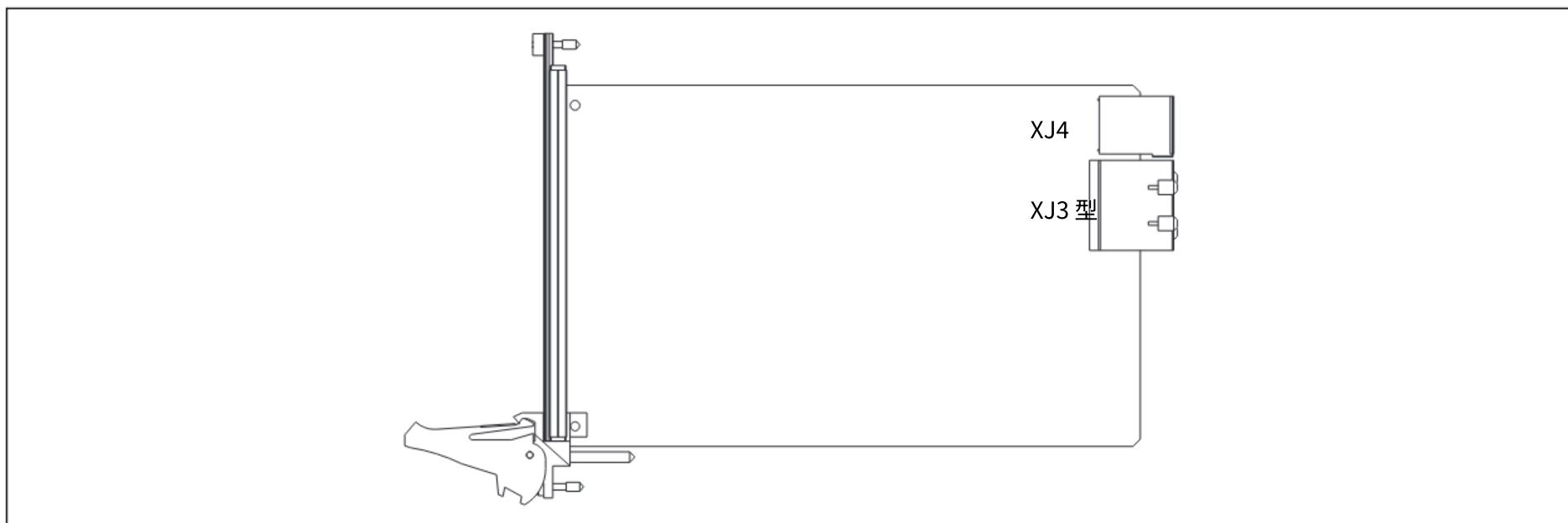


图 2-5.3U PXI Express 外设模块

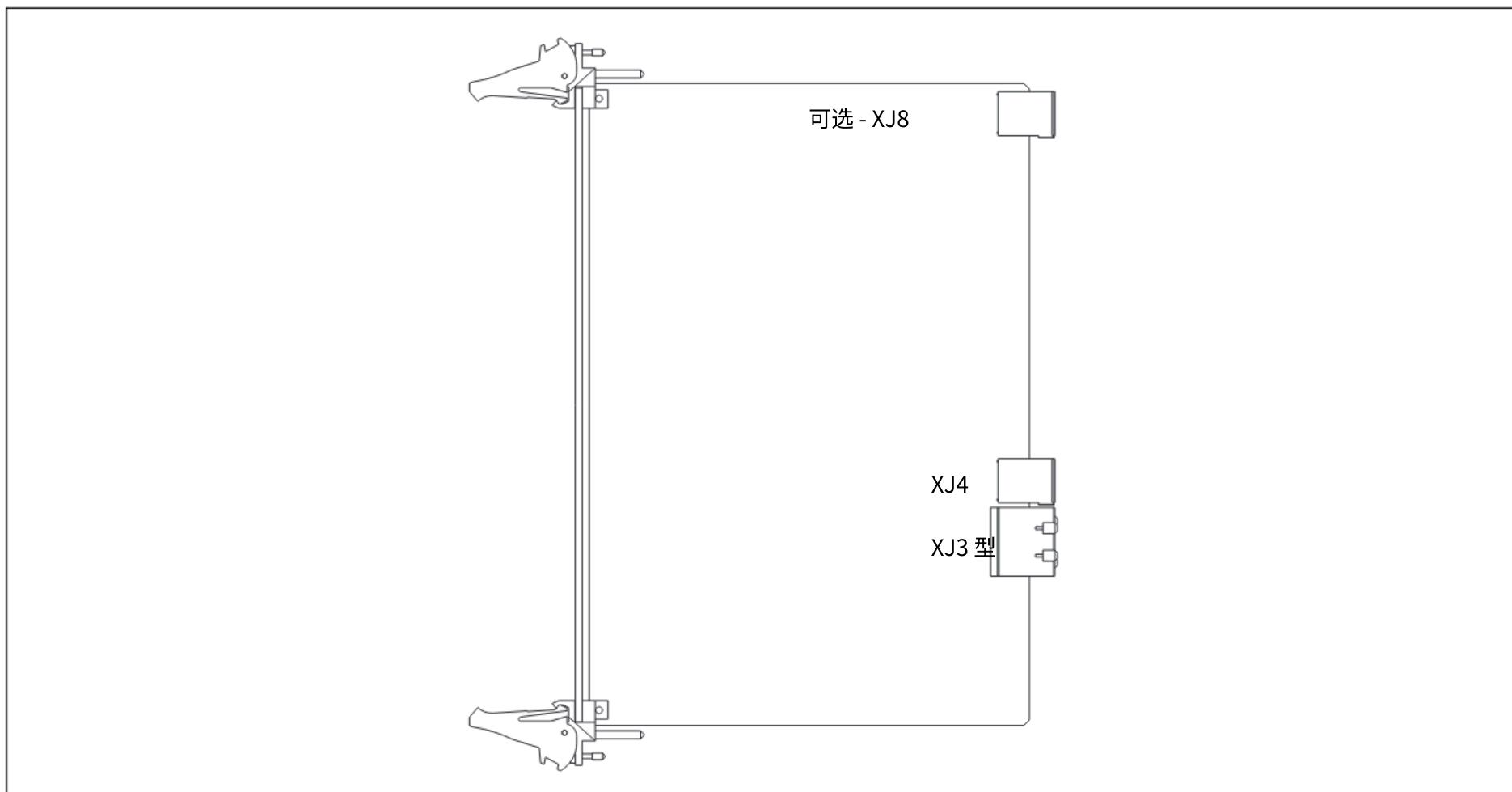


图 2-6.6U PXI Express 外设模块

2. PXI Express Architecture Overview

Figures 2-7 and 2-8 show the 3U and 6U PXI Express Peripheral Slots, respectively.

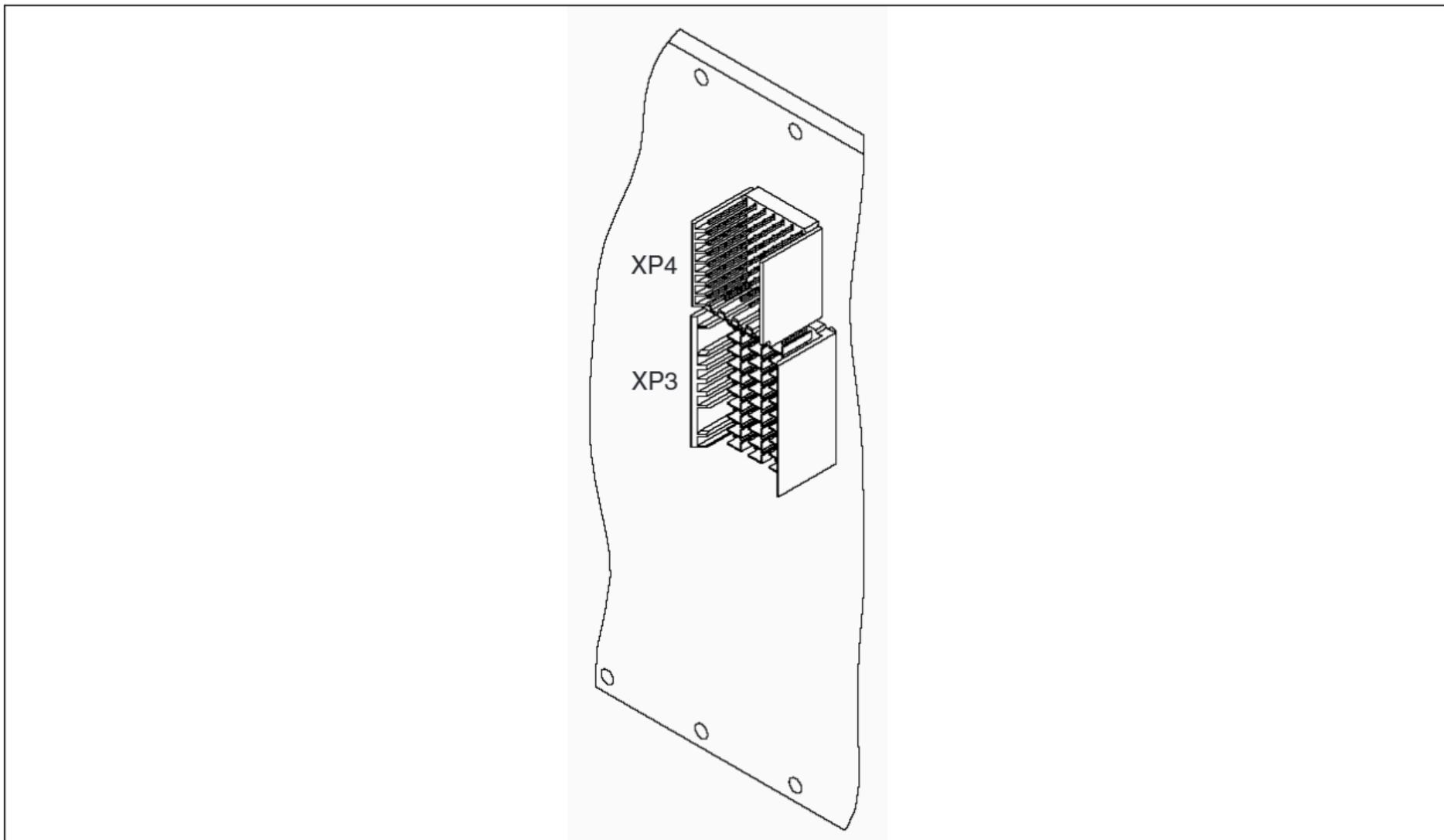


Figure 2-7. 3U PXI Express Peripheral Slot



2. PXI Express 架构概述

图 2-7 和 2-8 分别显示了 3U 和 6U PXI Express 外设插槽。

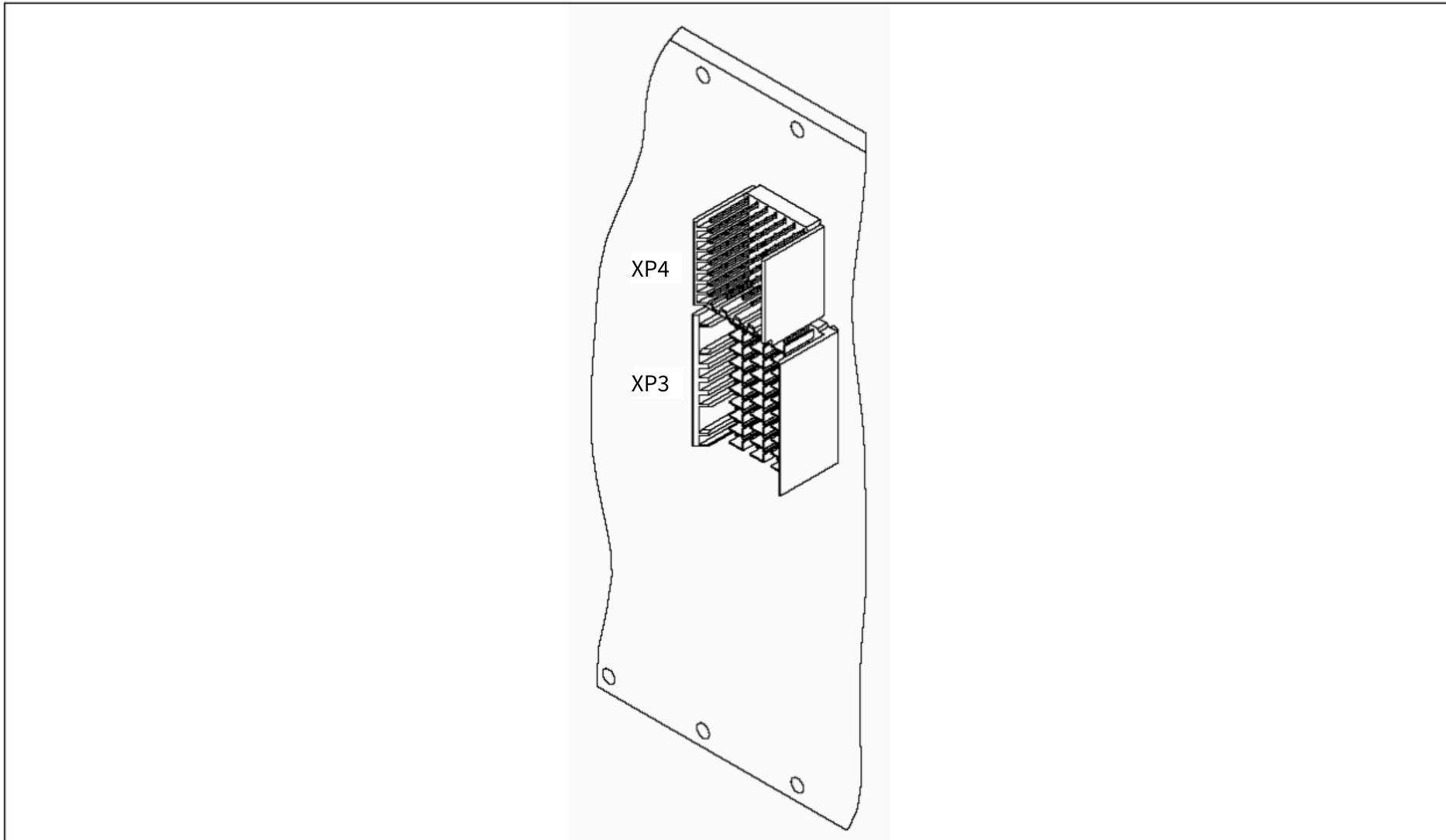


图 2-7.3U PXI Express 外设插槽



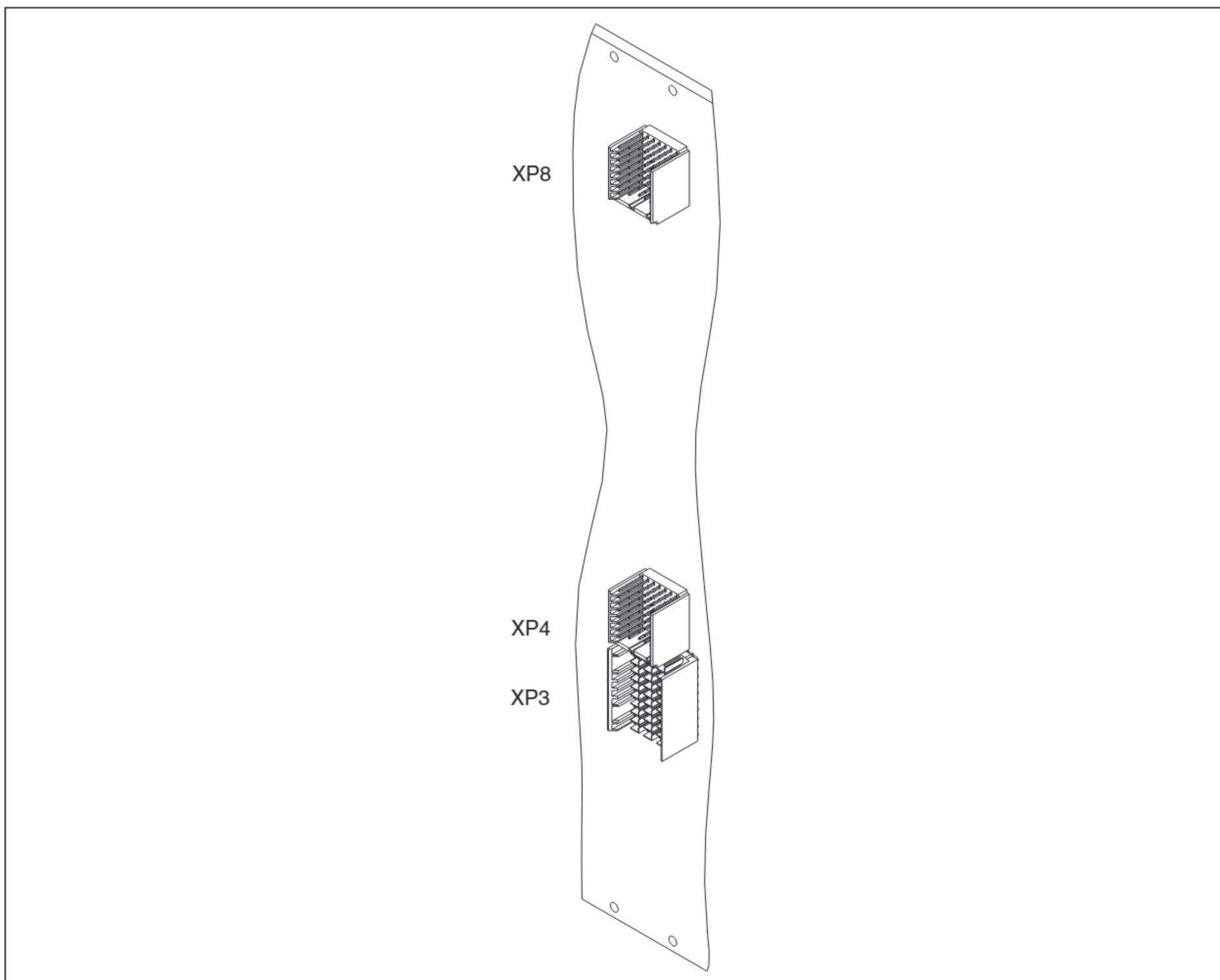


Figure 2-8. 6U PXI Express Peripheral Slot

2.1.1.3 3U and 6U PXI Express Hybrid Peripheral Slot

3U Hybrid Peripheral Slots have three connectors: P1, XP3, and XP4. A simplified description of the connector functionality is that P1/J1 are for 32 bit PCI, XP3/XJ3 are for PCI Express and Differential Triggers and Timing, and XP4/XJ4 is for instrumentation signals defined in the PXI-1 specification. 6U Hybrid Peripheral Slots have four connectors: P1, XP3, XP4, and XP8. P3, P4, and P5 are not allowed.

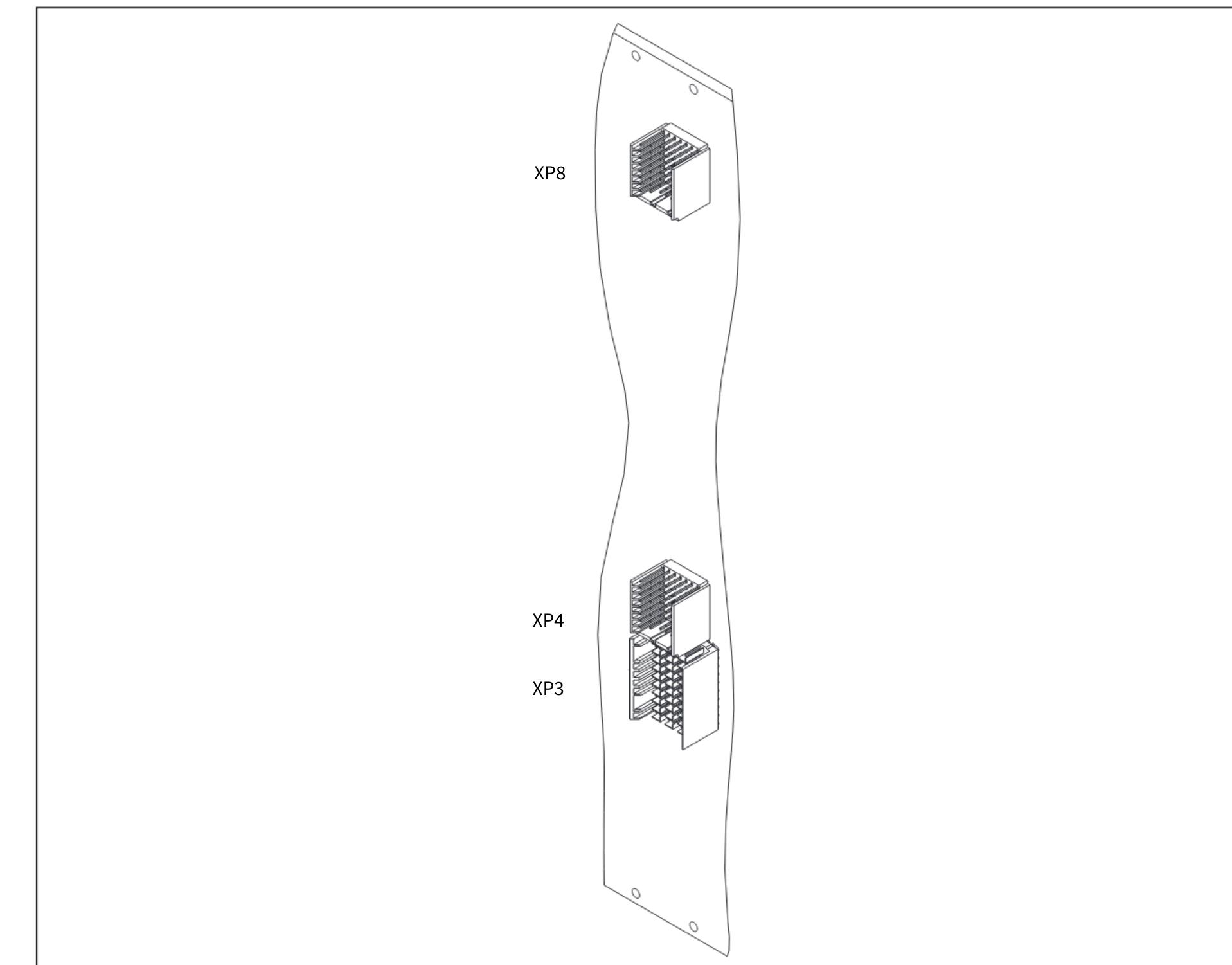


图 2-8.6U PXI Express 外设插槽

2.1.1.3 3U 和 6U PXI Express 混合外设插槽

3U 混合外设插槽具有三个连接器：P1、XP3 和 XP4。连接器功能的简化描述是，P1/J1 用于 32 位 PCI，XP3/XJ3 用于 PCI Express 和差分触发和定时，XP4/XJ4 用于 PXI-1 规范中定义的仪器信号。6U 混合外设插槽有四个连接器：P1、XP3、XP4 和 XP8。不允许使用 P3、P4 和 P5。

2. PXI Express Architecture Overview

Figures 2-9 and 2-10 show the 3U and 6U PXI Express Hybrid Slots, respectively.

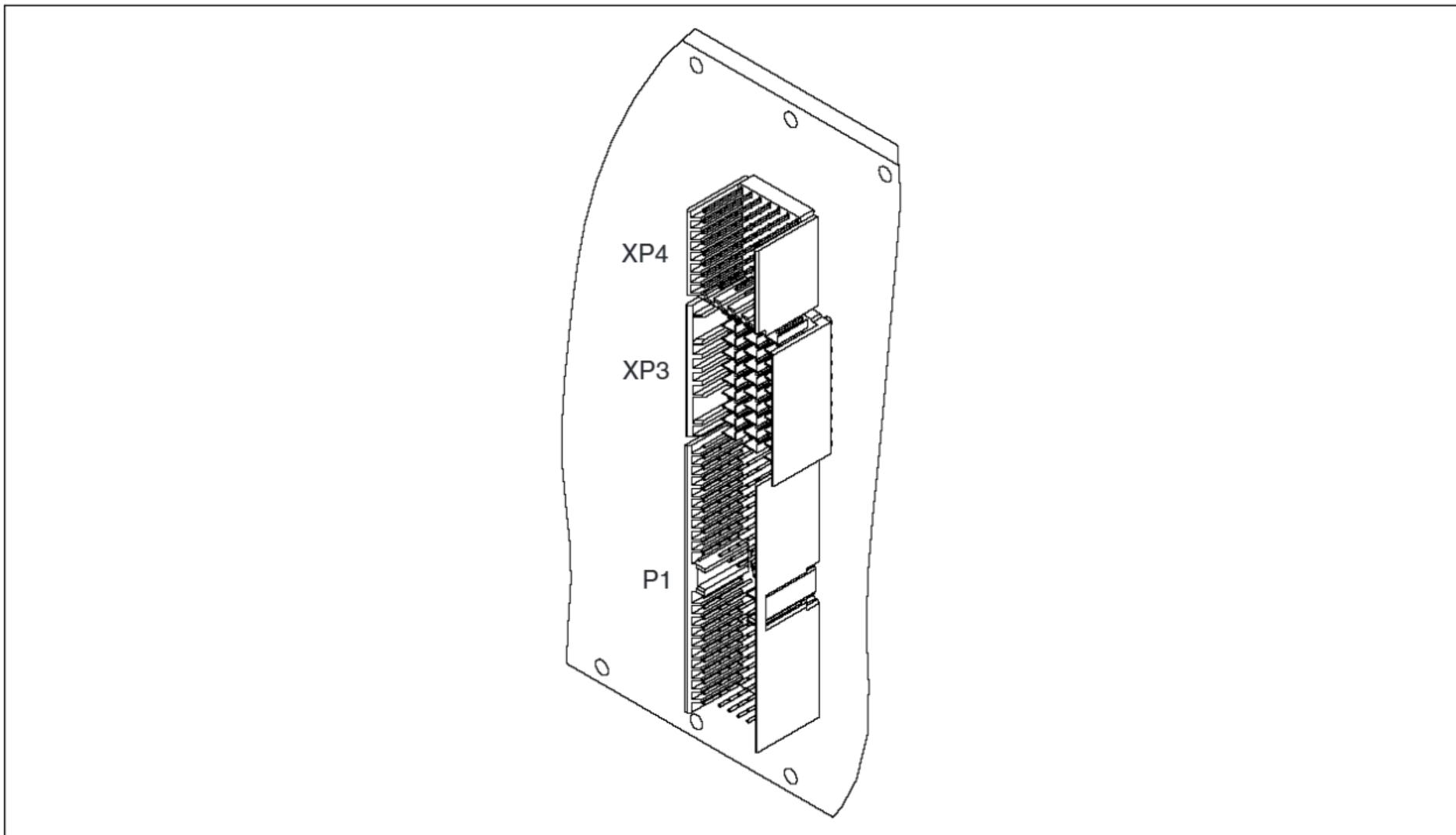


Figure 2-9. 3U PXI Express Hybrid Peripheral Slot



2. PXI Express 架构概述

图 2-9 和 2-10 分别显示了 3U 和 6U PXI Express 混合插槽。

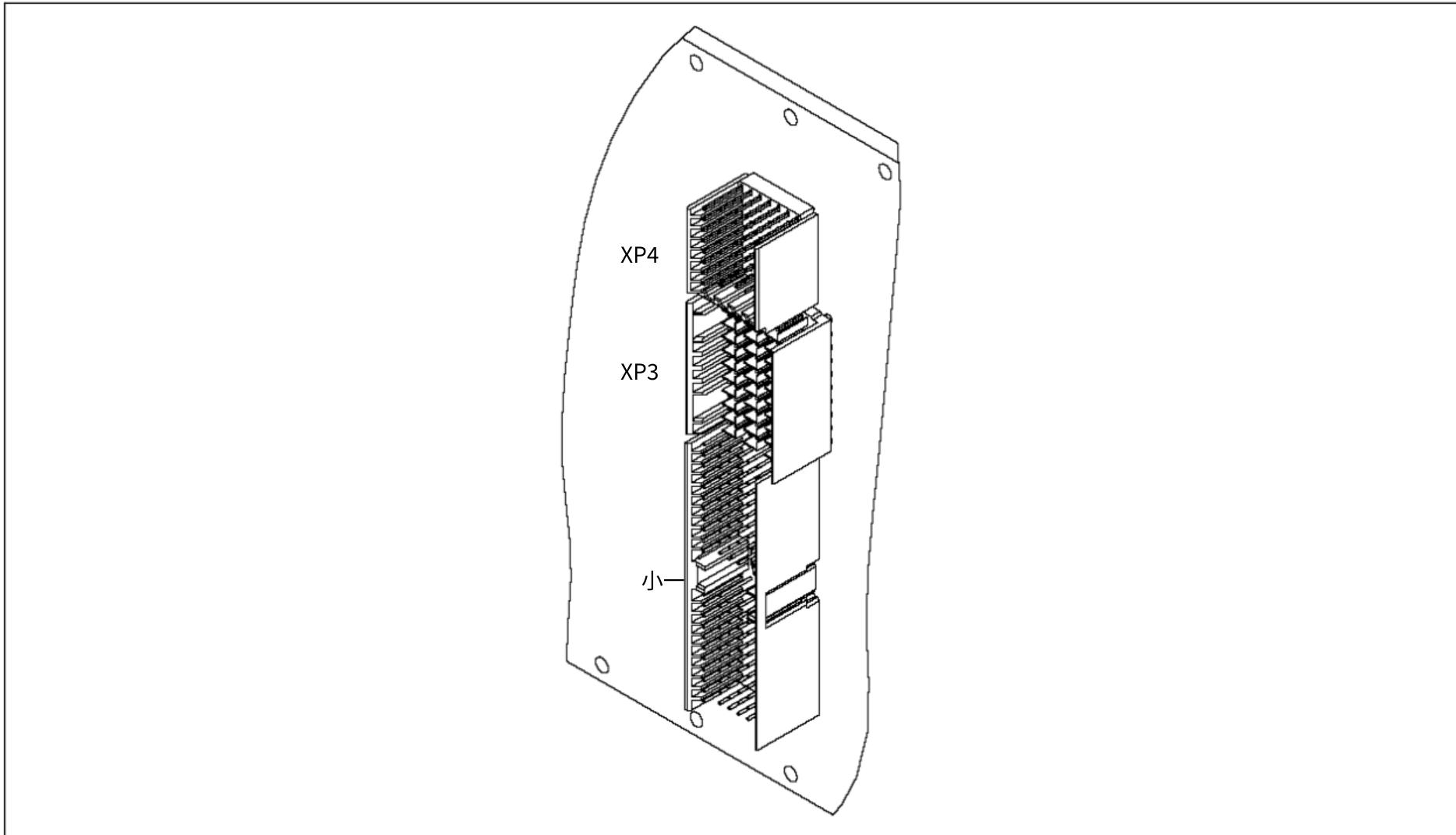


图 2-9.3U PXI Express 混合外设插槽



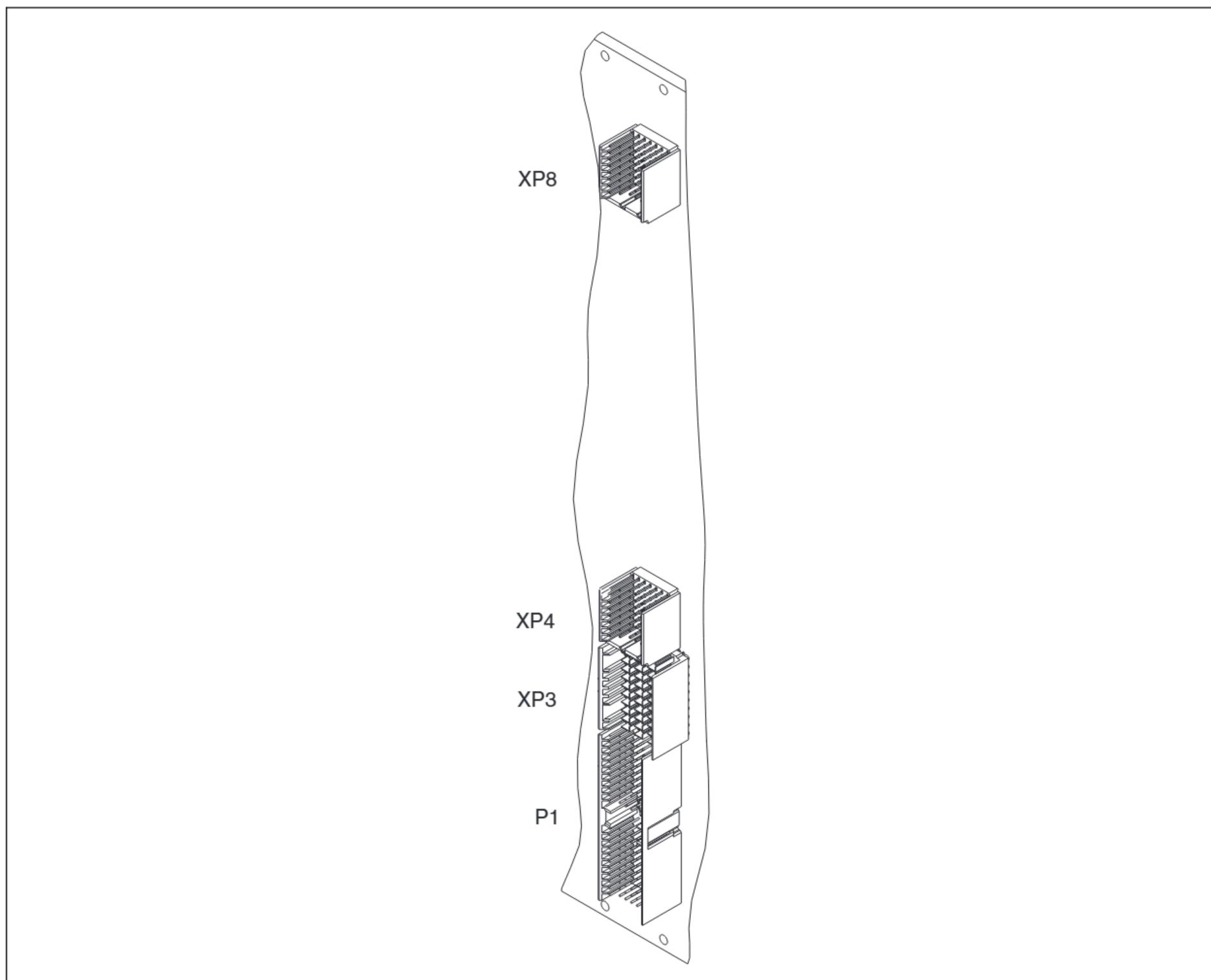


Figure 2-10. 6U PXI Express Hybrid Peripheral Slot

2.1.1.4 3U and 6U PXI Express System Timing Module and Slot

PXI Express introduces new 3U and 6U Modules called a System Timing Module. It also introduces the associated slots for 3U and 6U called a System Timing Slot.

The 3U System Timing Module has four connectors, TJ1, TJ2, XJ3 and XJ4, as shown in Figure 2-11. A simplified description of the connector functionality is TJ1/TP1 and TJ2/TP2 are for fanout of the Differential and Star Triggers, XP3/XJ3 are for PCI Express and Differential Triggers and Timing, and XP4/XJ4 is for instrumentation signals that are defined in the PXI-1 specification.

The 3U Slot has three required connectors: TP2, XP3, and XP4. TP1 is Optional for backplanes that have seven or fewer slots requiring differential triggers.

A 6U System Timing Module has the same connectors as the 3U Timing Module, plus the Optional XJ8 connector for additional power.

A 6U System Timing Module designed for 6U Chassis that support stacking 3U Modules with more than 18 Slots has the additional TJ5 and TJ6 connectors. This allows the 6U System Timing Module to connect to additional triggers.

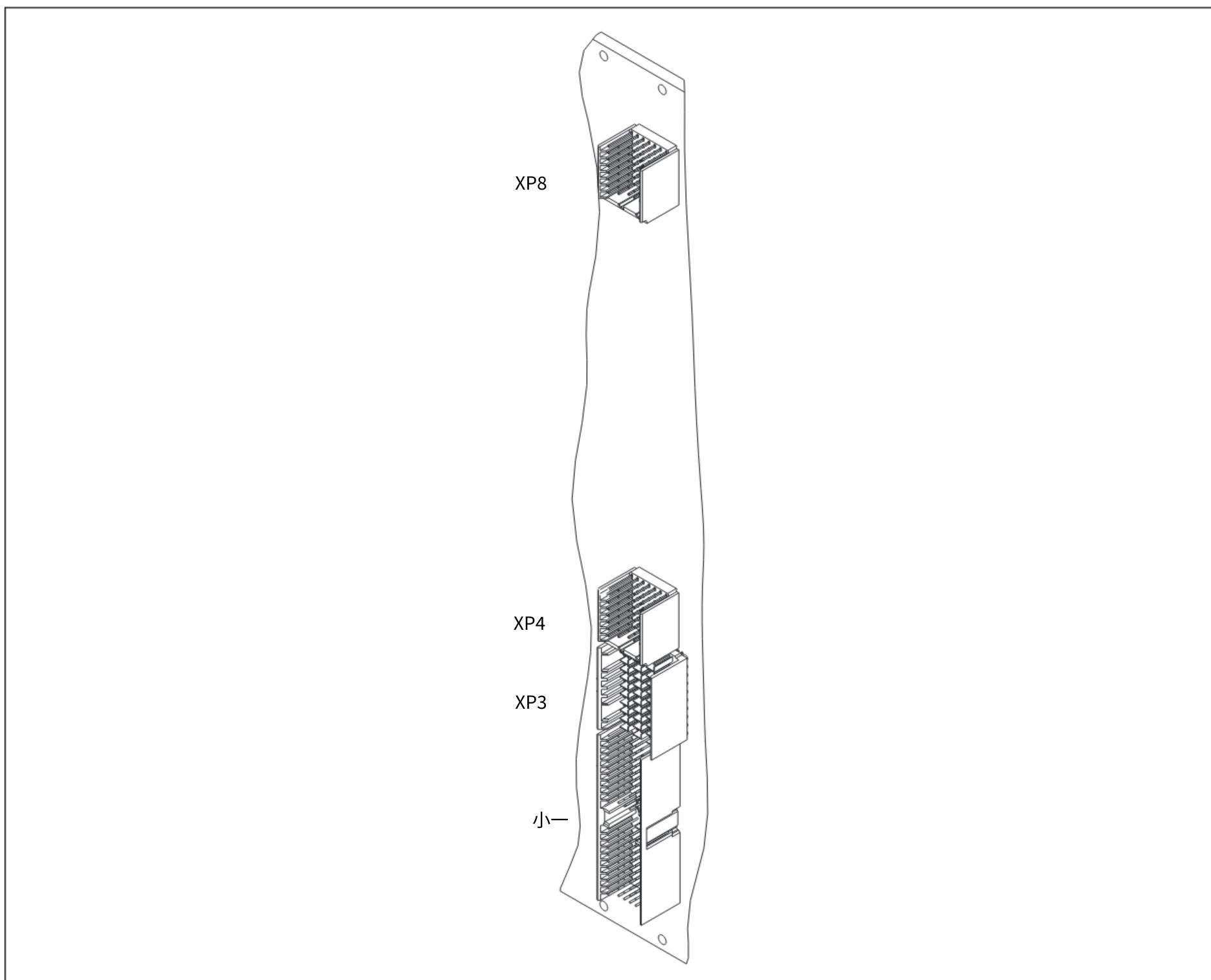


图 2-10.6U PXI Express 混合外设插槽

2.1.1.4 3U 和 6U PXI Express 系统时序模块和插槽

PXI Express 推出了新的 3U 和 6U 模块，称为系统时序模块。它还引入了 3U 和 6U 的相关插槽，称为系统时序插槽。

3U 系统定时模块有四个连接器，TJ1、TJ2、XJ3 和 XJ4，如图 2-11 所示。连接器功能的简化描述是 TJ1/TP1 和 TJ2/TP2 用于差分触发器和星形触发器的扇出，XP3/XJ3 用于 PCI Express 和差分触发和定时，XP4/XJ4 用于 PXI-1 规范中定义的仪器信号。

3U 插槽有三个必需的连接器：TP2、XP3 和 XP4。TP1 对于具有七个或更少插槽且需要差分触发器的背板是可选的。

6U 系统定时模块具有与 3U 定时模块相同的连接器，以及用于额外电源的可选 XJ8 连接器。

专为 6U 机箱设计的 6U 系统定时模块支持堆叠具有 18 个以上插槽的 3U 模块，具有额外的 TJ5 和 TJ6 连接器。这允许 6U 系统定时模块连接到其他触发器。

2. PXI Express Architecture Overview

A 6U System Timing Slot that does not allow stacking 3U System Timing Modules has four required connectors: TP2, XP3, XP4, and XP8. TP1 is Optional for backplanes with seven or fewer slots requiring differential triggers.

A 6U System Timing Slot that supports stacking 3U System Timing Modules has seven required connectors: TP1, TP2, XP3, XP4, upper TP2, upper XP3, and upper XP4. The upper TP1 connector is Optional for backplanes with 24 or fewer slots requiring differential triggers.

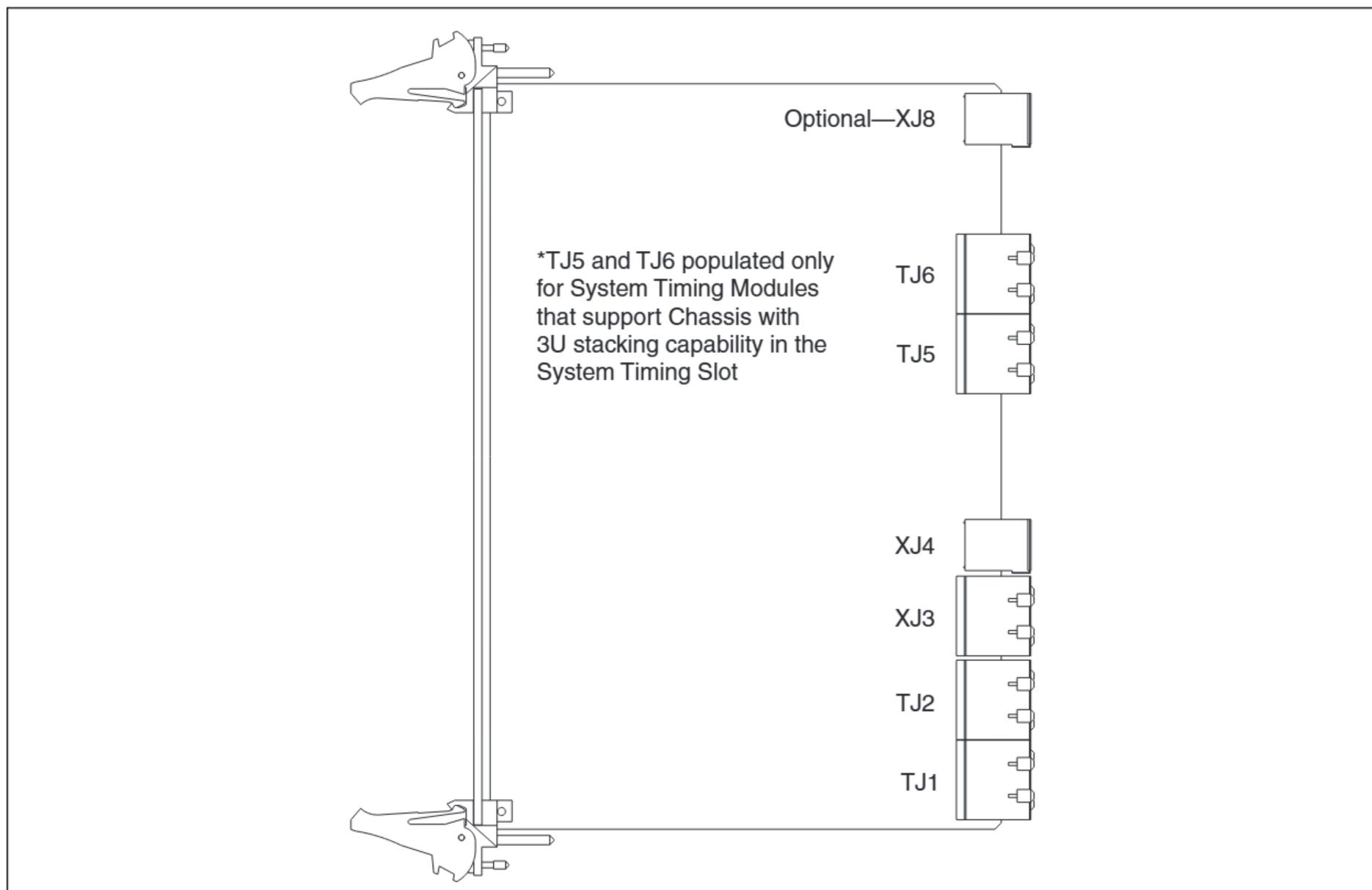


Figure 2-11. 6U PXI Express System Timing Module

2. PXI Express 架构概述

不允许堆叠 3U 系统时序模块的 6U 系统时序插槽有四个必需的连接器：TP2、XP3、XP4 和 XP8。TP1 对于需要差分触发器的七个或更少插槽的背板是可选的。

支持堆叠 3U 系统时序模块的 6U 系统时序插槽有七个必需的连接器：TP1、TP2、XP3、XP4、上 TP2、上 XP3 和上 XP4。对于需要差分触发器的 24 个或更少插槽的背板，上部 TP1 连接器是可选的。

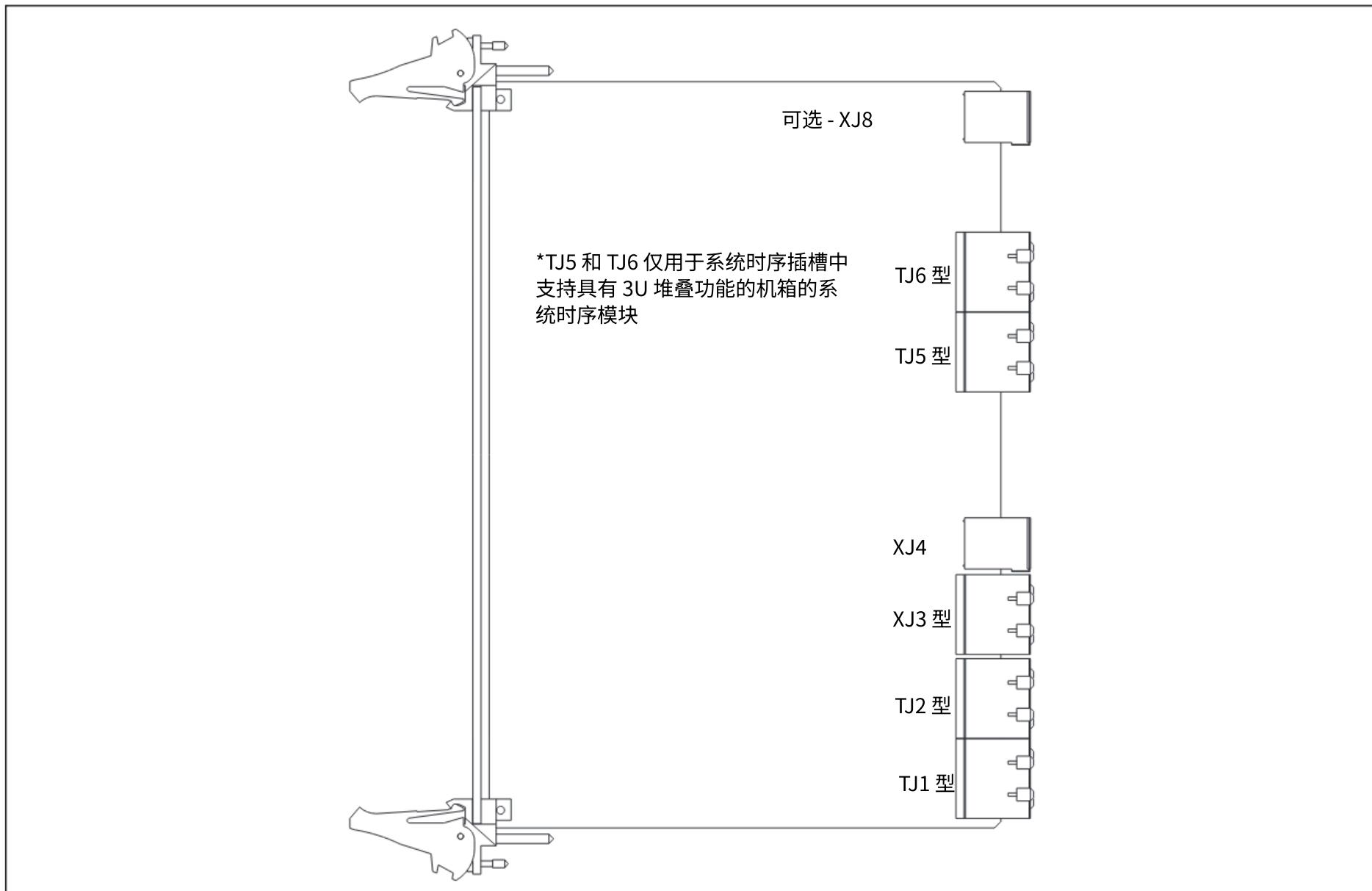


图 2-11.6U PXI Express 系统时序模块



The 3U PXI Express System Timing Slot is shown in Figure 2-12.

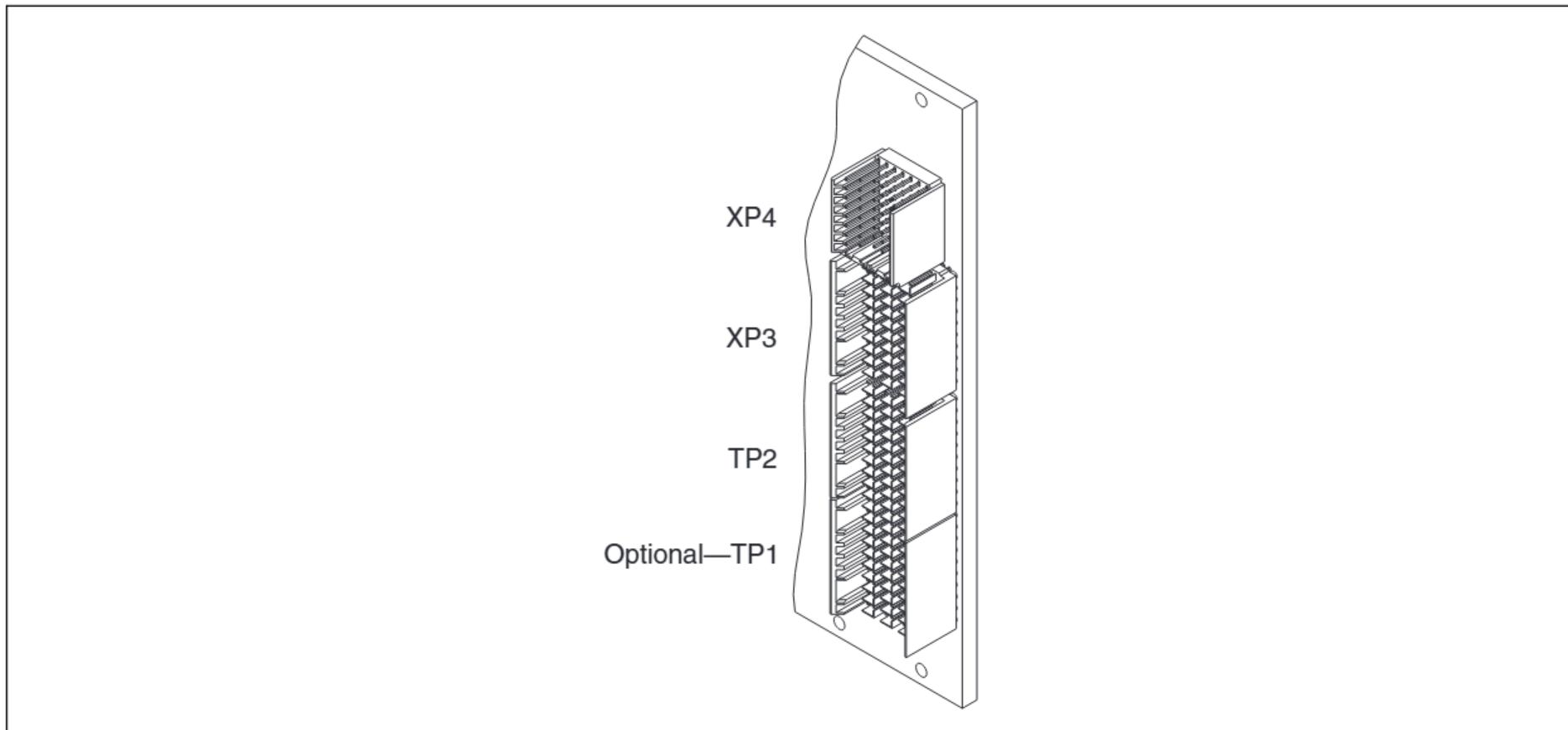


Figure 2-12. 3U PXI Express System Timing Slot

The 6U Timing Module Slot is shown in Figures 2-13 and 2-14.

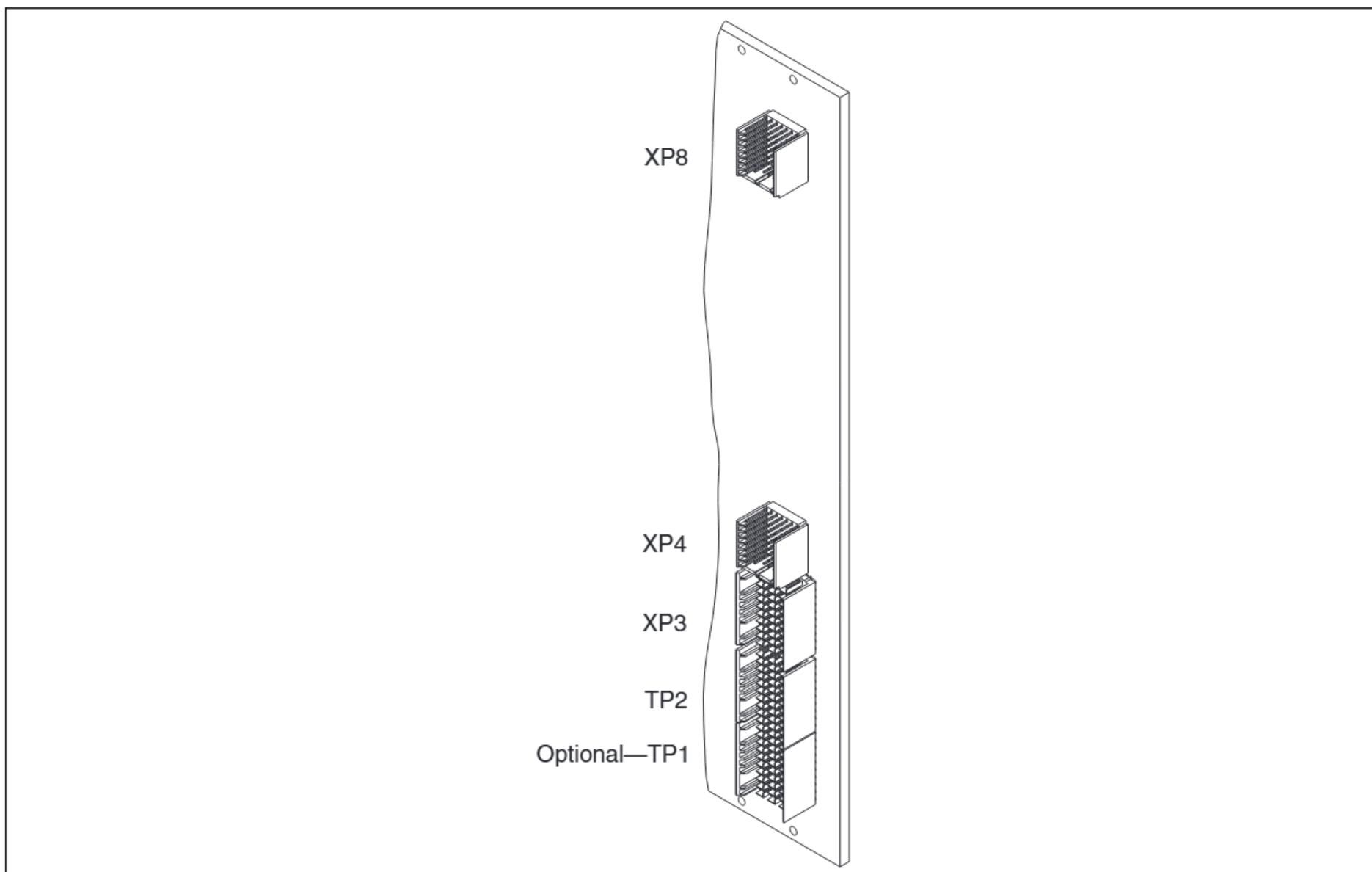


Figure 2-13. 6U PXI Express System Timing Slot



3U PXI Express 系统时序插槽如图 2-12 所示。

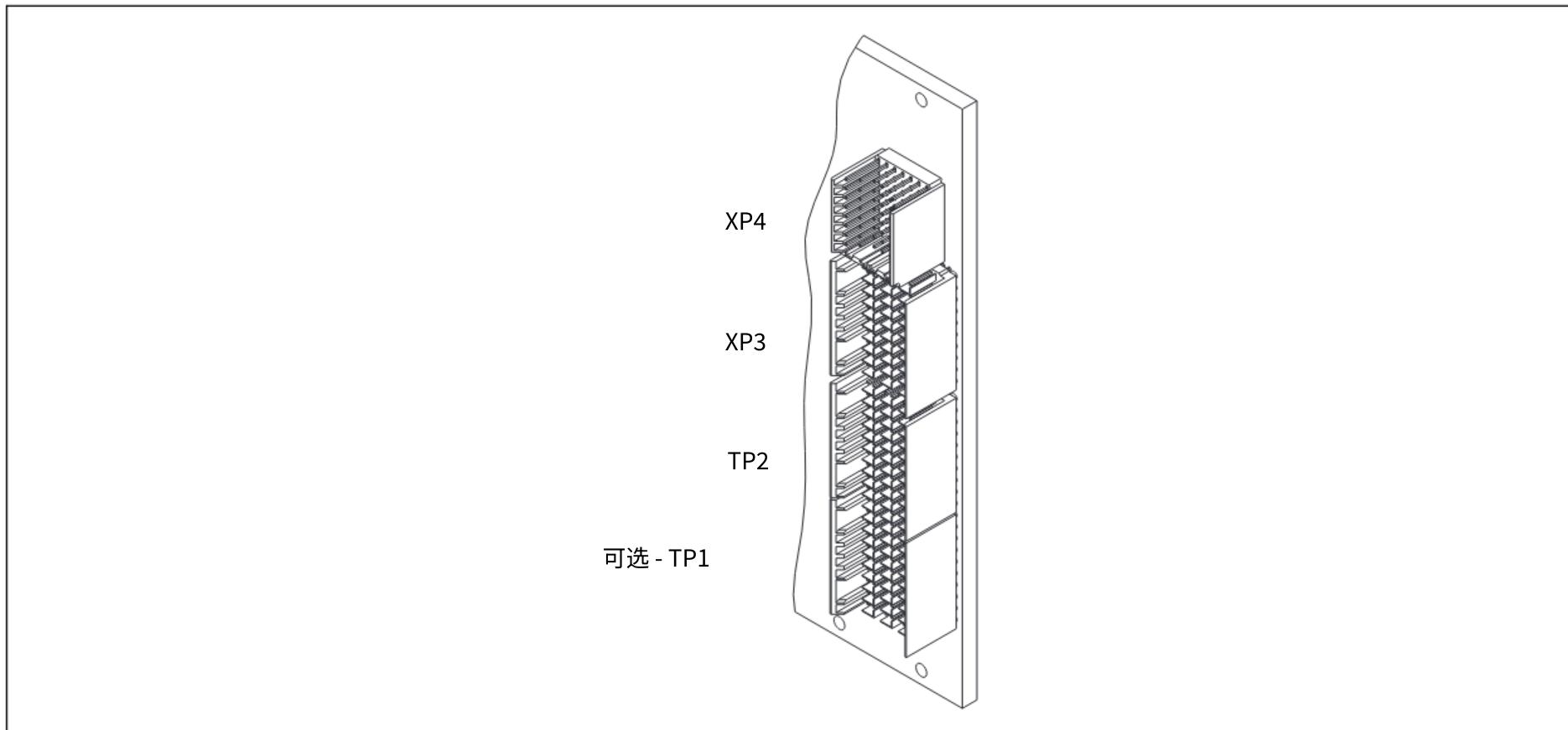


图 2-12.3U PXI Express 系统时序插槽

6U 定时模块插槽如图 2-13 和 2-14 所示。

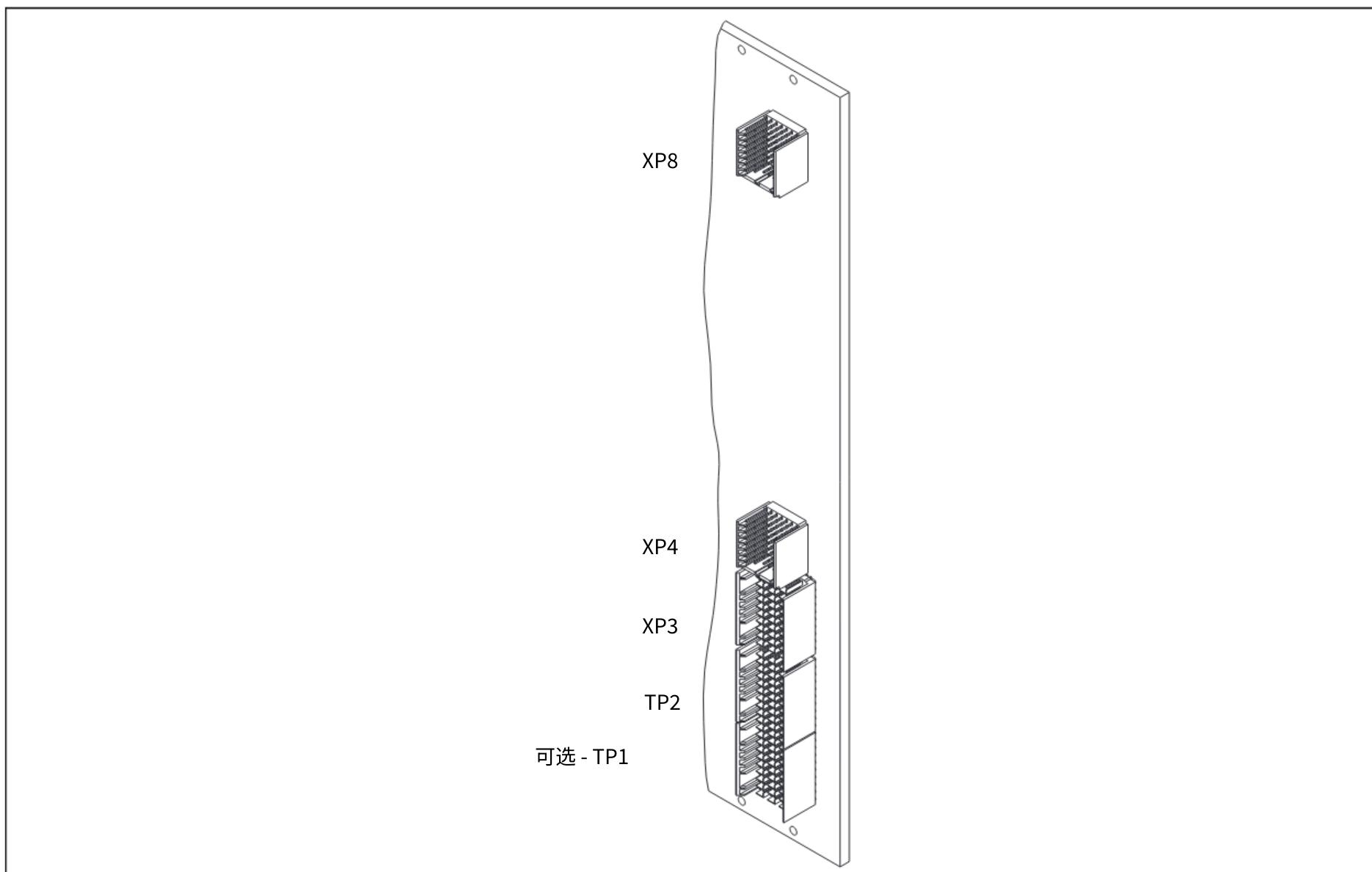


图 2-13.6U PXI Express 系统时序插槽

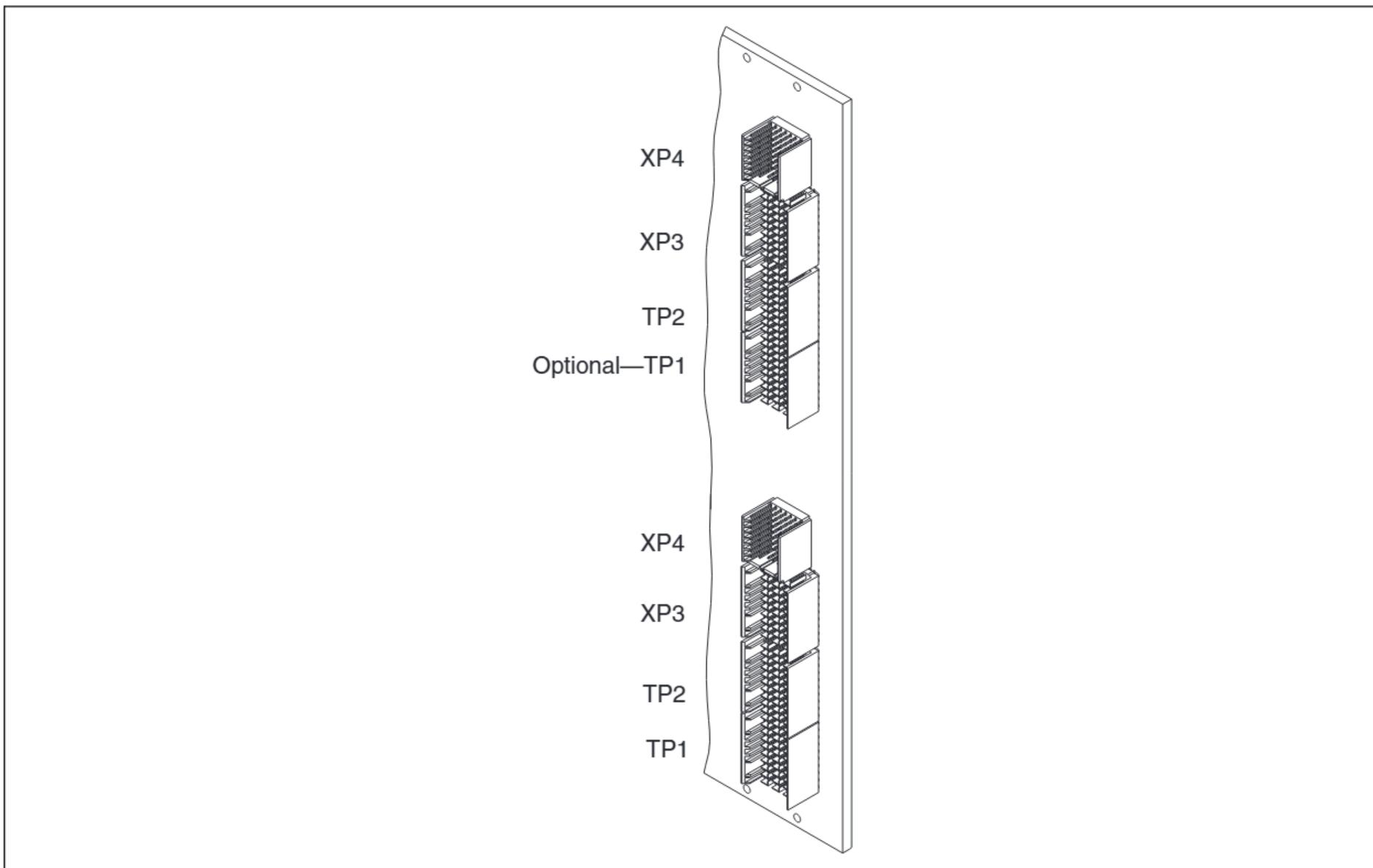


Figure 2-14. 6U PXI Express System Timing Slot with Stacked 3U Support

2.1.1.5 PXI-1 Slot



In a PXI Express Chassis, there may be slots that support PXI boards as they are defined in PXI-1 (*PXI Hardware Specification*, Revision 2.2). These slots meet the mechanical requirements of the *PXI Hardware Specification* and are referred to as PXI-1 slots.

2.1.1.6 3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module

PXI-1 or an associated ECN defines a 3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module that consists of a 3U or 6U PXI-1 Module where the J2 HM connector has been replaced with an eHM connector. The eHM connector is a modified 2 mm HM connector that includes application keying and is installed in the same location as the upper eight columns of the PXI-1 J2 connector. This board type may be used in any PXI-1 or PXI Express Hybrid Slot. Figures 2-15 and 2-16 show the 3U and 6U Hybrid Slot Compatible PXI-1 Modules.

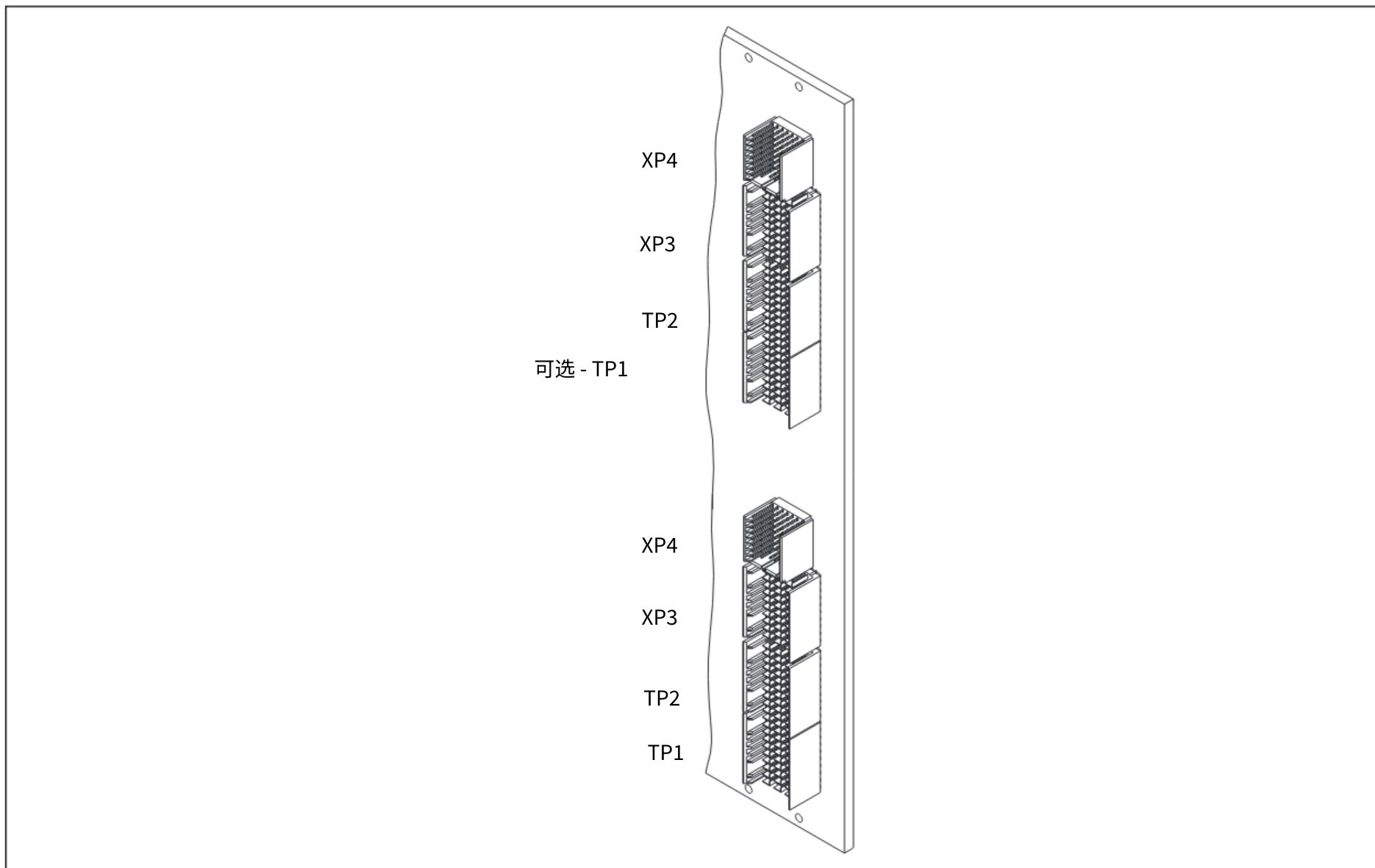


图 2-14.支持堆叠 3U 的 6U PXI Express 系统时序插槽



2.1.1.5 PXI-1 插槽

在 PXI Express 机箱中，可能存在支持 PXI-1（PXI 硬件规范，修订版 2.2）中定义的 PXI 板的插槽。这些插槽满足 PXI 硬件规范的机械要求，称为 PXI-1 插槽。

2.1.1.6 兼容 3U 和 6U 混合插槽的 PXI-1 外设模块

PXI-1 或相关 ECN 定义了一个 3U 和 6U 混合插槽兼容 PXI-1 外设模块，该模块由一个 3U 或 6U PXI-1 模块组成，其中 J2 HM 连接器已替换为 eHM 连接器。eHM 连接器是一个改进的 2 mm HM 连接器，包括应用程序键控，安装在与 PXI-1 J2 连接器的上八列相同的位置。此板类型可用于任何 PXI-1 或 PXI Express 混合插槽。图 2-15 和 2-16 显示了 3U 和 6U 混合插槽兼容的 PXI-1 模块。

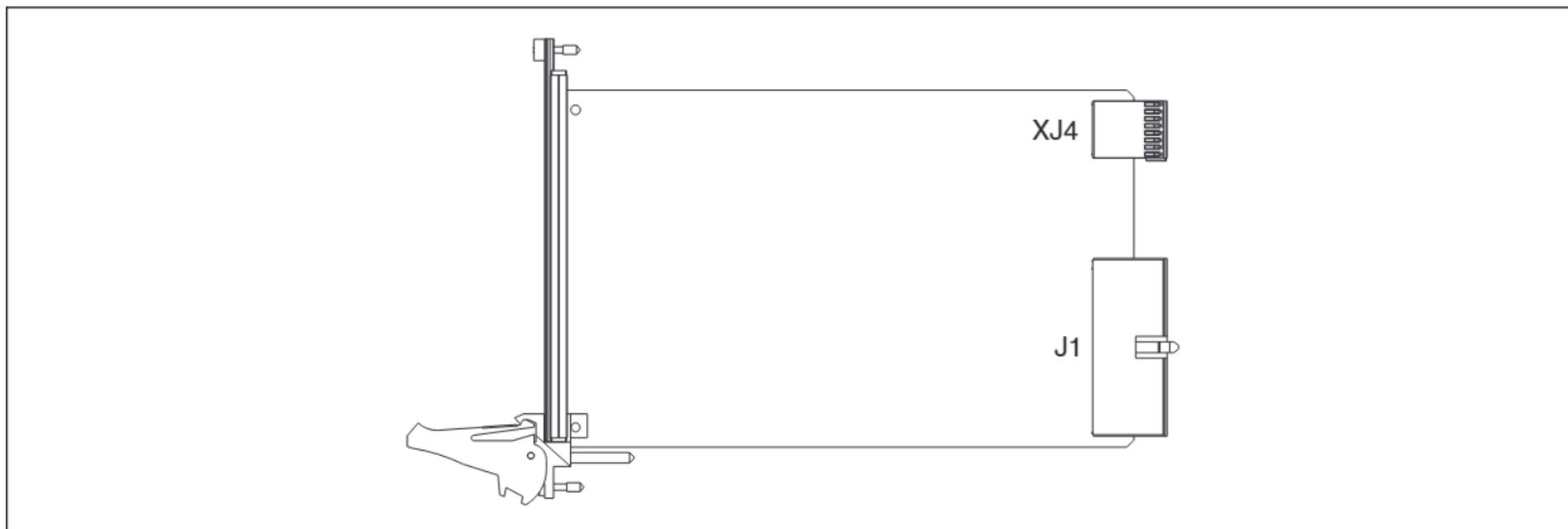


Figure 2-15. 3U Hybrid Peripheral Slot Compatible PXI-1 Module

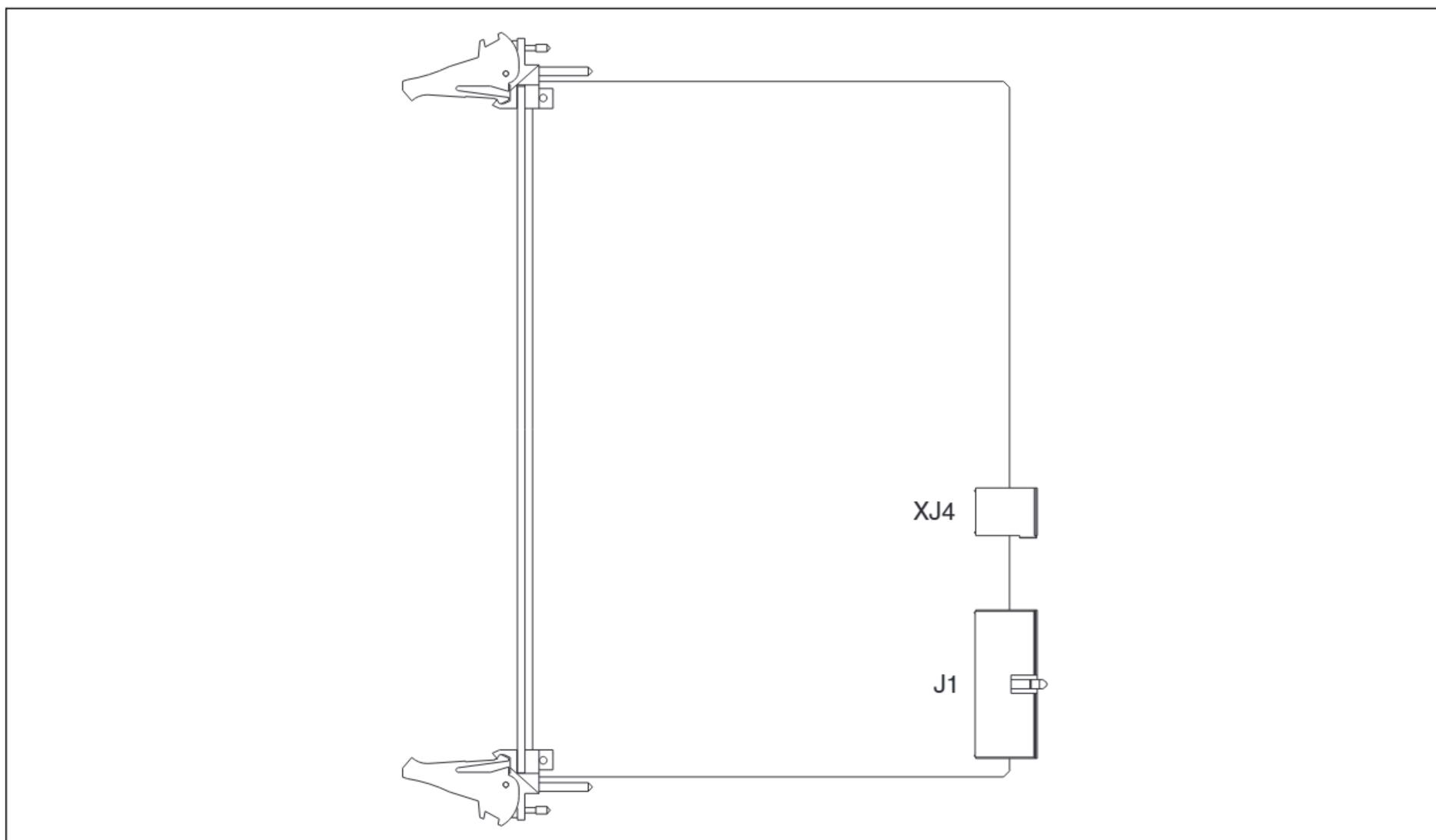


Figure 2-16. 6U Hybrid Peripheral Slot Compatible PXI-1 Module

2.1.2 System Slot and System Timing Module Location

PXI Express defines the System Slot location to be the furthest left slot within a Chassis and to be numbered Slot 1. This defined arrangement is a subset of the numerous possible configurations allowed by CompactPCI Express (a CompactPCI Express System Slot may be located anywhere on a backplane). Defining a single location for the System Slot simplifies integration and increases the degree of compatibility between PXI Express Controllers and Chassis. Furthermore, the *PXI Express Hardware Specification* requires that, if necessary, the System Module should expand to the left into what are defined as Controller expansion slots. Expanding to the left prevents System Modules from using up valuable Peripheral Slots.

Some PXI Express Chassis may integrate the System Module functionality within the Chassis. In such a system, a System Slot is not required, and Peripheral Slots begin their numbering with 2.

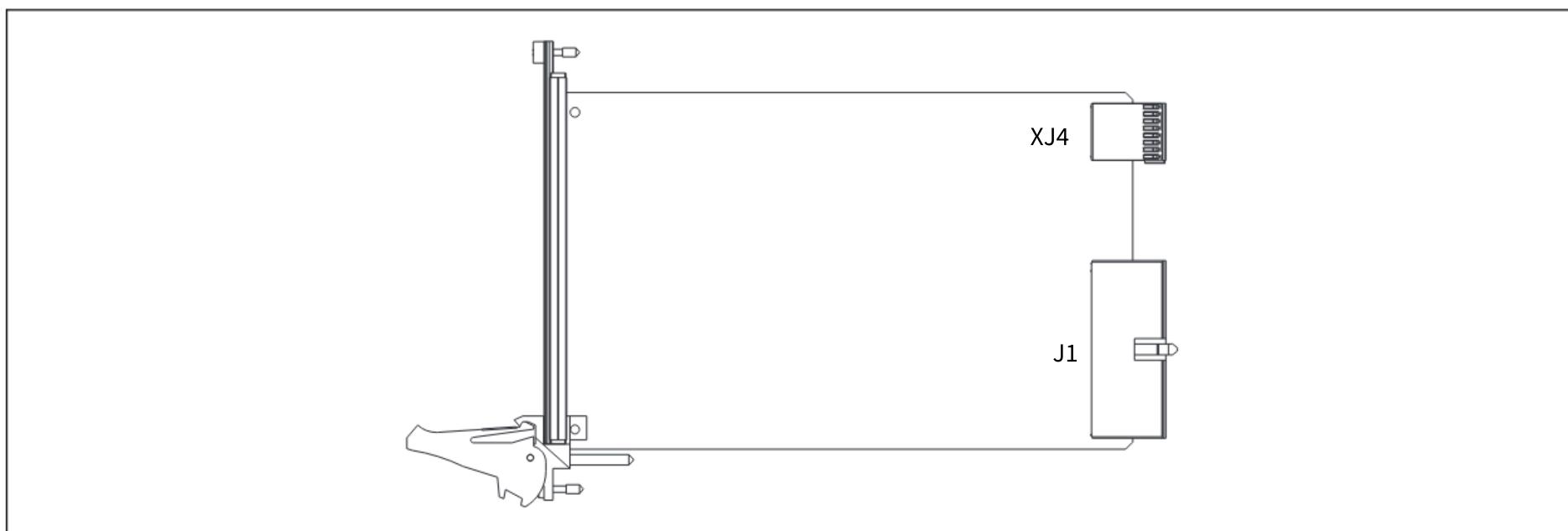


图 2-15.3U 混合外设插槽兼容 PXI-1 模块

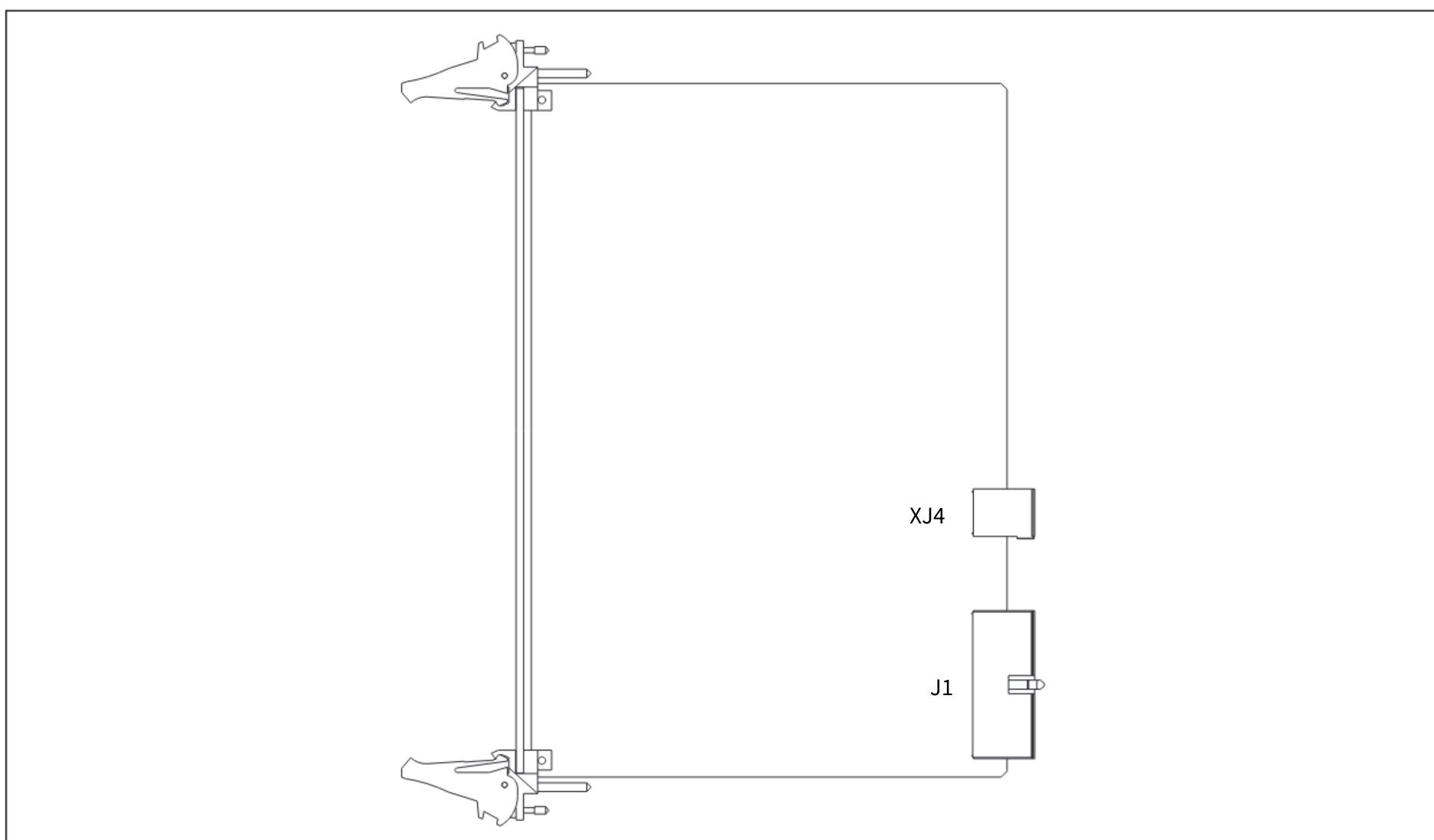


图 2-16.6U 混合外设插槽兼容 PXI-1 模块

2.1.2 系统插槽和系统时序模块位置

PXI Express 将系统插槽位置定义为机箱内最左侧的插槽，编号为插槽 1。这种定义的排列是 CompactPCI Express 允许的众多可能配置的子集（CompactPCI Express 系统插槽可以位于背板上的任何位置）。为系统插槽定义单个位置可以简化集成，并提高 PXI Express 控制器和机箱之间的兼容性程度。此外，PXI Express 硬件规范要求，如有必要，系统模块应向左扩展为定义为控制器扩展插槽。

向左展开可防止系统模块耗尽宝贵的外围设备插槽。

某些 PXI Express 机箱可能会在机箱中集成系统模块功能。在这样的系统中，不需要系统插槽，外设插槽以 2 开始编号。

PXI Express defines a System Timing Slot that can accept a PXI Express Peripheral Module or a System Timing Module that can provide individual triggers to all other Peripheral Modules and allow the replacement of the System reference clock. The location of the System Timing Slot is not mandated by the specification, which allows backplane designers to optimize the backplane for cost.

2.1.3 Additional Mechanical Features

In addition to the features defined by the PXI-1 Specification, PXI Express has added additional suggestions for cooling and for the measurement and specification of acoustic noise levels.

2.1.4 Interoperability with CompactPCI Express

Interoperability among PXI Express-compliant products and standard CompactPCI Express products is a very important feature provided by this specification and the CompactPCI Specification. Some PXI Express-compatible systems may require components that do not implement PXI Express-specific features. For example, a user may want to use a standard CompactPCI Express network interface Module in a PXI Express Chassis. Likewise, some users may choose to use a PXI Express-compatible Module in a standard CompactPCI Express Chassis. In these cases, the user cannot use PXI Express-specific Functions, but still can use the basic Module Functions.

Note that interoperability between PXI Express products and other application-specific implementations of CompactPCI Express products (which may define other signal definitions for the I/O pins of the XP4/XJ4 connectors) is not guaranteed. The CompactPCI Express specification provides mechanical keying of the XP4/XJ4 connectors for both PXI Express products and application-specific CompactPCI Express products to prevent electrical conflict between them.

2.1.5 Typical System Components

Figure 2-17 presents an example PXI Express system to help illustrate the following key words (in *italics*). A PXI Express System is composed of a *Chassis* that supports the PXI Express *backplane* and provides the means for supporting the System Controller and Peripheral *Modules*. The Chassis may have one *System Slot* and must have one or more *Peripheral Slots*. Any number of *System Expansion Slots* may be available to the left of the System Slot. The *System Timing Slot* may reside in any of the available slots to the right of Slot 1. The backplane carries the *interface connectors* (XP1,XJ2, etc.) and provides the interconnection between the Controller, Peripheral and Timing Slots.



PXI Express 定义了一个系统时序插槽，该插槽可以接受 PXI Express 外设模块或系统时序模块，该模块可以为所有其他外设模块提供单独的触发器，并允许替换系统参考时钟。规范没有规定系统时序插槽的位置，这使得背板设计人员可以优化背板的成本。

2.1.3 其他机械特性

除了 PXI-1 规范中定义的功能外，PXI Express 还增加了有关冷却以及声学噪声电平测量和规范的其他建议。

2.1.4 与 CompactPCI Express 的互作性

PXI Express 兼容产品和标准 CompactPCI Express 产品之间的互作性是本规范和 CompactPCI 规范提供的一项非常重要的功能。某些 PXI Express 兼容系统可能需要未实现 PXI Express 特定功能的组件。例如，用户可能希望在 PXI Express 机箱中使用标准 CompactPCI Express 网络接口模块。同样，某些用户可能会选择在标准 CompactPCI Express 机箱中使用 PXI Express 兼容模块。在这些情况下，用户无法使用 PXI Express 特定功能，但仍可以使用基本模块功能。

请注意，不保证 PXI Express 产品与 CompactPCI Express 产品的其他特定应用实现（可能为 XP4/XJ4 连接器的 I/O 引脚定义其他信号定义）之间的互作性。CompactPCI Express 规范为 PXI Express 产品和特定应用的 CompactPCI Express 产品提供了 XP4/XJ4 连接器的机械键控，以防止它们之间的电气冲突。

2.1.5 典型系统组件

图 2-17 提供了一个 PXI Express 系统示例，以帮助说明以下关键字（斜体）。PXI Express 系统由一个支持 PXI Express 背板的机箱组成，并提供支持系统控制器和外设模块的方法。机箱可以有一个系统插槽，并且必须有一个或多个外设插槽。系统插槽的左侧可以有任何数量的系统扩展插槽。系统时序插槽可以位于插槽 1 右侧的任何可用插槽中。背板带有接口连接器（XP1、XJ2 等），并提供控制器、外设和时序插槽之间的互连。



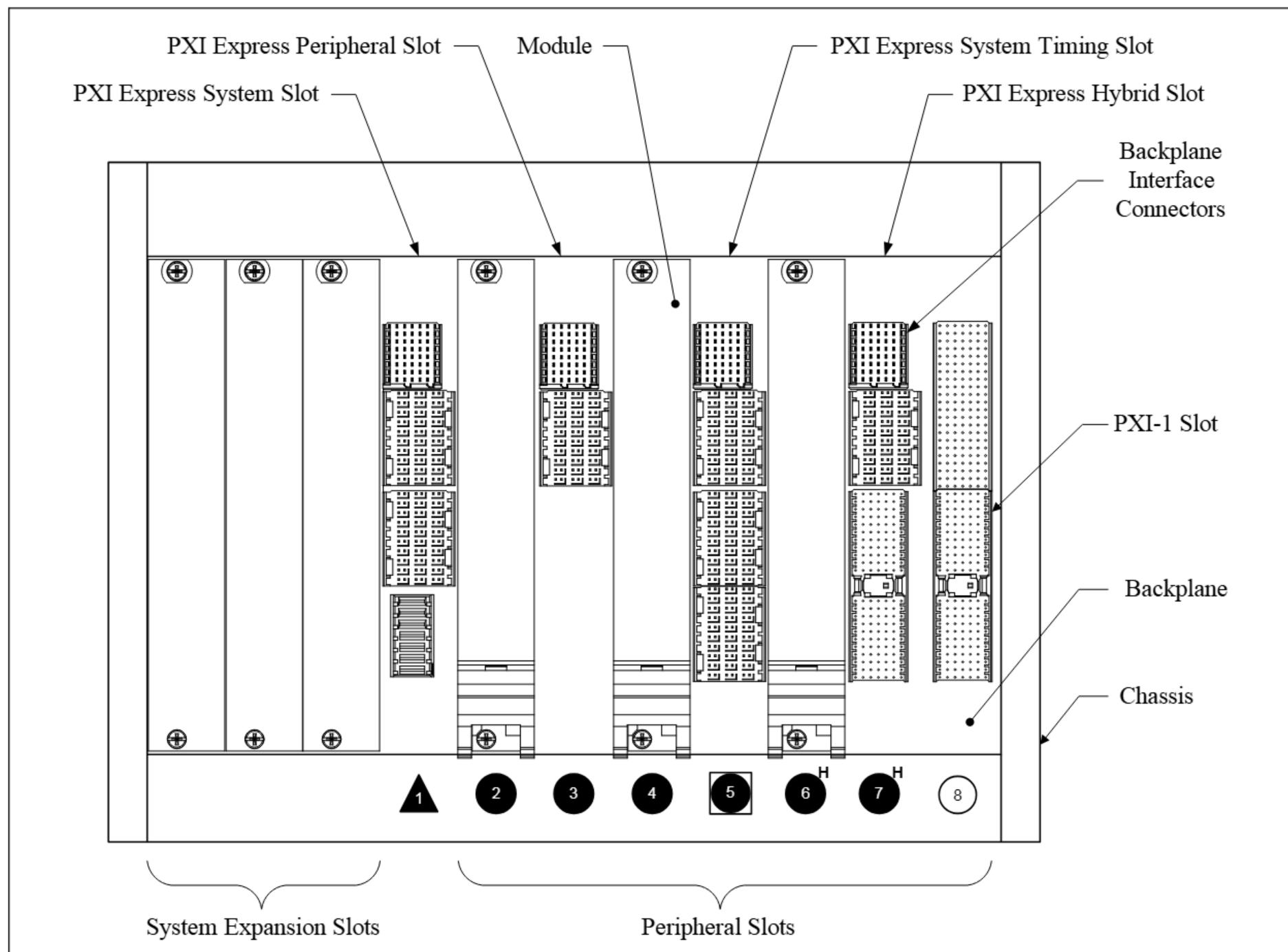


Figure 2-17. Typical System Components

2.1.6 Chassis Supporting Stacking 3U Modules in a 6U Slot

Just as with the PXI-1 Specification, PXI Express allows for efficient use of 3U Modules in a 6U Chassis. 6U PXI Express Chassis can support stacking of certain combinations of 3U Modules in a single 6U Slot. This allows one 3U Module to be plugged into the lower position of a 6U Slot, and another 3U Module to be plugged into the upper position of the same 6U Slot simultaneously. This can be accomplished mechanically using a 3U/3U adapter or using commercially available Subrack center extrusions. A 6U PXI Express Chassis may have any number of 6U Slots that support this feature. Figure 2-18 shows a general configuration of a 6U Chassis supporting 3U Module stacking. A 6U PXI Express Chassis may have any number of 6U Slots that support this feature.

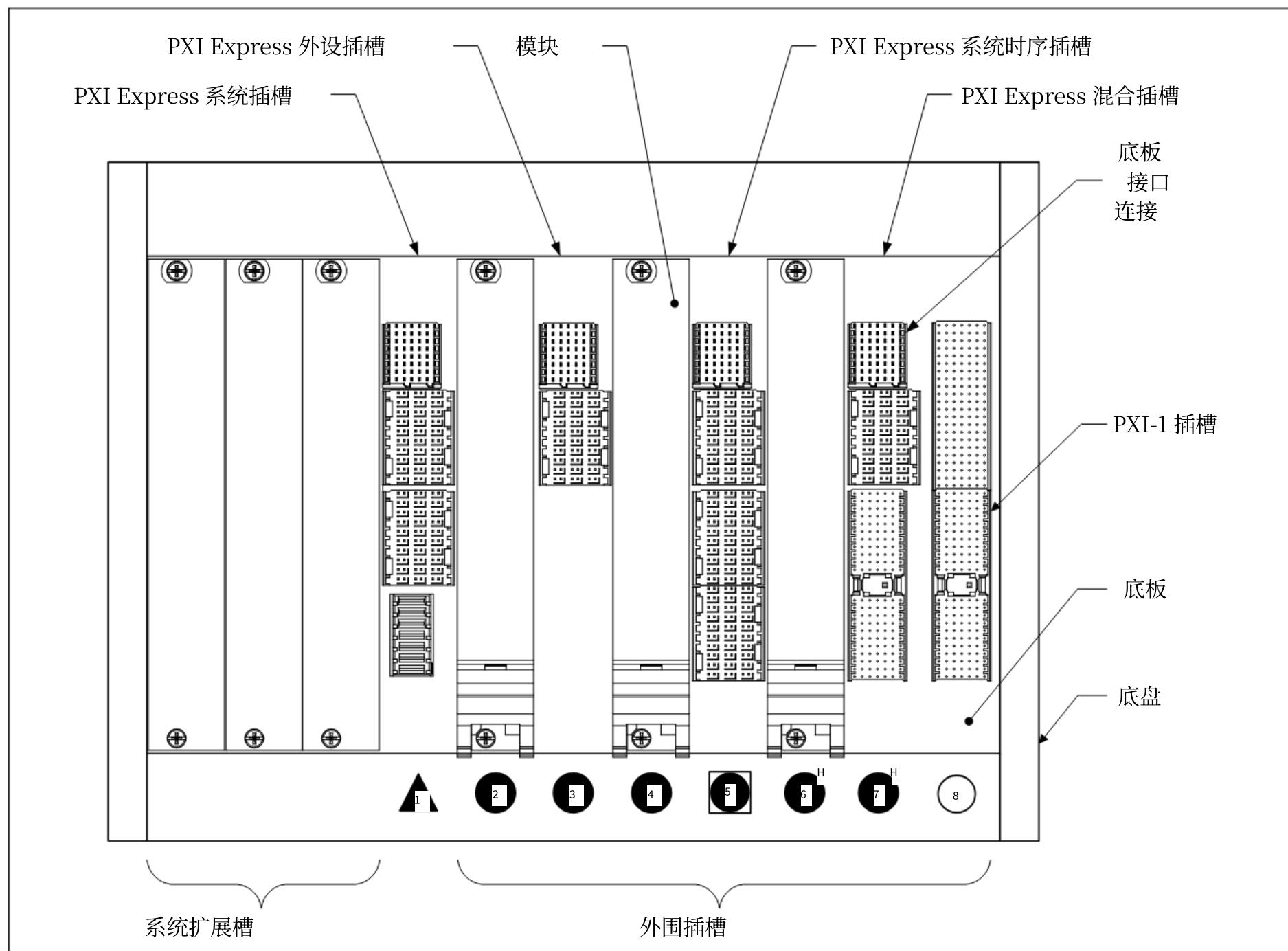


图 2-17. 典型系统组件

2.1.6 机箱支持在 6U 插槽中堆叠 3U 模块

与 PXI-1 规范一样，PXI Express 允许在 6U 机箱中高效使用 3U 模块。6U PXI Express 机箱可以支持在单个 6U 插槽中堆叠某些 3U 模块组合。这允许将一个 3U 模块插入 6U 插槽的下部位置，同时将另一个 3U 模块插入同一 6U 插槽的上部位置。这可以使用 3U/3U 适配器或使用市售的 Subrack 中心挤压件以机械方式完成。6U PXI Express 机箱可以有任意数量的支持此功能的 6U 插槽。图 2-18 显示了支持 3U 模块堆叠的 6U 机箱的一般配置。6U PXI Express 机箱可以有任意数量的支持此功能的 6U 插槽。

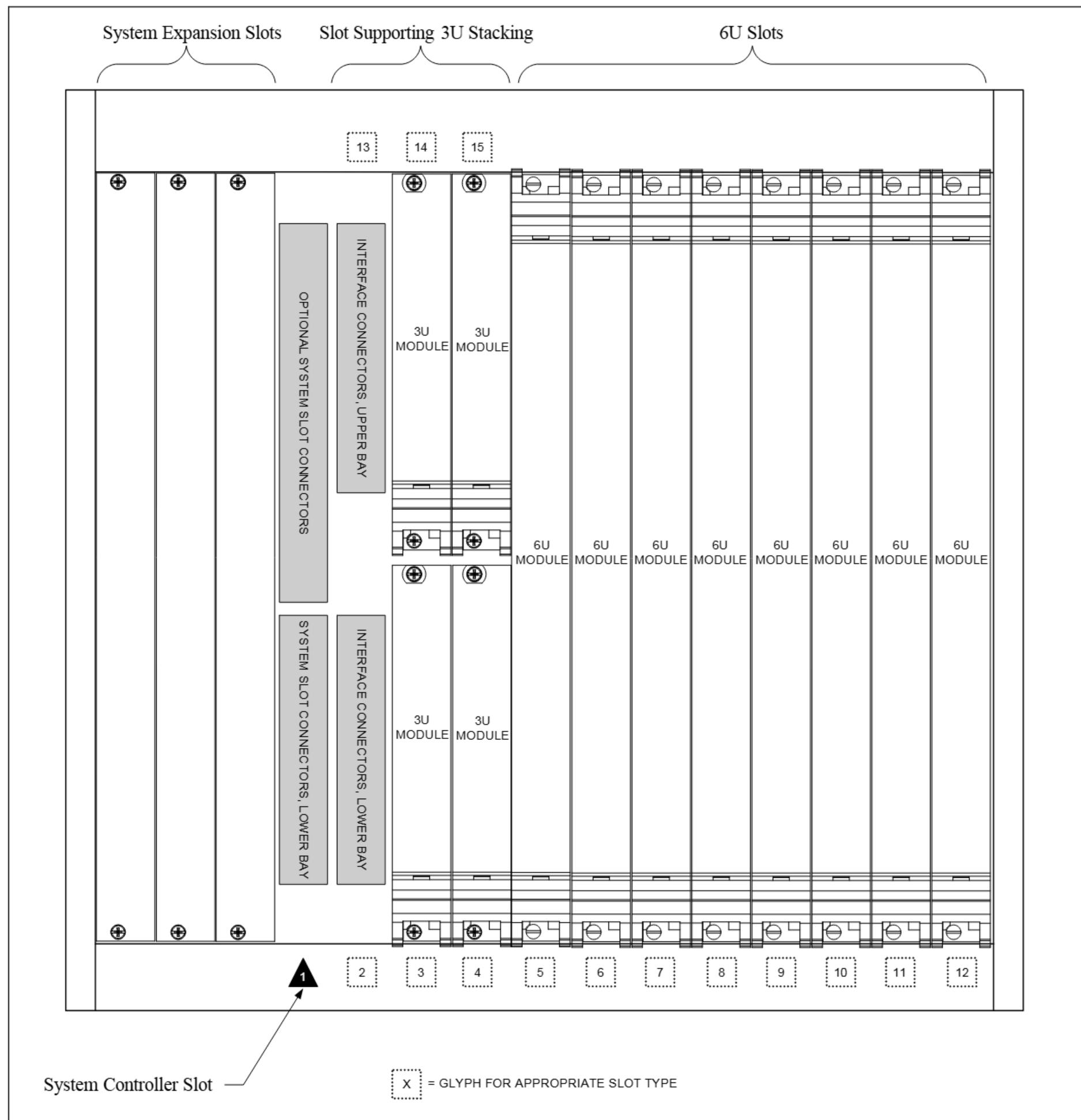


Figure 2-18. Example of a PXI Express Chassis that Supports 3U Stacking

2.2 Electrical Architecture Overview

In the same way that PXI combined instrumentation features with the desktop computer bus standard of PCI, PXI Express combines instrumentation features with the new desktop computer bus standard of PCI Express. The instrumentation features of PXI Express include many of the PXI instrumentation features, as well as a new differential 100 MHz system clock, new point-to-point differential triggers, and a new point-to-point variable frequency clock. These features are implemented on the backplane for the highest performance instrumentation timing and synchronization.

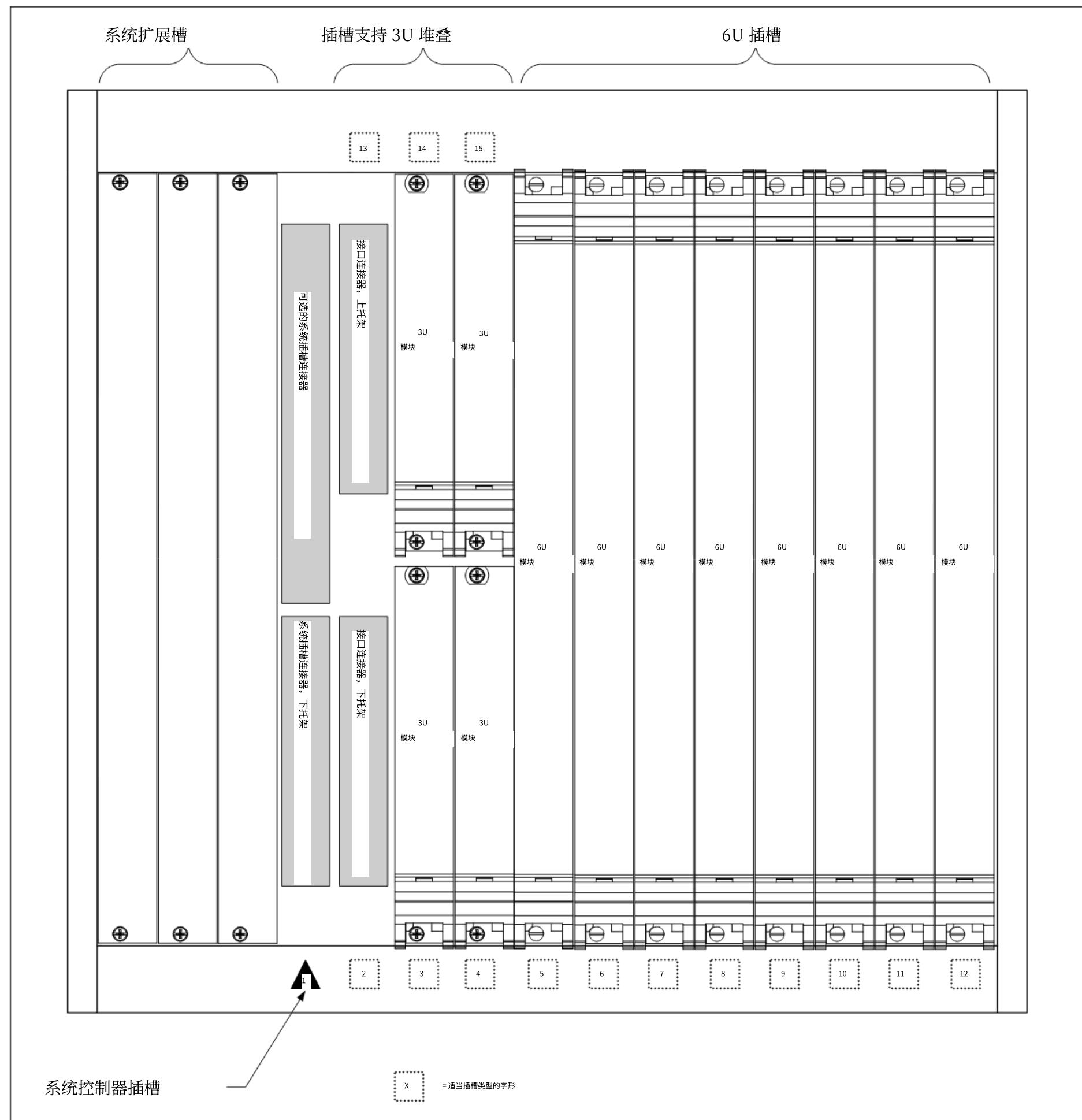


图 2-18. 支持 3U 堆叠的 PXI Express 机箱示例

2.2 电气架构概述

与 PXI 将仪器功能与 PCI 的台式计算机总线标准相结合的方式相同, PXI Express 将仪器仪表功能与 PCI Express 的新台式计算机总线标准相结合。PXI Express 的仪器仪表功能包括许多 PXI 仪器功能, 以及新的差分 100 MHz 系统时钟、新的点对点差分触发器和新的点对点变频时钟。这些功能在背板上实现, 以实现最高性能的仪器定时和同步。

2.2.1 Features Leveraged from CompactPCI Express

PCI Express is one of the main features that PXI Express leverages from CompactPCI Express. PXI Express Systems can have up to 6 GBytes/sec per direction of data moving to and from the System Module, and an individual PXI Express Peripheral Module can have up to 2 GB per direction. Considering that PCI Express Switches have the ability for multiple separate data paths to be transferring data between PCI Express devices at the same time, the possibility exists for data rates above 32 GB/s per direction within a PXI Express System. The amount of bandwidth for a system is implementation specific and allows PXI Express suppliers to develop systems that meet their customers' needs in terms of cost and performance.

Electrical rules that are leveraged from the CompactPCI Express specification into PXI Express include but are not limited to the following:

- PCI Express transmit and receive electrical signaling definitions and budgets
- PCI Express reference clock
- PCI Express sideband signals
- SMBus
- Backplane identification and capability via SMBus
- Signals used for power supply control
- Power supply requirements
- Module and slot pin assignments with the exception of the additional instrumentation signals
- PCI with certain slot types

Table 2-2 shows the components that are interoperable between the two specifications. Note that when PXI Express Modules are used in CompactPCI Express Chassis, the PXI Express Module's instrumentation features are not usable.

Table 2-2. PXI and PXI Express Module Interoperability



PXI Express Component	CompactPCI Express Component						
	System Slot	System Board	Type 2 Peripheral Slot	Type 2 Peripheral Board	Hybrid Slot	Legacy Slot	CompactPCI Peripheral Board
PXI Express System Slot		OK					
PXI Express System Module	OK						
PXI Express Peripheral Slot				OK			
PXI Express Peripheral Module			OK		OK		
PXI Express Hybrid Slot				OK			OK ¹
Hybrid Slot Compatible PXI-1 Module					OK	OK	
System Timing Slot				OK			
System Timing Module			OK				
PXI-1 Slot							OK
PXI-1 Module						OK	

¹ CompactPCI Peripheral Board will work if it has J1 only.

2.2.1 CompactPCI Express 利用的功能

PCI Express 是 PXI Express 利用 CompactPCI Express 的主要功能之一。PXI Express 系统每个方向的数据最多可达到 6 GBytes/秒，单个 PXI Express 外设模块每个方向最多可传输 2 GB。考虑到 PCI Express 交换机能够让多个单独的数据路径同时在 PCI Express 设备之间传输数据，因此 PXI Express 系统内每个方向的数据速率有可能超过 32 GB/s。系统的带宽量是特定于实现的，允许 PXI Express 供应商

开发满足客户成本和性能需求的系统。

从 CompactPCI Express 规范到 PXI Express 中的电气规则包括但不限于以下内容：

- PCI Express 发送和接收电信号定义和预算
- PCI Express 参考时钟
- PCI Express 边带信号
- 中小型企业
- 通过 SMBus 进行背板识别和功能
- 用于电源控制的信号
- 电源要求
- 模块和插槽引脚分配，附加仪表信号除外
- 具有某些插槽类型的 PCI

表 2-2 显示了两种规格之间可互作的组件。请注意，当 PXI Express 模块在 CompactPCI Express 机箱中使用时，PXI Express 模块的仪器功能不可用。

表 2-2.PXI 和 PXI Express 模块互作性

PXI Express 组件	CompactPCI Express 组件						
	系统槽	系统板	类型 2 外设槽	类型 2 外设板	混合槽	遗产槽	紧凑型 PCI 外设板
PXI Express 系统插槽		还行					
PXI Express 系统模块	还行						
PXI Express 外设插槽				还行			
PXI Express 外设模块			还行		还行		
PXI Express 混合插槽				还行			还行
混合插槽兼容 PXI-1 模块					还行	还行	
系统时序插槽				还行			
系统时序模块			还行				
PXI-1 插槽							还行
PXI-1 模块						还行	

¹ 如果 CompactPCI 外围板只有 J1，它就可以工作。

2.2.2 Features Leveraged from the PXI Hardware Specification

PXI Express products can take advantage of the increase in data performance while implementing the instrumentation features in the PXI-1 Specification. Each PXI Express Module and slot type defined in this specification can leverage the PXI 10 MHz system clock (PXI_CLK10), the PXI-bused trigger lines, a Local Bus line, and PXI star trigger as defined in the PXI-1 Specification, in addition to the new instrumentation features defined in this specification. PXI-1 slots implemented in PXI Express systems also maintain the PXI Local Bus. PXI Express slots have the potential for a virtual local bus by taking advantage of PCI Express Switches allowing multiple data paths to transfer data between PCI Express devices at the same time. Determinism of data movement with such a virtual local bus may be PCI Express Switch and data dependent.

2.2.3 New Instrumentation Features

The system timing and synchronization capabilities of PXI are a key differentiation from other instrumentation form factors. PXI was created by adding those features to the high-bandwidth PCI bus and compact modular form factor of CompactPCI while maintaining reasonable implementation cost. The timing and triggering capabilities of PXI are retained in this specification and will continue to solve many system applications in PXI. With the advances in technology affording higher performance, low-cost differential signaling, and the differential connectors necessary for PCI Express already required, PXI Express builds on the existing capabilities by providing a differential system clock, differential synchronization, and differential star trigger and clock signals from a new System Timing Module. The key advantages of providing differential clocking and synchronization is the increased noise immunity provided to instrumentation clocks and the ability to transmit higher frequency clocks. These high-frequency clocks not only allow for higher performance, but also match well with modern processes and allow for low-cost products to remove clock multiplication circuits in many cases. The new features are added in a way to be compatible and highly interoperable with existing PXI Modules. The following sections will describe the new additions. Figure 2-19 shows one example of how the instrumentation signals are implemented on a PXI Express backplane that has a System Timing Slot.



2.2.2 PXI 硬件规范中利用的功能

PXI Express 产品可以在实现 PXI-1 规范中的仪器功能时利用数据性能的提高。除了本规范中定义的新仪器功能外，本规范中定义的每个 PXI Express 模块和插槽类型都可以利用 PXI-1 规范中定义的 PXI 10 MHz 系统时钟 (PXI_CLK10)、PXI 总线触发线、本地总线和 PXI 星形触发。PXI Express 系统中实现的 PXI-1 插槽也保留了 PXI 本地总线。PXI Express 插槽通过利用 PCI Express 交换机，允许多个数据路径同时在 PCI Express 设备之间传输数据，从而具有虚拟本地总线的潜力。

使用此类虚拟本地总线的数据移动的确定性可能取决于 PCI Express 交换机和数据。

2.2.3 新的仪器功能

PXI 的系统定时和同步功能是与其他仪器外形尺寸的关键区别。PXI 是通过将这些功能添加到 CompactPCI 的高带宽 PCI 总线和紧凑的模块化外形中而创建的，同时保持合理的实施成本。本规范保留了 PXI 的定时和触发功能，并将继续解决 PXI 中的许多系统应用。随着技术的进步，提供了更高的性能、低成本的差分信号以及 PCI Express 所需的差分连接器，PXI Express 在现有功能的基础上提供了来自新系统时序模块的差分系统时钟、差分同步以及差分星形触发和时钟信号。提供的主要优势

差分时钟和同步是为仪器时钟提供的增强抗噪性和传输更高频率时钟的能力。这些高频时钟不仅可以实现更高的性能，而且与现代工艺非常匹配，并允许低成本产品在许多情况下消除时钟倍增电路。添加新功能的方式与现有 PXI 模块兼容并高度互作。以下部分将介绍新增功能。图 2-19 显示了如何在具有系统时序插槽的 PXI Express 背板上实现仪器信号的一个示例。



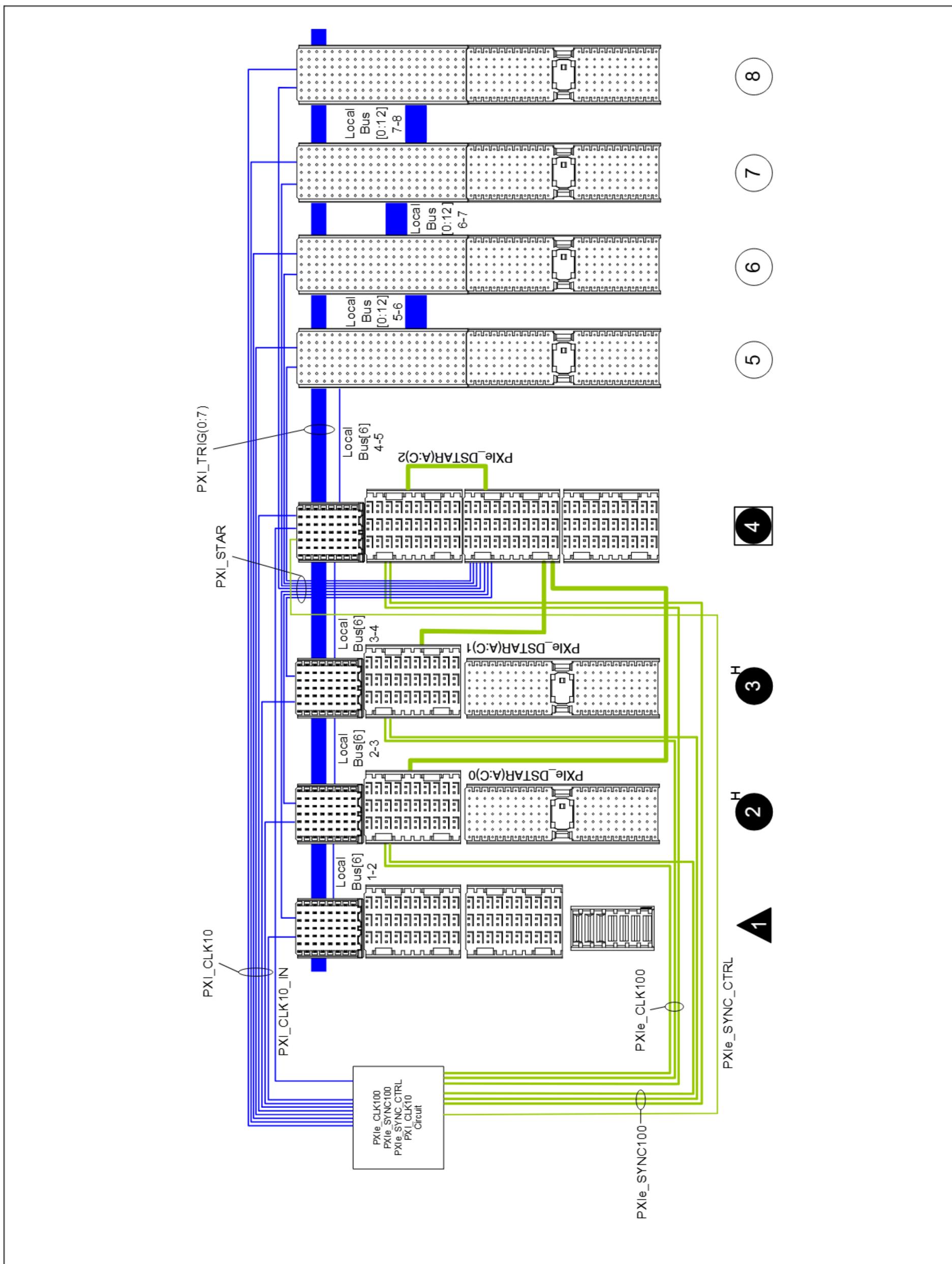


Figure 2-19. Instrumentation Signal Implementation Example

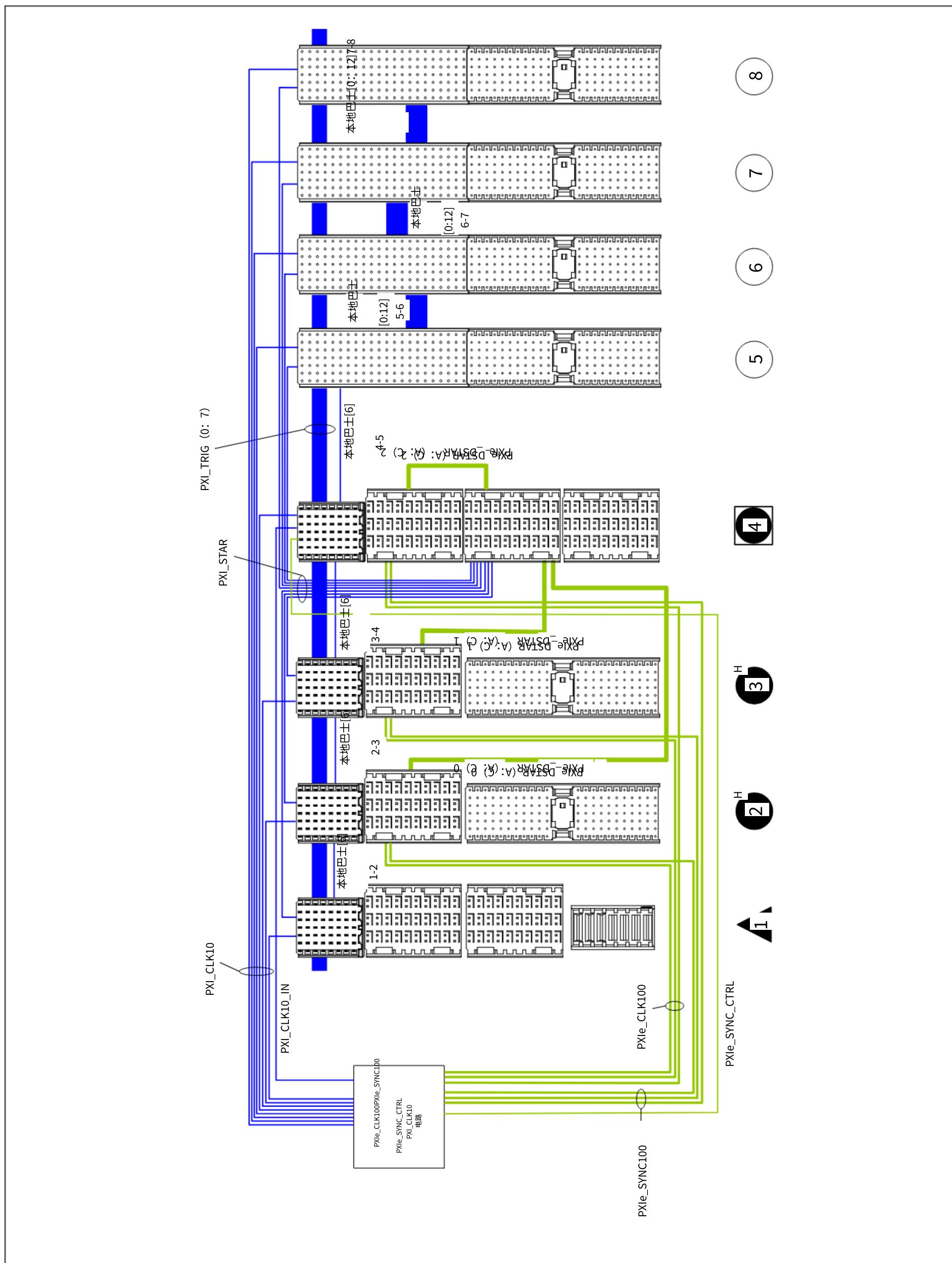


图 2-19. 仪表信号实现示例

Figure 2-20 shows how the instrumentation signals are mapped to the connectors of the Hybrid Slot, PXI Express Peripheral Slot, and the System Timing Slot.

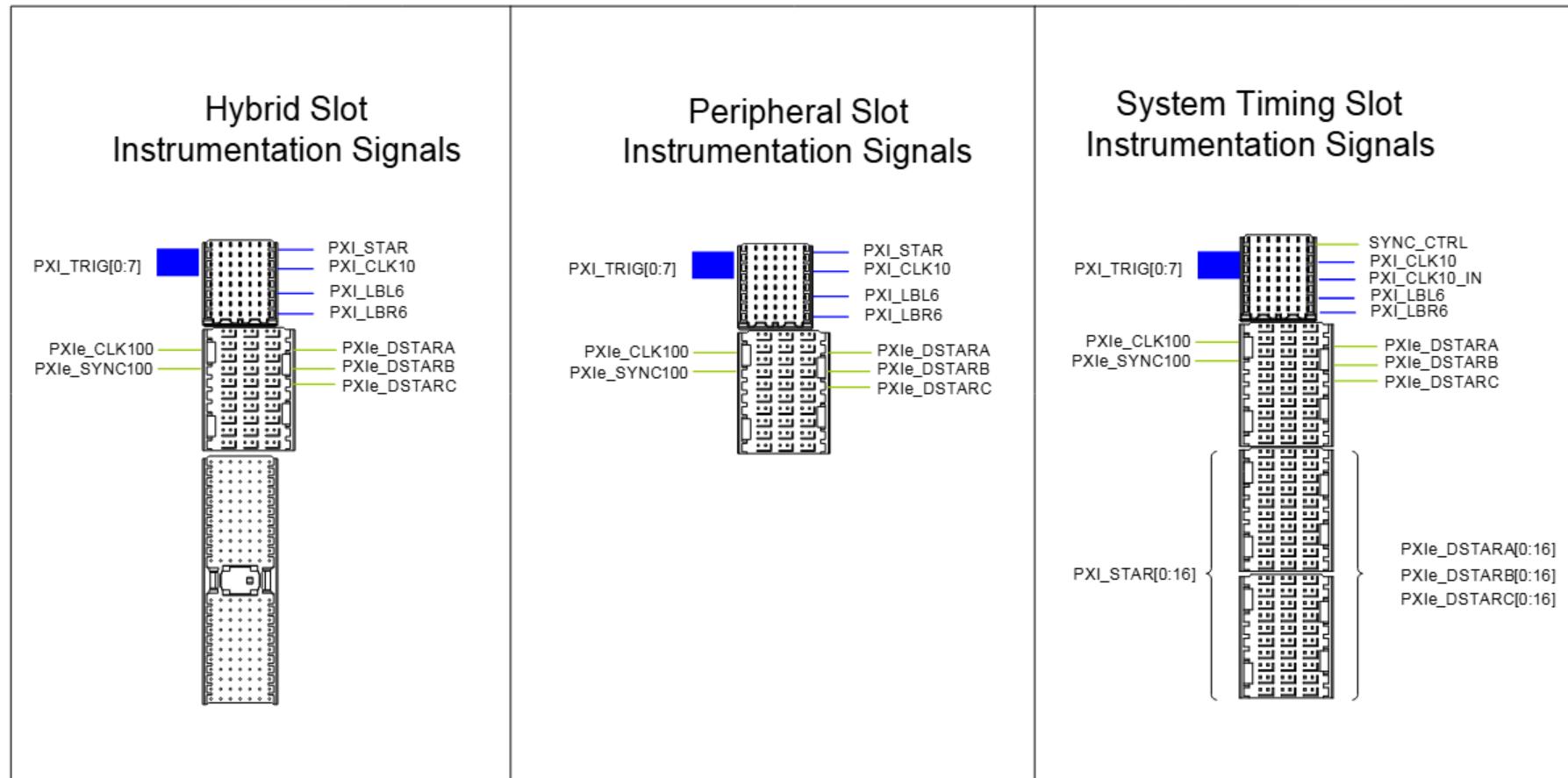


Figure 2-20. Instrumentation Signals Connector Mapping

2.2.3.1 High-Frequency System Reference Clock

The High-Frequency System Reference Clock, or PXIE_CLK100 as it is called out in the specification, is the most significant addition for timing in PXI Express. This signal provides a differential, 100 MHz LVPECL clock to each PXI Express Peripheral Slot in the system. Advancing technology has allowed PXI to adopt differential clocking, which provides for increased noise immunity in the backplane. This allows instrumentation Modules to receive a clock with low jitter and improve overall system performance. The differential technology also allows for a higher frequency reference clock of 100 MHz. This not only allows for higher performance clocking, but also allows the cost of Modules to be lowered by eliminating clock multiplication for Modules able to work with PXIE_CLK100 and divisions directly. The PXIE_CLK100 is added into the specification in a way to be completely interoperable with PXI_CLK10. The PXI_CLK10 and PXIE_CLK100 are phase aligned and allow for highly accurate synchronization of devices, including all PXI-1 compliant devices, no matter which clock is used.



2.2.3.2 Differential Synchronization Signal

With the High-Frequency System Reference Clock (PXIE_CLK100) comes the need to accurately synchronize Modules using this reference clock along with those using PXI_CLK10. The Differential Synchronization Signal or PXIE_SYNC100 is routed by the backplane to each Module and provides this capability. This signal is synchronous to PXIE_CLK100 and asserts one out of every 10 clocks to indicate the phase relationship of the 10 MHz and 100 MHz reference clocks. This is key for synchronization and triggering in that it allows the existing triggering capabilities to be used and interoperate. Devices using the Trigger Bus can send triggers synchronous to PXI_CLK10 no matter what system reference clock is used. The PXIE_SYNC100 also provides a synchronization signal for Modules wanting to divide the 100 MHz reference clock for use on the Module. This allows multiple Modules to begin the clock division on the same clock edge without requiring a high-frequency trigger bus.

图 2-20 显示了仪器信号如何映射到混合插槽、PXI Express 外设插槽和系统定时插槽的连接器。

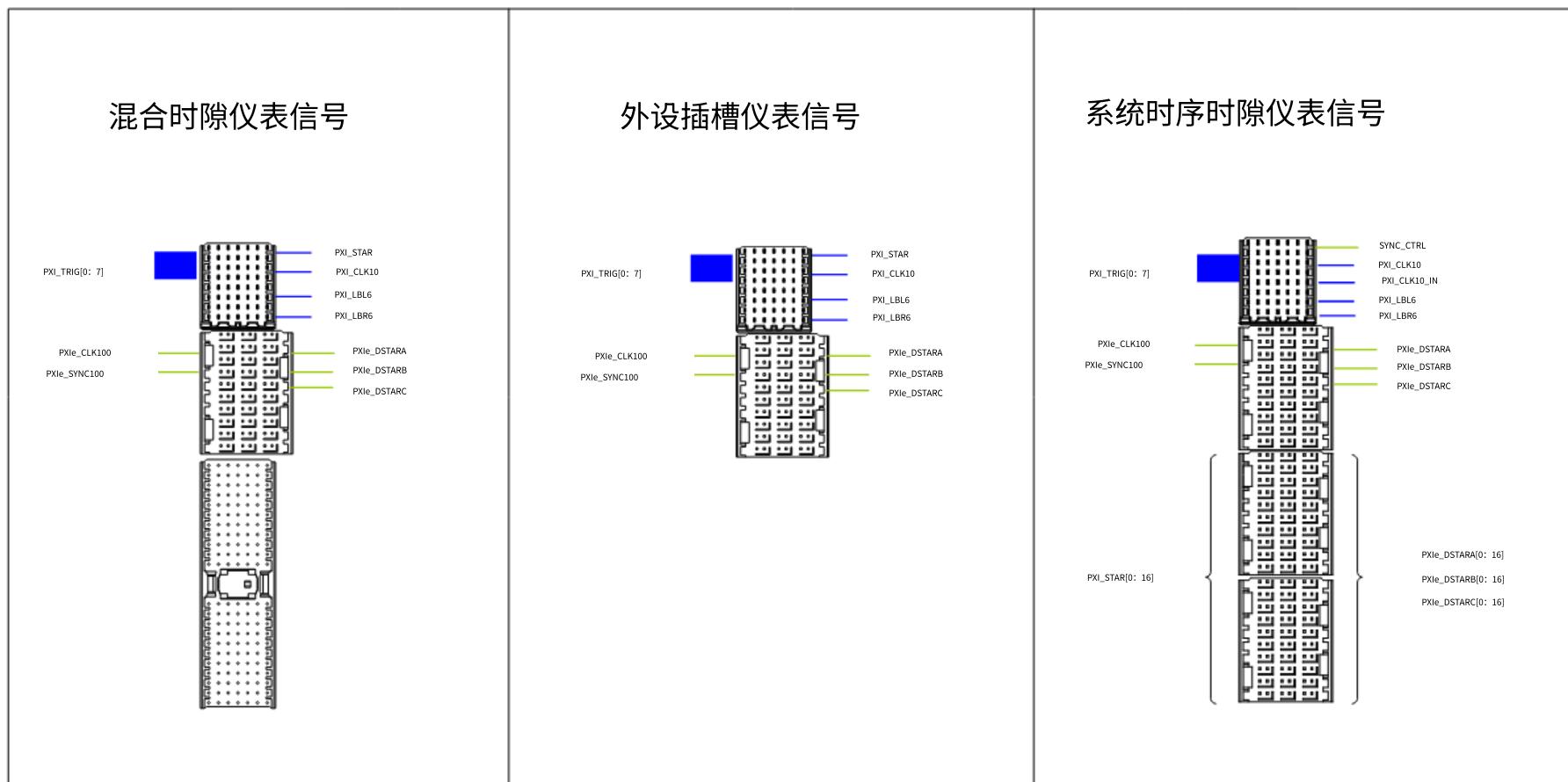


图 2-20. 仪表信号连接器映射

2.2.3.1 高频系统参考时钟

高频系统参考时钟（规范中称为 PXIE_CLK100）是 PXI Express 中最重要的时序补充。该信号为系统中的每个 PXI Express 外设插槽提供差分 100 MHz LVPECL 时钟。先进的技术使 PXI 能够采用差分时钟，从而提高背板的抗噪能力。这使得仪器模块能够接收低抖动的时钟，并提高整体系统性能。差分技术还允许 100 MHz 的更高频率参考时钟。这不仅允许更高性能的时钟，而且还可以通过消除能够直接使用 PXIE_CLK100 和分频的模块的时钟倍增来降低模块的成本。该 PXIE_CLK100 以与 PXI_CLK10 完全互作的方式添加到规范中。PXI_CLK10 和 PXIE_CLK100 相位对齐，无论使用哪个时钟，都可以对设备（包括所有符合 PXI-1 标准的设备）进行高精度同步。



2.2.3.2 差分同步信号

使用高频系统参考时钟（PXIE_CLK100）需要使用该参考时钟的模块与使用 PXI_CLK10 的模块进行精确同步。差分同步信号或 PXIE_SYNC100 通过背板路由到每个模块并提供此功能。该信号与 PXIE_CLK100 同步，每 10 个时钟中就有一个置位，以指示 10 MHz 和 100 MHz 参考时钟的相位关系。这是同步和触发的关键，因为它允许使用和互作现有的触发功能。无论使用什么系统参考时钟，使用触发总线的设备都可以同步发送触发器到 PXI_CLK10。该 PXIE_SYNC100 还为想要分频 100 MHz 参考时钟以在模块上使用的模块提供同步信号。这允许多个模块在同一时钟边沿上开始时钟分频，而无需高频触发总线。

2.2.3.3 Differential Triggers

Previous PXI specifications could take advantage of the low cost of TTL logic to provide a complete timing and synchronization system. While TTL logic provided efficient implementations, it does come with a limit on the frequencies that may be transmitted in the system. With PXI Express, the clocking and triggering system can take advantage of the lowered cost of differential signaling and provide high-quality and high-frequency connections to each Module. In the same way that PXI_STAR allows a direct connection between each Module to a central timing resource, the Differential Star Triggers allows for three direct, high-frequency connections back to the System Timing Module. A key benefit of these signals is the ability to transmit high-frequency, high-quality clocks to and from Modules in a PXI system. By having multiple connections, a larger number of system applications may be solved by providing increased routing capabilities. While a primary application of PXIe_DSTAR will be clock distribution, the signals are flexible and allow for a large number of unique applications of these connections.

2.2.3.4 System Timing Module

The Slot 2 or Star Trigger Slot of PXI-1 provides access to advanced system timing applications with individual connections to each Module and the ability to replace the system clock reference. With the addition of the Differential Star Triggers and High-Frequency System Reference Clock, a larger number of high-performance connections are required to be provided by the backplane to the Modules. The System Timing Module (STM) is the connection point for the three starred signals added to each Module. The STM becomes the central connection point and routing manager for the most advanced timing and synchronization capabilities for a PXI Express system. The System Timing Module in PXI Express Systems replaces the Star Trigger Module defined in PXI-1 while it retains the connection point for PXI_STAR to each Module and it provides the connection point for clock replacement in the backplane. The STM is also key in providing the access to support highly synchronized systems across multiple Chassis of heterogeneous systems. While backplanes will provide the capability to support an STM, the System Timing Slot (STS) may accept a PXI Express Peripheral Module if the advanced timing synchronization capabilities are not necessary in a system.



2.2.4 Slot Identification

PXI Express has explicit hardware support for geographical addressing. A PXI Express device can determine its slot number by reading the GA(4:0) pins. Previously, to create the `pxisys.ini` file describing the topology of the PXI system, a PXI resource manager needed to use the run time PCI device tree, the `chassis.ini` files, and vendor-specific information about the PCI topology of the Slot 1 Controller. Using the new hardware support, a full PCI bus tree is no longer needed. Each Module can discover its slot number independently.

2.2.4.1 Module Drivers and the GA Pins

For instrument drivers, VISA implementations, and application software to find a particular device by slot number, the driver for each Module must provide a mechanism to report its slot number to other software components in the system. This mechanism is defined in the PXI-6: *PXI Express Software Specification*.

2.2.4.2 Determining the Chassis Number

Although there is explicit hardware support for determining a Module's slot number, the mechanism for determining a Chassis number requires knowledge of the bus and device numbers of some of the PCI Express Switches and of the Modules in the system. The PXI Express Software specification describes the interfaces for discovering the Chassis number for a PXI Express Module.

2.2.3.3 差动触发器

以前的 PXI 规范可以利用 TTL 逻辑的低成本来提供完整的定时和同步系统。虽然 TTL 逻辑提供了高效的实现，但它确实对系统中可能传输的频率有限制。借助 PXI Express，时钟和触发系统可以利用差分信号的降低成本，并提供高质量和

与每个模块的高频连接。与 PXI_STAR 允许每个模块之间直接连接到中央定时资源的方式相同，差分星形触发器允许三个直接的高频连接回系统定时模块。这些信号的一个主要优点是能够在 PXI 系统中的模块之间传输高频、高质量的时钟。通过具有多个连接，可以通过提供增强的路由功能来解决更多的系统应用。虽然 PXIE_DSTAR 的主要应用是时钟分配，但信号是灵活的，允许这些连接的大量独特应用。

2.2.3.4 系统时序模块

PXI-1 的插槽 2 或星形触发器插槽提供了对高级系统时序应用程序的访问，通过与每个模块的单独连接，并能够替换系统时钟参考。随着差分星形触发器和高频系统参考时钟的添加，背板需要为模块提供更多的高性能连接。系统时序模块 (STM) 是添加到每个模块的三个星形信号的连接点。STM 成为 PXI Express 系统最先进的时序和同步功能的中央连接点和路由管理器。PXI Express 系统中的系统时序模块取代了 PXI-1 中定义的星形触发模块，同时保留了每个模块 PXI_STAR 的连接点，并提供了用于背板中时钟替换的连接点。STM 也是提供跨多个异构系统机箱支持高度同步系统的访问的关键。虽然背板将提供支持 STM 的功能，但如果系统中不需要高级时序同步功能，则系统时序插槽 (STS) 可以接受 PXI Express 外设模块。



2.2.4 插槽识别

PXI Express 具有对地理寻址的明确硬件支持。PXI Express 设备可以通过读取 GA (4: 0) 引脚来确定其插槽号。以前，要创建描述 PXI 系统拓扑的 pxisys.ini 文件，PXI 资源管理器需要使用运行时 PCI 设备树、chassis.ini 文件以及有关插槽 1 控制器的 PCI 拓扑的供应商特定信息。使用新的硬件支持，不再需要完整的 PCI 总线树。每个模块都可以独立发现其插槽号。

2.2.4.1 模块驱动器和 GA 引脚

对于仪器驱动程序、VISA 实现和应用软件来说，要通过插槽号查找特定设备，每个模块的驱动程序必须提供一种机制，以将其插槽号报告给系统中的其他软件组件。PXI-6: PXI Express 软件规范中定义了此机制。

2.2.4.2 确定底盘编号

尽管有明确的硬件支持来确定模块的插槽号，但确定机箱号的机制需要了解系统中某些 PCI Express 交换机和模块的总线和设备号。PXI Express 软件规范描述了用于发现 PXI Express 模块机箱号的接口。

2.2.5 Controller Identification

PXI Express has hardware support for identification of a PXI Express Chassis using an EEPROM on the SMBus. PXI Express also uses information about the bus numbers of the links from the system Module to the Chassis to enumerate which devices are in which Chassis. Therefore, the *PXI Express Software Specification* defines a mechanism for identifying what Controllers exist, how those Controllers access the SMBus, and what bus numbers are subordinate to that Controller.

The *PXI Express Software Specification* specifies an interface for accessing the SMBus using a Slot 1 Controller. There is a one-to-one correspondence between Slot 1 Controllers and instances of the PXI Express SMBus Controller interface.

2.2.6 Chassis Identification

PXI Express leverages the requirements set in the CompactPCI Express specification for the Backplane Identification and Capability EPROM. This EPROM is accessed by the system Module via the SMBus and gives the PXI Express system a way to uniquely identify the vendor, model, revision, and serial number of the Chassis. It also provides information on the slots within the Chassis and the PCI Express topology. This information can be used by software to load a Chassis driver to provide additional information about the Chassis or access backplane and Chassis functionality.

2.2.7 Power Requirements

The power requirements for PXI Express systems include the following defined in CompactPCI Express:

- Power rails
- Current capacity of the power pins for a slot
- Regulation
- Ripple and noise
- Decoupling
- Power rail timing
- Power supply signals to and from the system Module



PXI Express additionally includes Chassis power supply minimum current requirements per voltage rail for each slot type. This guarantees a high level of interoperability between Modules and Chassis and gives guidance to PXI Express Module designers on how much current they can expect from a Chassis. Power requirements for PXI-1 slots implemented in PXI Express systems are defined in the PXI-1 Specification.

2.3 Software Architecture Overview

PXI Express introduces new software features for managing the new hardware features of CompactPCI Express and PXI Express. These new features include:

- A software interface for accessing SMBus devices, such as the serial EEPROM of each Chassis.
- A software interface for accessing the slot number of each Module as provided by the GA pins.
- A mechanism for associating a Chassis number with the Modules in each Chassis.
- A software protocol for enumerating PXI components, such as Controllers, Modules, Chassis, and other resources.
- A namespace for those PXI components.
- A general registration mechanism for services implemented by the drivers for PXI components.
- Standard software interfaces for services implemented by Controllers, Chassis and Modules.

2.2.5 控制器识别

PXI Express 具有硬件支持，可使用 SMBus 上的 EEPROM 识别 PXI Express 机箱。PXI Express 还使用有关从系统模块到机箱的链路的总线号的信息来枚举哪些设备位于哪个机箱中。因此，PXI Express 软件规范定义了一种机制，用于识别存在哪些控制器、这些控制器如何访问 SMBus 以及哪些总线号从属于该控制器。

PXI Express 软件规范规定了使用插槽 1 控制器访问 SMBus 的接口。插槽 1 控制器与 PXI Express SMBus 控制器接口的实例之间存在一对一的对应关系。

2.2.6 底盘识别

PXI Express 利用 CompactPCI Express 规范中为背板识别和功能 EPROM 设置的要求。系统模块通过 SMBus 访问此 EPROM，并为 PXI Express 系统提供了一种唯一标识机箱的供应商、型号、版本和序列号的方法。它还提供有关机箱内插槽和 PCI Express 拓扑的信息。软件可以使用此信息加载机箱驱动程序，以提供有关机箱或访问背板和机箱功能的其他信息。

2.2.7 电源要求

PXI Express 系统的电源要求包括 CompactPCI Express 中定义的以下内容：

- 电源轨
- 插槽电源引脚的电流容量
- 调节
- 纹波和噪声
- 解耦
- 电源轨正时
- 与系统模块之间的电源信号



PXI Express 还包括每种插槽类型的每个电压轨的机箱电源最小电流要求。这保证了模块和机箱之间的高水平互操作性，并为 PXI Express 模块设计人员提供了有关机箱预期电流的指导。PXI-1 规范中定义了 PXI Express 系统中实现的 PXI-1 插槽的电源要求。

2.3 软件架构概述

PXI Express 引入了新的软件功能，用于管理 CompactPCI Express 和 PXI Express 的新硬件功能。这些新功能包括：

- 用于访问 SMBus 设备的软件接口，例如每个机箱的串行 EEPROM。
- 用于访问 GA 引脚提供的每个模块的插槽号的软件接口。
- 用于将机箱编号与每个机箱中的模块相关联的机制。
- 用于枚举 PXI 组件（例如控制器、模块、机箱和其他资源）的软件协议。
- 这些 PXI 组件的命名空间。
- PXI 组件驱动程序实现的服务的通用注册机制。
- 控制器、机箱和模块实施的服务的标准软件接口。

The *PXI Express Software Specification* requires each Controller, Chassis, and Module to include software implementing certain services, and to register those services. By creating standards for these services and how they are registered, the *PXI Express Software Specification* provides a new level of interoperability. If, for example, a Controller, a Chassis, a Module, and a VISA implementation are each provided by a different vendor, all of the following are possible:

- The VISA implementation can determine the physical location of the Module by interacting with the Module driver.
- The Chassis driver can control backplane resources by using the SMBus driver on the Slot 1 Controller.
- A configuration tool can determine the list of Chassis and Modules in the system.

The new software requirements and features for PXI Express are specified in the *PXI Express Software Specification*.



PXI Express 软件规范要求每个控制器、机箱和模块都包含实现某些服务的软件，并注册这些服务。通过为这些服务及其注册方式创建标准，PXI Express 软件规范提供了新的互操作性水平。例如，如果控制器、机箱、模块和 VISA 实现均由不同的供应商提供，则以下所有操作都是可能的：

- VISA 实现可以通过与模块驱动程序交互来确定模块的物理位置。
- 机箱驱动程序可以使用插槽 1 控制器上的 SMBus 驱动程序来控制背板资源。
- 配置工具可以确定系统中的机箱和模块列表。

PXI Express 的新软件要求和功能在 PXI Express 软件规范中有所规定。



This Page Intentionally Left Blank



此页面故意留空



3. Mechanical Requirements

This section defines the mechanical requirements for PXI Express systems. It discusses the maximum number of slots, the location of the system slot, slot numbering, PXI-1 slots, Chassis requirements, connector requirements, Module types, the interoperability of the Controller with the Chassis, the PXI Express logo/glyphs, environmental testing, and cooling.

3.1 Drawing Standard

The drawings in this specification shall be interpreted per ANSI Y14.100.

3.2 Dimensional Units

Dimensions in this specification are in millimeters unless otherwise specified.

3.3 Chassis Subrack Mechanical Requirements

RULE: Just as with PXI-1, CompactPCI, and CompactPCI Express, a PXI Express Chassis SHALL use PICMG 2.0-compliant Chassis Subracks.

3.4 Minimum Slot Requirements to be a PXI Express Chassis

RULE: A PXI Express Chassis SHALL at least have either one PXI Express Peripheral Slot or one Hybrid Slot.

RULE: A PXI Express Chassis SHALL NOT have a Star Trigger Slot as defined in the PXI-1 Specification.

RECOMMENDATION: A PXI Express Chassis SHOULD have a System Timing Slot.



3.5 Features Leveraged from PXI-1: PXI Hardware Specification

3.5.1 Maximum Number of Slots

Since the CompactPCI Express specification accommodates 31 slots based on the definition of the Geographical Addressing pins, it is necessary to limit a PXI Express Chassis to 31 slots.

RULE: A PXI Express Chassis SHALL NOT have more than 31 slots.

3.5.2 System Slot Location and Rules

All PXI Express-compatible systems require a backplane/Chassis, a System Timing Slot, and at least either one PXI Express Peripheral Slot or one Hybrid Slot. A System Slot is not a requirement if the system Module functionality is built into the Chassis. If the Chassis does have a System Slot, it allows users to mix and match different Controllers. However, because the CompactPCI Express specification allows a System Slot to be located anywhere relative to Peripheral Slots, the possibility for confusion and incompatibility exists. To address this problem the following rules must be followed for PXI Express-compatible systems:

RULE: The System Slot SHALL be defined as the leftmost PXI slot in a PXI Chassis/backplane. For documentation purposes, this slot is counted as one *System Slot*.

RECOMMENDATION: If the System Module requires more than one slot width, it SHOULD extend to the LEFT of the System Slot in full slot increments (one slot equals 20.32 mm, or 0.8 in.) into additional Controller expansion slots.

3. 机械要求

本节定义了 PXI Express 系统的机械要求。它讨论了最大插槽数、系统插槽的位置、插槽编号、PXI-1 插槽、机箱要求、连接器要求、模块类型、控制器与机箱的互作性、PXI Express 徽标/字形、环境测试和冷却。

3.1 图纸标准

本规范中的图纸应根据 ANSI Y14.100 进行解释。

3.2 维度单位

除非另有说明，否则本规范中的尺寸以毫米为单位。

3.3 机箱子机架机械要求

规则：与 PXI-1、CompactPCI 和 CompactPCI Express 一样，PXI Express 机箱应使用符合 PICMG 2.0 标准的机箱子机架。

3.4 成为 PXI Express 机箱的最低插槽要求

规则：PXI Express 机箱应至少具有一个 PXI Express 外设插槽或一个混合插槽。

规则：PXI Express 机箱不得具有 PXI-1 规范中定义的星形触发插槽。

建议：PXI Express 机箱应具有系统定时插槽。



3.5 PXI-1 利用的功能：PXI 硬件规格

3.5.1 最大插槽数

由于 CompactPCI Express 规范根据地理寻址引脚的定义可容纳 31 个插槽，因此有必要将 PXI Express 机箱限制为 31 个插槽。

规则：PXI Express 机箱的插槽不得超过 31 个。

3.5.2 系统插槽位置和规则

所有与 PXI Express 兼容的系统都需要一个背板/机箱、一个系统时序插槽，以及至少一个 PXI Express 外设插槽或一个混合插槽。如果系统模块功能内置于机箱中，则不需要系统插槽。如果机箱确实有系统插槽，则允许用户混合和匹配不同的控制器。但是，由于 CompactPCI Express 规范允许系统插槽位于相对于外设插槽的任何位置，因此存在混淆和不兼容的可能性。要解决此问题，PXI Express 兼容系统必须遵循以下规则：

规则：系统插槽应定义为 PXI 机箱/背板中最左侧的 PXI 插槽。出于文档目的，此插槽计为一个系统插槽。

建议：如果系统模块需要多个插槽宽度，则它应以全插槽增量（一个插槽等于 20.32 毫米或 0.8 英寸）延伸到系统插槽的左侧，以进入其他控制器扩展插槽。

OBSERVATION: In a PXI Express system, these additional Controller slots are for physical expansion of the System Controller Module only and cannot support Peripheral Modules. These slots DO NOT have connectors that interface to PCI Express links routed on the backplane.

OBSERVATION: Extending the System Module to the LEFT allows all PXI Express Peripheral Slots to be used.

RECOMMENDATION: The System Module SHOULD NOT extend to the RIGHT of the System Slot into Peripheral Slots.

OBSERVATION: If a System Module expands to the right, the number of usable PXI Express Peripheral Slots may be compromised.

RULE: Every PXI Express System Module SHALL clearly document how many Controller expansion slots (to the left of the System Slot) and Peripheral Slots it occupies.

RULE: Every PXI Express Chassis SHALL clearly document how many Peripheral and Controller Expansion Slots are available.

OBSERVATION: The two preceding rules help ensure that end users can easily determine whether a particular Controller-Chassis pair is compatible and how many Peripheral Slots are available.

Figure 2-17 depicts typical System Expansion Slot designations in a PXI Express System.

3.5.3 Slot Numbering and Orientation

PXI Express Chassis slot numbering is handled the same way that the PXI-1 Specification requires. The exception is that PXI Express allows for Chassis that have the System Module to be built in.

RULE: PXI Express Chassis with a System Slot SHALL meet the slot numbering requirements set in the PXI-1 Specification.



RULE: PXI Express Chassis without a System Slot (the System Module is built in), SHALL meet the slot numbering requirements set in the PXI-1 Specification, except the slots will have their numbering begin at the number 2.

PERMISSION: Slot orientation and numbering schemes other than those defined in PXI-1 MAY be used as long as it is clear and logical for the end user.

3.5.4 PXI-1 Slot

In a PXI Express Chassis, there may be slots that support PXI boards as they are defined in PXI-1 (*PXI Hardware Specification*, Revision 2.2). These slots meet the mechanical requirements of the *PXI Hardware Specification* and are referred to as PXI-1 slots.

PERMISSION: PXI-1 3U and 6U Peripheral Modules and Slots are MAY be used in PXI Express Systems.

RULE: PXI-1 slots in a PXI Express Chassis SHALL meet the mechanical requirements set in the PXI-1 Specification.

RULE: PXI-1 Peripheral Modules SHALL NOT be plugged into Hybrid Peripheral Slots unless they meet the requirements for Hybrid Slot Compatible PXI-1 Modules as defined by this specification.

RECOMMENDATION: PXI-1 3U and 6U Peripheral Modules SHOULD also meet the side-2 component height recommendation as defined by the CompactPCI Express specification to minimize mechanical interference issues.

3. 机械要求

观察：在 PXI Express 系统中，这些额外的控制器插槽仅用于系统控制器模块的物理扩展，不支持外围设备模块。这些插槽没有连接到背板上布线的 PCI Express 链路的连接器。

观察：将系统模块向左扩展允许使用所有 PXI Express 外设插槽。

建议：系统模块不应延伸到系统插槽的右侧进入外围设备插槽。

观察：如果系统模块向右扩展，则可用的 PXI Express 外设插槽的数量可能会受到影响。

规则：每个 PXI Express 系统模块都应清楚地记录它占用了多少个控制器扩展插槽（位于系统插槽的左侧）和外设插槽。

规则：每个 PXI Express 机箱都应清楚地记录有多少个可用的外设和控制器扩展插槽。

观察：上述两条规则有助于确保最终用户可以轻松确定特定的控制器-机箱对是否兼容以及有多少个外设插槽可用。

图 2-17 描述了 PXI Express 系统中的典型系统扩展槽名称。

3.5.3 插槽编号和方向

PXI Express 机箱插槽编号的处理方式与 PXI-1 规范要求的处理方式相同。例外情况是 PXI Express 允许内置系统模块的机箱。

规则：带有系统插槽的 PXI Express 机箱应满足 PXI-1 规范中设置的插槽编号要求。

规则：没有系统插槽（内置系统模块）的 PXI Express 机箱应满足 PXI-1 规范中设置的插槽编号要求，但插槽的编号将从数字 2 开始。

权限：可以使用 PXI-1 中定义的插槽方向和编号方案，只要对最终用户来说清晰且合乎逻辑即可。

3.5.4 PXI-1 插槽

在 PXI Express 机箱中，可能存在支持 PXI-1（PXI 硬件规范，修订版 2.2）中定义的 PXI 板的插槽。这些插槽满足 PXI 硬件规范的机械要求，称为 PXI-1 插槽。

许可：PXI-1 3U 和 6U 外设模块和插槽可用于 PXI Express 系统。

规则：PXI Express 机箱中的 PXI-1 插槽应满足 PXI-1 规范中设定的机械要求。

规则：PXI-1 外设模块不得插入混合外设插槽，除非它们满足本规范中定义的混合插槽兼容 PXI-1 模块的要求。

建议：PXI-1 3U 和 6U 外设模块也应满足 CompactPCI Express 规范中定义的侧 2 组件高度建议，以最大限度地减少机械干扰问题。

3.5.5 Hybrid Slot-Compatible PXI-1 Peripheral Modules

PXI-1 or an associated ECN defines a 3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module that consists of a 3U or 6U PXI-1 Module where the J2 HM connector has been replaced with an eHM connector. The eHM connector is a modified 2 mm HM connector that includes application keying and is installed in the same location as the upper eight columns of the PXI-1 J2 connector. This board type may be used in any PXI-1 or PXI Express Hybrid Slot.

OBSERVATION: A Hybrid Slot Compatible PXI-1 Peripheral Module MAY be used in a legacy PXI-1 or PXI Express Hybrid Slot.

3.6 Features Leveraged from CompactPCI Express Specification

Just as PXI-1 was based on CompactPCI, PXI Express is based on CompactPCI Express, which has integrated PCI Express into a CompactPCI type architecture. This section outlines the features rules, suggestions, permissions, and observations leveraged from that specification.

RULE: All mechanical requirements defined by the CompactPCI Express specification SHALL be met unless stated otherwise in this specification.

3.6.1 Module Connector Requirements

3.6.1.1 Advanced Differential Fabric (ADF) Connector

RULE: PXI Express Modules SHALL use the ADF-F-3-10-2-F-25 connector as defined by the CompactPCI Express specification.

3.6.1.2 Enriched Hard-Metric (eHM) Connector

RULE: PXI Express Modules SHALL use the eHM-F2 connector as defined by the CompactPCI Express specification.

3.6.1.3 Universal Power (UPM) Connector

RULE: System Controller Modules SHALL use the UPM-M-7 or UPM-M-7-HP connector as defined by the CompactPCI Express specification.

3.6.2 Backplane Connector Requirements

3.6.2.1 Advanced Differential Fabric (ADF) Connector

RULE: PXI Express Slots SHALL use the ADF-M-3-10-2-B-25 or ADF-M-3-10-2-S-25-0100 connector as defined by the CompactPCI Express specification.

3.6.2.2 Enriched Hard-Metric (eHM) Connector

RULE: PXI Express Slots SHALL use the eHM-M2-HP or eHM-M2 connector as defined by the CompactPCI Express specification.

3.6.2.3 Universal Power (UPM) Connector

RULE: System Controller Slots SHALL use the UPM-F-7 connector as defined by the CompactPCI Express specification.

3.5.5 混合插槽兼容 PXI-1 外设模块

PXI-1 或相关 ECN 定义了一个 3U 和 6U 混合插槽兼容 PXI-1 外设模块，该模块由一个 3U 或 6U PXI-1 模块组成，其中 J2 HM 连接器已替换为 eHM 连接器。eHM 连接器是一种改进的 2 mm HM 连接器，包括应用程序键控，并安装在与 PXI-1 J2 连接器的上八列相同的位置。此板类型可用于任何 PXI-1 或 PXI Express 混合插槽。

观察：混合插槽兼容的 PXI-1 外设模块可以用于传统的 PXI-1 或 PXI Express 混合插槽。

3.6 CompactPCI Express 规范中利用的功能

正如 PXI-1 基于 CompactPCI 一样，PXI Express 也基于 CompactPCI Express，后者已将 PCI Express 集成到 CompactPCI 类型的架构中。本节概述了该规范中利用的功能规则、建议、权限和观察结果。

规则：除非本规范中另有说明，否则应满足 CompactPCI Express 规范定义的所有机械要求。

3.6.1 模块连接器要求

3.6.1.1 高级差分结构（ADF）连接器

规则：PXI Express 模块应使用 CompactPCI Express 规范中定义的 ADF-F-3-10-2-F-25 连接器。

3.6.1.2 强化硬公制（eHM）连接器

规则：PXI Express 模块应使用 CompactPCI Express 规范中定义的 eHM-F2 连接器。

3.6.1.3 通用电源（UPM）连接器

规则：系统控制器模块应使用 CompactPCI Express 规范定义的 UPM-M-7 或 UPM-M-7-HP 连接器。

3.6.2 背板连接器要求

3.6.2.1 高级差分结构（ADF）连接器

规则：PXI Express 插槽应使用 CompactPCI Express 规范定义的 ADF-M-3-10-2-B-25 或 ADF-M-3-10-2-S-25-0100 连接器。

3.6.2.2 强化硬公制（eHM）连接器

规则：PXI Express 插槽应使用 CompactPCI Express 规范中定义的 eHM-M2-HP 或 eHM-M2 连接器。

3.6.2.3 通用电源（UPM）连接器

规则：系统控制器插槽应使用 CompactPCI Express 规范定义的 UPM-F-7 连接器。

3.6.3 3U and 6U Module Requirements

3.6.3.1 System Module

RULE: 3U and 6U PXI Express Modules SHALL meet the mechanical requirements as defined in the CompactPCI Express specification.

OBSERVATION: 6U PXI Express System Modules and backplanes MAY use J3/P3, J4/P4, and J5/P5 if desired for rear I/O applications.

3.6.3.2 PXI Express Peripheral Module

RULE: The 3U PXI Express Peripheral Modules SHALL meet the mechanical requirements for the 3U Type 2 Peripheral Module as defined in the CompactPCI Express specification.

RULE: The 6U PXI Express Peripheral Modules SHALL meet the mechanical requirements for 6U Type 2 Peripheral Boards as defined in the CompactPCI Express specification with the exception that the J3/J4/J5 connectors SHALL NOT be used. The 6U PXI Express Peripheral Module PCB SHALL meet the requirements defined by Figure 3-1.

RULE: 6U PXI Express Peripheral Modules that are not 6U System Timing Modules SHALL NOT have any connectors other than the XJ3, XJ4, and XJ8 connectors.

PERMISSION: 6U PXI Express Peripheral Modules MAY populate the Optional eHM connector, in the XJ8 position as shown in Figure 3-1, when additional power is required.



3.6.3 3U 和 6U 模块要求

3.6.3.1 系统模块

规则：3U 和 6U PXI Express 模块应满足 CompactPCI Express 规范中定义的机械要求。

观察：如果需要，6U PXI Express 系统模块和背板可以使用 J3/P3、J4/P4 和 J5/P5 用于后置 I/O 应用。

3.6.3.2 PXI Express 外设模块

规则：3U PXI Express 外设模块应满足 CompactPCI Express 规范中定义的 3U Type 2 外设模块的机械要求。

规则：6U PXI Express 外设模块应满足 CompactPCI Express 规范中定义的 6U Type 2 外设板的机械要求，但 J3/J4/J5 连接器除外。6U PXI Express 外设模块 PCB 应满足图 3-1 中定义的要求。

规则：非 6U 系统定时模块的 6U PXI Express 外设模块不得具有除 XJ3、XJ4 和 XJ8 连接器以外的任何连接器。

许可：当需要额外电源时，6U PXI Express 外设模块可以将可选 eHM 连接器安装在 XJ8 位置，如图 3-1 所示。



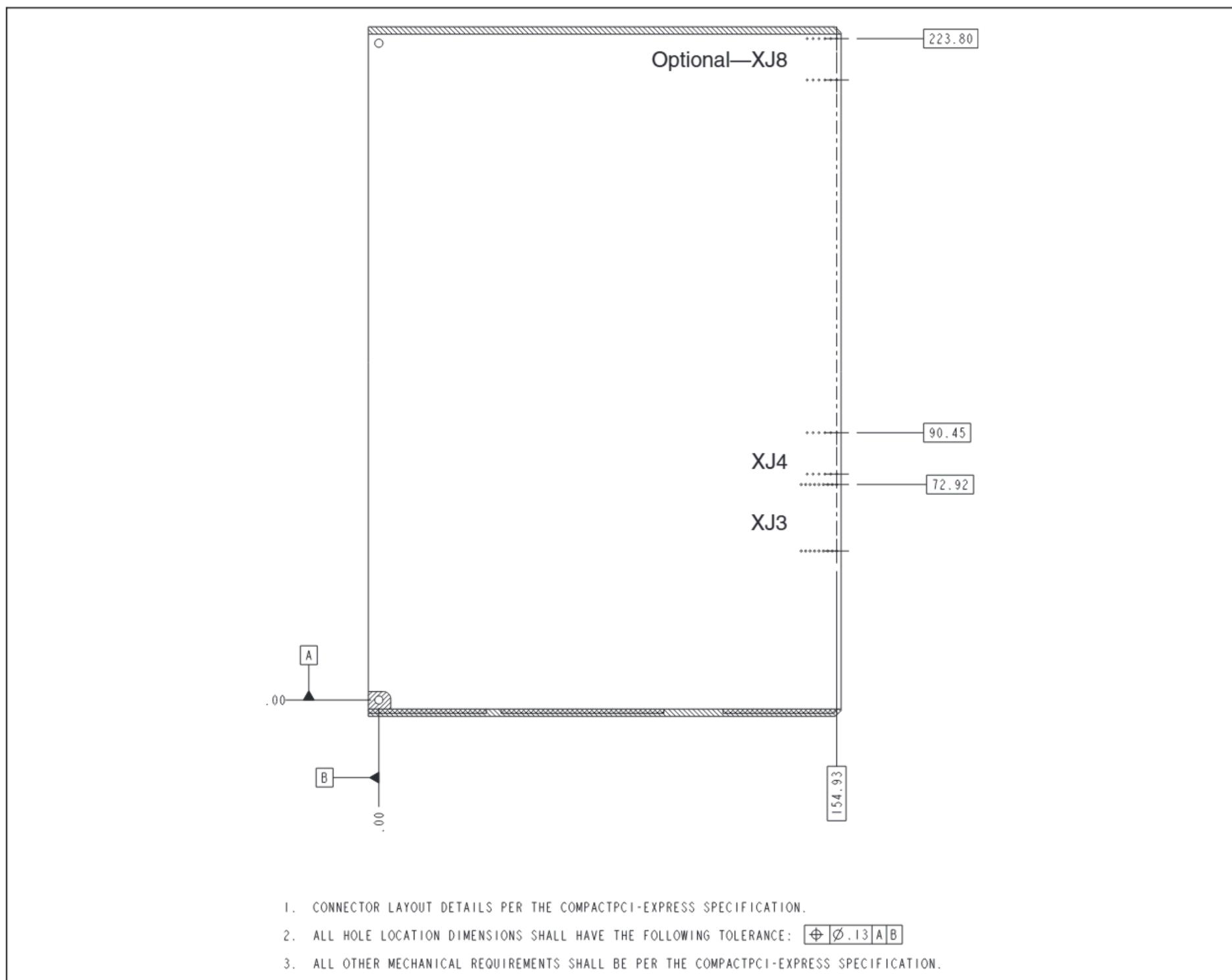


Figure 3-1. 6U PXI Express Peripheral Module PCB



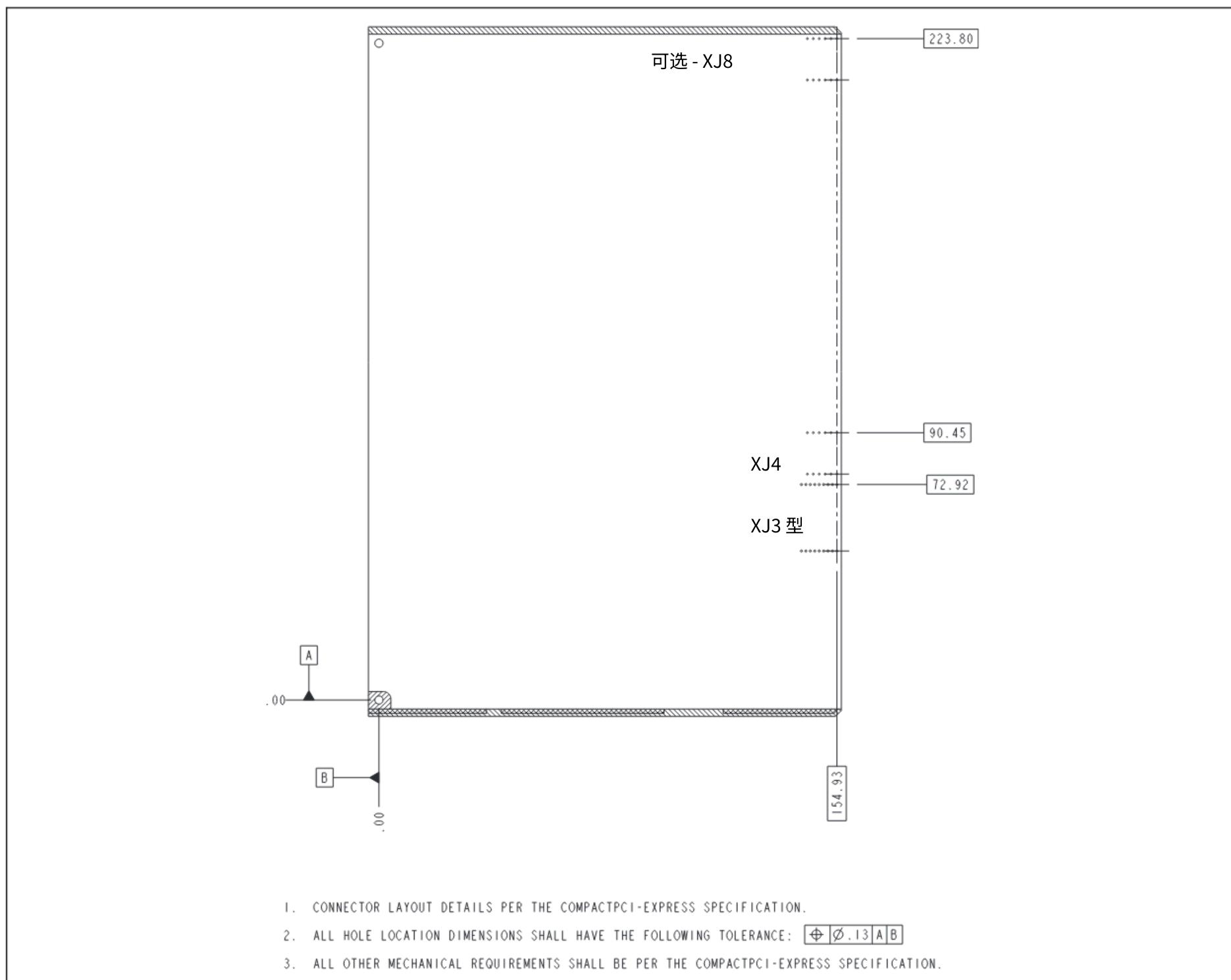


图 3-1.6U PXI Express 外设模块 PCB

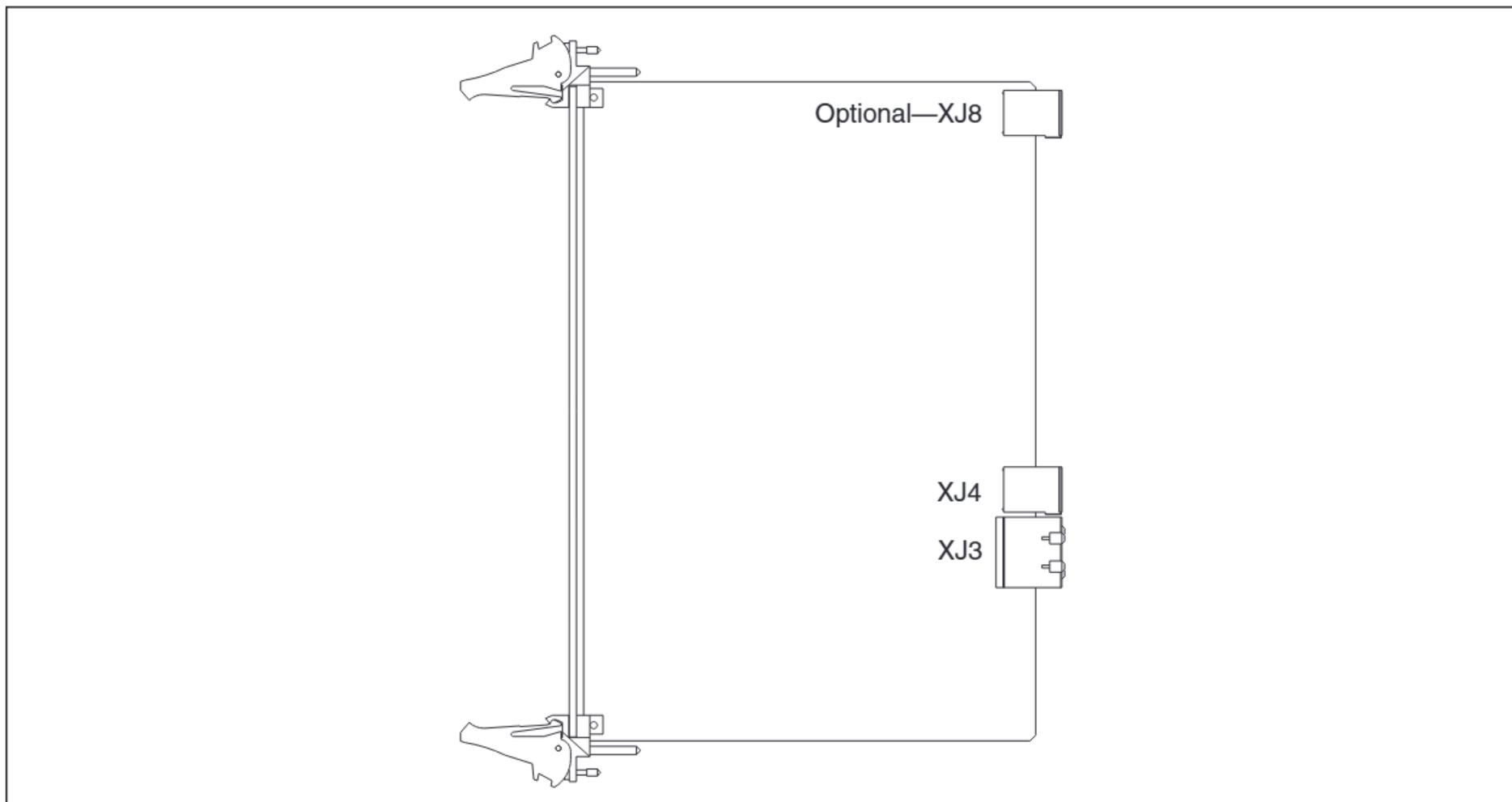


Figure 3-2. 6U PXI Express Peripheral Module

3.6.4 Backplane Requirements

RULE: 3U and 6U PXI Express backplanes SHALL meet the size, mechanical mounting hole, and tolerance requirements as defined in the CompactPCI Express specification.

Requirements for the various connector locations are defined in further detail in the following sections.



3.6.4.1 System Slot

RULE: 3U and 6U PXI Express System Slots SHALL meet the mechanical requirements defined in the CompactPCI Express specification.

PERMISSION: As with CompactPCI Express, 6U System Slots MAY use J3/J4/J5 if desired for rear I/O applications.

3.6.4.2 Peripheral Slot

RULE: 3U PXI Express Peripheral Slots SHALL meet the mechanical requirements for 3U Type 2 Peripheral Slots as defined in the CompactPCI Express specification.

RULE: 6U PXI Express Peripheral Slots SHALL meet the mechanical requirements for 6U Type 2 Peripheral Slots as defined in the CompactPCI Express specification with the exception that an additional XP8 eHM connector SHALL be populated in the location shown in Figure 3-3.

3. 机械要求

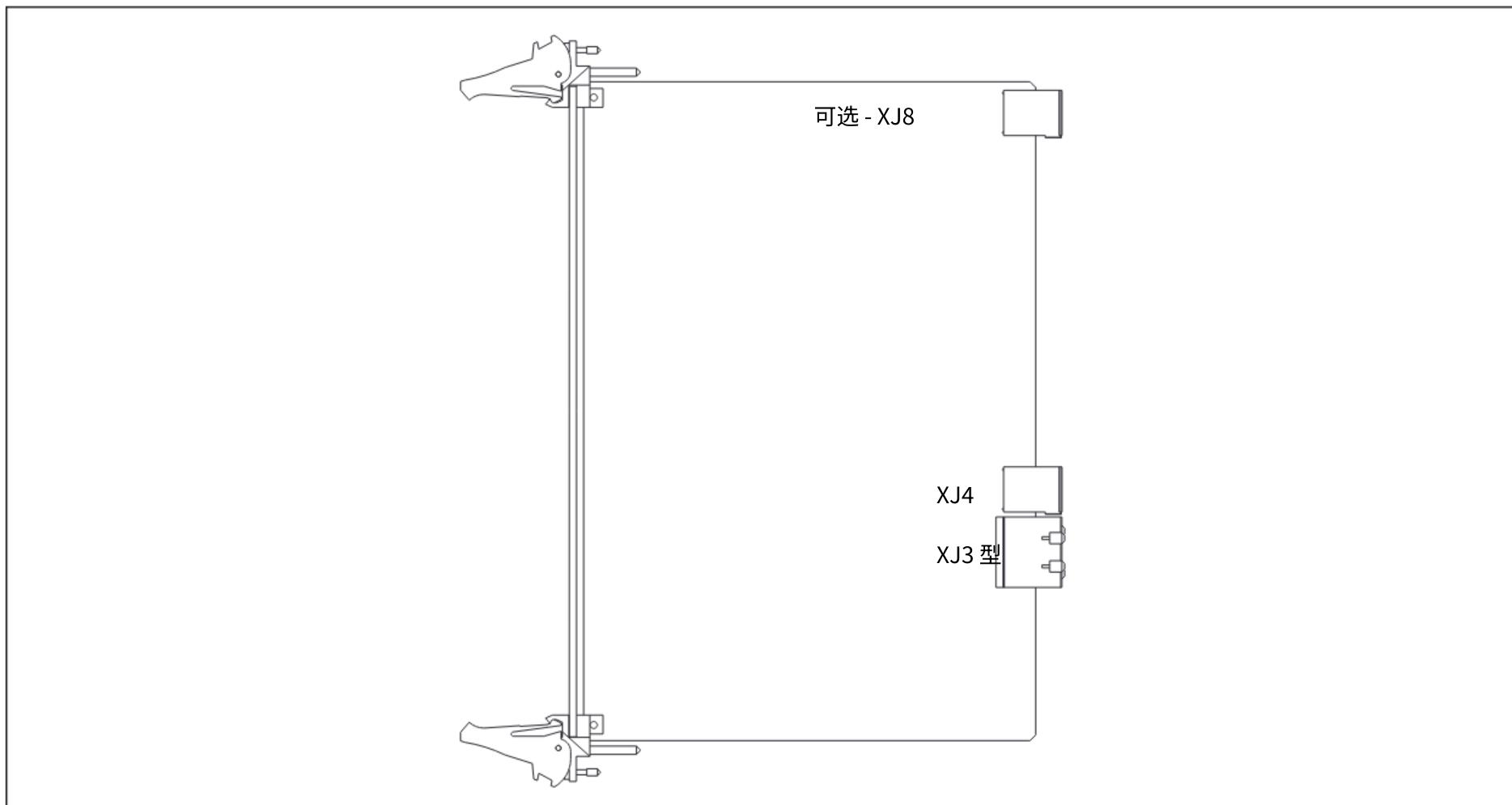


图 3-2.6U PXI Express 外设模块

3.6.4 背板要求

规则：3U 和 6U PXI Express 背板应满足 CompactPCI Express 规范中定义的尺寸、机械安装孔和公差要求。

以下部分将进一步详细定义各种连接器位置的要求。



3.6.4.1 系统插槽

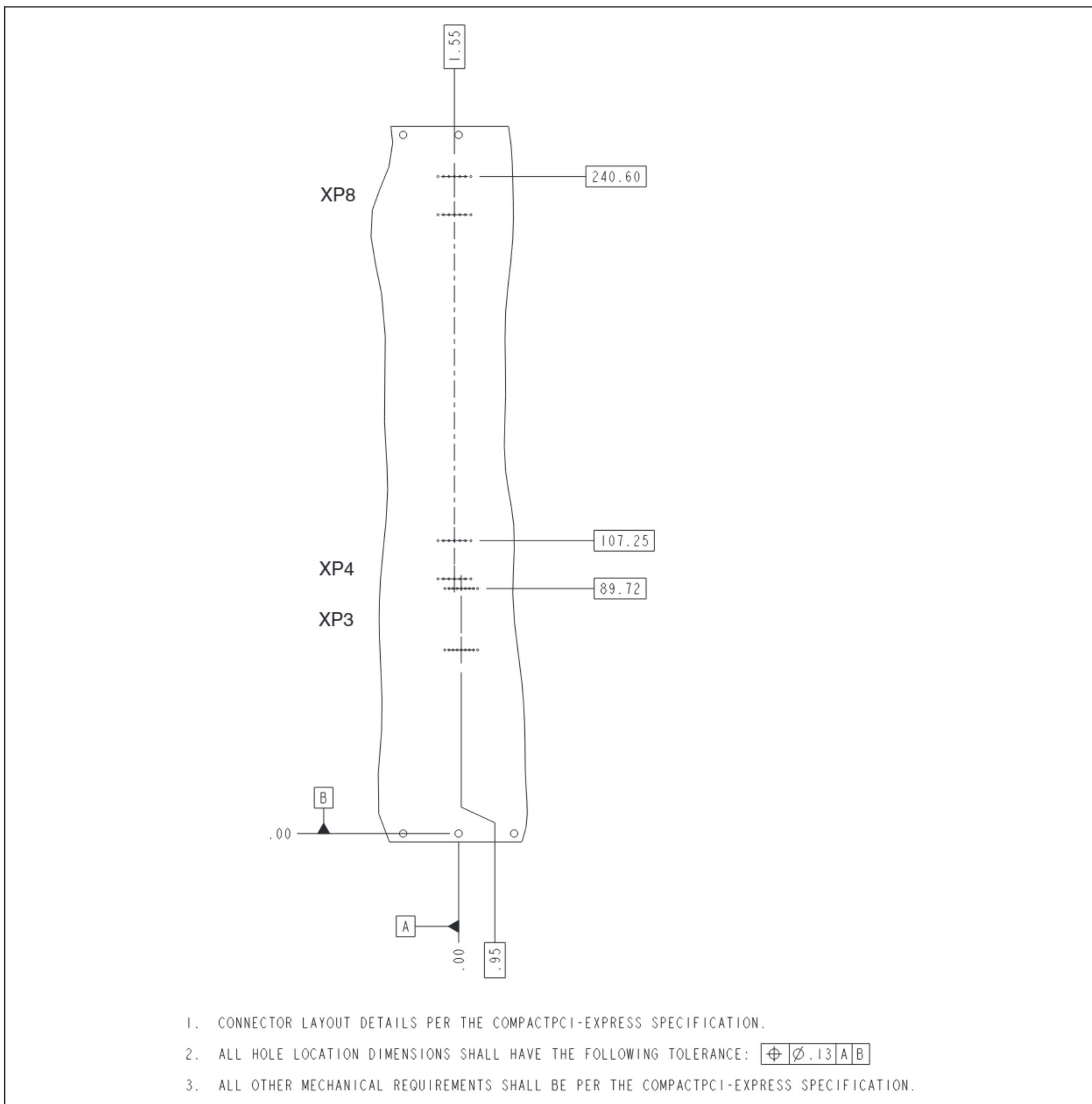
规则：3U 和 6U PXI Express 系统插槽应满足 CompactPCI Express 规范中定义的机械要求。

许可：与 CompactPCI Express 一样，如果需要用于后置 I/O 应用，6U 系统插槽可以使用 J3/J4/J5。

3.6.4.2 Peripheral Slot

规则：3U PXI Express 外设插槽应满足 CompactPCI Express 规范中定义的 3U Type 2 外设插槽的机械要求。

规则：6U PXI Express 外设插槽应满足 CompactPCI Express 规范中定义的 6U Type 2 外设插槽的机械要求，但应在图 3-3 所示的位置填充一个额外的 XP8 eHM 连接器。

**Figure 3-3. 6U PXI Express Peripheral Slot**

3.6.4.3 PXI Express Hybrid Peripheral Slot

RULE: 3U PXI Express Hybrid Peripheral Slots SHALL meet the mechanical requirements for 3U Hybrid Peripheral Slots as defined in the CompactPCI Express specification.

RULE: 6U PXI Express Hybrid Peripheral Slots SHALL meet the mechanical requirements for 6U Hybrid Peripheral Slots as defined in the CompactPCI Express (PICMG EXP.0) specification, with the exceptions that the XP8 eHM connector SHALL be populated in the position shown in Figure 3-4, and the legacy P3/P4/P5 connectors SHALL NOT be used.

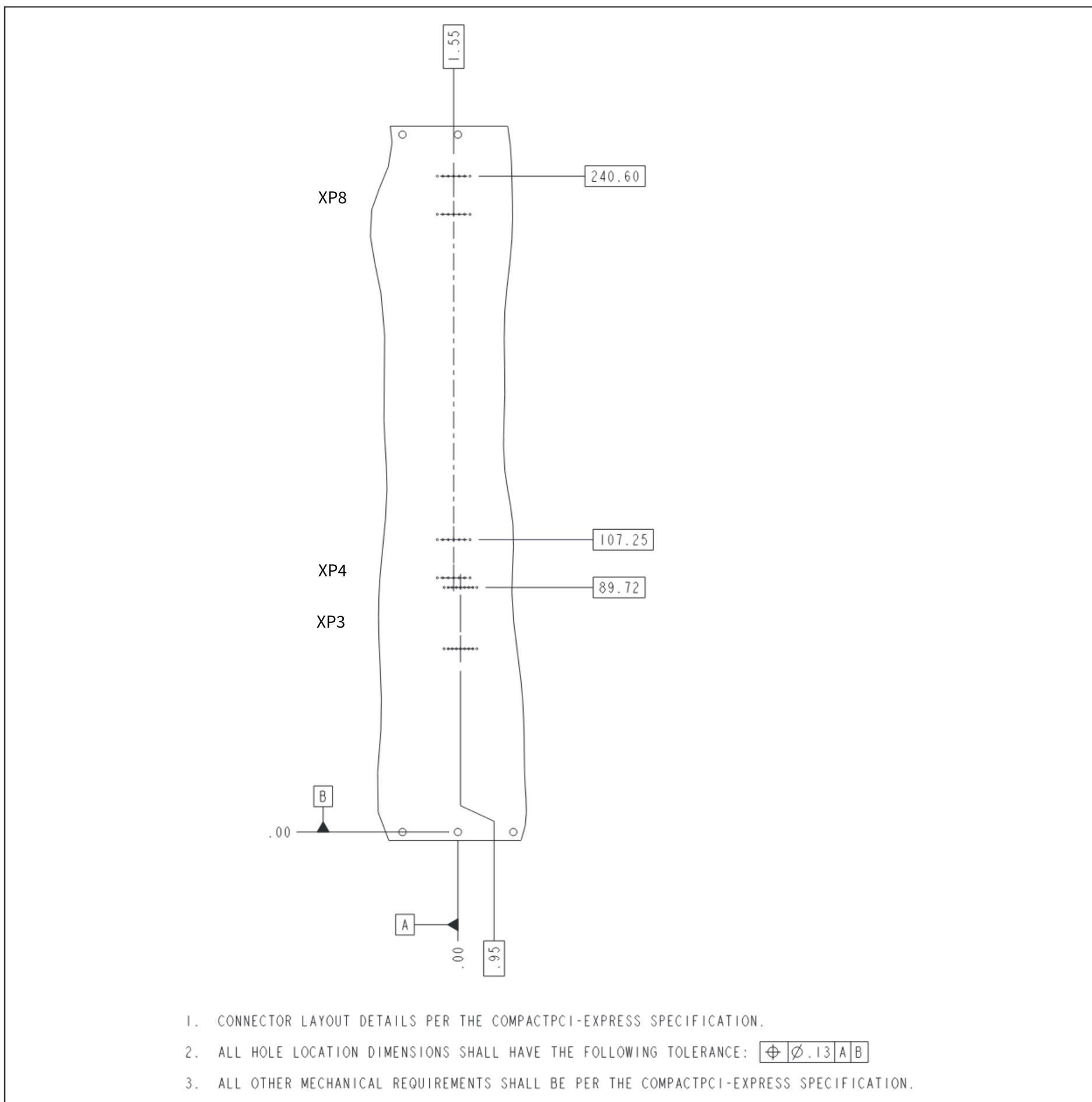


图 3-3.6U PXI Express 外设插槽

3.6.4.3 PXI Express 混合外设插槽

规则：3U PXI Express 混合外设插槽应满足 CompactPCI Express 规范中定义的 3U 混合外设插槽的机械要求。

规则：6U PXI Express 混合外设插槽应满足 CompactPCI Express (PICMG EXP.0) 规范中定义的 6U 混合外设插槽的机械要求，但 XP8 eHM 连接器应填充在图 3-4 所示的位置，并且不应使用旧版 P3/P4/P5 连接器。

3. Mechanical Requirements

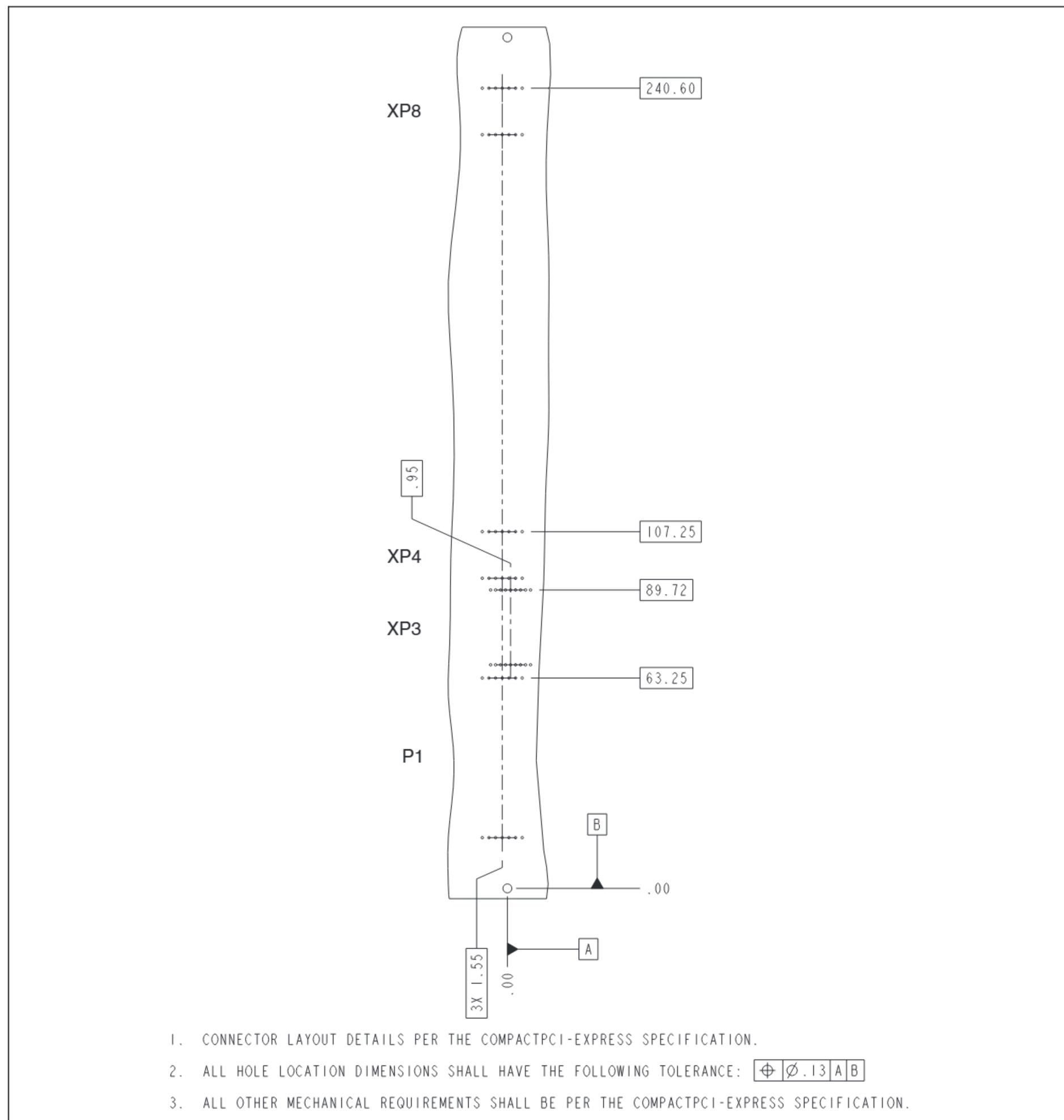


Figure 3-4. 6U PXI Express Hybrid Slot

3.7 New Module and Slot Types

3.7.1 PXI Express System Timing Module Requirements

RULE: 3U PXI Express System Timing Modules SHALL meet the mechanical requirements as defined in Figure 3-5.

3. 机械要求

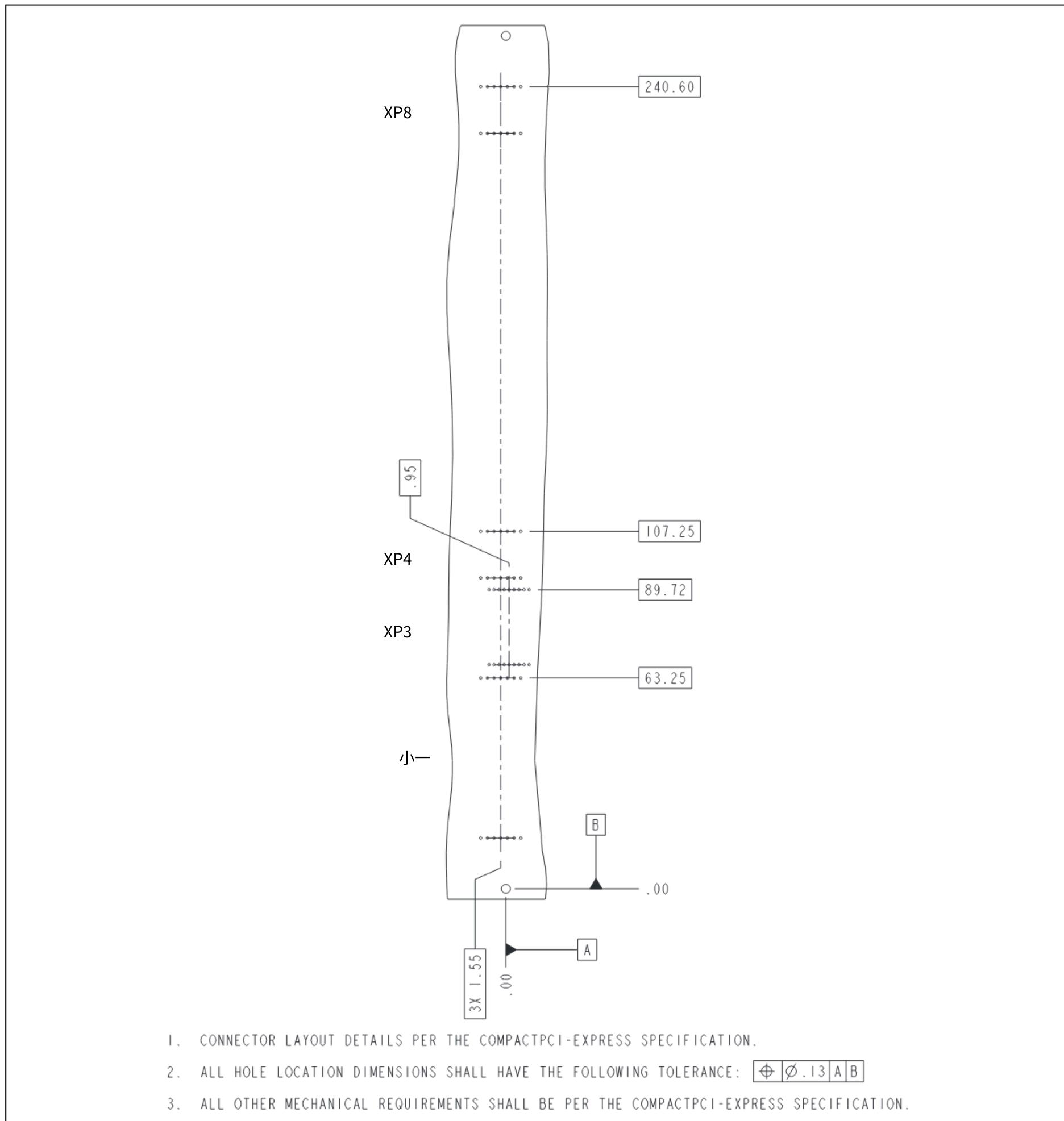


图 3-4.6U PXI Express 混合插槽

3.7 新的模块和插槽类型

3.7.1 PXI Express 系统定时模块要求

规则：3U PXI Express 系统定时模块应满足图 3-5 中定义的机械要求。

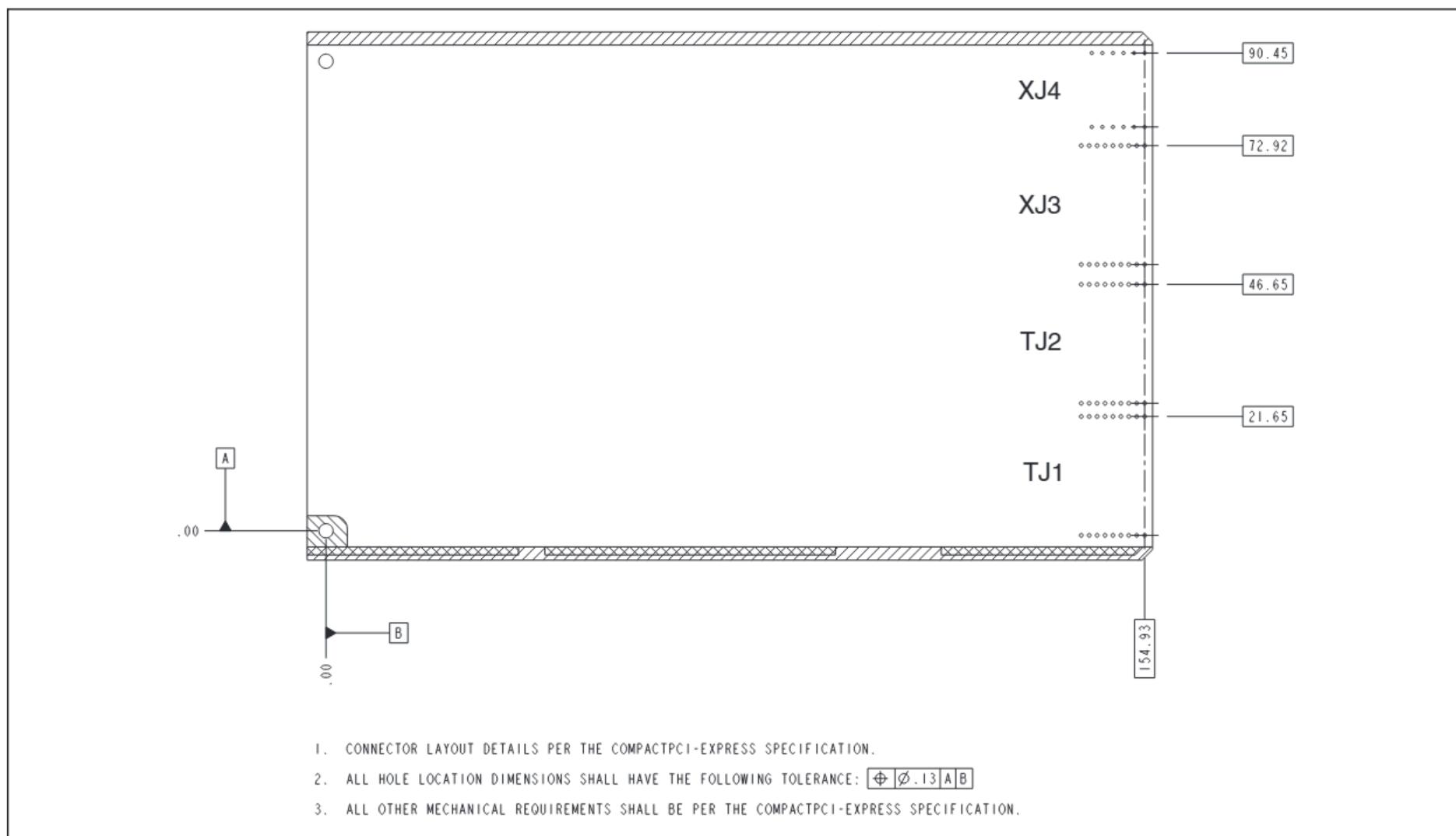


Figure 3-5. 3U PXI Express System Timing Module PCB



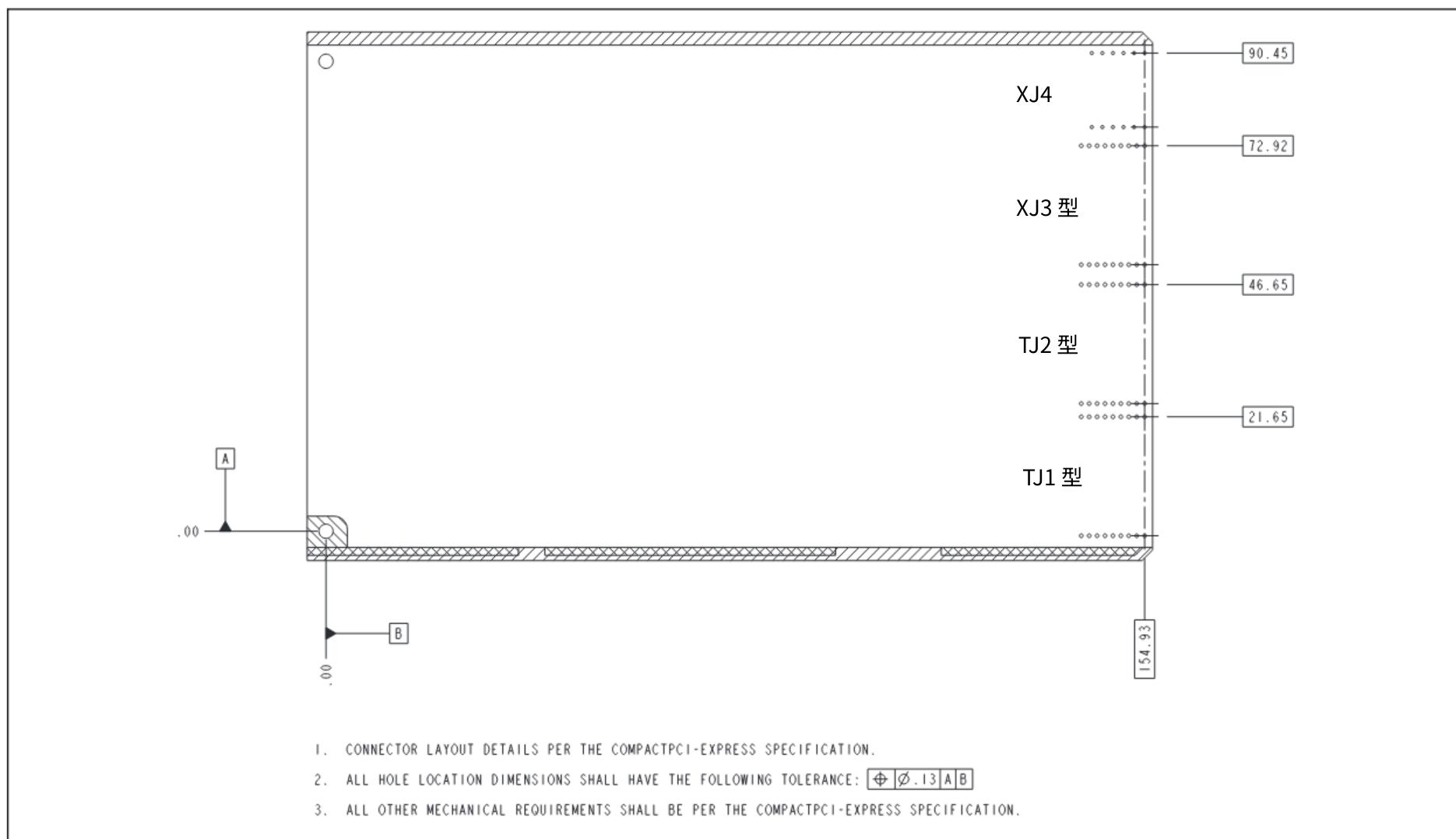


图 3-5.3U PXI Express 系统时序模块 PCB



3. Mechanical Requirements

RULE: 6U PXI Express System Timing Module PCBs SHALL meet the mechanical requirements as defined in Figure 3-6.

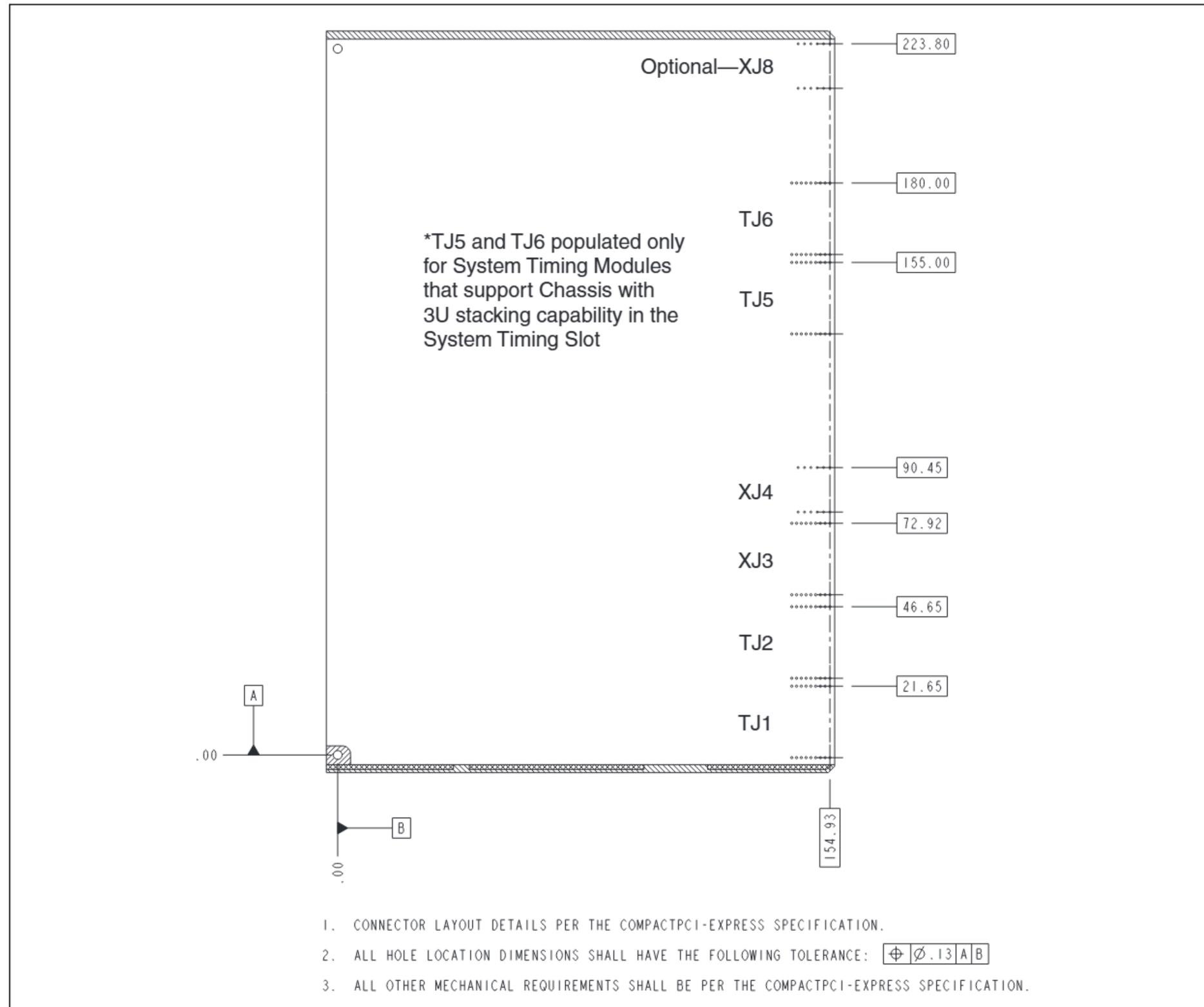


Figure 3-6. 6U PXI Express System Timing Module PCB

PERMISSION: A 6U PXI Express System Timing Module MAY populate TJ5 and TJ6 connectors to allow it to be used in a Chassis that requires such a Module to provide enough star triggers or differential triggers, or in a Chassis that supports stacking 3U System Timing Modules.

3.7.2 Backplane Requirements for New Slot Types

RULE: 3U and 6U PXI Express backplanes SHALL meet the size, mechanical mounting hole, and tolerance requirements as defined in the CompactPCI Express specification.

Requirements for the various connector locations are defined in further detail in the following sections.

3.7.2.1 PXI Express System Timing Slot Requirements

RULE: 3U PXI Express System Timing Slots SHALL meet the mechanical requirements as defined in Figure 3-7.

3. 机械要求

规则：6U PXI Express 系统定时模块 PCB 应满足图 3-6 中定义的机械要求。

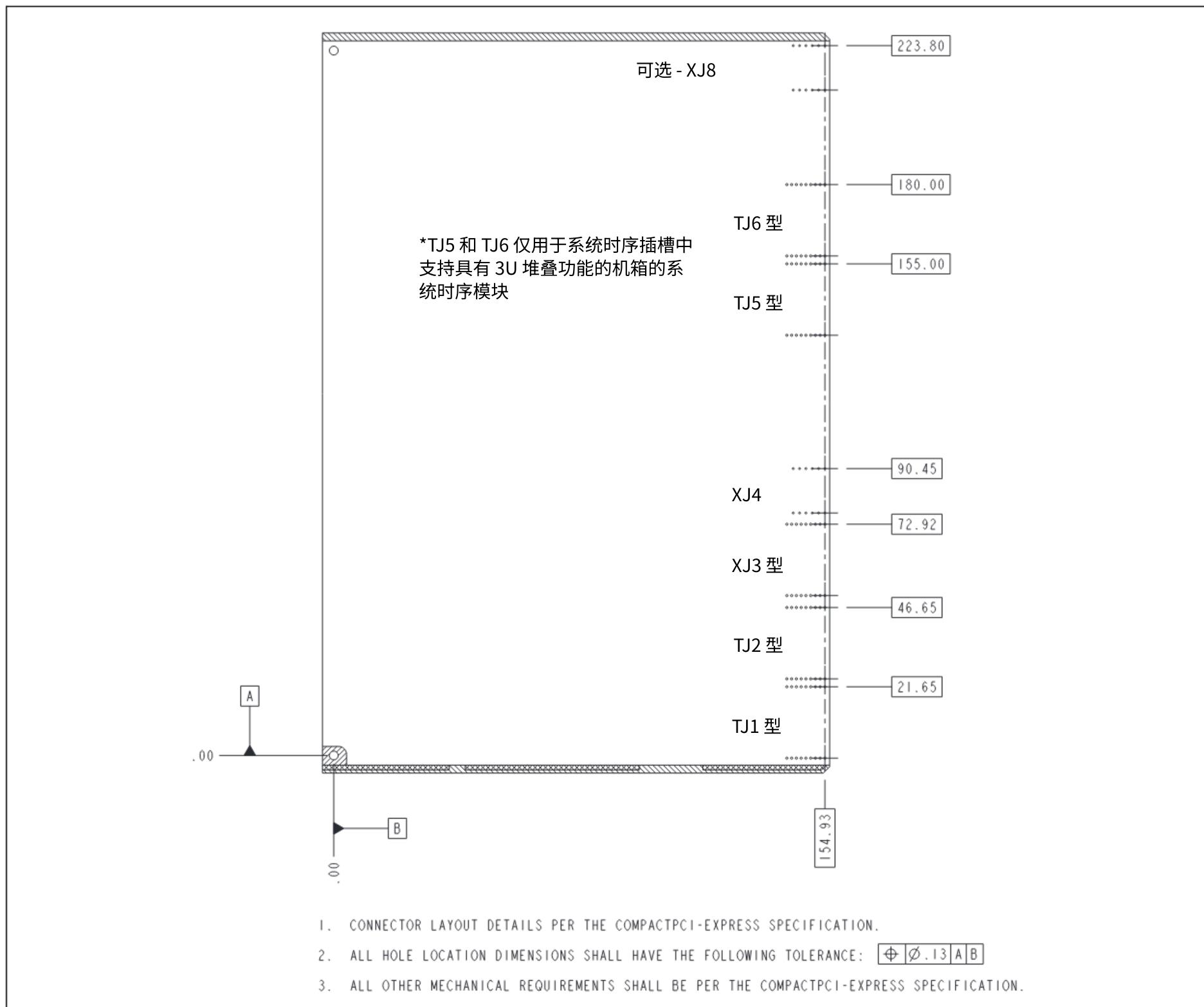


图 3-6.6U PXI Express 系统定时模块 PCB

许可：6U PXI Express 系统时序模块可以填充 TJ5 和 TJ6 连接器，以允许其用于需要此类模块提供足够星形触发器或差分触发器的机箱，或支持堆叠 3U 系统时序模块的机箱中。

3.7.2 新插槽类型的背板要求

规则：3U 和 6U PXI Express 背板应满足 CompactPCI Express 规范中定义的尺寸、机械安装孔和公差要求。

以下部分将进一步详细定义各种连接器位置的要求。

3.7.2.1 PXI Express 系统时序插槽要求

规则：3U PXI Express 系统定时插槽应满足图 3-7 中定义的机械要求。

RULE: 6U PXI Express System Timing Slots SHALL meet the mechanical requirements as defined in Figure 3-8.

RULE: 6U PXI Express System Timing Slots that support stacking 3U System Timing Modules SHALL meet the mechanical requirements as defined in Figure 3-9.

RULE: If the TP1 connector is not populated on a System Timing Slot, there SHALL be a 2.2 mm maximum component height restriction zone on the backplane where the TP1 connector would normally be to avoid interference with System Timing Modules that have TJ1 populated.

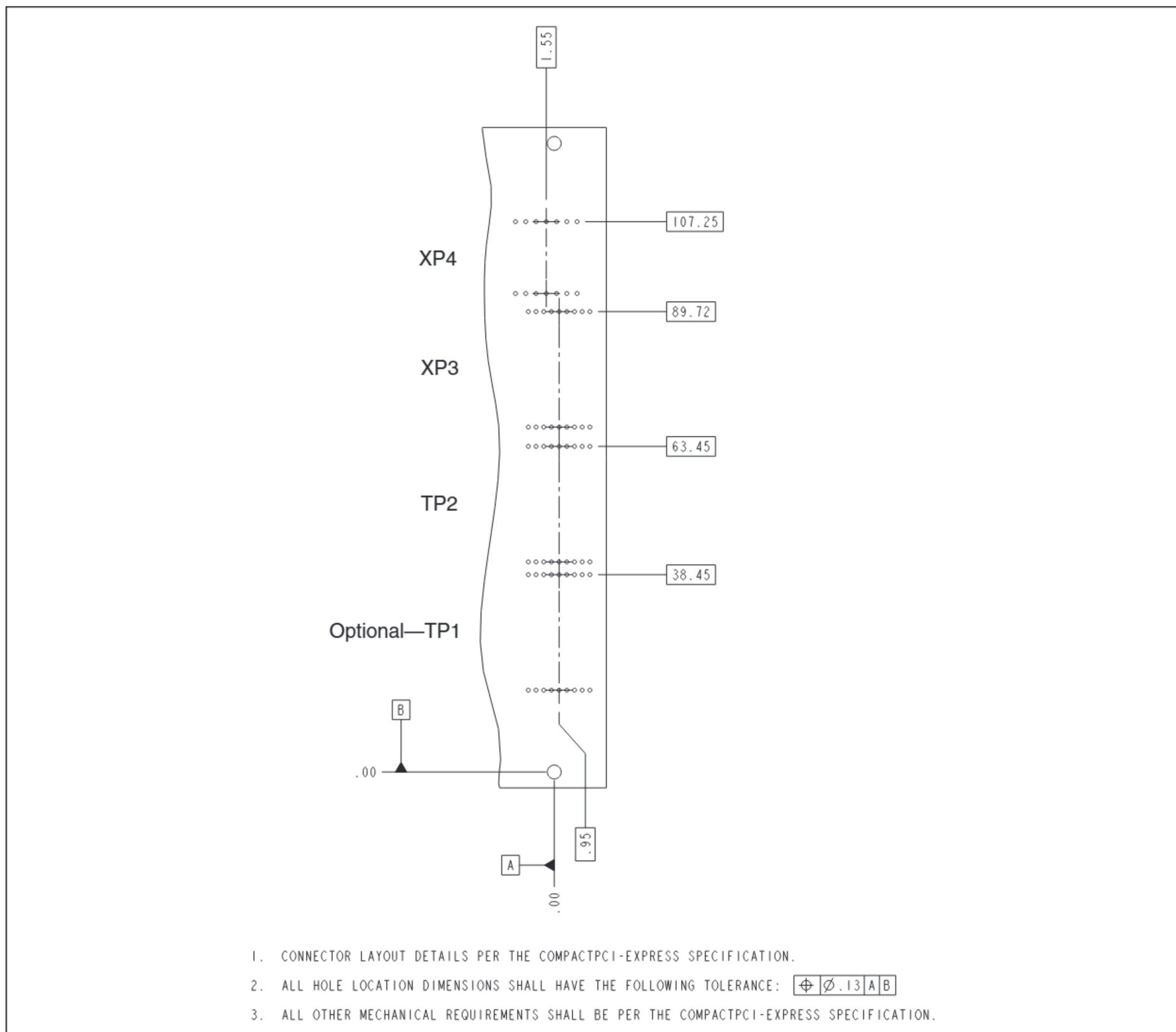


Figure 3-7. 3U PXI Express System Timing Slot Backplane Dimensions

规则：6U PXI Express 系统定时插槽应满足图 3-8 中定义的机械要求。

规则：支持堆叠的 6U PXI Express 系统时序插槽 3U 系统时序模块应满足图 3-9 中定义的机械要求。

规则：如果 TP1 连接器未安装在系统定时插槽上，则背板上应有一个 2.2 毫米的最大组件高度限制区域，TP1 连接器通常位于该区域，以避免干扰已填充 TJ1 的系统定时模块。

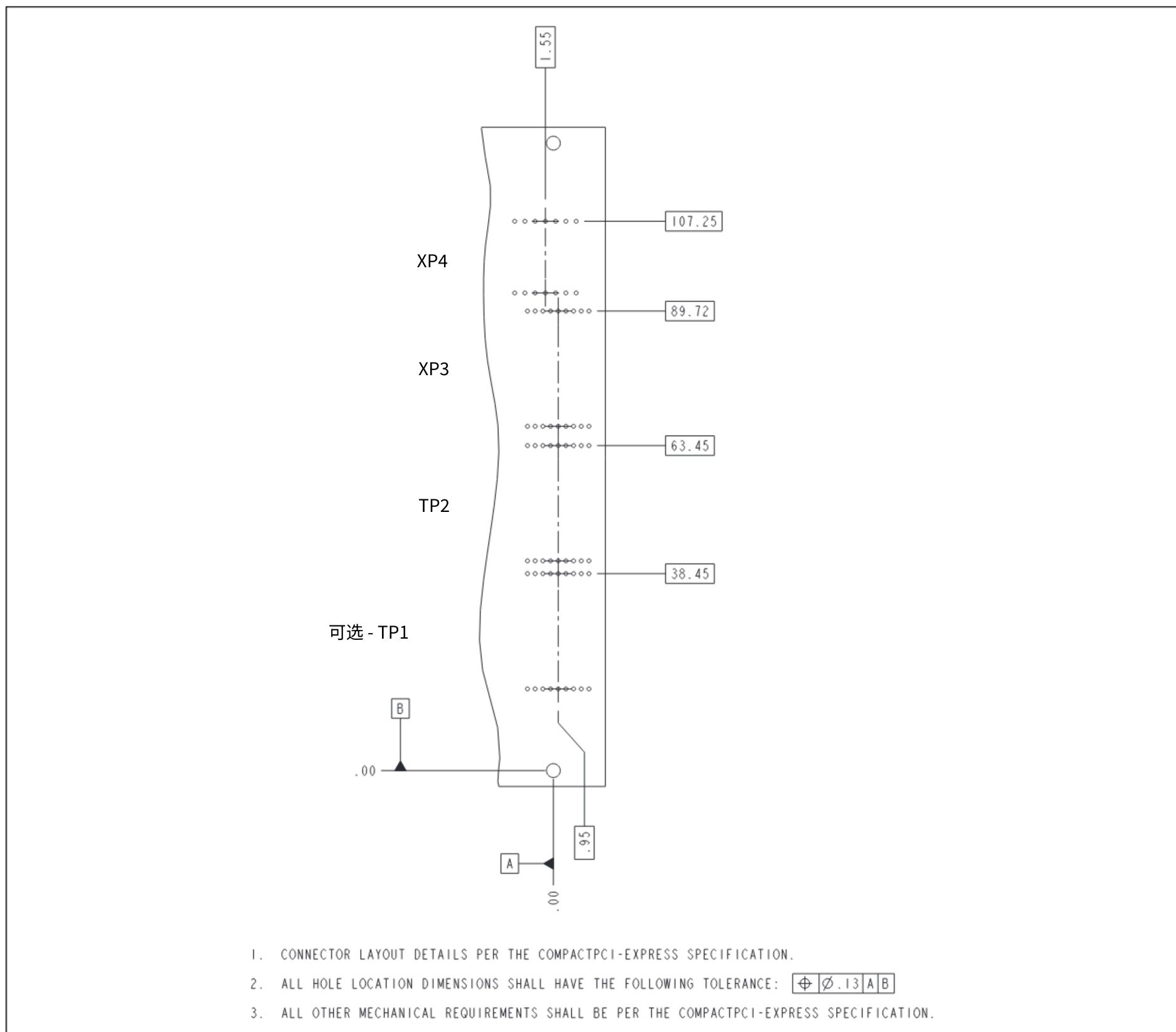


图 3-7.3U PXI Express 系统定时插槽背板尺寸

3. Mechanical Requirements

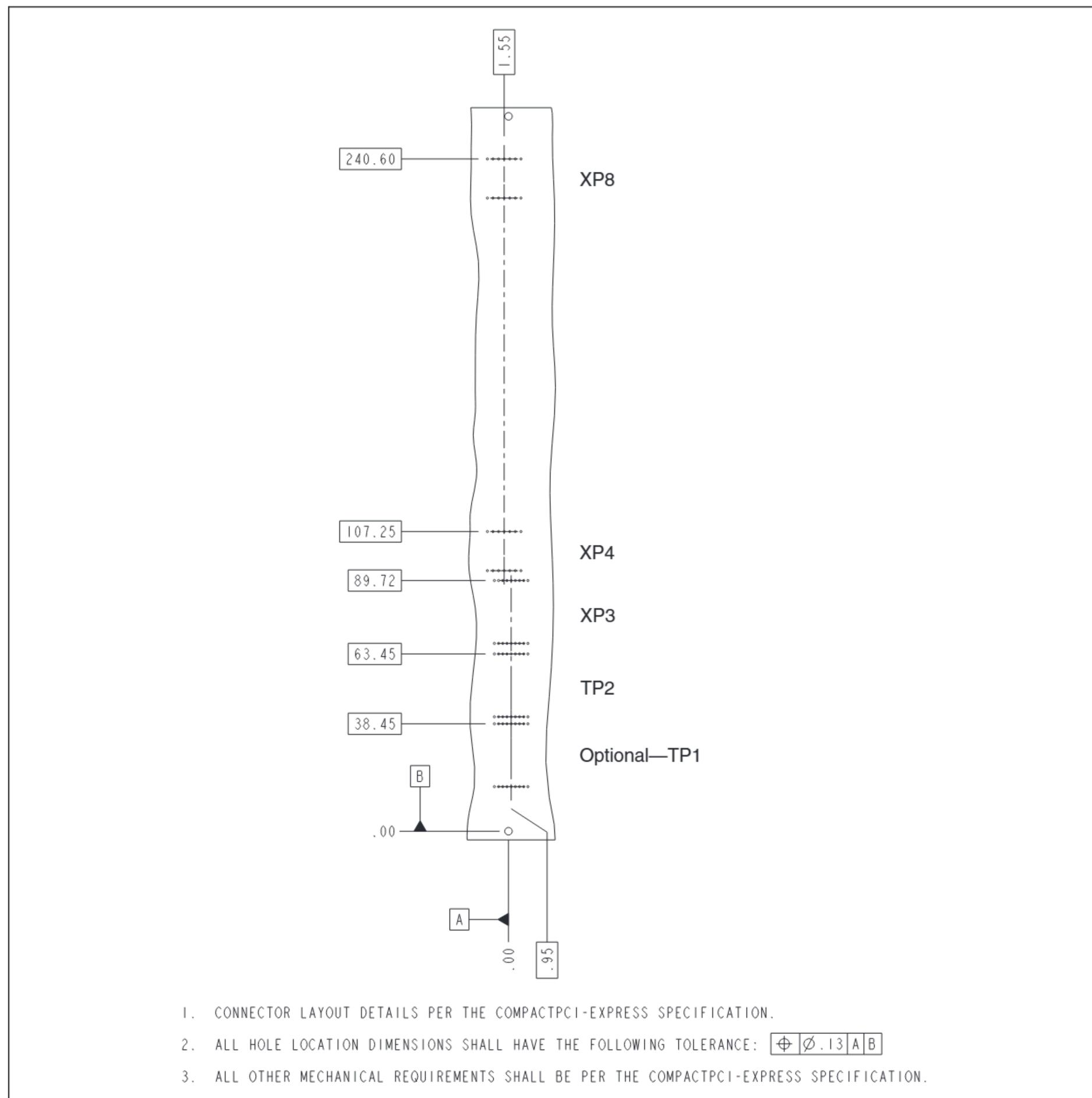


Figure 3-8. 6U PXI Express System Timing Slot Backplane Dimensions

3. 机械要求

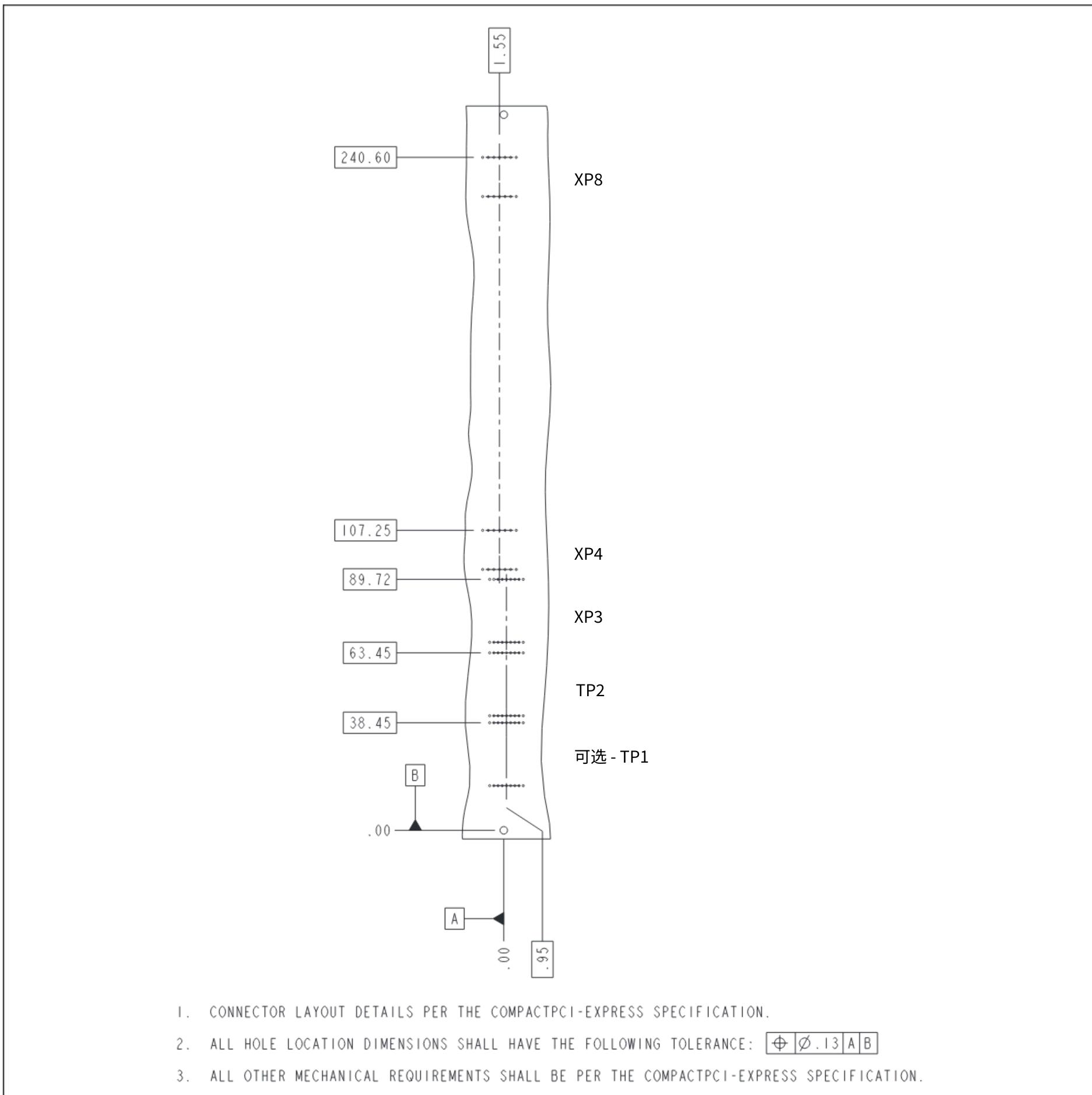


图 3-8.6U PXI Express 系统定时插槽背板尺寸

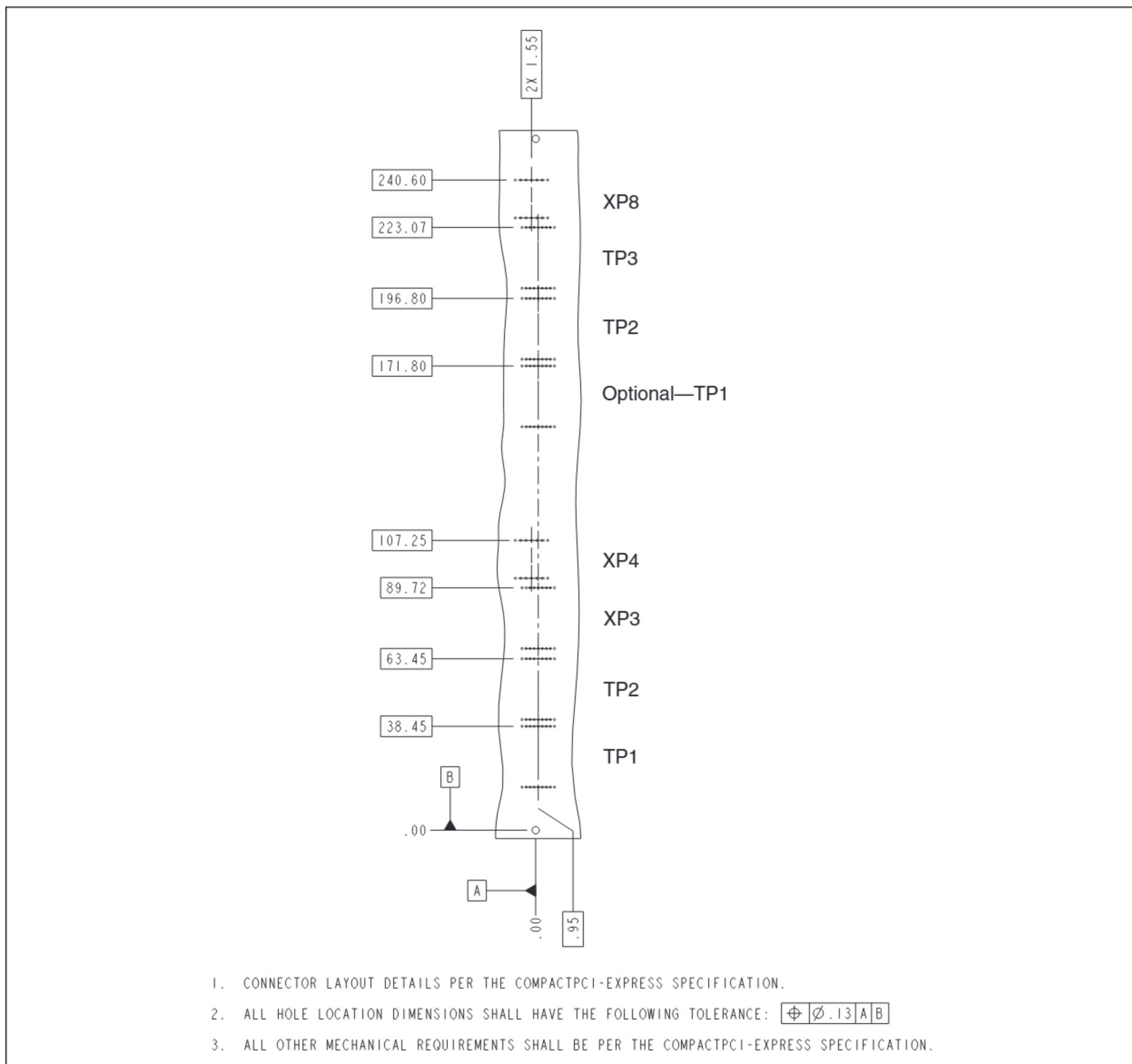


Figure 3-9. 6U PXI Express System Timing Slot with Stacked Support Backplane Dimensions

RULE: For applications where the backplane TP1 connector is Optional, there SHALL be a 2.2 mm max high component keep out region on the backplane in the TP1 area to avoid interference with timing Modules that have TJ1 populated.

PERMISSION: If a 3U PXI Express backplane can connect all slots that can connect to star triggers and differential triggers via the TP2 connector, the TP1 connector MAY NOT be populated.

PERMISSION: A 6U PXI Express backplane, to provide enough differential triggers and star triggers to all slots that can connect to them, could support either stacking two 3U System Timing Modules or a 6U System Timing Module with additional connectors. If such a 6U PXI Express backplane can connect all slots that can connect to star triggers and differential triggers without using the TP5 connector, the TP5 connector MAY NOT be populated.

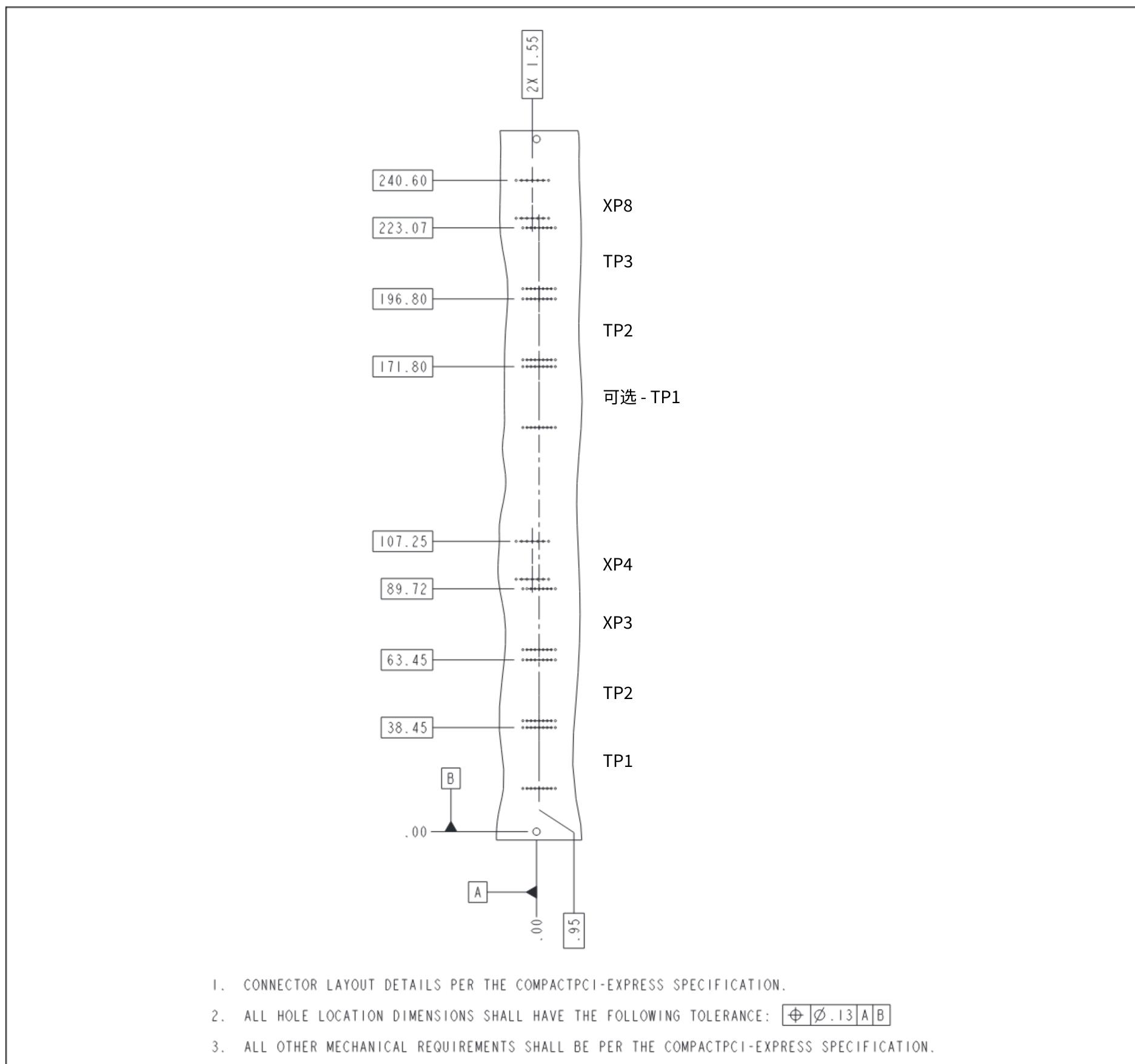


图 3-9.6U PXI Express 系统时序插槽，带堆叠支撑背板尺寸

规则：对于背板 TP1 连接器是可选的应用，背板上的 TP2.2 区域应有一个最大 1 毫米高的分量禁区，以避免干扰装有 TJ1 的定时模块。

权限：如果 3U PXI Express 背板可以通过 TP2 连接器连接所有可连接到星形触发器和差分触发器的插槽，则 TP1 连接器可能不会被填充。

许可：6U PXI Express 背板可以为所有可以连接到它们的插槽提供足够的差分触发器和星形触发器，可以支持堆叠两个 3U 系统时序模块或一个带有附加连接器的 6U 系统时序模块。如果这样的 6U PXI Express 背板可以在不使用 TP5 连接器的情况下连接所有可以连接到星形触发器和差分触发器的插槽，则 TP5 连接器可能不会被填充。

3.8 Requirements for Stacking 3U Modules in 6U Slots

Just as with the PXI-1 specification, PXI Express allows for efficient use of 3U Modules in a 6U Chassis.

Mechanically, this configuration can be accomplished by making use of center extrusions fixed within the Chassis to physically support the insertion, extraction, and mounting of the lower and upper 3U Modules residing in a 6U Slot. Alternatively, this may be accomplished mechanically by a stacking adapter attached to the two 3U Modules prior to insertion into the 6U Slot. Figure 2-18 shows an example of a 6U Chassis that supports stacking 3U Modules.

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL populate the appropriate connectors in the lower half of the 6U Slot to implement a lower 3U Slot according to the type of 3U Slot being implemented (System, Hybrid, PXI Express Peripheral, PXI-1, or System Timing Slot).

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL populate the appropriate connectors in the upper half of the 6U Slot to implement an upper 3U Slot according to the type of 3U Slot being implemented (Hybrid, PXI Express Peripheral, PXI-1, or System Timing Slot).

RULE: Table 3-1 shows the upper 3U Slot that SHALL and SHALL NOT be implemented based on how the lower 3U Slot is implemented within a 6U Slot of a PXI Express Chassis that supports stacking 3U Modules.

Table 3-1. Upper and Lower 3U Slot Implementation

Lower 3U Slot	Upper 3U Slot				
	System	PXIe Peripheral	System Timing	Hybrid Peripheral	PXI 2.X Peripheral
System	No	Yes	No	Yes	Yes
PXIe Peripheral	No	Yes	No	Yes	No
System Timing	No	Yes	Yes	No	No
Hybrid Peripheral	No	Yes	No	Yes	No
PXI 2.X Peripheral	No	Yes	No	Yes	Yes



OBSERVATION: An upper 3U System Timing Slot is not allowed above any slot other than the lower 3U System Timing Slot.

OBSERVATION: Upper 3U System Slots are not allowed.

OBSERVATION: A lower slot that is a PXI Express Peripheral Slot, System Timing Slot, or a Hybrid Peripheral Slot cannot have a PXI-1 Peripheral Slot in the upper position. This is so a 6U Module can have the upper eHM connector for extra power and still plug into 6U Slots that support stacking 3U Modules.

3.9 PXI Logo

PXI Express products use the same logo as PXI products. PXI Express Peripheral Modules, PXI Express System Modules, PXI Express System Timing Modules, and PXI Express Chassis may have the PXI Express logo on their marketing material, datasheets, and manuals to help customers identify that the PXI products have PCI Express capabilities.

3.8 在 6U 插槽中堆叠 3U 模块的要求

与 PXI-1 规范一样，PXI Express 允许在 6U 机箱中高效使用 3U 模块。

在机械上，可以通过使用固定在机箱内的中心挤压件来物理支持驻留在 6U 插槽中的下部和上部 3U 模块的插入、拔出和安装来实现此配置。或者，这可以通过在插入 3U 插槽之前连接到两个 6U 模块的堆叠适配器来机械地完成。图 2-18 显示了支持堆叠 3U 模块的 6U 机箱的示例。

规则：支持堆叠 3U 模块的 6U PXI Express 机箱应根据所实施的 3U 插槽类型（系统、混合、PXI Express 外设、PXI-1 或系统时序插槽）在 6U 插槽的下半部分填充适当的连接器，以实现较低的 3U 插槽。

规则：支持堆叠 3U 模块的 6U PXI Express 机箱应根据所实施的 3U 插槽类型（混合、PXI Express 外设、PXI-1 或系统时序插槽）在 6U 插槽的上半部分填充适当的连接器，以实现上 3U 插槽。

规则：表 3-1 显示了根据支持堆叠 3U 模块的 PXI Express 机箱的 6U 插槽中实现下部 3U 插槽的方式，应实现和不应实现的上层 3U 插槽。

表 3-1. 上 3U 插槽和下 3U 插槽实现

较低的 3U 插槽	上 3U 插槽				
	系统	PXIe 外设	系统时序	混合 外设	PXI 2.X 外设
系统	不	是的	不	是的	是的
PXIe 外设	不	是的	不	是的	不
系统时序	不	是的	是的	不	不
混合 外设	不	是的	不	是的	不
PXI 2.X 外设	不	是的	不	是的	是的

观察：除较低的 3U 系统时序插槽外，不允许在较低的 3U 系统时序插槽之外的任何插槽上方放置上层 3U 系统时序插槽。

观察：不允许使用上层 3U 系统插槽。

观察：作为 PXI Express 外设插槽、系统时序插槽或混合外设插槽的下部插槽不能在上部位置有 PXI-1 外设插槽。这样，6U 模块就可以具有上部 eHM 连接器以获得额外电源，并且仍然可以插入支持堆叠 3U 模块的 6U 插槽。

3.9 PXI 徽标

PXI Express 产品使用与 PXI 产品相同的徽标。PXI Express 外设模块、PXI Express 系统模块、PXI Express 系统定时模块和 PXI Express 机箱的营销材料、数据表和手册上可能带有 PXI Express 徽标，以帮助客户识别 PXI 产品具有 PCI Express 功能。

PERMISSION: Vendors who are members of the PXI Systems Alliance MAY use the PXI logo as defined below on either the front panel or the injector/ejector handle of products claiming full compliance with the *PXI Express Hardware Specification*.

RULE: If the PXI logo is used, the vendor SHALL obtain a license to use the trademarked logo from the PXI System Alliance.

RULE: If the PXI logo is used, it SHALL NOT be altered in any way other than scale. The logo SHALL NOT incorporate any additions.

Figure 3-10 shows the PXI logo. PXI Systems Alliance members can obtain logo artwork and the license from the alliance.



Figure 3-10. PXI Logo

RULE: Vendors who are members of the PXI Systems Alliance SHALL NOT use the PXI Express logo as defined below on any part of PXI or PXI Express hardware products.

PERMISSION: Vendors who are members of the PXI Systems Alliance MAY use the PXI Express logo as defined below in the marketing material, datasheets, and manuals of PXI Express Peripheral Modules, PXI Express System Modules, PXI Express System Timing Modules, and PXI Express Chassis claiming full compliance with the *PXI Express Hardware Specification*.

RULE: If the PXI Express logo is used, the vendor SHALL obtain a license to use the trademarked logo from the PXI System Alliance.

RULE: If the PXI Express logo is used, it SHALL NOT be altered in any way other than scale. The logo SHALL NOT incorporate any additions.

Figure 3-11 shows the PXI Express logo. PXI Systems Alliance members can obtain logo artwork and the license from the alliance.



Figure 3-11. PXI Express Logo

3.10 Chassis with Built-In System Modules

PERMISSION: A PXI Express Chassis MAY have a built-in System Module and therefore not have a System Slot.

许可：作为 PXI 系统联盟成员的供应商可以在声称完全符合 PXI Express 硬件规范的产品的前面板或进样器/顶出器手柄上使用下述定义的 PXI 徽标。

规则：如果使用 PXI 徽标，则供应商应从 PXI 系统联盟获得使用商标徽标的许可。

规则：如果使用 PXI 徽标，则不得以比例以外的任何方式更改。徽标不得包含任何添加内容。

图 3-10 显示了 PXI 徽标。PXI 系统联盟成员可以从联盟获得徽标图稿和许可证。



图 3-10.PXI 徽标

规则：PXI 系统联盟成员的供应商不得在 PXI 或 PXI Express 硬件产品的任何部分使用下述定义的 PXI Express 徽标。

许可：PXI 系统联盟成员的供应商可以使用 PXI Express 外设模块、PXI Express 系统模块、PXI Express 系统定时模块和 PXI Express 机箱的营销材料、数据表和手册中定义的 PXI Express 徽标，并声称完全符合 PXI Express 硬件规范。

规则：如果使用 PXI Express 徽标，则供应商应从 PXI 系统联盟获得使用商标徽标的许可。



规则：如果使用 PXI Express 徽标，则不得以比例以外的任何方式更改。徽标不得包含任何添加内容。

图 3-11 显示了 PXI Express 徽标。PXI 系统联盟成员可以从联盟获得徽标图稿和许可证。



图 3-11.PXI Express 徽标

3.10 内置系统模块的机箱

权限：PXI Express 机箱可能具有内置系统模块，因此没有系统插槽。

3.11 Cooling Requirements

3.11.1 Module Cooling Requirements

RULE: Modules SHALL be designed to allow a suitable airflow path from bottom to the top of the Module as shown in Figure 3-12.

OBSERVATION: Airflow, and thus cooling, through a Module depends on the Chassis as well as the Module design. Modules with a lower airflow resistance will receive more airflow, and those with higher resistance will receive less air flow for a given Chassis.

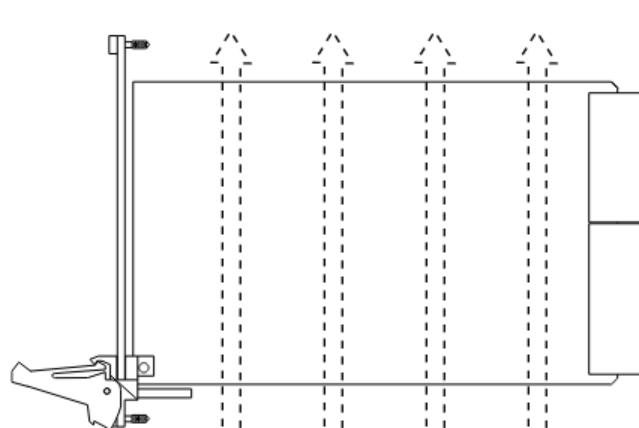


Figure 3-12. Cooling Airflow Direction in a PXI Express System

RULE: Module manufacturers SHALL document and make available to the customer the nominal and peak power dissipated by the Module, by voltage rail, under normal operating conditions.

RECOMMENDATION: Single-width 3U Modules SHOULD NOT dissipate more than 30 W within the Chassis.

RECOMMENDATION: Single-width 6U Modules SHOULD NOT dissipate more than 60 W within the Chassis.

OBSERVATION: 6U Chassis typically require more airflow per slot than a 3U Chassis for a given ambient temperature specification due to preheating effects



3.11.2 Chassis Cooling Requirements

RULE: Chassis SHALL provide forced airflow that flows from the bottom to the top of a Module as shown in Figure 3-12.

OBSERVATION: For typical Chassis configurations, the airflow through a slot will be flowing against gravity or upwards, (that is, in the same direction of naturally rising hot air). This specification does not, however, preclude other Module orientations such as horizontal.

RULE: Chassis manufacturers SHALL document and make available to the customer the maximum total power that a given Chassis can dissipate within the Subrack and the maximum power it can dissipate for the worst-case slot. Furthermore, the manufacturer SHALL document and make available to the customer the specific test procedure used to determine these power dissipation levels.

RECOMMENDATION: The worst-case slot power dissipation value SHOULD be based not only on how much power may be available to a given slot, but also on the cooling capabilities of the Chassis for the worst-case slot.

RECOMMENDATION: Thermal load cards SHOULD be used in all Chassis slots while determining the cooling capabilities for the Chassis and the worst slot.

3.11 冷却要求

3.11.1 模块冷却要求

规则：模块的设计应允许从模块底部到顶部的合适气流路径，如图 3-12 所示。

观察：通过模块的气流和冷却取决于机箱和模块设计。对于给定的机箱，气流阻力较低的模块将接收更多的气流，而阻力较高的模块将接收到较少的气流。

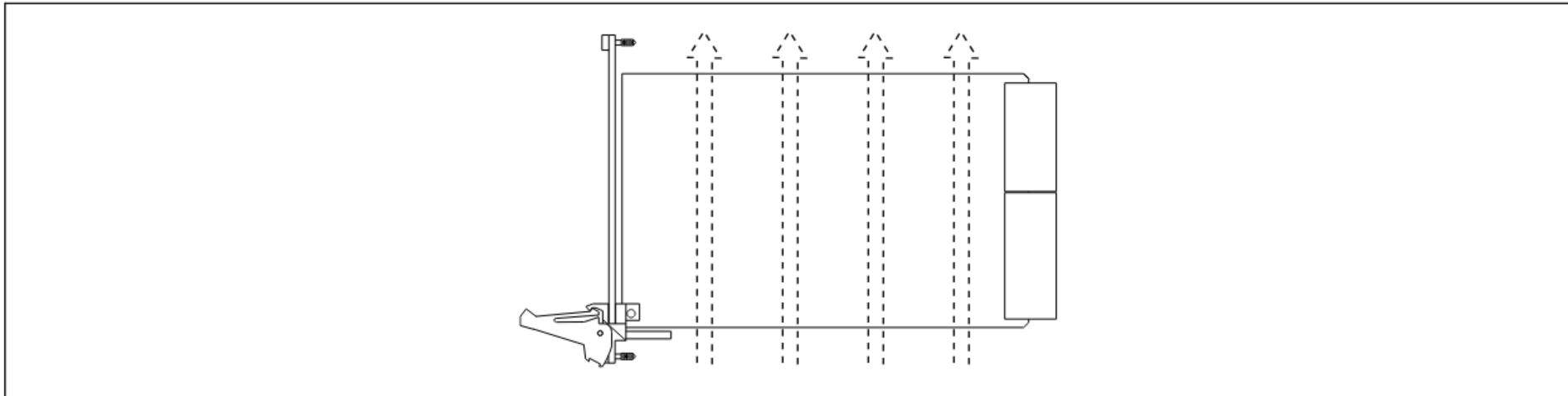


图 3-12.PXI Express 系统中的冷却气流方向

规则：模块制造商应记录并向客户提供模块在正常工作条件下通过电压轨耗散的标称功率和峰值功率。

建议：单宽 3U 模块在机箱内的功耗不应超过 30 W。

建议：单宽 6U 模块在机箱内的功耗不应超过 60 W。



观察：由于预热效应，对于给定的环境温度规格，6U 机箱通常比 3U 机箱需要每个插槽更多的气流

3.11.2 机箱冷却要求

规则：机箱应提供从模块底部流向顶部的强制气流，如图 3-12 所示。

观察：对于典型的底盘配置，通过槽的气流将逆重力或向上流动（即，直接在自然上升的热空气中流动）。但是，此规范并不排除其他模块方向，例如水平方向。

规则：机箱制造商应记录并向客户提供给定机箱在子机架内可以耗散的最大总功率，以及在最坏情况下插槽可以耗散的最大功率。此外，制造商应记录并向客户提供用于确定这些功耗水平的特定测试程序。

建议：最坏情况下的插槽功耗值不仅应基于给定插槽的可用功率，还应基于最坏情况下插槽的机箱冷却能力。

建议：在确定机箱和最差插槽的冷却能力时，应在所有机箱插槽中使用热负载卡。

RULE: PXI Chassis SHALL have filler panels installed in slots that do not have Modules populated.

OBSERVATION: If filler panels are not installed in slots that do not have populated Modules, proper Module cooling cannot be guaranteed.

3.12 Environmental Specifications

RECOMMENDATION: The environmental testing listed below SHOULD be carried out according to the procedures described in IEC 60068.

RULE: Test results and reports generated for environmental testing SHALL be made available to end users of PXI Express Systems. All manufacturers of PXI Express Chassis and Modules SHALL supply the required environmental ratings, as described below, for their products.

RECOMMENDATION: All manufacturers SHOULD provide the required environmental ratings, as described below, in their product datasheets.

RULE: If a manufacturer chooses to use environmental testing procedures other than those recommended above, these procedures, in addition to the test results and reports, SHALL be documented and made available to the customer.

OBSERVATION: It is the system integrator's responsibility to select Modules and Chassis appropriate for the application's environmental requirements.

3.12.1 Temperature Specifications

RULE: PXI Chassis and Modules SHALL be tested for storage and operating temperature ranges.

3.12.2 Humidity Specifications

RECOMMENDATION: PXI Express Chassis and Modules SHOULD be tested for humidity.



3.12.3 Vibration Specifications

RECOMMENDATION: PXI Express Chassis and Modules SHOULD be tested for vibration.

3.12.4 Acoustic Noise Specifications

RECOMMENDATION: All PXI Express Chassis SHOULD be tested for acoustic noise levels (A-weighted sound pressure level, L_{PA}). This acoustic testing SHOULD be carried out according to ISO-7779 on a standard test table at the operator position. Chassis testing SHOULD be conducted with the Chassis running at full load with front panels installed. If multiple fan speed options are available, the sound pressure levels SHALL be provided for the various fan speed options.

OBSERVATION: A-weighted sound power level, L_{WA} , may also be provided. This acoustic testing SHOULD be carried out according to ISO-7779 on a standard test table.

3.13 PXI Express Compatibility Glyphs

3.13.1 Module Glyphs

RULE: The PXI Express System Module compatibility glyph shown in Figure 3-13 SHALL be visible on front panels of PXI Express System Modules.

规则：PXI 机箱应将填充面板安装在未填充模块的插槽中。

观察：如果填充板未安装在未安装模块的插槽中，则无法保证适当的模块冷却。

3.12 环境规格

建议：下面列出的环境测试应按照 IEC 60068 中描述的程序进行。

规则：为环境测试生成的测试结果和报告应提供给 PXI Express 系统的最终用户。PXI Express 机箱和模块的所有制造商都应为其产品提供所需的环境等级，如下所述。

建议：所有制造商都应在其产品数据表中提供所需的环境等级，如下所述。

规则：如果制造商选择使用上述推荐以外的环境测试程序，则除了测试结果和报告外，这些程序还应记录在案并提供给客户。

观察：系统集成商有责任选择适合应用环境要求的模块和机箱。

3.12.1 温度规格

规则：PXI 机箱和模块应针对存储和工作温度范围进行测试。

3.12.2 湿度规格

建议：PXI Express 机箱和模块应进行湿度测试。

3.12.3 振动规格

建议：应对 PXI Express 机箱和模块进行振动测试。

3.12.4 声学噪声规格

建议：所有 PXI Express 机箱都应进行声学噪声级测试（A 加权声压级，L）。此声学测试应根据 ISO-7779 在操作员位置的标准测试台上进行。机箱测试应在机箱满载运行并安装前面板的情况下进行。如果有多个风扇速度选项可用，则应为各种风扇速度选项提供声压级。

观察：也可以提供 A 加权声功率级 L。该声学测试应根据 ISO-7779 在标准测试台上进行。

3.13 PXI Express 兼容性字形

3.13.1 模块字形

规则：图 3-13 所示的 PXI Express 系统模块兼容性字形应在 PXI Express 系统模块的前面板上可见。

3. Mechanical Requirements

RULE: The PXI Express Peripheral Module compatibility glyph shown in Figure 3-13 SHALL be visible on front panels of PXI Express Peripheral Modules.

RULE: The PXI Express System Timing Module compatibility glyph shown in Figure 3-13 SHALL be visible on front panels of PXI Express System Timing Modules.

OBSERVATION: PXI-1 Modules and Hybrid Slot Compatible PXI-1 Modules have visible the Peripheral Module glyph defined in the PXI-1 specification.

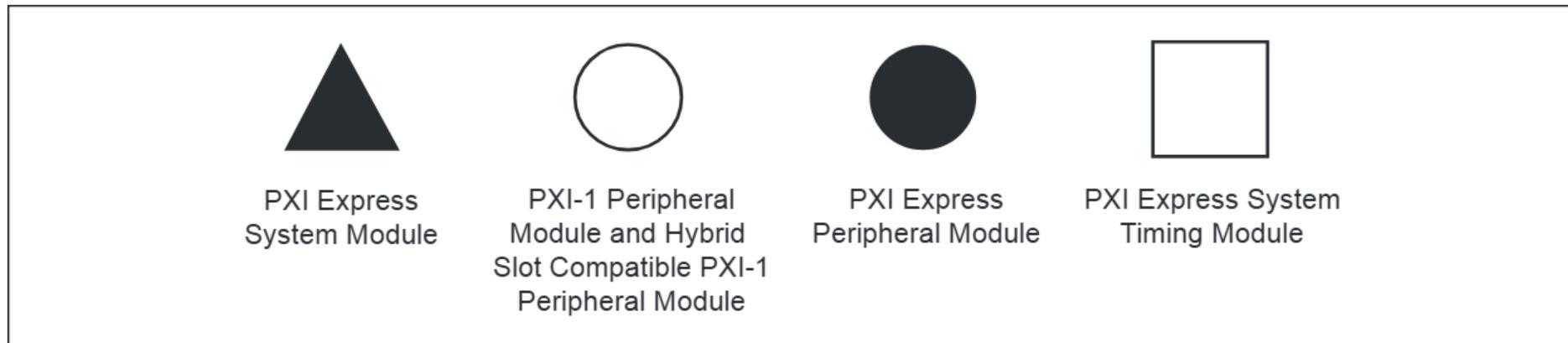


Figure 3-13. Module Glyphs

3.13.2 Chassis Slot Glyphs

RULE: The PXI Express System Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express System Slot on a PXI Express Chassis with the slot number indicated inside the glyph.

RULE: The PXI Express Peripheral Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express Peripheral Slots on a PXI Express Chassis with the slot number indicated inside the glyph.

RULE: The PXI Express Hybrid Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express Hybrid Slots on a PXI Express Chassis with the slot number indicated inside the glyph.

RULE: The PXI Express System Timing Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express System Timing Slot on a PXI Express Chassis with the slot number indicated inside the glyph.

OBSERVATION: PXI-1 Slots have visible the Peripheral Slot glyph defined in the PXI-1 specification.

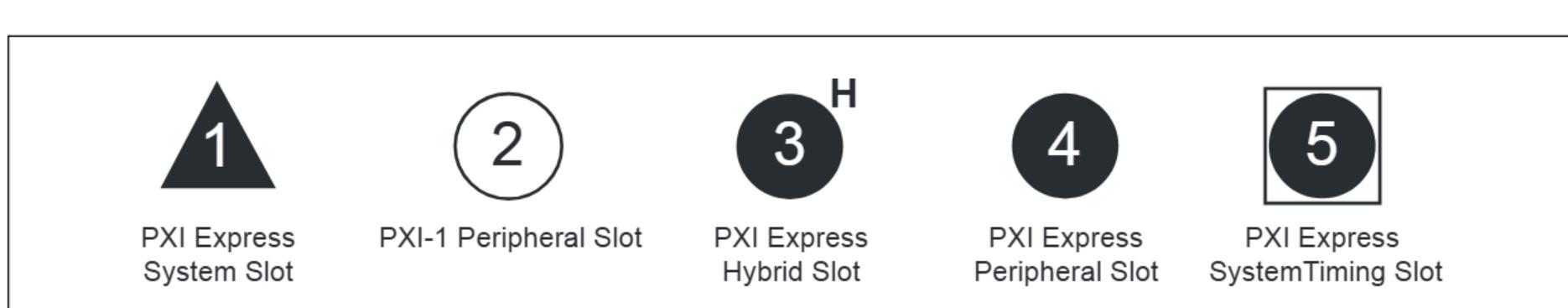


Figure 3-14. Slot Glyphs

3. 机械要求

规则：图 3-13 所示的 PXI Express 外设模块兼容性字形应在 PXI Express 外设模块的前面板上可见。

规则：图 3-13 所示的 PXI Express 系统定时模块兼容性字形应在 PXI Express 系统定时模块的前面板上可见。

观察：PXI-1 模块和混合插槽兼容 PXI-1 模块具有 PXI-1 规范中定义的外设模块字形。

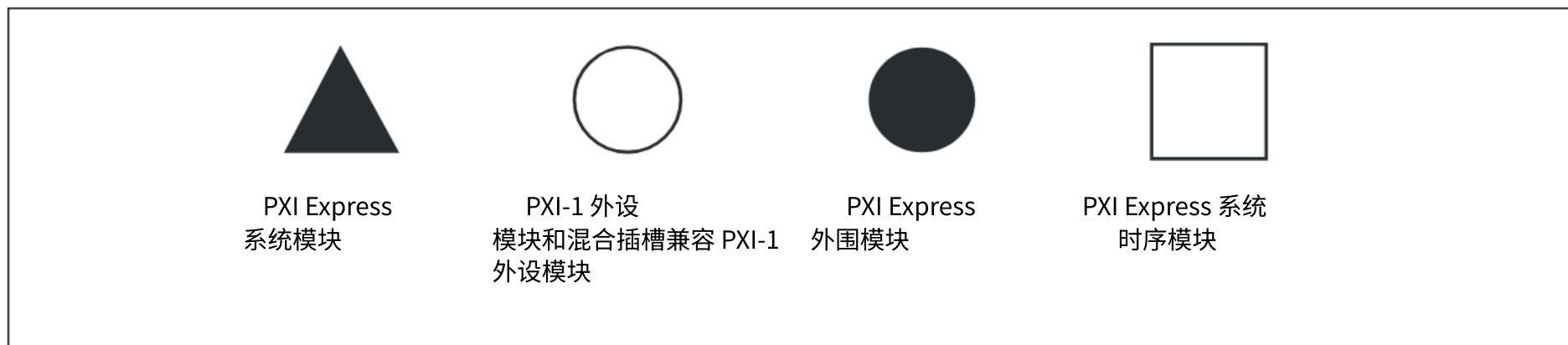


图 3-13.模块字形

3.13.2 机箱插槽字形

规则：图 3-14 所示的 PXI Express 系统插槽兼容性字形应在 PXI Express 机箱上的 PXI Express 系统插槽的正下方可见，字形内指示插槽编号。

规则：图 3-14 中所示的 PXI Express 外设插槽兼容性字形应在 PXI Express 机箱上的 PXI Express 外设插槽的正下方可见，字形内指示插槽编号。

规则：图 3-14 所示的 PXI Express 混合插槽兼容性字形应在 PXI Express 机箱上的 PXI Express 混合插槽正下方可见，字形内指示插槽编号。

规则：图 3-14 所示的 PXI Express 系统时序插槽兼容性字形应在 PXI Express 机箱上的 PXI Express 系统时序插槽的正下方可见，字形内指示插槽编号。

观察：PXI-1 插槽具有 PXI-1 规范中定义的外设插槽字形。



图 3-14.插槽字形

4. Electrical Requirements

This section discusses the detailed electrical requirements for developing PXI Express-compatible Peripheral Modules, System Modules, System Timing Modules, and backplanes. It also discusses appropriate connector pinouts, power supply requirements, and 6U form factor implementation issues.

4.1 PCI Signals

PXI Express backplanes may contain Hybrid Slots or PXI-1 Slots. These slots contain pins for PCI functionality that are defined in the PXI-1 and PICMG 2.0 specifications.

4.1.1 Hybrid Slot Requirements

RULE: Hybrid Slots in PXI Express backplanes SHALL meet the requirements of the PXI-1 specification for the signals on the P1 connector.

RULE: The address line to IDSEL mapping based on logical slot number defined in the PICMG 2.0 specification SHALL be used for Hybrid Slots.

RULE: The interrupt assignments based on logical slot number defined in the PICMG 2.0 specification SHALL be used for Hybrid Slots.

4.1.2 PXI-1 Slot Requirements

RULE: PXI-1 slots in PXI Express backplanes SHALL meet the requirements of the PXI-1 specification for the signals on the P1 and P2 connectors.

RULE: The address line to IDSEL mapping based on logical slot number defined in the PICMG 2.0 specification SHALL be used for PXI-1 slots.

RULE: The interrupt assignments based on logical slot number defined in the PICMG 2.0 specification SHALL be used for PXI-1 slots.



4.2 CPCI Express Signals

The signals involved in PCI Express communication, as well as various sideband signals used by PXI Express Modules and slots, are defined in the *CompactPCI Express Specification*. PXI Express developers need to follow the requirements of the *CompactPCI Express Specification* as well as the requirements of this specification when developing PXI Express backplanes and Modules.

4.2.1 System Module/Slot Requirements

RULE: PXI Express System Modules and System Slots SHALL meet all requirements for System Boards and System Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-1.

Table 4-1. System Module and Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link

4. 电气要求

本节讨论开发与 PXI Express 兼容的外设模块、系统模块、系统时序模块和背板的详细电气要求。本节还讨论了适当的连接器引脚排列、电源要求和 6U 外形尺寸实现问题。

4.1 PCI 信号

PXI Express 背板可能包含混合插槽或 PXI-1 插槽。这些插槽包含 PXI-1 和 PICMG 2.0 规范中定义的 PCI 功能引脚。

4.1.1 混合时隙要求

规则：PXI Express 背板中的混合插槽应满足 PXI-1 规范对 P1 连接器上信号的要求。

规则：基于 PICMG 2.0 规范中定义的逻辑插槽号的地址行到 IDSEL 映射应用于混合插槽。

规则：基于 PICMG 2.0 规范中定义的逻辑时隙号的中断分配应用于混合时隙。

4.1.2 PXI-1 插槽要求

规则：PXI Express 背板中的 PXI-1 插槽应满足 PXI-1 规范对 P1 和 P2 连接器上信号的要求。

规则：基于 PICMG 2.0 规范中定义的逻辑槽号的地址行到 IDSEL 映射应用于 PXI-1 插槽。

规则：基于 PICMG 2.0 规范中定义的逻辑时隙号的中断分配应用于 PXI-1 时隙。

4.2 CPCI Express 信号

PCI Express 通信中涉及的信号，以及 PXI Express 模块和插槽使用的各种边带信号，在 CompactPCI Express 规范中定义。PXI Express 开发人员在开发 PXI Express 背板和模块时，需要遵循 CompactPCI Express 规范的要求以及本规范的要求。

4.2.1 系统模块/插槽要求

规则：PXI Express 系统模块和系统插槽应满足 CompactPCI Express 规范中定义的系统板和系统插槽对表 4-1 中所列信号的所有要求。

表 4-1. 系统模块和插槽要求

信号名称	注意
yPET 像素	其中 y 是链路，x 是链路中的车道
yPETnx	其中 y 是链路，x 是链路中的车道
yPERpx	其中 y 是链路，x 是链路中的车道
yPERnx	其中 y 是链路，x 是链路中的车道
yRefClk+	其中 y 是链接

4. Electrical Requirements

Table 4-1. System Module and Slot Requirements (Continued)

Signal Name	Note
yRefClk-	where y is the Link
PWR_OK	
PS_ON	
LINKCAP	
PWRBTN#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
5V	
3.3V	
5VAux	
GND	



Within the *CompactPCI Express Specification*, two backplane routing schemes are allowed for the System Slot: a 4 Link configuration and a 2 Link configuration.

PERMISSION: PXI Express backplanes MAY follow either the 4 Link routing configuration or the 2 Link routing configuration as defined by the *CompactPCI Express Specification*.

RULE: System Modules SHALL provide 4 Links.

PERMISSION: Some System Modules MAY be able to combine the four smaller Links into two larger Links.

4. 电气要求

表 4-1. 系统模块和插槽要求 (续)

信号名称	注意
yRefClk-	其中 y 是链接
PWR_OK	
PS_ON	
链接帽	
PWRBTN #	
SMBDAT	
三井住友国际	
珀斯特 #	
GA4..GA0	
西森 #	
唤醒 #	
警报 #	
I/O	本规范中定义了其中几个信号，用于仪表功能。
呼吸道合胞病毒	本规范中定义了其中几个信号，用于仪表功能。
12 伏	
5 伏	
3.3 伏	
5V 汽车	
接地	



在 CompactPCI Express 规范中，系统插槽允许使用两种背板布线方案：4 链路配置和 2 链路配置。

权限：PXI Express 背板可以遵循 CompactPCI Express 规范中定义的 4 链路路由配置或 2 链路路由配置。

规则：系统模块应提供 4 个链路。

权限：某些系统模块可能能够将四个较小的链接合并为两个较大的链接。

4.2.2 PXI Express Peripheral Module / Slot Requirements

RULE: PXI Express Peripheral Modules and Peripheral Slots SHALL meet all requirements for Type 2 Peripheral Boards and Type 2 Peripheral Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-2.

Table 4-2. PXI Express Peripheral Module and Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link
yRefClk-	where y is the Link
ATNLED	
ATNSW#	
PRSNT#	
PWREN#	
MPWRGD#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
3.3V	
5VAux	
GND	



4.2.2 PXI Express 外设模块/插槽要求

规则：PXI Express 外设模块和外设插槽应满足 CompactPCI Express 规范中定义的 2 类外设板和 2 类外设插槽对表 4-2 中所列信号的所有要求。

表 4-2.PXI Express 外设模块和插槽要求

信号名称	注意
yPET 像素	其中 y 是链路, x 是链路中的车道
yPETnx	其中 y 是链路, x 是链路中的车道
yPERpx	其中 y 是链路, x 是链路中的车道
yPERnx	其中 y 是链路, x 是链路中的车道
yRefClk+	其中 y 是链接
yRefClk-	其中 y 是链接
ATNLED 的	
新南威尔士州 #	
PRSNT #	
PWREN 的 #	
MPWRGD #	
SMBDAT	
三井住友国际	
珀斯特 #	
GA4..GA0	
西森 #	
唤醒 #	
警报 #	
I/O	本规范中定义了其中几个信号，用于仪表功能。
呼吸道合胞病毒	本规范中定义了其中几个信号，用于仪表功能。
12 伏	
3.3 伏	
5V 汽车	
接地	



4.2.3 System Timing Module/Slot Requirements

RULE: PXI Express System Timing Modules and System Timing Slots SHALL meet all requirements for Type 2 Peripheral Boards and Type 2 Peripheral Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-3.

Table 4-3. System Timing Module and Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link
yRefClk-	where y is the Link
ATNLED	
ATNSW#	
PRSNT#	
PWREN#	
MPWRGD#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
3.3V	
5VAux	
GND	



4.2.3 系统时序模块/插槽要求

规则：PXI Express 系统时序模块和系统时序插槽应满足 CompactPCI Express 规范中定义的表 4-3 中所列信号的 2 类外设板和 2 类外设插槽的所有要求。

表 4-3. 系统定时模块和插槽要求

信号名称	注意
yPET 像素	其中 y 是链路, x 是链路中的车道
yPETnx	其中 y 是链路, x 是链路中的车道
yPERpx	其中 y 是链路, x 是链路中的车道
yPERnx	其中 y 是链路, x 是链路中的车道
yRefClk+	其中 y 是链接
yRefClk-	其中 y 是链接
ATNLED 的	
新南威尔士州 #	
PRSNT #	
PWREN 的 #	
MPWRGD #	
SMBDAT	
三井住友国际	
珀斯特 #	
GA4..GA0	
西森 #	
唤醒 #	
警报 #	
I/O	本规范中定义了其中几个信号，用于仪表功能。
呼吸道合胞病毒	本规范中定义了其中几个信号，用于仪表功能。
12 伏	
3.3 伏	
5V 汽车	
接地	



4.2.4 Hybrid Slot Requirements

RULE: PXI Express Hybrid Slots SHALL meet all requirements for Type 2 Peripheral Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-4.

Table 4-4. Hybrid Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link
yRefClk-	where y is the Link
ATNLED	
ATNSW#	
PRSNT#	
PWREN#	
MPWRGD#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
5V	
3.3V	
5VAux	
GND	



4.2.4 混合时隙要求

规则：PXI Express 混合插槽应满足 CompactPCI Express 规范中定义的表 4-4 中所列信号的 2 类外设插槽的所有要求。

表 4-4.混合插槽要求

信号名称	注意
yPET 像素	其中 y 是链路, x 是链路中的车道
yPETnx	其中 y 是链路, x 是链路中的车道
yPERpx	其中 y 是链路, x 是链路中的车道
yPERnx	其中 y 是链路, x 是链路中的车道
yRefClk+	其中 y 是链接
yRefClk-	其中 y 是链接
ATNLED 的	
新南威尔士州 #	
PRSNT #	
PWREN 的 #	
MPWRGD #	
SMBDAT	
三井住友国际	
珀斯特 #	
GA4..GA0	
西森 #	
唤醒 #	
警报 #	
I/O	本规范中定义了其中几个信号，用于仪表功能。
呼吸道合胞病毒	本规范中定义了其中几个信号，用于仪表功能。
12 伏	
5 伏	
3.3 伏	
5V 汽车	
接地	



4.3 PXI-1 Instrumentation Signals

This specification retains all the timing and synchronization capabilities of the PXI-1 specification. That feature set can solve a wide range of system applications and remains a key advantage for PXI systems. Retaining this complete compatibility also allows for seamless migration of existing architectures into new PXI Express systems.

4.3.1 Reference Clock: PXI_CLK10

The PXI_CLK10 signal remains a primary method of synchronization of PXI Modules and is carried forward to this specification. Due to the relationship between PXI_CLK10 and PXIe_CLK100, the rules for implementing PXI_CLK10 within PXI Express backplanes, Peripheral Modules, and System Timing Modules is defined in the *PXI Express Timing References* section of this specification. The requirements in this section for PXI_CLK10 make it compatible with PXI-1 Peripheral Modules.

4.3.2 Trigger Bus

RULE: The trigger bus, PXI_TRIGGER[0:7], on PXI Express Chassis, Peripheral Modules, System Modules, and System Timing Modules SHALL meet the electrical requirements in PXI-1 for all rules, except the following changes.

- (1) The definition of a PXI segment no longer depends on a PCI bridging segments. It is inconvenient and adds no value to tie Data Bus topology and Trigger Bus topology.

RULE: For each PXI trigger bus segment in a PXI Chassis, the PXI Chassis SHALL bus the PXI_TRIGGER[0:7] signal to each PXI slot (System and Peripheral) in that segment. A Chassis SHALL NOT directly connect PXI_TRIGGER buses from different PXI trigger bus segments. If a System Slot controls multiple PXI segments, it SHALL NOT directly connect PXI trigger buses from different segments. A trigger bus segment SHALL NOT have more than eight trigger loads. A trigger load is defined as a trigger buffer device or Slot connection.

- (2) Termination is added to both ends of the trigger bus to improve signal quality by more effectively preventing reflections.

RULE: PXI_TRIGGER[0:7] SHALL be AC terminated with a $50\ \Omega$ resistor and 33 pF cap at both ends of the bus segment in addition to the diode termination required in the PXI-1 specification as shown in Figure 4-1.

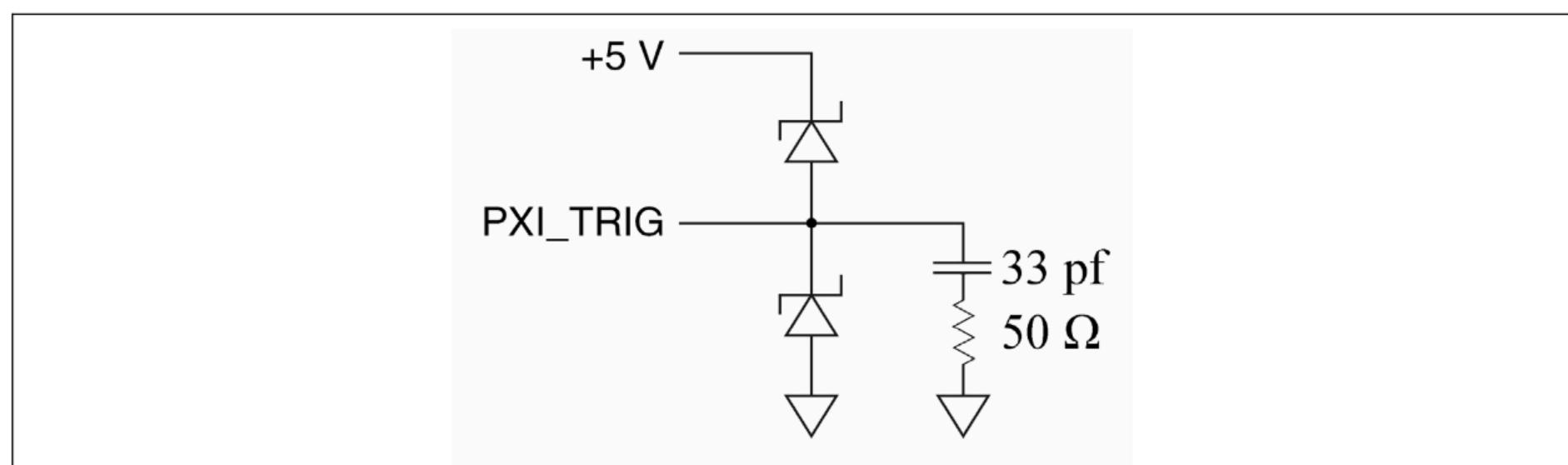


Figure 4-1. PXI Trigger Bus Termination

- (3) A pullup is added to the backplane to guarantee a stable state on the trigger line when the bus is in high impedance. The Module pull-up restriction is simplified.

RULE: PXI_TRIGGER[0:7] SHALL be pulled to the 5 V rail with a $2.2\text{ k}\Omega$ pullup on one end of the bus segment.

4.3 PXI-1 仪器信号

该规范保留了 PXI-1 规范的所有定时和同步功能。该功能集可以解决广泛的系统应用，并且仍然是 PXI 系统的关键优势。保持这种完全的兼容性还允许将现有架构无缝迁移到新的 PXI Express 系统中。

4.3.1 参考时钟：PXI_CLK10

PXI_CLK10 信号仍然是 PXI 模块同步的主要方法，并延续到本规范中。由于 PXI_CLK10 和 PXIe_CLK100 之间的关系，在本规范的 PXI Express 时序参考部分中定义了在 PXI Express 背板、外设模块和系统时序模块中实现 PXI_CLK10 的规则。本节中对 PXI_CLK10 的要求使其与 PXI-1 外设模块兼容。

4.3.2 触发总线

规则：PXI Express 机箱、外设模块、系统模块和系统定时模块上的触发总线 PXI_TRIGGER[0: 7]应满足 PXI-1 中所有规则的电气要求，但以下更改除外。

(1) PXI 段的定义不再依赖于 PCI 桥接段。连接数据总线拓扑和触发总线拓扑不方便，并且不会增加任何价值。

规则：对于 PXI 机箱中的每个 PXI 触发总线段，PXI 机箱应将 PXI_TRIGGER[0: 7]信号总线到该段中的每个 PXI 插槽（系统和外设）。机箱不得直接连接来自不同 PXI 触发总线段的 PXI_TRIGGER 总线。如果系统插槽控制多个 PXI 段，则它不应直接连接来自不同段的 PXI 触发总线。触发总线段不应具有超过八个触发负载。触发负载定义为触发缓冲区设备或插槽连接。

(2) 在触发母线的两端增加终端，通过更有效地防止反射来提高信号质量。

规则：PXI_TRIGGER[0: 7]应采用交流端接，除了 PXI-1 规范中要求的二极管端接外，总线段两端还应使用 50Ω 电阻和 33 pF 电容进行交流端接，如图 4-1 所示。

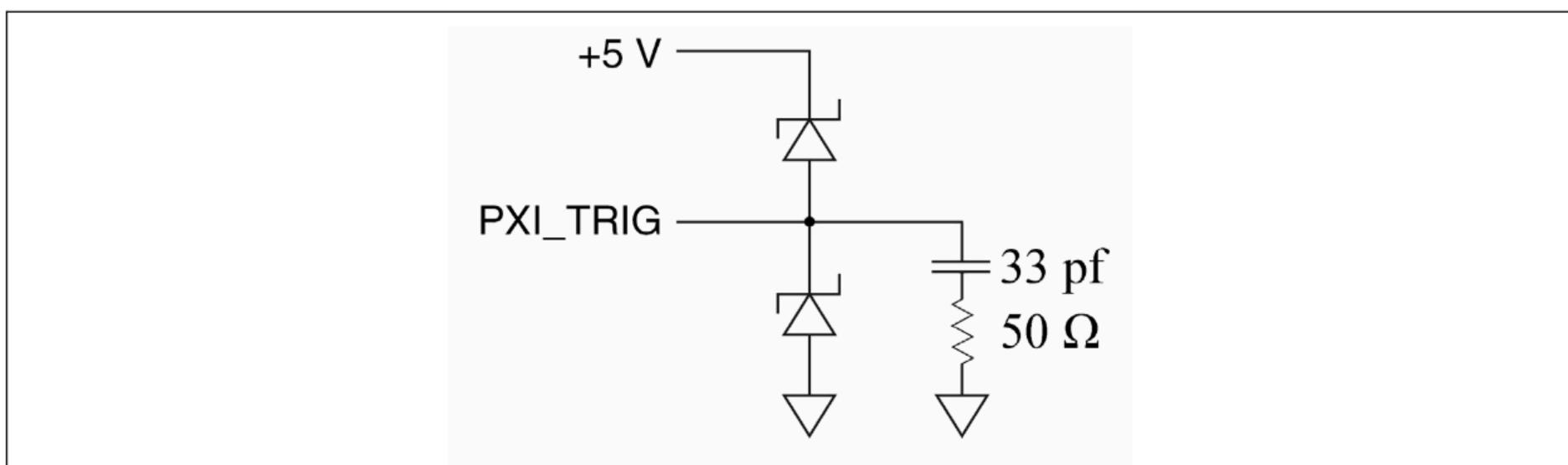


图 4-1.PXI 触发总线终端

(3) 背板上加上拉，保证总线高阻抗时触发线稳定状态。简化了模块上拉限制。

规则：PXI_TRIGGER[0: 7] 应拉至 5 V 电源轨，总线段一端上拉 $2.2\text{ k}\Omega$ 。

PERMISSION: Modules MAY place a pull-up of 20 K Ω or greater value on PXI_TRIGGER[0:7].

(4) The characteristic impedance of the backplane is changed to $65 \Omega \pm 10\%$ to allow backplanes to be built with more cost-effective trace widths.

RULE: The *unloaded* characteristic impedance for the backplane $Z_{l,\min}$ SHALL be $65 \Omega \pm 10\%$ using a stripline transmission line geometry.

(5) The maximum length stub allowed on a Module is increased to 3 in. to make Module trigger routing easier.

RULE: Printed circuit board trace lengths for PXI trigger bus signals on modules SHALL be less than or equal to 3 in.

The following new recommendations are made:

RECOMMENDATION: Synchronous trigger Clk to Out-Tval defined in the PXI-1 specification SHOULD be less than 20 ns to allow extra time for the signal to propagate through multiple bus segments and bridges. This recommendation precludes sending data on falling edge and receiving on rising edge.

RECOMMENDATION: Type A drivers are no longer recommended. When sending clocks or edges across the backplane, the driver SHOULD be a slow slew rate driver to minimize reflections.

4.3.3 Star Trigger

The PXI_STAR signal is routed by the backplane as a point-to-point connection back to the System Timing Slot. A System Timing Module may be used in this Slot to have private transmission of clocks or triggers to each Module connected to a PXI_STAR.

RULE: The PXI_STAR signals SHALL meet all requirements called out in the PXI-1 specification.

In the PXI-1 specification, there is a recommended mapping of PXI star triggers to Peripheral Slots. In the case of a PXI Express System Timing Slot, the PXI star triggers are allowed to route to any Peripheral Slot. Software is made aware of this mapping by a .ini file.

PERMISSION: A PXI_STAR signal from a PXI Express System Timing Slot MAY route to any slot.

RULE: Every slot in a PXI Express Chassis, except for the PXI Express System Timing Slot, SHALL have a PXI star trigger routed to it from the PXI Express System Timing Slot, unless the number of slots requiring PXI star triggers exceeds the number of available PXI star triggers.

OBSERVATION: The PXI Express System Controller Slot has a PXI star trigger connected to it from the PXI Express System Timing Slot.

OBSERVATION: The PXI_STAR signal to slot mapping is specified in the Chassis .ini file according to the format specified in the *PXI Express Software Specification*.

4.3.4 Local Bus

PXI-1 Implemented a 13 line daisy-chained local bus between adjacent Peripheral Slots. PXI Express modules maintain the PXI_LBL6 and PXI_LBR6 signals.

RULE: The PXI_LBL6 and PXI_LBR6 signals SHALL meet all requirements called out in the PXI-1 specification for local bus signals.

OBSERVATION: The PXI Express System Slot has the PXI_LBR6 signal defined but no PXI_LBL6 signal defined because there are no PXI Express Slots to the left of the System Slot.

许可：模块可以在 PXI_TRIGGER 上放置 $20\text{ k}\Omega$ 或更高值的上拉 [0: 7]。

(4) 背板的特性阻抗改为 $65\text{ }\Omega \pm 10\%$ ，以使背板能够构建具有更具成本效益的走线宽度。

规则：使用带状线传输线槽形状，背板 Z 的空载特性阻抗应为 $65\text{ }\Omega \pm 10\%$ 。

(5) 模块上允许的最大长度存根增加到 3 英寸。使模块触发布线更容易。

规则：模块上 PXI 触发总线信号的印刷电路板走线长度应小于或等于 3 英寸。

提出以下新建议：

建议：PXI-1 规范中定义的同步触发 Clk 到输出-Tval 应小于 20 ns，以便信号有额外的时间通过多个总线段和电桥传播。

此建议禁止在下降沿发送数据和在上升沿接收数据。

建议：不再建议使用 A 类驱动程序。通过背板发送时钟或边沿时，驱动程序应为慢速转换速率驱动器，以最大程度地减少反射。

4.3.3 星形触发器

PXI_STAR 信号由背板作为点对点连接路由回系统定时插槽。系统定时模块可用于此插槽，以便将触发器时钟私有传输到连接到 PXI_STAR 的每个模块。

规则：PXI_STAR 信号应满足 PXI-1 规范中规定的所有要求。

在 PXI-1 规范中，建议将 PXI 星形触发器映射到外设插槽。对于 PXI Express 系统定时隙，PXI 星形触发器可以路由到任何外设插槽。

软件通过.ini 文件知道此映射。

权限：来自 PXI Express 系统时序插槽的 PXI_STAR 信号可以路由到任何插槽。

规则：PXI Express 机箱中的每个插槽（PXI Express 系统定时插槽除外）都应有一个从 PXI Express 系统定时插槽路由到的 PXI 星形触发器，除非需要 PXI 星形触发器的插槽数量超过可用的 PXI 星形触发器的数量。

观察：PXI Express 系统控制器插槽有一个 PXI 星形触发器，从 PXI Express 系统时序插槽连接到它。

观察：根据 PXI Express 软件规范中指定的格式，在机箱.ini 文件中指定了 PXI_STAR 信号到插槽的映射。

4.3.4 当地巴士

PXI-1 在相邻外设插槽之间实现了 13 线菊花链本地总线。PXI Express 模块保持 PXI_LBL6 和 PXI_LBR6 信号。

规则：PXI_LBL6 和 PXI_LBR6 信号应满足 PXI-1 规范中针对本地总线信号的所有要求。

观察：PXI Express 系统插槽定义了 PXI_LBR6 信号，但未定义 PXI_LBL6 信号，因为系统插槽左侧没有 PXI Express 插槽。

4.4 PXI Express Timing References

4.4.1 Backplane Requirements

The PXI Express backplane is responsible for providing a common reference clock for synchronization of multiple Modules in an instrumentation system. To that end, the backplane provides 10 MHz and 100 MHz clocks independently to each Peripheral Slot with single-source, single-destination connections. The low slot-to-slot skew makes these clocks ideal for qualifying trigger protocols. The 100 MHz clock is a fast-switching LVPECL clock for precise timing. The 10 MHz TTL/CMOS clock preserves compatibility with PXI Modules.

4.4.1.1 PXIE_CLK100

RULE: The PXIE_CLK100 signal provided by the backplane SHALL be a 100 MHz, differential, 3.3 V LVPECL clock. Its frequency accuracy SHALL be ± 100 ppm or better over the specified operating temperature and time.

RULE: When each line of the PXIE_CLK100 pair is terminated with a 50Ω load to 1.30 V (or Thévenin equivalent), the absolute value of the differential voltage across the pair at the Peripheral Module connector SHALL be 800 mV nominally and SHALL NOT be less than 400 mV (except during transition) or greater than 1000 mV. The V_{OH} level for each line SHALL be greater than 2.0 V and less than 2.5 V.

RULE: The PXIE_CLK100 signal SHALL have a duty cycle between 45% and 55%, measured by the differential 0 V transition times. The 20%-to-80% rise and fall times SHALL NOT exceed 350 ps.

RULE: The PXIE_CLK100 signal to each Peripheral Slot SHALL be driven by an independent differential LVPECL driver. The backplane SHALL transmit the signal to each slot with a balanced transmission line pair having a differential impedance of $100 \Omega \pm 10 \Omega$. The backplane SHALL NOT include any termination or bias network on the transmission line.



OBSERVATION: Equivalently, each trace in the transmission line pairs must have an odd-mode impedance of $50 \Omega \pm 5 \Omega$.

RULE: The time skew between rising or falling edges of the PXIE_CLK100 signals at any two Peripheral Module connectors SHALL NOT exceed 200 ps. The edges are defined as the differential 0 V transition times and are measured where each signal pin enters the Peripheral Module circuit board.

RECOMMENDATION: PXIE_CLK100 is capable of high performance. Jitter SHOULD be kept under 5 ps rms from 12 kHz to 20 MHz, and 5 ps rms from 10 Hz to 12 kHz.

4.4.1.2 PXI_CLK10

RULE: The PXI_CLK10 provided by the backplane SHALL be a 10 MHz TTL signal, with V_{OH} no less than 2.4 V and V_{OL} no greater than 0.5 V. PXI_CLK10 SHALL NOT exceed 3.3 V.

RULE: The frequency accuracy SHALL be ± 100 ppm or better over the specified operating temperature and time.

RULE: The PXI_CLK10 signal SHALL have a duty cycle between 45% and 55%, measured by the 1.5 V transition times.

RULE: The PXI_CLK10 signal to each Peripheral Slot SHALL be driven by an independent buffer that has a source impedance matched to the transmission line. Each transmission line SHALL have $65 \Omega \pm 10 \Omega$ characteristic impedance, and each driver SHALL have a source impedance of $65 \Omega \pm 10 \Omega$.

4.4 PXI Express 时序参考

4.4.1 背板要求

PXI Express 背板负责为仪器系统中多个模块的同步提供公共参考时钟。为此，背板通过单源、单目标连接为每个外设插槽提供独立的 10 MHz 和 100 MHz 时钟。低插槽间偏斜使这些时钟成为合格触发协议的理想选择。100 MHz 时钟是一种快速开关 LVPECL 时钟，用于精确计时。10 MHz TTL/CMOS 时钟保持了与 PXI 模块的兼容性。

4.4.1.1 PXIe_CLK100

规则：背板提供的 PXIe_CLK100 信号应为 100 MHz、差分、3.3 V LVPECL 时钟。在规定的工作温度和时间内，其频率精度应为 ±100 ppm 或更高。

规则：当 PXIe_CLK100 对的每条线路以 50Ω 负载端接至 1.30 V（或 Thévenin 等效值）时，外围模块连接器处对两端的差分电压的绝对值应为 800 mV，且不应低于 400 mV（过渡期间除外）或大于 1000 mV。每条线路的 Vlevel 应大于 2.0 V 且小于 2.5 V。

规则：PXIe_CLK100 信号的占空比应在 45% 和 55% 之间，通过差分 0 V 转换时间测量。20% 至 80% 的上升和下降时间不应超过 350 ps。

规则：到每个外设插槽的 PXIe_CLK100 信号应由独立的差分 LVPECL 驱动器驱动。背板应将信号传输到具有差分阻抗为 $100\Omega \pm 10\Omega$ 的平衡传输线对的每个插槽。背板不应包括传输线上的任何终端或偏置网络。

观察：同样，传输线对中的每条走线必须具有 $50\Omega \pm 5\Omega$ 的奇模阻抗。

规则：任意两个外围模块连接器上 PXIe_CLK100 信号的上升沿或下降沿之间的时间偏差不应超过 200 ps。边沿定义为差分 0 V 转换时间，并在每个信号引脚进入外围模块电路板的地方进行测量。

建议：PXIe_CLK100 能够实现高性能。抖动应保持在 12 kHz 至 20 MHz 的 5 ps rms 以下，在 10 Hz 至 12 kHz 的 5 ps rms 以下。



4.4.1.2 PXI_CLK10

规则：背板提供的 PXI_CLK10 应为 10 MHz TTL 信号，V 不小于 2.4 V 且 V 不大于 0.5 V。PXI_CLK10 不得超过 3.3 V。

规则：在规定的工作温度和时间内，频率精度应为 ±100 ppm 或更高。

规则：PXI_CLK10 信号的占空比应在 45% 和 55% 之间，以 1.5 V 转换时间测量。

规则：每个外设时隙的 PXI_CLK10 信号应由具有与传输线匹配的源阻抗的独立缓冲器驱动。每条传输线应具有 $65\Omega \pm 10\Omega$ 特性阻抗，每个驱动器应具有 $65\Omega \pm 10\Omega$ 的源阻抗。

OBSERVATION: In most cases it will necessary to place a resistor in series with the driver so that the total output impedance is $65\ \Omega$.

RULE: The time skew between the rising or falling edges of the PXI_CLK10 signals at any two Peripheral Module connectors SHALL NOT exceed 1 ns. The edges are defined as the 1.5 V transition times and are measured where each signal pin enters the Peripheral Module circuit board.

RECOMMENDATION: The use of low-cost PLL buffers for driving the clock to each slot MAY lead to excessive jitter and therefore SHOULD NOT be used.

4.4.1.3 PXIe_SYNC100

PXIe_SYNC100 is a differential signal distributed to each Peripheral Slot by the Chassis backplane resource. PXIe_SYNC100 asserts as a 10 ns pulse synchronous to PXIe_CLK100 with a frequency determined by the system. The assertion of that pulse is coordinated with the rising edge of the PXI_CLK10 signal.

The relationship of PXIe_SYNC100 to PXI_CLK10 allows a Peripheral Module to create a local version of PXI_CLK10 that is in phase with the PXI_CLK10 signal and can be used to send triggers to, and receive triggers from, devices that use PXI_CLK10. A device receiving PXIe_SYNC100 in this manner can therefore perform PXI_CLK10-synchronous communication without actually connecting to the PXI_CLK10 signal. This can be useful for devices with PLLs or DLLs that cannot lock to a frequency as low as 10 MHz.

RULE: The PXIe_SYNC100 signal provided by the backplane SHALL be a differential 3.3 V LVPECL signal.

RULE: When each line of the PXIe_SYNC100 pair is terminated with a $50\ \Omega$ load to 1.30 V (or Thévenin equivalent), the absolute value of the differential voltage across the pair at the Peripheral Module connector SHALL be 800 mV nominally and SHALL NOT be less than 400 mV (except during transition) or greater than 1000 mV. The V_{OH} level for each line SHALL be greater than 2.0 V and less than 2.5 V.

RULE: The 20%-to-80% rise and fall times for PXIe_SYNC100 SHALL NOT exceed 350 ps.

RULE: The PXIe_SYNC100 signal to each Peripheral Slot SHALL be driven by an independent differential LVPECL driver. The backplane SHALL transmit the signal to each slot with a balanced transmission line pair having a differential impedance of $100\ \Omega \pm 10\ \Omega$. The backplane SHALL NOT include any termination or bias network on the transmission line.

OBSERVATION: Equivalently, each trace in the transmission line pairs must have an odd-mode impedance of $50\ \Omega \pm 5\ \Omega$.

4.4.1.4 Timing, Switching, and PXIe_SYNC_CTRL

RULE: PXI_CLK10 SHALL be synchronous to PXIe_CLK100. Each rising edge of PXI_CLK10 SHALL assert no earlier than 1 ns before the rising edge of PXIe_CLK100 and no later than 6.5 ns after the PXIe_CLK100 rising edge, as measured where each signal pin enters the Peripheral Module circuit board. The rising edges are defined as the differential 0 V transition times for PXIe_CLK100 and 1.5 V transition times for PXI_CLK10.

观察：在大多数情况下，需要将电阻器与驱动器串联，使总输出阻抗为 65Ω 。

规则：任意两个外围模块连接器上 PXI_CLK10 信号的上升沿或下降沿之间的时间偏差不应超过 1 ns。边沿定义为 1.5 V 转换时间，并在每个信号引脚进入外围模块电路板的位置进行测量。

建议：使用低成本 PLL 缓冲器将时钟驱动到每个插槽可能会导致过大的抖动，因此不应使用。

4.4.1.3 PXIe_SYNC100

PXIe_SYNC100 是由机箱背板资源分配到每个外设插槽的差分信号。PXIe_SYNC100 作为与系统确定的频率 PXIe_CLK100 同步的 10 ns 脉冲置位。该脉冲的置位与 PXI_CLK10 信号的上升沿相协调。

PXIe_SYNC100 与 PXI_CLK10 的关系允许外设模块创建与 PXI_CLK10 信号同相的本地版本的 PXI_CLK10，可用于向使用 PXI_CLK10 的设备发送触发器和接收触发器。因此，以这种方式接收 PXIe_SYNC100 的设备可以执行 PXI_CLK10 同步通信，而无需实际连接到 PXI_CLK10 信号。

这对于具有无法锁定到低至 10 MHz 频率的 PLL 或 DLL 的设备非常有用。

规则：背板提供的 PXIe_SYNC100 信号应为差分 3.3 V LVPECL 信号。

规则：当 PXIe_SYNC100 对的每条线路以 50Ω 负载端接至 1.30 V（或 Thévenin 等效值）时，外围模块连接器处对两端的差分电压的绝对值应为 800 mV，且不得低于 400 mV（过渡期间除外）或大于 1000 mV。每条线路的 Vlevel 应大于 2.0 V 且小于 2.5 V。



规则：PXIe_SYNC100 的 20% 至 80% 上升和下降时间不得超过 350 ps。

规则：到每个外设插槽的 PXIe_SYNC100 信号应由独立的差分 LVPECL 驱动器驱动。背板应使用差分阻抗为 $100 \Omega \pm 10 \Omega$ 的平衡传输线对将信号传输到每个插槽。背板不应包括传输线上的任何终端或偏置网络。

观察：同样，传输线对中的每条走线必须具有 $50 \Omega \pm 5 \Omega$ 的奇模阻抗。

4.4.1.4 定时、切换和 PXIe_SYNC_CTRL

规则：PXI_CLK10 应与 PXIe_CLK100 同步。PXI_CLK10 的每个上升沿应不早于 PXIe_CLK100 的上升沿前 1 ns，在 PXIe_CLK100 上升沿之后不迟于 6.5 ns，如每个信号引脚进入外围模块电路板的位置所测量的那样。上升沿定义为 PXIe_CLK100 的差分 0 V 转换时间和 PXI_CLK10 的 1.5 V 转换时间。

4. Electrical Requirements

Figure 4-2 and Table 4-5 illustrate this relationship:

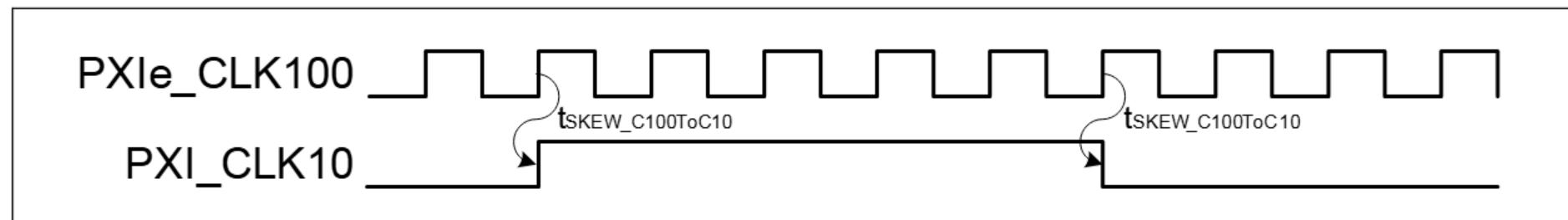


Figure 4-2. Timing relationship of PXI_CLK10 to PXIe_CLK100

Table 4-5. Timing relationship of PXI_CLK10 to PXIe_CLK100

Description	Parameter	Min	Max
Delay from rising edge of PXIe_CLK100 to either edge of PXI_CLK10 (at PXI Express connector)	tSKEW_C100ToC10	-1 ns	6.5 ns

RECOMMENDATION: A backplane SHOULD allow PXI_CLK10 and PXIe_CLK100 to be derived from the PXI_CLK10_IN signal from the System Timing Slot or another external source to allow for a more accurate or stable reference.

RULE: If a backplane allows PXI_CLK10 to be received from the System Timing Slot, the backplane SHALL have a $1500 \Omega \pm 5\%$ pull-down resistor to ground on the PXIe_CLK10_IN signal. The receiving circuitry for this signal on the backplane SHALL be TTL compatible and 5V tolerant, with V_{IH} no greater than 2.0 V and V_{IL} no less than 0.8 V.

RULE: If PXI_CLK10 is switched between sources, the minimum pulse width (high or low) created on PXI_CLK10 SHALL NOT be less than 30 ns and the minimum time between successive edges of the same polarity SHALL NOT be less than 80 ns. The minimum pulse width (high or low) created on PXIe_CLK100 SHALL NOT be less than 2.5 ns and the minimum time between successive edges of the same polarity SHALL NOT be less than 8 ns.

OBSERVATION: The preceding rule is intended to prevent a state machine from being corrupted by glitches in the clock during transition.

RULE: The PXI Express backplane resource SHALL ensure that PXI_CLK10 asserts with the next rising edge of PXIe_CLK100 after the rising edge of PXIe_CLK100 where PXIe_SYNC100 was asserted.

RULE: PXIe_SYNC100 SHALL meet the timing requirements shown in Figure 4-3 and Table 4-6, as measured where each signal pin enters the Peripheral Module circuit board.

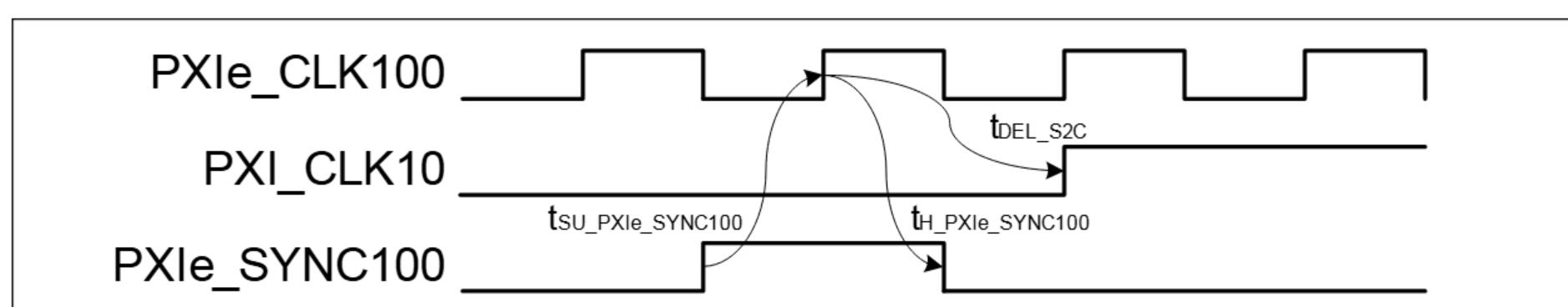


Figure 4-3. Timing Relationship of PXIe_SYNC100 to PXI_CLK10 and PXIe_CLK100

4. 电气要求

图 4-2 和表 4-5 说明了这种关系：

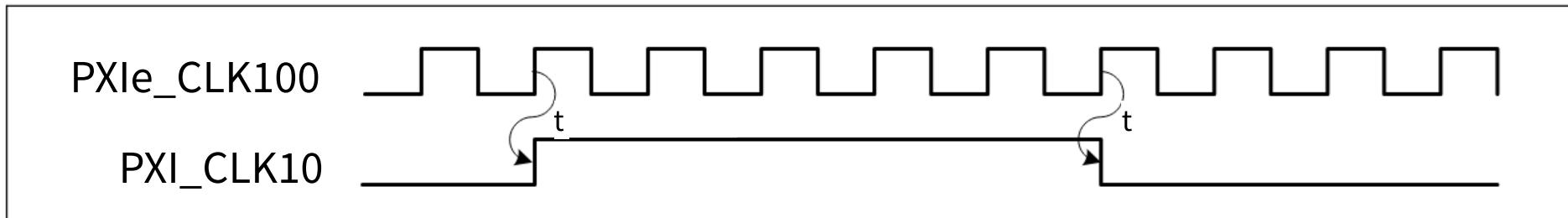


图 4-2.PXI_CLK10 与 PXIe_CLK100 的时序关系

表 4-5.PXI_CLK10 与 PXIe_CLK100 的时序关系

描述	参数	最小值	麦克斯
从 PXIe_CLK100 的上升沿到 PXI_CLK10 的任一边缘的延迟 (在 PXI Express 连接器上)	tSKEW_C100ToC10	-1 纳秒	6.5 纳秒

建议：背板应允许从系统时序插槽或其他外部源的 PXI_CLK10_IN 信号中获取 PXI_CLK10 和 PXIe_CLK100，以实现更准确或更稳定的参考。

规则：如果背板允许从系统定时插槽接收 PXI_CLK10，则背板应在 PXIe_CLK10_IN 信号上具有 $1500 \Omega \pm 5\%$ 的下拉电阻器接地。背板上此信号的接收电路应兼容 TTL 且容限为 5V， V_{no} 大于 2.0 V 且 V_{no} 小于 0.8 V。

规则：如果 PXI_CLK10 在源之间切换，则在 PXI_CLK10 上产生的最小脉冲宽度（高或低）不应小于 30 ns，相同极性的连续边沿之间的最长时间不应小于 80 ns。在 PXIe_CLK100 上产生的最小脉冲宽度（高或低）不应小于 2.5 ns，相同极性的连续边沿之间的最长时间不应小于 8 ns。

观察：前面的规则旨在防止状态机在转换期间因时钟故障而损坏。



规则：PXI Express 背板资源应确保 PXI_CLK10 在置位的 PXIe_CLK100 上升沿之后的下一个 PXIe_CLK100 上升沿置位 PXIe_SYNC100。

规则：PXIe_SYNC100 应满足图 4-3 和表 4-6 中所示的时序要求，如每个信号引脚进入外围模块电路板的位置测量的那样。

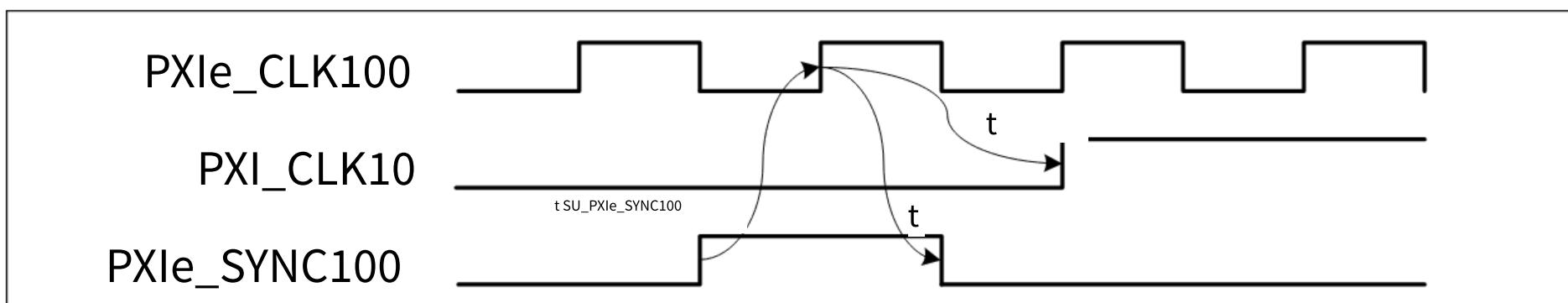


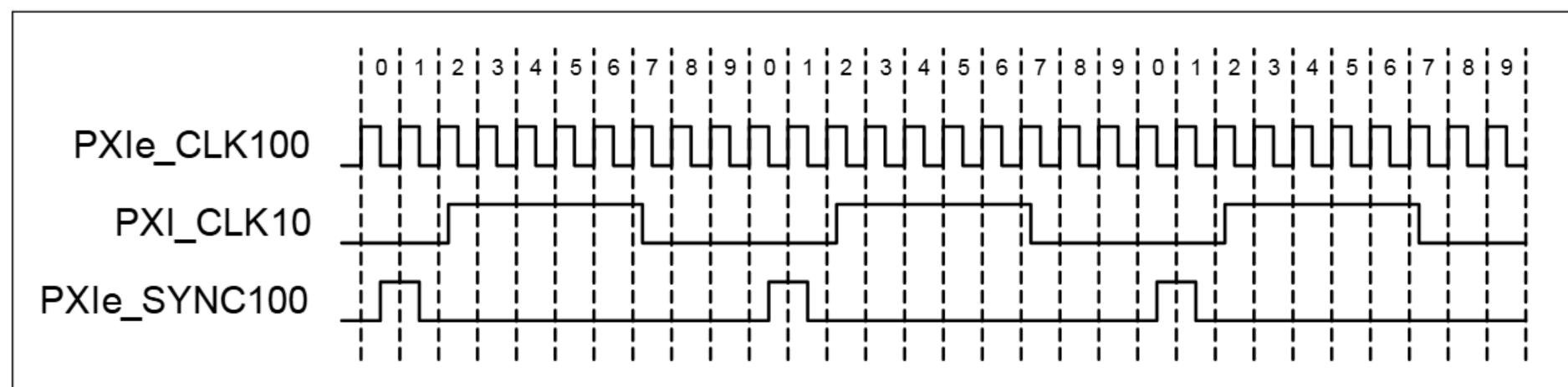
图 4-3.PXIe_SYNC100 与 PXI_CLK10 和 PXIe_CLK100 的时序关系

Table 4-6. Timing Relationship of PXIE_SYNC100 to PXI_CLK10 and PXIE_CLK100

Description	Parameter	Min	Max
Setup from edge of PXIE_SYNC100 to rising edge of PXIE_CLK100 (at PXIE connector)	$t_{SU_PXIE_SYNC100}$	3 ns	—
Hold from rising edge of PXIE_CLK100 to edge of PXIE_SYNC100 (at PXIE connector)	$t_H_{PXIE_SYNC100}$	1 ns	—
Delay from rising edge of PXIE_CLK100 where PXIE_SYNC100 is asserted to next rising edge of PXI_CLK10 (at PXIE connector)	t_{DEL_S2C}	10 ns + $t_{SKew_C100ToC10.min}$	10 ns + $t_{SKew_C100ToC10.max}$

OBSERVATION: Timing parameter t_{DEL_S2C} is listed to illustrate the relationship between PXIE_SYNC100 and PXI_CLK10 and will be met automatically if all other timing rules are followed.

Figure 4-4 shows an expanded relationship of PXIE_CLK100, PXIE_SYNC100, and PXI_CLK10. In this example, PXIE_SYNC100 has the default 10 MHz behavior.

**Figure 4-4.** PXIE_SYNC100 Default Behavior

In Figure 4-4, PXIE_SYNC100 pulses high for one PXIE_CLK100 cycle and remains low for 9 PXIE_CLK100 cycles. The high pulse precedes the rising edge of PXI_CLK10, making the creation of an onboard version of PXI_CLK10 possible. Refer to the PXI Express Peripheral Module Requirements section for more information.

RULE: The PXI Express backplane resource SHALL implement the PXIE_SYNC100 default behavior.

PERMISSION: PXIE_SYNC100 MAY be driven by the backplane at a frequency other than 10 MHz, including driving it as a nonperiodic signal, as long as its assertion and deassertion follow the timing rules in the above table.

PERMISSION: When a backplane implements nondefault behavior for PXIE_SYNC100, the backplane MAY use PXIE_SYNC_CTRL from the System Timing Module to control that behavior.

The above permissions allow devices to use PXIE_SYNC100 to communicate via synchronous triggers even when those devices are electrically farther apart than 100 ns. For example, two PXIE Chassis can coordinate their PXIE_SYNC_CTRL signals so that their PXIE_SYNC100 signals toggle at 5 MHz in phase with each other. Instead of using CLK10 to send and receive triggers, Modules in each Chassis use flip-flops clocked by PXIE_CLK100 and enabled by PXIE_SYNC100. With a 5 MHz PXIE_SYNC100, these Modules now have 200 ns to propagate a trigger from a device in one Chassis to a device in another. And because

表 4-6.PXIe_SYNC100 与 PXI_CLK10 和 PXIe_CLK100 的时序关系

描述	参数	最小值	麦克斯
从 PXIe_SYNC100 边缘到 PXIe_CLK100 上升沿的设置（在 PXIe 连接器上）	tSU_PXIe_SYNC100	3 纳秒	—
从 PXIe_CLK100 的上升沿到 PXIe_SYNC100 的边缘（在 PXIe 连接器处）	tH_PXIe_SYNC100	1 纳秒	—
从断位 PXIe_SYNC100 的 PXIe_CLK100 上升沿到下一个上升沿 PXI_CLK10 的延迟（在 PXIe 连接器处）	tDEL_S2C	10 纳秒 + tSKEW_C100ToC10.min	10 纳秒 + tSKEW_C100ToC10.max

观察 **:tD[时序参数]** 是为了说明 PXIe_SYNC100 和 PXI_CLK10 之间的关系，如果遵循所有其他计时规则，则会自动满足。

图 4-4 显示了 PXIe_CLK100、PXIe_SYNC100 和 PXI_CLK10 的扩展关系。在本例中，PXIe_SYNC100 具有默认的 10 MHz 行为。

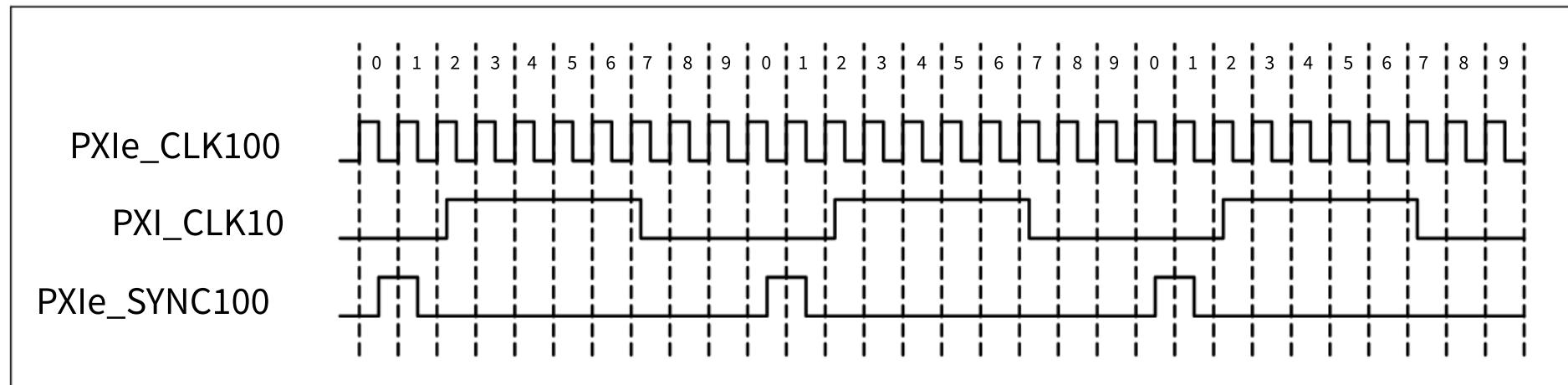


图 4-4.PXIe_SYNC100 默认行为

在图 4-4 中，PXIe_SYNC100 脉冲在一个 PXIe_CLK100 周期内保持高电平，并在 9 个 PXIe_CLK100 周期内保持低电平。高脉冲先于 PXIe_CLK10 的上升沿，因此可以创建板载版本的 PXI_CLK10。有关更多信息，请参阅 PXI Express 外设模块要求部分。

规则：PXI Express 背板资源应实现 PXIe_SYNC100 默认行为。

许可：PXIe_SYNC100 可以由背板以 10 MHz 以外的频率驱动，包括将其作为非周期性信号驱动，只要其断言和取消断言遵循上表中的定时规则。

权限：当背板实现 PXIe_SYNC100 的非默认行为时，背板可以使用系统时钟模块中的 PXIe_SYNC_CTRL 来控制该行为。

上述权限允许设备使用 PXIe_SYNC100 通过同步触发器进行通信，即使这些设备的电气距离超过 100 ns。例如，两个 PXIe 机箱可以协调其 PXIe_SYNC_CTRL 信号，以便它们的 PXIe_SYNC100 信号彼此以 5 MHz 的相位切换。每个机箱中的模块不使用 CLK10 发送和接收触发器，而是使用由 PXIe_CLK100 时钟并由 PXIe_SYNC100 启用的触发器。在 5 MHz PXIe_SYNC100 下，这些模块现在有 200 ns 的时间将触发器从一个机箱中的设备传播到另一个机箱中的设备。而且因为

4. Electrical Requirements

PXIe_SYNC100 always maintains its relationship to PXI_CLK10, the performance of Modules that use PXI_CLK10 is not affected.

The System Timing Module drives PXIe_SYNC_CTRL synchronous to PXI_CLK10 and is used by the backplane resource to determine when to assert PXIe_SYNC100. Figures 4-5 and 4-6 show some possible behaviors:

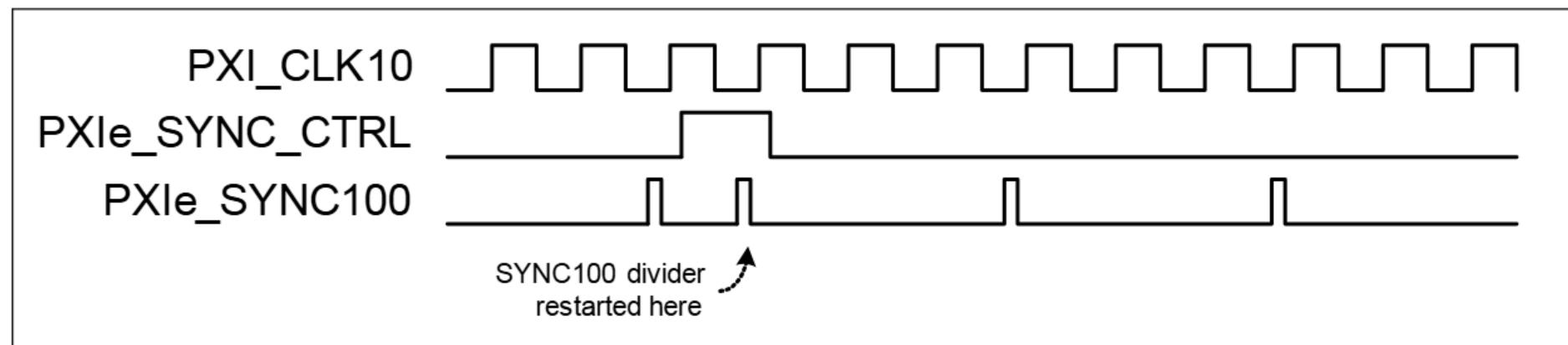


Figure 4-5. PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart

In this case, the backplane resource is configured to drive PXIe_SYNC100 at 3.33 MHz and to use PXIe_SYNC_CTRL to reset its counter. The assertion of PXIe_SYNC_CTRL causes the counter to start over, adjusting the phase of the PXIe_SYNC100 signal. This allows multiple Chassis that create 3.33 MHz PXIe_SYNC100 signals to have their respective PXIe_SYNC100 signals in phase with each other.

RULE: If a backplane receives PXIe_SYNC_CTRL from the System Timing Slot, the PXI Express backplane resource default behavior SHALL be to interpret a high level on PXIe_SYNC_CTRL as a synchronous restart, according to Figure 4-5. The PXI Express backplane resource default behavior SHALL ignore a low level on PXIe_SYNC_CTRL.

RULE: A PXI Express backplane resource that implements behaviors for PXIe_SYNC_CTRL other than the default behavior SHALL implement the default behavior until programmed to do otherwise at run time.



Figure 4-6 shows an alternate behavior for PXIe_SYNC_CTRL.

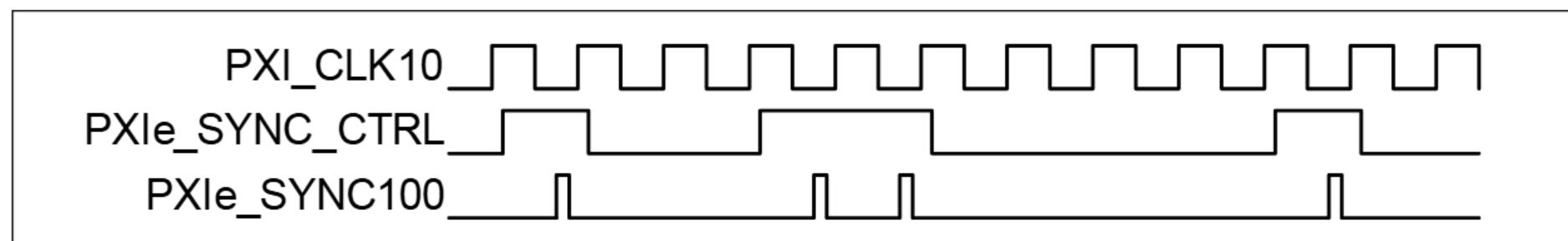


Figure 4-6. PXIe_SYNC100 Using PXIe_SYNC_CTRL as Enable

In this case, the backplane resource uses PXIe_SYNC_CTRL as an enable. Every rising PXI_CLK10 edge where PXIe_SYNC_CTRL is Asserted is preceded by a PXIe_SYNC100 pulse.

RULE: If a backplane receives PXIe_SYNC_CTRL from the System Timing Slot, the backplane SHALL have a pull-down resistor to ground on the PXIe_SYNC_CTRL signal with a value between 10 KΩ and 100 KΩ. Receiving circuitry for this signal on the backplane SHALL have a minimum VIH no greater than 2.0 V and a maximum VIL no less than 0.8 V.

4. 电气要求

PXIe_SYNC100 始终保持与 PXIe_CLK10 的关系，则使用 PXI_CLK10 的模块的性能不受影响。

系统定时模块将 PXIe_SYNC_CTRL 与 PXI_CLK10 同步驱动，并由背板资源用于确定何时置位 PXIe_SYNC100。图 4-5 和 4-6 显示了一些可能的行为：

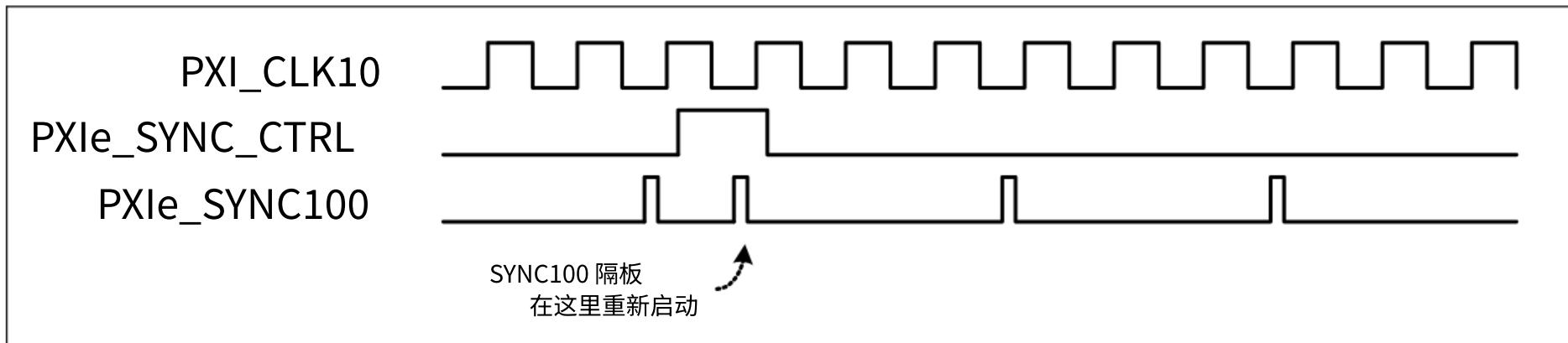


图 4-5. 使用 PXIe_SYNC_CTRL 作为重启时在 3.33 MHz 时 PXIe_SYNC100

在这种情况下，背板资源配置为以 3.33 MHz 驱动 PXIe_SYNC100，并使用 PXIe_SYNC_CTRL 重置其计数器。PXIe_SYNC_CTRL 的断言会导致计数器重新开始，调整 PXIe_SYNC100 信号的相位。这允许创建 3.33 MHz PXIe_SYNC100 信号的多个机箱使其各自的 PXIe_SYNC100 信号彼此同相。

规则：如果背板从系统时序插槽接收 PXIe_SYNC_CTRL，则 PXI Express 背板资源默认行为应是将 PXIe_SYNC_CTRL 上的高电平解释为同步重启，如图 4-5 所示。PXI Express 背板资源默认行为应忽略 PXIe_SYNC_CTRL 上的低电平。

规则：为默认行为以外的 PXIe_SYNC_CTRL 实现行为的 PXI Express 背板资源应实现默认行为，直到在运行时被编程为其他行为。



图 4-6 显示了 PXIe_SYNC_CTRL 的替代行为。

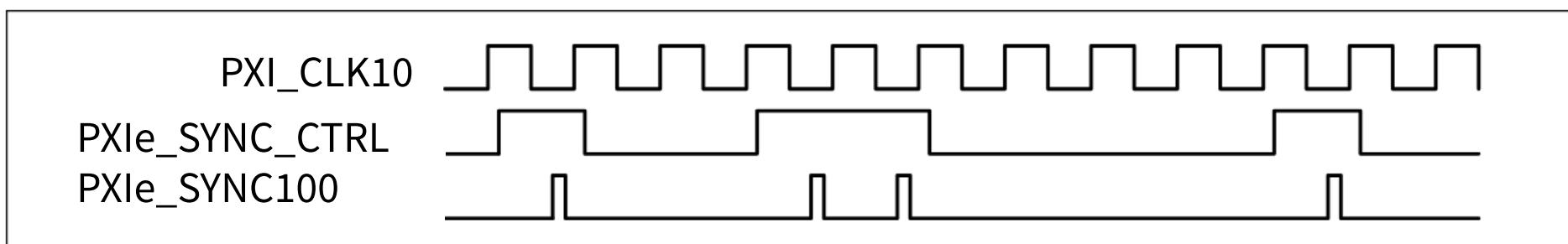


图 4-6.PXIe_SYNC100 使用 PXIe_SYNC_CTRL 作为启用

在这种情况下，背板资源使用 PXIe_SYNC_CTRL 作为启用。PXIe_SYNC_CTRL 被断言的每个上升沿前面都有一个 PXIe_SYNC100 脉冲。

规则：如果背板从系统定时槽接收 PXIe_SYNC_CTRL，则背板应在 PXIe_SYNC_CTRL 信号上具有值在 10 K Ω 和 100 K Ω 之间的下拉电阻器接地。背板上此信号的接收电路应具有不大于 2.0 V 的最小 VIH 和不低于 0.8 V 的最大 VIL。

4.4.2 System Timing Module Requirements

RULE: If a System Timing Module drives the SYNC_CTRL signal, it SHALL ensure SYNC_CTRL meets the timing requirements shown in Figure 4-7 and Table 4-7.

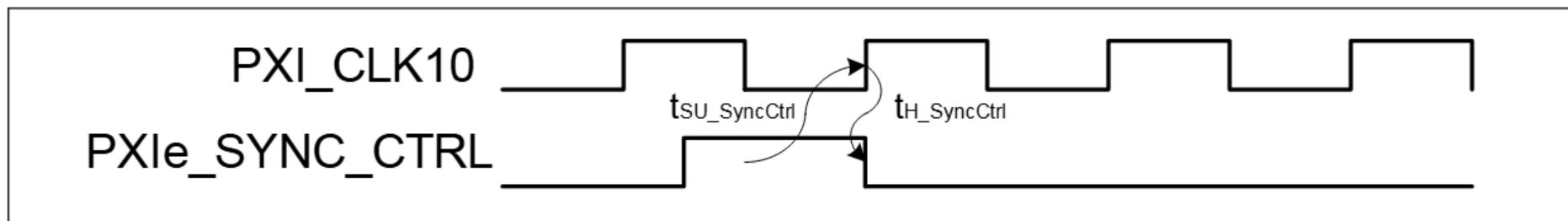


Figure 4-7. Timing Relationship between SYNC_CTRL and PXI_CLK10

Table 4-7. Timing Relationship between SYNC_CTRL and PXI_CLK10

Description	Parameter	Min	Max
Setup from edge of PXIe_SYNC_CTRL to rising edge of PXI_CLK10 (at PXI Express connector)	t _{SU_SYNC_CTRL}	50 ns	—
Hold from rising edge of PXI_CLK10 to edge of PXIe_SYNC_CTRL (at PXI Express connector)	t _{H_SYNC_CTRL}	0 ns	—

OBSERVATION: The large minimum time for t_{SU_SYNC_CTRL} allows the backplane resource to receive SYNC_CTRL using flip-flops clocked by PXIe_CLK100 and have time to assert PXIe_SYNC100 before the next edge of PXI_CLK10.

RULE: A System Timing Module driving PXI_CLK10_IN SHALL have a driver with a source impedance of $65 \Omega \pm 10\%$. The characteristic impedance of the circuit board trace from the driver to the PXI_CLK10_IN connection SHALL be $65 \Omega \pm 10\%$. The signal SHALL be a 10 MHz TTL signal, with VOH no less than 2.4 V and VOL no greater than 0.5 V.

OBSERVATION: In most cases it will be necessary to place a resistor in series with the driver so that the total output impedance is 65Ω .



4.4.3 Peripheral Module Requirements

4.4.3.1 PXIe_CLK100

RULE: If a Peripheral Module uses PXIe_CLK100, it SHALL terminate both lines with a $50 \Omega (\pm 5 \Omega)$ load to 1.3 V (± 0.2 V) or Thévenin equivalent. If a Peripheral Module does not use PXIe_CLK100, it SHALL leave the lines unconnected and unterminated.

4.4.2 系统时序模块要求

规则：如果系统定时模块驱动 SYNC_CTRL 信号，则应确保 SYNC_CTRL 满足图 4-7 和表 4-7 中所示的定时要求。

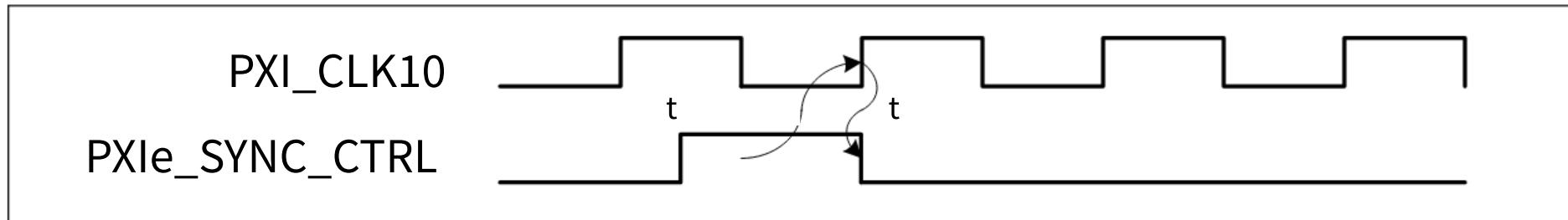


图 4-7.SYNC_CTRL 和 PXI_CLK10 之间的时序关系

表 4-7.SYNC_CTRL 与 PXI_CLK10 之间的时序关系

描述	参数	最小值	麦克斯
从 PXIe_SYNC_CTRL 边缘到 PXI_CLK10 上升沿的设置（在 PXI Express 连接器上）	tSU_SYNC_CTRL	50 纳秒	—
从 PXI_CLK10 的上升沿到 PXIe_SYNC_CTRL 的边缘（在 PXI Express 连接器上）	tH_SYNC_CTRL	0 纳秒	—

观察 SY 最短时间 RL 允许背板资源使用 PXIe_CLK100 时钟的触发器接收 SYNC_CTRL，并有时间在下一个 PXI_CLK10 边缘之前断言 PXIe_SYNC100。

规则：驱动 PXI_CLK10_IN 的系统定时模块应具有源阻抗为 $65 \Omega \pm 10\%$ 的驱动器。从驱动器到 PXI_CLK10_IN 连接的电路板走线的特性阻抗应为 $65 \Omega \pm 10\%$ 。信号应为 10 MHz TTL 信号，VOH 不低于 2.4 V，VOL 不大于 0.5 V。

观察：在大多数情况下，需要将电阻器与驱动器串联，使总输出阻抗为 65Ω 。



4.4.3 外围模块要求

4.4.3.1 PXIe_CLK100

规则：如果外围设备模块使用 PXIe_CLK100，它应以 50Ω ($\pm 5 \Omega$) 的负载终止两条线路，以达到 1.3 V ($\pm 0.2 \text{ V}$) 或 Thévenin 等效值。如果外围设备模块不使用 PXIe_CLK100，它应保持线路未连接和末端接。

4. Electrical Requirements

RECOMMENDATION: Peripheral Modules SHOULD terminate the PXIE_CLK100 signal with the following circuit:

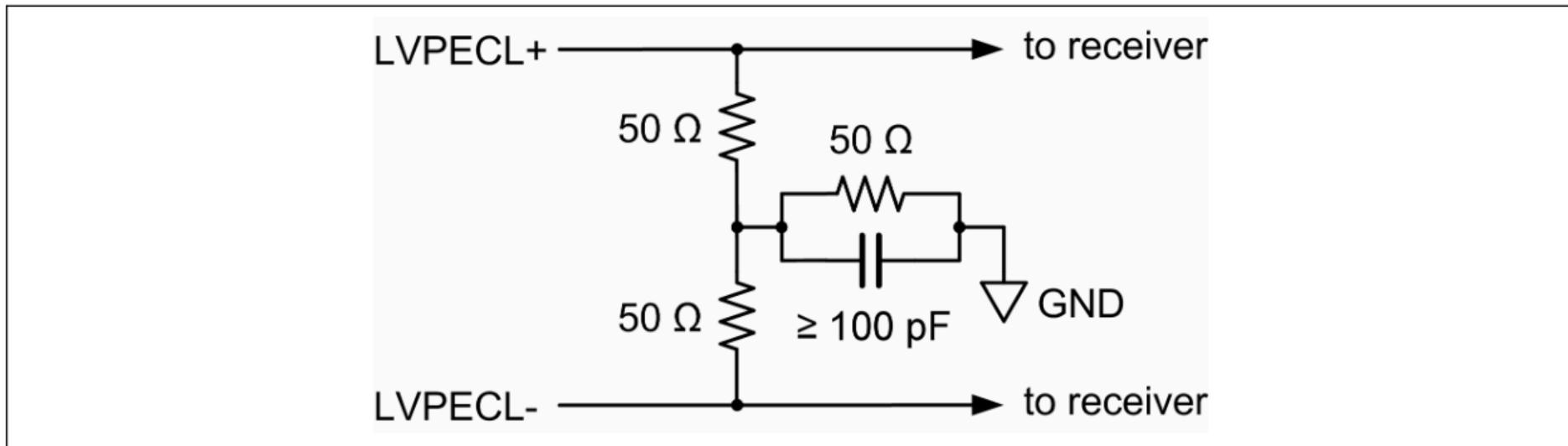


Figure 4-8. Peripheral Module Circuit for Terminating PXIE_CLK100 Signal

RULE: Peripheral Modules SHALL NOT terminate PXIE_CLK100 more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of $100 \Omega \pm 10 \Omega$.

RECOMMENDATION: Because of the fast rise- and fall-times of the PXIE_CLK100 signal, signal integrity will be best at or very near the termination. In Peripheral Modules, the electrical length of the connections beyond the termination SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIE_CLK100. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.4.3.2 PXI_CLK10

RULE: Peripheral Module PXI_CLK10 Receivers SHALL be 3.3 V tolerant, with V_{IH} no greater than 2.0 V and V_{IL} no less than 0.8 V. Peripheral Modules SHALL NOT terminate PXI_CLK10. Board traces from the connector to the PXI_CLK10 Receivers SHALL have a characteristic impedance of $65 \Omega \pm 10 \Omega$.

4.4.3.3 PXIE_SYNC100

RULE: If a Peripheral Module uses PXIE_SYNC100, it SHALL terminate both lines with a $50 \Omega (\pm 5 \Omega)$ load to 1.3 V (± 0.2 V) or Thévenin equivalent. If a Peripheral Module does not use PXIE_SYNC100, it SHALL leave the lines unconnected and unterminated.



4. 电气要求

建议：外围设备模块应使用以下电路终止 PXIe_CLK100 信号：

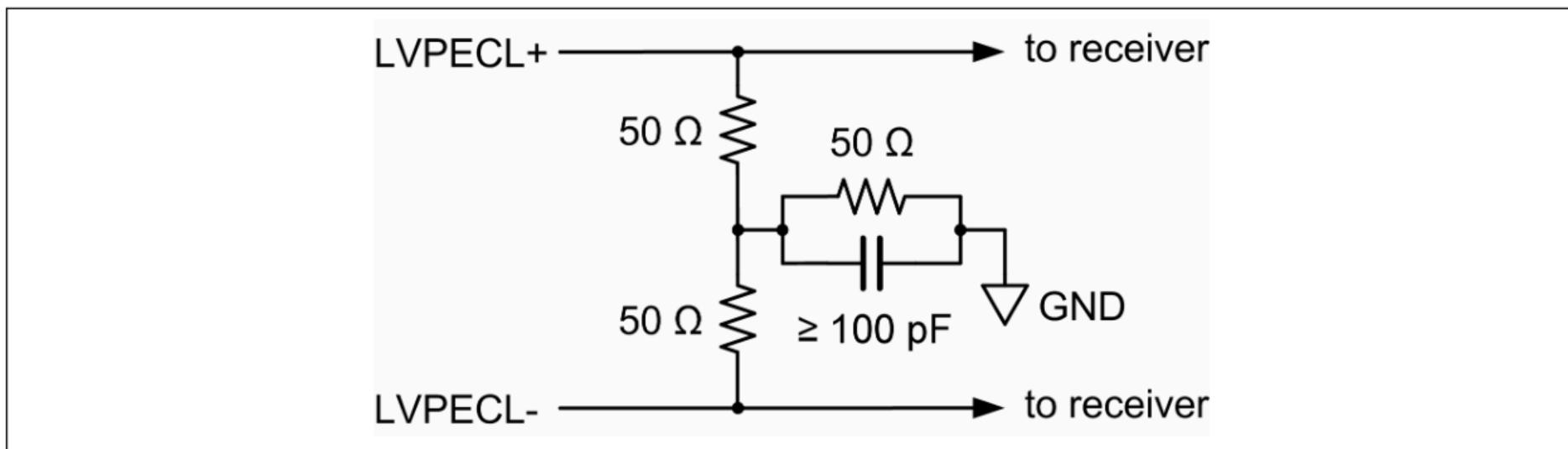


图 4-8. 用于终端 PXIe_CLK100 信号的外围模块电路

规则：外围模块的端接电气长度不得超过背板连接器 PXIe_CLK100 1 ns。背板连接器和端接之间的任何传输线都应具有 $100 \Omega \pm 10 \Omega$ 的特性差阻抗。

建议：由于 PXIe_CLK100 信号的上升和下降时间较快，因此信号完整性在端接处或非常接近端接处时将达到最佳状态。在外设模块中，端接之外的连接的电气长度不应超过 160 ps，在典型的玻璃环氧树脂电路板中，走线长度约为 25 mm。为了保持良好的信号完整性，外设模块应仅将一个有源接收器连接到 PXIe_CLK100。如果使用多个接收器，则应仔细模拟配置以确保波形表现良好。

4.4.3.2 PXI_CLK10

规则：接收器 PXI_CLK10 外围模块应具有 3.3 V 容差，V 不大于 2.0 V 且 V 不小于 0.8 V。外围模块不得端接 PXI_CLK10。从连接器到 PXI_CLK10 接收器的电路板走线应具有 $65 \Omega \pm 10 \Omega$ 的特性阻抗。

4.4.3.3 PXIe_SYNC100

规则：如果外围设备模块使用 PXIe_SYNC100，它应以 50Ω ($\pm 5 \Omega$) 负载端接两条线路，负载为 1.3 V (± 0.2 V) 或 Thévenin 等效值。如果外围模块不使用 PXIe_SYNC100，则应使线路未连接且未端接。



RECOMMENDATION: Peripheral Modules SHOULD terminate the PXIE_SYNC100 signal with the following circuit:

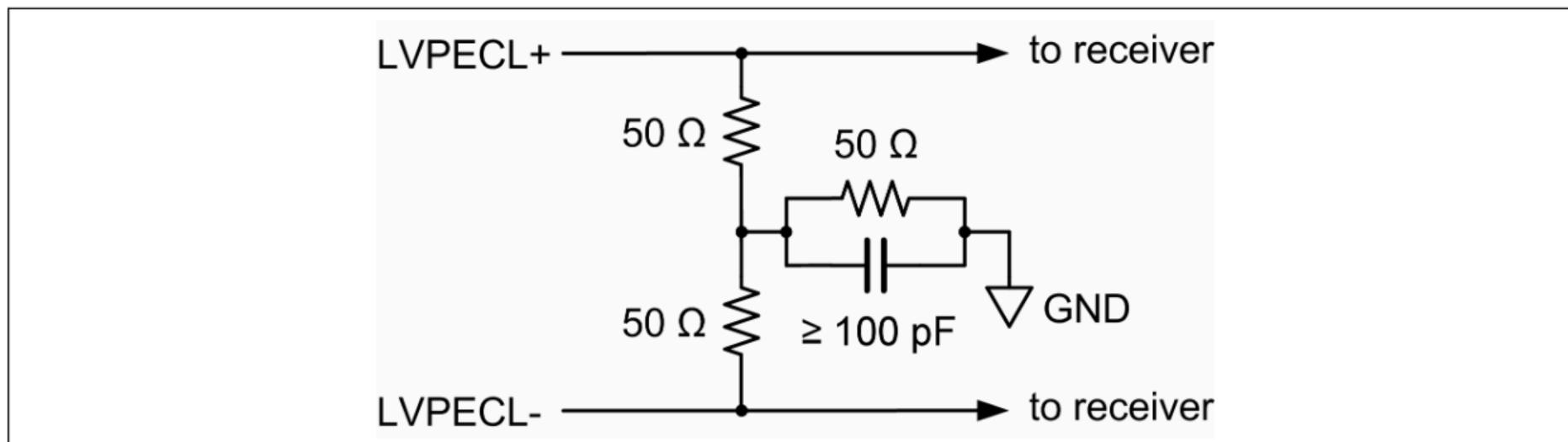


Figure 4-9. Peripheral Module Circuit for Terminating PXIE_SYNC100 Circuit

RULE: Peripheral Modules SHALL NOT terminate PXIE_SYNC100 more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of $100 \Omega \pm 10 \Omega$.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIE_SYNC100 signal, signal integrity will be best at or very near the termination. In Peripheral Modules, the electrical length of the connections beyond the termination SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIE_CLK100. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

Because the assertion of PXIE_SYNC100 always precedes the rising edge of PXI_CLK10 according to the rules above, a PXI Express Peripheral Module can create a signal that is in phase with PXI_CLK10 without connecting to PXIE_CLK10.

Figure 4-10 shows an example of a circuit that accomplishes this.

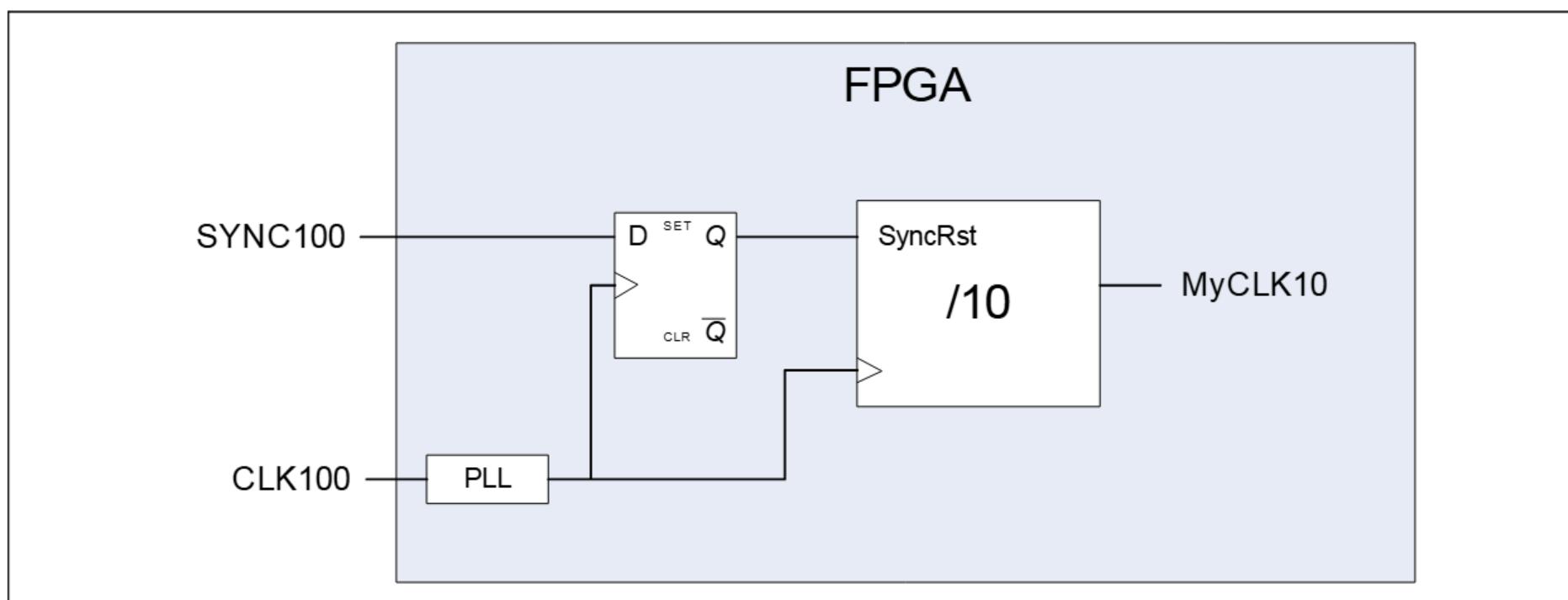


Figure 4-10. Circuit to recreate PXI_CLK10 Internally as MyCLK10

SYNC100 is captured by a flip-flop, the output of which is used to synchronously reset a divider that divides PXIE_CLK100 by 10. The resulting signal is in phase with PXI_CLK10. Note that this circuit will create a signal in phase with PXI_CLK10 even if the frequency of PXIE_SYNC100 is not 10 MHz.

建议：外围模块应使用以下电路终止 PXIE_SYNC100 信号：

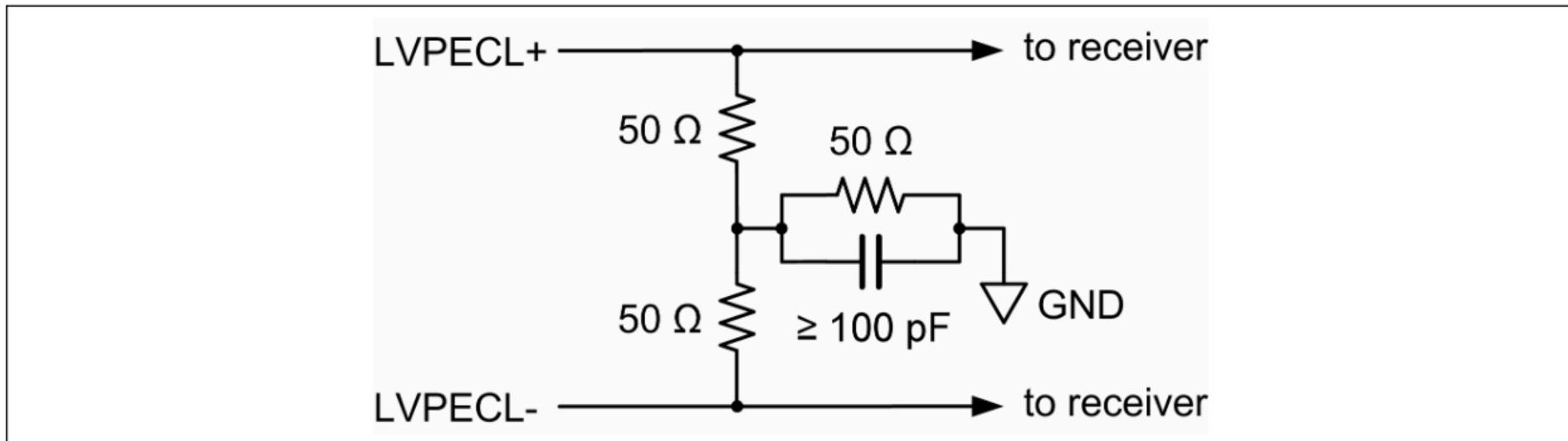


图 4-9. 用于端接 PXIE_SYNC100 电路的外围模块电路

规则：外围模块的端接距离不得超过背板连接器 PXIE_SYNC100 1 ns 以上。背板连接器和端接之间的任何传输线应具有 $100 \Omega \pm 10 \Omega$ 的特性差阻抗。

建议：由于 PXIE_SYNC100 信号的上升和下降时间很快，信号完整性在端接处或非常接近端接处时将达到最佳状态。在外围设备模块中，端接之外的连接的电气长度不应超过 160 ps，在典型的玻璃环氧树脂电路板中，走线长度约为 25 mm。为了保持良好的信号完整性，外围设备模块应仅将一个有源接收器连接到 PXIE_CLK100。如果使用多个接收器，则应仔细模拟配置以确保波形表现良好。

根据上述规则，由于 PXIE_SYNC100 的断言始终先于 PXI_CLK10 的上升沿，因此 PXI Express 外设模块可以在不连接到 PXIE_CLK10 的情况下创建与 PXI_CLK10 同相的信号。



图 4-10 显示了实现此目的的电路示例。

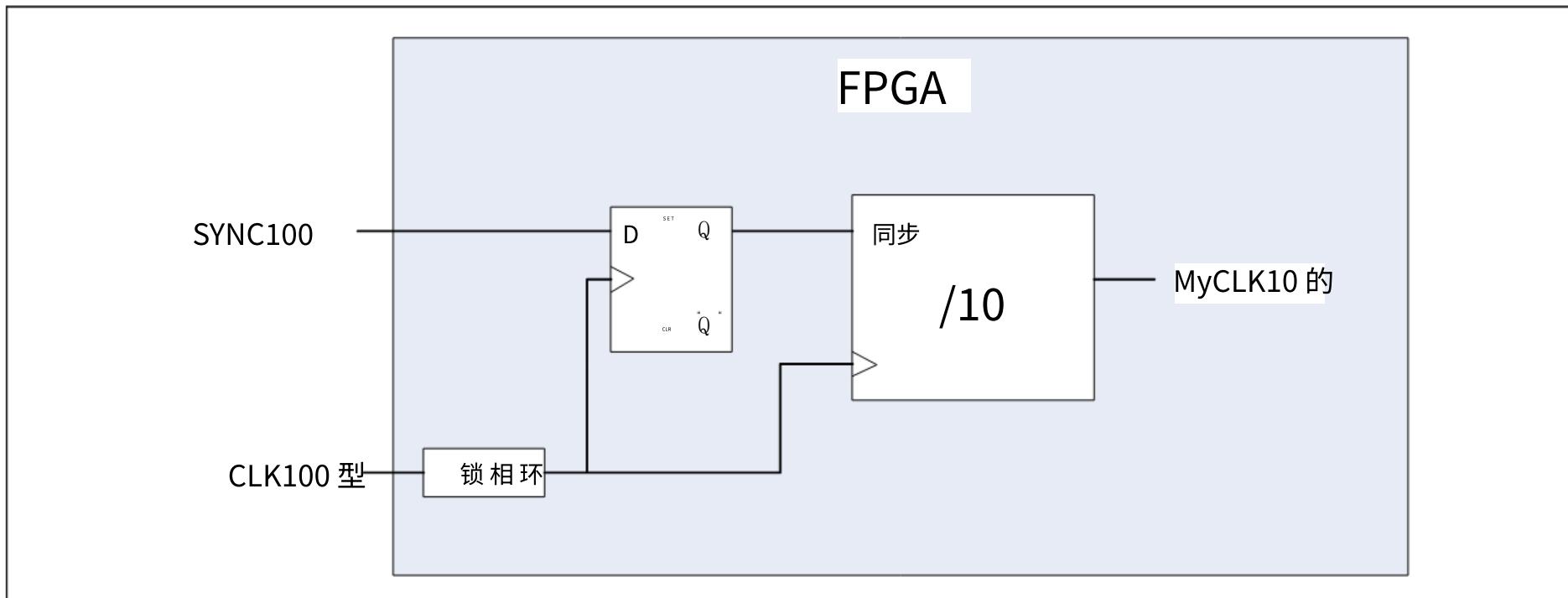


图 4-10. 在内部重新创建 PXI_CLK10 为 MyCLK10 的电路

SYNC100 由触发器捕获，其输出用于同步复位将 PXIE_CLK100 除以 10 的分频器。生成的信号与 PXI_CLK10 同相。请注意，即使 PXIE_SYNC100 的频率不是 10 MHz，该电路也会产生与 PXI_CLK10 同相的信号。

OBSERVATION: The maximum skew of MyCLK10 and PXI_CLK10 is determined by the skew of PXIE_CLK100 between slots, the skew between PXI_CLK10 and PXIE_CLK100, the clock-to-out time of flip-flops internal to the FPGA, and the insertion delay of the PXIE_CLK100 signal (including added jitter).

4.5 Differential Triggers

The PXIE_DSTARA, PXIE_DSTARB, and PXIE_DSTARC signals are differential point-to-point connections between the System Timing Slot and the Peripheral Slots. For each of these three signals, there is an independent differential pair between each Peripheral Slot and the System Timing Slot. Additionally, all signals are matched length.

PXIE_DSTARA is designed for distributing high-speed, high-quality clock signals from the System Timing Slot to the peripherals.

PXIE_DSTARB is designed for distributing high-speed, high-quality trigger signals from the System Timing Slot to the peripherals.

PXIE_DSTARC is designed for sending high-speed, high-quality trigger or clock signals from the peripherals to the System Timing Slot.

The PXIE_DSTARA signal is a fast-switching LVPECL clock for precise timing. The PXIE_DSTARB and PXIE_DSTARC signals are fast-switching LVDS clock/triggers for high-speed synchronization while maintaining compatibility with common FPGAs and other ICs.

4.5.1 Chassis Requirements

If a PXI Express System Timing Slot is implemented within a PXI Express Chassis, there will be a set of three differential pairs connecting each slot to the System Timing Slot in a star configuration for the purpose of timing and synchronization. The low slot-to-slot skew and signal-to-signal skew make these ideal for transferring a clock and synchronous trigger. These differential pairs will be referred to as a PXIE DSTAR set. To make backplane routing possible and reasonable, the Chassis developer will have the flexibility to route any PXIE DSTAR set to any slot provided that members of the set are not split between separate slots.



The rules and recommendations in this section only apply if the PXI Express Chassis implements a System Timing Slot.

RULE: A PXIE DSTAR set SHALL be defined as containing the three differential signal pairs (PXIE_DSTARA n , PXIE_DSTARB n , PXIE_DSTARC n), where n denotes the PXIE DSTAR set number.

RULE: All differential pairs within a PXIE DSTAR set SHALL be routed to the same slot.

RULE: If a PXIE DSTAR set is routed to a Peripheral Slot, its signals SHALL be connected to the Peripheral Slot according to Table 4-8, where n denotes PXIE DSTAR set number.

Table 4-8. PXIE_DSTAR Set Mapping

Differential System Timing Pair	Peripheral Slot Pair on XP3
PXIE_DSTARA n +	PXIE_DSTARA+
PXIE_DSTARA n -	PXIE_DSTARA-
PXIE_DSTARB n +	PXIE_DSTARB+
PXIE_DSTARB n -	PXIE_DSTARB-

4. 电气要求

观察：MyCLK10 和 PXI_CLK10 的最大偏斜由时隙之间的 PXIE_CLK100 偏斜、PXI_CLK10 和 PXIE_CLK100 之间的偏斜、FPGA 内部触发器的时钟到输出时间以及 PXIE_CLK100 信号的插入延迟（包括附加抖动）决定。

4.5 差动触发器

PXIE_DSTARA、PXIE_DSTARB 和 PXIE_DSTARC 信号是系统时序时隙和外设时隙之间的差分点对点连接。对于这三个信号中的每一个，每个外设时隙和系统时序时隙之间都有一个独立的差分对。此外，所有信号的长度都是匹配的。

PXIE_DSTARA 设计用于将高速、高质量的时钟信号从系统时序插槽分配到外设。

PXIE_DSTARB 设计用于将高速、高质量的触发信号从系统定时插槽分配到外设。

PXIE_DSTARC 设计用于将高速、高质量的触发或时钟信号从外设发送到系统时序插槽。

PXIE_DSTARA 信号是用于精确定时的快速开关 LVPECL 时钟。PXIE_DSTARB 和 PXIE_DSTARC 信号是用于高速同步的快速开关 LVDS 时钟/触发器，同时保持与常见 FPGA 和其他 IC 的兼容性。

4.5.1 机箱要求

如果 PXI Express 系统时序插槽是在 PXI Express 机箱中实现的，则将有一组三个差分对将每个插槽连接到星形配置中的系统时序插槽，以进行时序和同步。低插槽到插槽偏斜和信信号偏斜使它们成为传输时钟和同步触发器的理想选择。这些差分对将称为 PXIE DSTAR 集。为了使背板布线成为可能且合理，机箱开发人员可以灵活地将任何 PXIE DSTAR 集路由到任何插槽，前提是该集的成员不在单独的插槽之间拆分。



本节中的规则和建议仅在 PXI Express 机箱实现系统时序插槽时适用。

规则：PXIE DSTAR 集应定义为包含三个差分信号对（PXIE_DSTARAn、PXIE_DSTARBn、PXIE_DSTARCn），其中 n 表示 PXIE DSTAR 集编号。

规则：PXIE DSTAR 集中的所有差分对应路由到同一插槽。

规则：如果 PXIE DSTAR 集被路由到外设插槽，则其信号应根据表 4-8 连接到外设插槽，其中 n 表示 PXIE DSTAR 集编号。

表 4-8.PXIE_DSTAR 集映射

差分系统时序对	XP3 上的外围设备插槽对
PXIE_DSTARAn+	PXIE_DSTARA+
PXIE_DSTARAn-	PXIE_DSTARA-
PXIE_DSTARBn+	PXIE_DSTARB+
PXIE_DSTARBn-	PXIE_DSTARB-

Table 4-8. PXIe_DSTAR Set Mapping (Continued)

Differential System Timing Pair	Peripheral Slot Pair on XP3
PXIe_DSTARC n +	PXIe_DSTARC+
PXIe_DSTARC n -	PXIe_DSTARC-

PERMISSION: A PXIe DSTAR set MAY be routed to the PXIe_DSTARA, PXIe_DSTARB and PXIe_DSTARC pins on any slot.

RULE: If a slot is connected to a PXIe DSTAR set from the System Timing Slot, it SHALL only be connected to the signals from one PXIe DSTAR set.

RULE: One PXIe DSTAR set SHALL be routed back to the PXI Express System Timing Slot XP3 connector following the interpair and pair-to-pair length matching requirements placed on these signals in this section.

RULE: Every PXI Express Peripheral Slot, PXI Express Hybrid Slot and PXI Express System Timing Slot SHALL have a PXIe DSTAR set routed to it from the PXI Express System Timing Slot unless the total number of these slots exceeds the number of available PXIe DSTAR sets.

OBSERVATION: The PXIe DSTAR set to slot mapping is specified in the Chassis .ini file according to the format specified in the *PXI Express Software Specification*.

OBSERVATION: The pinout for the System Timing Slot was chosen so that when placed in the middle of a backplane, the signal lengths can be kept to a minimum and the layer count will be minimized by keeping all or most of the differential pairs on one routing layer.

RULE: The backplane SHALL route the PXIe_DSTAR signals to each slot with balanced transmission line pairs having a differential impedance of $100 \Omega \pm 10 \Omega$.



OBSERVATION: Equivalently, each trace in the transmission line pairs SHOULD have an odd-mode impedance of $50 \Omega \pm 5 \Omega$.

RECOMMENDATION: All PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC pairs SHOULD be routed on a single layer referenced to a solid ground plane to improve radiated immunity when traces are floating.

RULE: The time skew of the propagation delay of any two PXIe_DSTAR pairs (including all PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC signals) across the backplane SHALL NOT exceed 150 ps, including the backplane connectors.

RULE: The time skew of the propagation delay of the two signals within a PXIe_DSTAR differential pair across the backplane SHALL NOT exceed 25 ps, including the backplane connectors.

4.5.2 PXIe Peripheral Module / Slot Requirements

4.5.2.1 PXIe_DSTARA

RULE: If a Peripheral Module receives PXIe_DSTARA, it SHALL terminate both lines with a $50 \Omega (\pm 5 \Omega)$ load to 1.3 V (± 0.2 V) or Thévenin equivalent. If a Peripheral Module does not receive PXIe_STARA, it SHALL leave the lines unconnected and unterminated.

表 4-8.PXIe_DSTAR 集映射 (续)

差分系统时序对	XP3 上的外围设备插槽对
PXIe_DSTARCn+	PXIe_DSTARC+
PXIe_DSTARCn-	PXIe_DSTARC-

权限：PXIe DSTAR 集可以路由到任何插槽上的 PXIe_DSTARA、PXIe_DSTARB 和 PXIe_DSTARC 引脚。

规则：如果一个插槽从系统时序插槽连接到 PXIe DSTAR 集，则它只能连接到来自一个 PXIe DSTAR 集的信号。

规则：一个 PXIe DSTAR 组应按照本节中对这些信号的对间和对对长度匹配要求路由回 PXI Express 系统时序插槽 XP3 连接器。

规则：每个 PXI Express 外设插槽、PXI Express 混合插槽和 PXI Express 系统时序插槽都应有一个 PXIe DSTAR 集，从 PXI Express 系统时序插槽路由到它，除非这些插槽的总数超过可用的 PXIe DSTAR 集的数量。

观察：PXIe DSTAR 设置为插槽映射是根据 PXI Express 软件规范中指定的格式在机箱.ini 文件中指定的。

观察：选择系统时序插槽的引脚排列，以便当放置在背板中间时，信号长度可以保持在最小值，并且通过将所有或大部分差分对保持在一个布线层上来最小化层数。

规则：背板应将 PXIe_DSTAR 信号路由到每个插槽，其差分阻抗为 $100 \Omega \pm 10 \Omega$ 的平衡传输线对。



观察：等效地，传输线对中的每条走线都应具有 $50 \Omega \pm 5 \Omega$ 的奇模阻抗。

建议：所有 PXIe_DSTARA、PXIe_DSTARB 和 PXIe_DSTARC 对都应布线在参考实心接地平面的单层上，以提高走线浮动时的辐射抗扰度。

规则：背板上任意两对 PXIe_DSTAR（包括所有 PXIe_DSTARA、PXIe_DSTARB 和 PXIe_DSTARC 信号）的传播延迟的时间偏差不得超过 150 ps，包括背板连接器。

规则：背板上 PXIe_DSTAR 差分对内两个信号传播延迟的时间偏差不应超过 25 ps，包括背板连接器。

4.5.2 PXIe 外设模块/插槽要求

4.5.2.1 PXIe_DSTARA

规则：如果外围设备模块接收到 PXIe_DSTARA，它应以 50Ω ($\pm 5 \Omega$) 负载终止两条线路，负载为 1.3 V ($\pm 0.2 \text{ V}$) 或 Thévenin 等效值。如果外围设备模块未接收 PXIe_STARA，则应使线路未连接且末端接。

4. Electrical Requirements

RECOMMENDATION: Peripheral Modules that are receiving PXIE_DSTARA SHOULD terminate the PXIE_DSTARA signal with the following circuit:

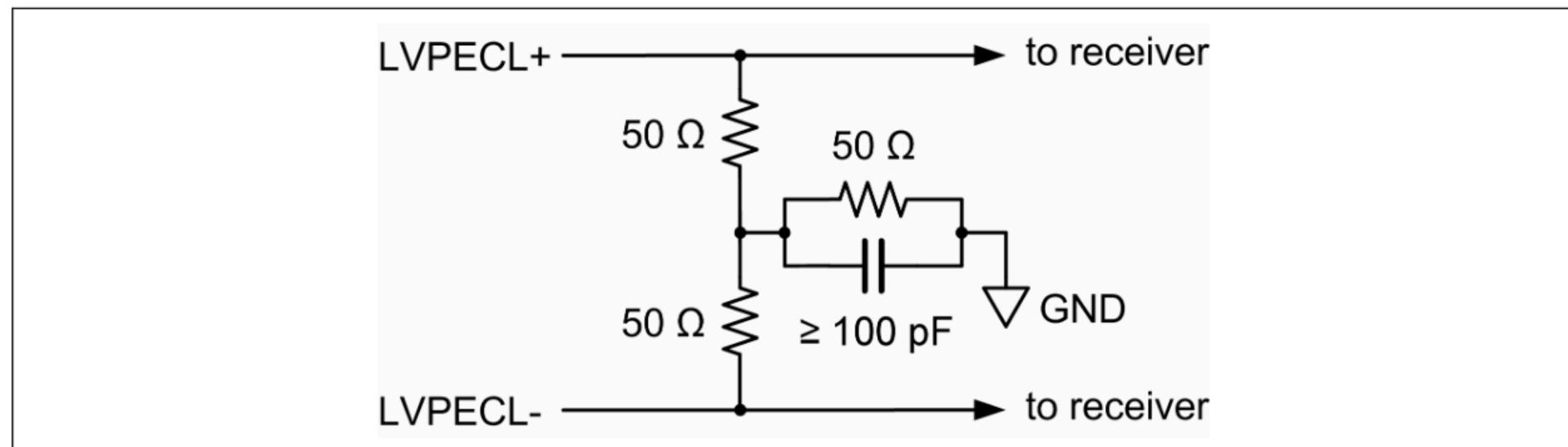


Figure 4-11. Peripheral Module Circuit for Terminating PXIE_DSTARA

RULE: Peripheral Modules SHALL NOT terminate PXIE_DSTARA more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of $100\ \Omega \pm 10\ \Omega$.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIE_DSTARA signal, signal integrity will be best at or very near the termination. The electrical length of the connections between the termination and the LVPECL Receiver SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIE_DSTARA. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.5.2.2 PXIE_DSTARB

RULE: If a Peripheral Module receives PXIE_DSTARB, it SHALL terminate the lines with a $100\ \Omega \pm 10\ \Omega$ differential resistor.

RULE: Peripheral Modules SHALL NOT terminate PXIE_DSTARB more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of $100\ \Omega \pm 10\ \Omega$.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIE_DSTARB signal, signal integrity will be best at or very near the termination. The electrical length of the connections between the termination and the LVDS Receiver SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIE_DSTARB. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.5.2.3 PXIE_DSTARC

RULE: If the Peripheral Module chooses to implement PXIE_DSTARC, the signal provided SHALL be a differential, LVDS signal. The Peripheral Module SHALL transmit the signal to the System Timing Slot with a balanced transmission line pair having a differential impedance of $100\ \Omega \pm 10\ \Omega$.

RULE: When the PXIE_DSTARC pair is terminated with a $100\ \Omega$ differential load at the Receiver, the voltage levels at the connector to the System Timing Module SHALL be compliant with the TIA/EIA-644 LVDS specification.

4. 电气要求

建议：接收 PXIE_DSTARA 的外设模块应通过以下电路终止 PXIE_DSTARA 信号：

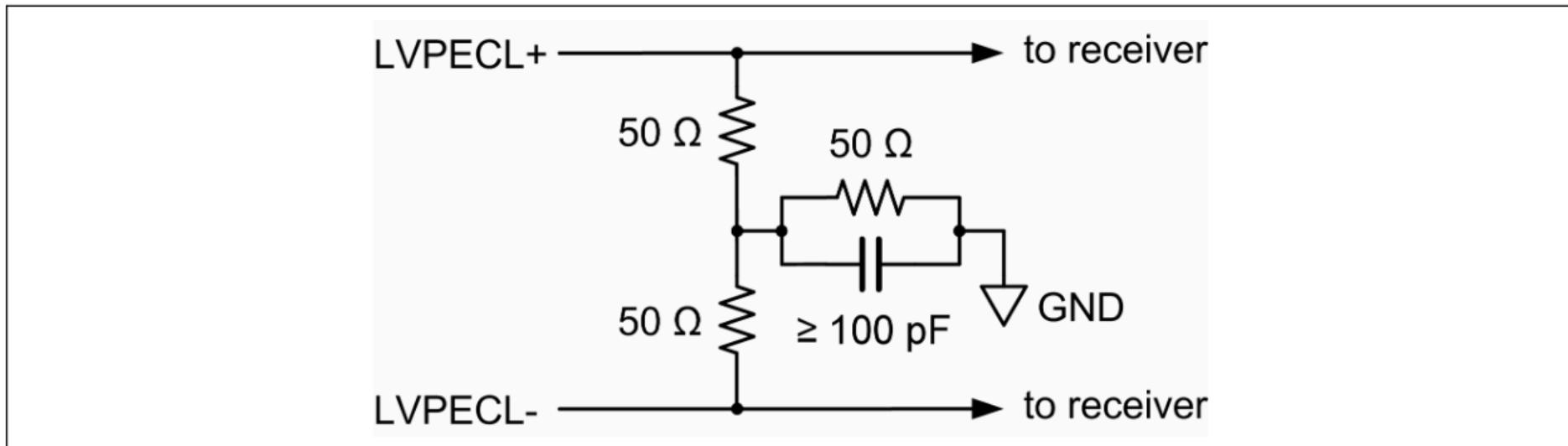


图 4-11. 用于端接 PXIE_DSTARA 的外围模块电路

规则：外围模块的端接距离不得超过背板连接器超过 1 ns PXIE_DSTARA。背板连接器和端接之间的任何传输线应具有 $100 \Omega \pm 10 \Omega$ 的特性差阻抗。

建议：由于 PXIE_DSTARA 信号的上升和下降时间很快，信号完整性在端接处或非常接近端接处时将达到最佳状态。端接和 LVPECL 接收器之间连接的电气长度不应超过 160 ps，在典型的玻璃环氧树脂电路板中，走线长度约为 25 mm。为了保持良好的信号完整性，外设模块应仅将一个有源接收器连接到 PXIE_DSTARA。如果使用多个接收器，则应仔细模拟配置以确保波形表现良好。

4.5.2.2 PXIE_DSTARB

规则：如果外围模块接收到 PXIE_DSTARB，它应使用 $100 \Omega \pm 10 \Omega$ 差分电阻器端接线路。

规则：外围模块的端接距离不得超过背板连接器 PXIE_DSTARB 1 ns 以上。背板连接器和端接之间的任何传输线应具有 $100 \Omega \pm 10 \Omega$ 的特性差阻抗。

建议：由于 PXIE_DSTARB 信号的上升和下降时间很快，信号完整性在端接处或非常接近端接处时将达到最佳状态。端接和 LVDS 接收器之间连接的电气长度不应超过 160 ps，在典型的玻璃环氧树脂电路板中，走线长度约为 25 mm。为了保持良好的信号完整性，外设模块应仅将一个有源接收器连接到 PXIE_DSTARB。如果使用多个接收器，则应仔细模拟配置以确保波形表现良好。



4.5.2.3 PXIE_DSTARC

规则：如果外设模块选择实现 PXIE_DSTARC，则提供的信号应为差分 LVDS 信号。外设模块应使用差分阻抗为 $100 \Omega \pm 10 \Omega$ 的平衡传输线对将信号传输到系统定时插槽。

规则：当 PXIE_DSTARC 对在接收器上以 100Ω 差分负载端接时，系统定时模块连接器处的电压电平应符合 TIA/EIA-644 LVDS 规范。

RULE: The signal source SHALL ensure that the LVDS driver is off (either tri-stated or driving a constant) by default, and MAY only enable it under software control when a Receiver with a $100\ \Omega$ differential termination resistor is known to exist.

4.5.3 System Timing Module/Slot Requirements

4.5.3.1 PXIE_DSTARA

RULE: The PXIE_DSTARA signals provided by the System Timing Module SHALL be differential 3.3 V LVPECL signals. The System Timing Module SHALL transmit the signals to all slots with balanced transmission line pairs having a differential impedance of $100\ \Omega \pm 10\ \Omega$. The System Timing Module SHALL NOT include any termination or bias network on the transmission lines, except to ensure that each driver is disabled when unterminated by a Module.

RULE: When each line of the PXIE_DSTARA pair is terminated with a $50\ \Omega$ load to 1.30 V (or Thévenin equivalent), the absolute value of the differential voltage across the pair at the Peripheral Module connector SHALL be 800 mV nominally and SHALL NOT be less than 400 mV (except during transition) or greater than 1000 mV. The V_{OH} level for each line SHALL be greater than 2.0 V and less than 2.5 V.

OBSERVATION: While many FPGAs have “LVPECL” output drivers, these drivers are generally not compatible with the aforementioned LVPECL requirement.

RULE: The PXIE_DSTARA signal to each Peripheral Slot SHALL be driven by an independent differential LVPECL driver.

RECOMMENDATION: The PXIE_DSTARA signal SHOULD have a duty cycle between 45% and 55%, measured by the differential 0 V transition times. The 20%-to-80% rise and fall times SHOULD NOT exceed 350 ps.



RECOMMENDATION: The time skew between rising or falling edges of the PXIE_DSTARA signals at any two connections to the backplane SHOULD NOT exceed 200 ps. The edges are defined as the differential 0 V transition times.

RECOMMENDATION: System Timing Modules SHOULD specify the maximum skew between all PXIE_DSTARA signals as provided to the pins of the connectors on the System Timing Module which connect it to the backplane.

4.5.3.2 PXIE_DSTARB

RULE: The PXIE_DSTARB signal provided by System Timing Module SHALL be a differential, LVDS signal. The System Timing Module SHALL transmit the signal to each slot with a balanced transmission line pair having a differential impedance of $100\ \Omega \pm 10\ \Omega$.

RULE: When the PXIE_DSTARB pair is terminated with a $100\ \Omega$ differential load at the Receiver the voltage levels at the connector to the Peripheral Module SHALL be compliant with the TIA/EIA-644 LVDS specification.

RULE: The signal source SHALL ensure that the LVDS driver is off (either tri-stated or driving a constant) by default, and may only enable it under software control when a Receiver with a $100\ \Omega$ differential termination resistor is known to exist.

RULE: The PXIE_DSTARB signal to each Peripheral Slot SHALL be driven by an independent differential LVDS driver.

规则：信号源应确保 LVDS 驱动器默认关闭（三态或驱动常数），并且仅当已知存在具有 100Ω 差分端接电阻的接收器时，才能在软件控制下启用它。

4.5.3 系统时序模块/插槽要求

4.5.3.1 PXIe_DSTARA

规则：系统定时模块提供的 PXIe_DSTARA 信号应为差分 3.3 V LVPECL 信号。系统定时模块应将信号传输到具有差分阻抗为 $100 \Omega \pm 10 \Omega$ 的平衡传输线对的所有插槽。系统定时模块“不应在传输线上包含任何端接或偏置网络，除非确保每个驱动器在被模块末端接时被禁用。”

规则：当 PXIe_DSTARA 对的每条线路以 50Ω 负载端接至 1.30 V（或 Thévenin 等效值）时，外围模块连接器处两对两端的差分电压的绝对值应标称为 800 mV，且不得低于 400 mV（过渡期间除外）或大于 1000 mV。每条线路的 Vlevel 应大于 2.0 V 且小于 2.5 V。

观察：虽然许多 FPGA 都有“LVPECL”输出驱动器，但这些驱动器通常与上述 LVPECL 要求不兼容。

规则：每个外设插槽的 PXIe_DSTARA 信号应由独立的差分 LVPECL 驱动器驱动。

建议：PXIe_DSTARA 信号的占空比应在 45% 至 55% 之间，以差分 0 V 转换时间测量。20% 至 80% 的上升和下降时间不应超过 350 ps。

建议：在背板的任意两个连接处，PXIe_DSTARA 信号的上升沿或下降沿之间的时间偏差不应超过 200 ps。边沿定义为差分 0 V 转换时间。



建议：系统定时模块应指定所有 PXIe_DSTARA 信号之间的最大偏斜，该信号提供给系统定时模块上将其连接到背板的连接器引脚。

4.5.3.2 PXIe_DSTARB

规则：系统定时模块提供的 PXIe_DSTARB 信号应为差分 LVDS 信号。系统定时模块应将信号传输到具有差分阻抗为 $100 \Omega \pm 10 \Omega$ 的平衡传输线对的每个插槽。

规则：当 PXIe_DSTARB 对在接收器上以 100Ω 差分负载端接时，外围模块连接器处的电压电平应符合 TIA/EIA-644 LVDS 规范。

规则：信号源应确保 LVDS 驱动器默认关闭（三态或驱动常数），并且只有在已知存在具有 100Ω 差分终端电阻的接收器时，才能在软件控制下启用它。

规则：每个外设插槽的 PXIe_DSTARB 信号应由独立的差分 LVDS 驱动器驱动。

RECOMMENDATION: System Timing Modules SHOULD specify the maximum skew between all PXIE_DSTARA and PXIE_DSTARB signals, as provided to the pins of the connectors on the System Timing Module which connect it to the backplane.

4.5.3.3 PXIE_DSTARC

RULE: If the System Timing Module receives PXIE_DSTARC, it SHALL terminate the pairs differentially with $100\ \Omega \pm 10\ \Omega$ resistors.

RULE: The System Timing Module SHALL NOT terminate PXIE_DSTARC more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of $100\ \Omega \pm 10\ \Omega$.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIE_DSTARC signal, signal integrity will be best at or very near the termination. The electrical length of the connections between the termination and the LVDS Receivers SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, the System Timing Module SHOULD connect only one active receiver to each PXIE_DSTARC pair. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.6 Slot Identification

Slot Identification in PXI Express is performed using the geographical address pins (GA) in each slot. The software mechanisms for reporting the value encoded on these pins is defined in the *PXI Express Software Specification*.

RULE: A PXI Express Module, other than a PXI Express System Module, must provide a software mechanism for the PXI Express System Module to read the value on pins GA(4:0) in the slot where the Module is located.



OBSERVATION: The System Module does not need to report its slot number via software, because it can be assumed to be in Slot 1.

OBSERVATION: PXI-1 Peripheral Modules and Hybrid Slot Compatible PXI-1 Peripheral Modules are not required to provide a software mechanism for the PXI Express System Module to read the value on pins GA(4:0) in the slot where the Module is located.

RULE: A PXI Express Module SHALL include software that reports its slot number using the interfaces specified in the *PXI Express Software Specification*.

4.7 Backplane Identification

RULE: PXI Express Chassis SHALL have the Backplane Identification and Capability Record implemented as a serial EEPROM or similar functioning device as defined by the *CompactPCI Express Specification*.

Within the Backplane Identification and Capability Record is a Peripheral Slot descriptor that requires additional definition and clarification to handle the System Timing Slot and the different names used for slots within PXI Express.

4. 电气要求

建议：系统定时模块应指定所有 PXIE_DSTARA 和 PXIE_DSTARB 信号之间的最大偏斜，如系统定时模块上将其连接到背板的连接器引脚所提供的。

4.5.3.3 PXIE_DSTARC

规则：如果系统定时模块接收到 PXIE_DSTARC，它应用 $100 \Omega \pm 10 \Omega$ 电阻器差分端接这些对。

规则：系统定时模块的端接距离不得超过背板连接器的电气长度 PXIE_DSTARC 1 ns。背板连接器和端接之间的任何传输线都应具有 $100 \Omega \pm 10 \Omega$ 的特性差分阻抗。

建议：由于 PXIE_DSTARC 信号的上升和下降时间很快，信号完整性在端接处或非常接近端接处时将达到最佳状态。端接和 LVDS 接收器之间连接的电气长度不应超过 160 ps，在典型的玻璃环氧树脂电路板中，走线长度约为 25 mm。为了保持良好的信号完整性，系统定时模块应仅将一个有源接收器连接到每对 PXIE_DSTARC。如果使用多个接收器，则应仔细模拟配置以确保波形表现良好。

4.6 插槽识别

PXI Express 中的插槽识别是使用每个插槽中的地理地址引脚 (GA) 执行的。用于报告这些引脚上编码的值的软件机制在 PXI Express 软件规范中定义。

规则：PXI Express 系统模块以外的 PXI Express 模块必须为 PXI Express 系统模块提供软件机制，以读取模块所在插槽中引脚 GA (4: 0) 上的值。



观察：系统模块不需要通过软件报告其插槽号，因为它可以假设在插槽 1 中。

观察：PXI-1 外设模块和混合插槽兼容 PXI-1 外设模块不需要为 PXI Express 系统模块提供软件机制来读取模块所在插槽中引脚 GA (4: 0) 上的值。

规则：PXI Express 模块应包括使用 PXI Express 软件规范中指定的接口报告其插槽号的软件。

4.7 背板识别

规则：PXI Express 机箱应将背板识别和功能记录实现为串行 EEPROM 或 CompactPCI Express 规范中定义的类似功能设备。

背板识别和功能记录中有一个外设插槽描述符，需要额外的定义和澄清来处理系统时序插槽以及 PXI Express 中用于插槽的不同名称。

RULE: Bits 2:0 of the Slot Type field of all Peripheral Slot Descriptors within a Backplane Identification and Capability Record of a PXI Express Chassis SHALL have the following definition:

Bits (2:0)
000 = N/A
001 = PXI Express Peripheral Slot
010 = PXI-1 Slot
011 = Hybrid Peripheral Slot
111 = System Timing Slot

4.8 SMBus Address Reservation

The SMBus allows backplane identification to be possible in PXI Express systems. It also allows for suppliers to implement Chassis-specific Functions without needing a PCI Express interface. The SMBus may connect to other devices on System Modules, so it is important that these other devices do not conflict with the Backplane Identification and Capability Record EEPROM and any Chassis-specific Functions. This section sets the requirements for SMBus addressing for any Chassis-specific Functions and CompactPCI Express sets addressing requirements for the Backplane Identification and Capability Record EEPROM.

Peripheral Module use of SMBus is also possible. To prevent addressing conflicts between Peripheral Modules and other devices on the SMBus, Peripheral Module SMBus devices are required to support the Address Resolution Protocol to have their address assigned.

PERMISSION: System Modules MAY connect devices related to System Module functionality to the SMBus.

OBSERVATION: The CompactPCI Express specification reserves SMBus address A4h for the Backplane Identification and Capability Record EEPROM. This requirement applies to PXI Express as well.

RULE: PXI Express System Modules SMBus devices that connect to the SMBus defined in this specification SHALL NOT use SMBus addresses 58h to 5Ch, C6h to C8h, and A4h.

RULE: Any SMBus devices within a PXI Express Chassis for Chassis-specific Functions other than the Backplane Identification and Capability Record EEPROM SHALL use addresses 58h to 5Ch.

OBSERVATION: The SMBus addresses specified are 8-bit addresses where the least significant bit represents read or write. This implies that for every even address, an odd address is reserved as well. For example, A4h is the SMBus address to write to the Backplane Identification and Capability Record EEPROM, and A5h is the address to read from the Backplane Identification and Capability Record EEPROM.

RULE: PXI Express Peripheral Modules that connect devices to the SMBus SHALL implement the Address Resolution Protocol (ARP) defined in the SMBus 2.0 Specification for setting their SMBus addresses of the devices.

4.9 Electrical Guidelines for 6U

In an effort to make efficient use of 3U PXI Express Modules in 6U PXI Express Chassis, the *PXI Express Hardware Specification* defines a 6U Slot that allows 3U Modules to be stacked within. This allows two 3U Modules to be used in 1 6U Slot. These systems have additional connectors in slots that support stacking 3U Modules. This section also covers the electrical rules associated with 6U PXI Express Chassis that support this feature and defines a 6U System Timing Module that can support the differential triggers for 3U Modules that are stacked in a 6U Slot.

规则：PXI Express 机箱背板标识和功能记录中所有外设插槽描述符的插槽类型字段的 2: 0 位应具有以下定义：

位 (2: 0)
000 = 不适用
001 = PXI Express 外设插槽
010 = PXI-1 插槽
011 = 混合外设插槽
111 = 系统时序插槽

4.8 SMBus 地址预留

SMBus 允许在 PXI Express 系统中进行背板识别。它还允许供应商实现特定于机箱的功能，而无需 PCI Express 接口。SMBus 可以连接到系统模块上的其他设备，因此这些其他设备不要与背板识别和功能记录 EEPROM 和任何机箱特定功能。本节设置了任何机箱特定功能的 SMBus 寻址要求，CompactPCI Express 设置了背板识别和功能记录 EEPROM 的寻址要求。

外围模块也可以使用 SMBus。为了防止解决外围模块与 SMBus 上其他设备之间的冲突，外围模块 SMBus 设备需要支持地址解析协议才能分配其地址。

权限：系统模块可以将与系统模块功能相关的设备连接到 SMBus。

观察：CompactPCI Express 规范为背板识别和功能记录 EEPROM 保留了 SMBus 地址 A4h。此要求也适用于 PXI Express。

规则：连接到本规范中定义的 SMBus 的 PXI Express 系统模块 SMBus 设备不得使用 SMBus 地址 58h 至 5Ch、C6h 至 C8h 和 A4h。

规则：PXI Express 机箱中用于机箱特定功能（背板识别和功能记录 EEPROM 除外）的任何 SMBus 设备应使用地址 58h 至 5Ch。

观察：指定的 SMBus 地址是 8 位地址，其中最低有效位表示读或写。这意味着对于每个偶数地址，也会保留一个奇数地址。例如，A4h 是写入背板标识和功能记录 EEPROM 的 SMBus 地址，A5h 是从背板标识和功能记录 EEPROM 读取的地址。

规则：将设备连接到 SMBus 的 PXI Express 外设模块应实现 SMBus 2.0 规范中定义的地址解析协议 (ARP)，以设置设备的 SMBus 地址。



4.9 6U 电气指南

为了在 6U PXI Express 机箱中有效利用 3U PXI Express 模块，PXI Express 硬件规范定义了一个 6U 插槽，允许将 3U 模块堆叠在其中。这允许在 1 个 6U 插槽中使用两个 3U 模块。这些系统的插槽中具有支持堆叠 3U 模块的附加连接器。本节还介绍了与支持此功能的 6U PXI Express 机箱相关的电气规则，并定义了一个 6U 系统时序模块，该模块可以支持堆叠在 6U 插槽中的 3U 模块的差分触发器。

4.9.1 6U Chassis that Support Stacking 3U Modules

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL route the signals for the upper and lower 3U Slots according to the type of 3U Slots being implemented within the 6U Slot (System, Hybrid, PXI Express Peripheral, PXI-1 or System Timing Slot).

RULE: If a PXI Express 6U Chassis that supports stacking 3U Modules cannot provide enough star triggers or differential triggers to support all slots via the lower 3U Slot within the System Timing Slot, the PXI Express 6U Chassis SHALL support stacking 3U System Timing Modules in the System Timing Slot.

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL implement a PXI Express Peripheral Slot or System Timing Slot only in the upper 3U Slot of a 6U System Timing Slot.

RULE: The PCI Express or PCI interfaces needed for the upper 3U Slots of PXI Express 6U Chassis that support stacking 3U Modules SHALL be provided by the backplane and SHALL NOT be provided by the System Controller Module.

OBSERVATION: The preceding rule allows most 6U CompactPCI Express System Modules to work in 6U PXI Express Chassis that support stacking 3U Modules.

4.10 Connector Pin Assignments

4.10.1 PXI Express Peripheral Slots and Modules

RULE: PXI Express Peripheral Slots and PXI Express Peripheral Modules SHALL use the pin assignments in Table 4-9.

Table 4-9. PXI Express Peripheral Slot and Module Pin Assignments



Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4 / XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	12V	12V	GND	GND	GND	GND	
4	GND	GND	GND	3.3V	3.3V	3.3V	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	PXle_CLK100+	PXle_CLK100-	GND	PXle_SYNC100+	PXle_SYNC100-	GND	PXle_DSTARC+	PXle_DSTARC-	GND	XP3 / XJ3 Connector
2	PRSNT#	PWREN#	GND	PXle_DSTARB+	PXle_DSTARB-	GND	PXle_DSTARA+	PXle_DSTARA-	GND	
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND	
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PETp1	1PETn1	GND	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND	
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND	
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND	
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND	

4.10.2 PXI Express System Slot and Modules

Two backplane routing schemes are allowed for the System Slot within the CompactPCI Express Specification. The 4 Link configuration maximizes the number of Links from the System Slot to Peripheral Slots, to Switches, to a Switch Slot, or PCI Express to PCI Bridges. However, the highest Lane count for each of the 4 Links is 4 lanes per Link. The 2 Link configuration assumes there are 2 Links coming from the System Board, where one of the Links can be up to eight lanes and the other Link can be up to 16 lanes.

4. 电气要求

4.9.1 支持堆叠 3U 模块的 6U 机箱

规则：支持堆叠 3U 模块的 6U PXI Express 机箱应根据 6U 插槽（系统、混合、PXI Express 外设、PXI-1 或系统时序插槽）内实现的 3U 插槽类型，为上部和下部 3U 插槽路由信号。

规则：如果支持堆叠 3U 模块的 PXI Express 6U 机箱无法提供足够的星形触发器或差分触发器，以通过系统时序插槽内的较低 3U 插槽支持所有插槽，则 PXI Express 6U 机箱应支持在系统时序插槽中堆叠 3U 系统时序模块。

规则：支持堆叠 3U 模块的 6U PXI Express 机箱应仅在 6U 系统时序插槽的上层 3U 插槽中实现 PXI Express 外设插槽或系统时序插槽。

规则：支持堆叠 3U 模块的 PXI Express 6U 机箱的上层 3U 插槽所需的 PCI Express 或 PCI 接口应由背板提供，而不应由系统控制器模块提供。

观察：上述规则允许大多数 6U CompactPCI Express 系统模块在支持堆叠 3U 模块的 6U PXI Express 机箱中工作。

4.10 连接器引脚分配

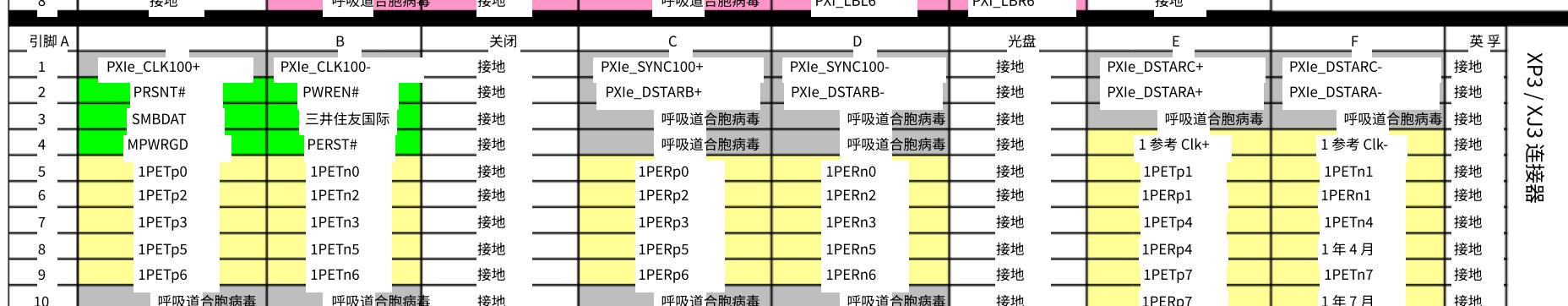
4.10.1 PXI Express 外设插槽和模块

规则：PXI Express 外设插槽和 PXI Express 外设模块应使用表 4-9 中的引脚分配。

表 4-9.PXI Express 外设插槽和模块引脚分配



引脚 Z	A	B	C	D	E	F
1	接地	GA4	GA3	GA2	GA1	GA0
2	接地	5 沃克斯	接地	系统#	唤醒#	接地
3	接地	12 伏	12 伏	接地	接地	接地
4	接地	接地	接地	3.3 伏	3.3 伏	3.3 伏
5	接地	PXI_TRIGGER3	PXI_TRIGGER4	PXI_TRIGGER5	PXI_TRIGGER6	PXI_TRIGGER7
6	接地	PXI_TRIGGER2	接地	ATNLED 的	PXI_STAR	PXI_CLK10
7	接地	PXI_TRIGGER1	PXI_TRIGGER0	ATNSW#	接地	PXI_TRIGGER7
8	接地	呼吸道合胞病毒	呼吸道合胞病毒	PXI_LBL6	PXI_LBR6	接地



引脚 A	B	关闭	C	D	光盘	E	F	英孚
1	PXIe_CLK100+	PXIe_CLK100-	PXIe_SYNC100+	PXIe_SYNC100-	接地	PXIe_DSTARC+	PXIe_DSTARC-	接地
2	PRSNT#	PWREN#	三井住友国际	接地	接地	PXIe_DSTARA+	PXIe_DSTARA-	接地
3	SMBDAT	MPWRGD	PERST#	接地	接地	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒
4	1PETp0	1PETn0	1PETp2	1PETn2	接地	1PETp0	1PETn0	1PETp1
5	1PETp2	1PETn2	1PETp3	1PETn3	接地	1PETp2	1PETn2	1PETn1
6	1PETp3	1PETn3	1PETp5	1PETn5	接地	1PETp3	1PETn3	1PETp1
7	1PETp5	1PETn5	1PETp6	1PETn6	接地	1PETp5	1PETn5	1PETp4
8	1PETp6	1PETn6	呼吸道合胞病毒	呼吸道合胞病毒	接地	1PETp6	1PETn6	1PETn4
9	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	接地	1PETp7	1PETn7	1PETp7
10	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	接地	1PETp7	1PETn7	1PETp7

4.10.2 PXI Express 系统插槽和模块

在 CompactPCI Express 规范中，系统插槽允许使用两种背板路由方案。4 链路配置可最大限度地提高从系统插槽到外围设备插槽、交换机、交换机插槽或 PCI Express 到 PCI 网桥的链路数量。但是，4 个链路中每个链路的最高通道数为每个链路 4 个通道。2 链路配置假设每 2 个链路来自主板，其中一个链路最多可以是 8 个通道，另一个链路最多可以是 16 个通道。

4.10.2.1 4 Link Configuration

RULE: PXI System Slots routed for the 4 Link Configuration SHALL use the pin assignments in Table 4-10.

RULE: PXI System Modules SHALL follow the pin assignments in Table 4-10 to support 4 Link operation.

Table 4-10. Pin Assignments for 4 Link Operation

Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4 / XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	RSV	RSV	RSV	RSV	RSV	GND	
4	GND	RSV	RSV	RSV	RSV	RSV	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND	
Pin	A	B	ab	C	D	cd	E	F
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#
3	SMBDAT	SMBCLK	GND	4RefClk+	4RefClk-	GND	2RefClk+	2RefClk-
4	RSV	PERST#	GND	3RefClk+	3RefClk-	GND	1RefClk+	1RefClk-
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	2PETp0	2PETn0
8	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PERp0	2PERn0
9	2PETp2	2PETn2	GND	2PERp2	2PERn2	GND	2PETp3	2PETn3
10	3PETp0	3PETn0	GND	3PERp0	3PERn0	GND	2PERp3	2PERn3
Pin	A	B	ab	C	D	cd	E	ef
1	3PETp1	3PETn1	GND	3PERp1	3PERn1	GND	3PETp2	3PETn2
2	3PETp3	3PETn3	GND	3PERp3	3PERn3	GND	3PERp2	3PERn2
3	4PETp0	4PETn0	GND	4PERp0	4PERn0	GND	4PETp1	4PETn1
4	4PETp2	4PETn2	GND	4PERp2	4PERn2	GND	4PERp1	4PERn1
5	4PETp3	4PETn3	GND	4PERp3	4PERn3	GND	RSV	RSV
6	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
7	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
8	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
9	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
10	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
Pin								
G	GND							
F	12V							
E	12V							
D	GND							
C	5V							
B	3.3V							
A	GND							

XP1 / XJ1 Connector



4.10.2.1 4 链路配置

规则：为 4 链路配置布线的 PXI 系统插槽应使用表 4-10 中的引脚分配。

规则：PXI 系统模块应遵循表 4-10 中的引脚分配，以支持 4 链路作。

表 4-10.4 链路作的引脚分配

引脚 Z	A	B	C	D	E	F	
1	接地	GA4	GA3	GA2	GA1	GA0	接地
2	接地	沃克斯	接地	系统#	唤醒#	警报#	接地
3	接地	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	接地
4	接地	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	接地
5	接地	PXI_TRIGGER3	PXI_TRIGGER4	PXI_TRIGGER5	接地	PXI_TRIGGER6	接地
6	接地	PXI_TRIGGER2	接地	呼吸道合胞病毒_STAR	PXI_CLK10	接地	
7	接地	PXI_TRIGGER1	PXI_TRIGGER0	呼吸道合胞病毒接地	PXI_TRIGGER7	接地	
8	接地	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	PXI_LBR6	接地

引脚 A	B	血型	C	D	光盘	E	F	英孚
1	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
2	呼吸道合胞病毒	呼吸道合胞病毒	接地	PWR_OK	PS_ON#	接地	链接帽	PWRBTN#
3	SMBDAT	三井住友国际	接地	4 参考 Clk+	4 参考 Clk-	接地	2 参考 Clk+	2RefClk-
4	呼吸道合胞病毒	PERST#	接地	3RefClk+	3RefClk-	接地	1 参考 Clk+	1 参考 Clk-
5	1PETp0	1PETn0	接地	1PERp0	1PERn0	接地	1PETp1	1PETn1
6	1PETp2	1PETn2	接地	1PERp2	1PERn2	接地	1PETp1	1PETn1
7	1PETp3	1PETn3	接地	1PERp3	1PERn3	接地	2PETp0	2PETn0
8	2PETp1	2PETn1	接地	2PERp1	2PERn1	接地	2PETp0	2PETn0
9	2PETp2	2PETn2	接地	2PERp2	2年 2月	接地	2PETp3	2PETn3
10	3PETp0	3PETn0	接地	3PERp0	3PERn0	接地	2PERp3	2PERn3

引脚 A	B	血型	C	D	光盘	E	F	英孚
1	3PETp1	3PETn1	接地	3PERp1	3PERn1	接地	3PETp2	3PETn2
2	3PETp3	3PETn3	接地	3PERp3	3PERn3	接地	3PERp2	3PERn2
3	4PETp0	4PETn0	接地	4PERp0	4PERn0	接地	4PETp1	4PETn1
4	4PETp2	4PETn2	接地	4PERp2	4PERn2	接地	4PERp1	4年 1月
5	4PETp3	4PETn3	接地	4PERp3	4PERn3	接地		
6	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
7	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
8	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
9	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
10	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒

针								
G GND								
传真 12V								
E 12 伏								
D GND								
C 5V								
B 3.3V								
A 接地								

XP1 / XJ1 连接器

4.10.2.2 2 Link Configuration

RULE: System Modules that can combine the four smaller Links into two larger Links SHALL follow the pin assignments in Table 4-11 when in 2 Link operation.

RULE: PXI System Slots routed for the 2 Link Configuration SHALL use the pin assignments in Table 4-11.

Table 4-11. Pin Assignments for 2 Link Operation

Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4 / XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	RSV	RSV	RSV	RSV	RSV	GND	
4	GND	RSV	RSV	RSV	RSV	RSV	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND	
Pin	A	B	ab	C	D	cd	E	F
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#
3	SMBDAT	SMBCLK	GND	RSVD	RSVD	GND	RSVD	RSVD
4	RSV	PERST#	GND	2RefClk+	2RefClk-	GND	1RefClk+	1RefClk-
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7
10	2PETp0	2PETn0	GND	2PERp0	2PERn0	GND	1PERp7	1PERn7
Pin	A	B	ab	C	D	cd	E	ef
1	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PETp2	2PETn2
2	2PETp3	2PETn3	GND	2PERp3	2PERn3	GND	2PERp2	2PERn2
3	2PETp4	2PETn4	GND	2PERp4	2PERn4	GND	2PETp5	2PETn5
4	2PETp6	2PETn6	GND	2PERp6	2PERn6	GND	2PERp5	2PERn5
5	2PETp7	2PETn7	GND	2PERp7	2PERn7	GND	2PETp8	2PETn8
6	2PETp9	2PETn9	GND	2PERp9	2PERn9	GND	2PERp8	2PERn8
7	2PETp10	2PETn10	GND	2PERp10	2PERn10	GND	2PETp11	2PETn11
8	2PETp12	2PETn12	GND	2PERp12	2PERn12	GND	2PERp11	2PERn11
9	2PETp13	2PETn13	GND	2PERp13	2PERn13	GND	2PETp14	2PETn14
10	2PETp15	2PETn15	GND	2PERp15	2PERn15	GND	2PERp14	2PERn14
Pin								
G	GND							
F	12V							
E	12V							
D	GND							
C	5V							
B	3.3V							
A	GND							

XP1 / XJ1 Connector

4. 电气要求

4.10.2.2 2 链路配置

规则：在 4 链路作时，可以将四个较小链路组合成两个较大链路的系统模块应遵循表 11-2 中的引脚分配。

规则：为 2 链路配置布线的 PXI 系统插槽应使用表 4-11 中的引脚分配。

表 4-11.2 链路作的引脚分配

引脚 Z	A	B	C	D	E	F	
1	接地	GA4	GA3	GA2	GA1	GA0	接地
2	接地	5 沃克斯	接地	系统#	唤醒#	警报#	接地
3	接地	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	接地
4	接地	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	呼吸道合胞病毒	接地
5	接地	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	接地	PXI_TRIG6	接地
6	接地	PXI_TRIG2	接地	呼吸道合胞病毒_STAR	PXI_CLK10	接地	
7	接地	PXI_TRIG1	PXI_TRIG0	呼吸道合胞病毒接地	PXI_TRIG7	接地	
8	接地	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒_LBR6	接地	

引脚 A	B	血型	C	D	光盘	E	F	英 孚
1	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
2	呼吸道合胞病毒	呼吸道合胞病毒	接地	PWR_OK	PS_ON#	接地	链接帽	PWRBTN#
3	SMBDAT	三井住友国际	接地	回复	回复	接地	回复	回复
4	呼吸道合胞病毒	PERST#	接地	2 参考 Clk+	2RefClk-	接地	1 参考 Clk+	1 参考 Clk-
5	1PETp0	1PETn0	接地	1PERp0	1PERn0	接地	1PETp1	1PETn1
6	1PETp2	1PETn2	接地	1PERp2	1PERn2	接地	1PERp1	1PERn1
7	1PETp3	1PETn3	接地	1PERp3	1PERn3	接地	1PETp4	1PETn4
8	1PETp5	1PETn5	接地	1PERp5	1PERn5	接地	1PERp4	1年 4 月
9	1PETp6	1PETn6	接地	1PERp6	1PERn6	接地	1PETp7	1PETn7
10	2PETp0	2PETn0	接地	2PERp0	2PERn0	接地	1PERp7	1年 7 月

引脚 A	B	血型	C	D	光盘	E	F	英 孚
1	2PETp1	2PETn1	接地	2PERp1	2PERn1	接地	2PETp2	2PETn2
2	2PETp3	2PETn3	接地	2PERp3	2PERn3	接地	2PERp2	2 年 2 月
3	2PETp4	2PETn4	接地	2PERp4	2 年 4 月	接地	2PETp5	2PETn5
4	2PETp6	2PETn6	接地	2PERp6	2PERn6	接地	2PERp5	2PERn5
5	2PETp7	2PETn7	接地	2PERp7	2 年 7 月	接地	2PETp8	2PETn8
6	2PETp9	2PETn9	接地	2PERp9	2 年 9 月	接地	2PERp8	2PERn8
7	2PETp10	2PETn10	接地	2PERp10	2 年 10 月	接地	2PETp11	2PETn11
8	2PETp12	2PETn12	接地	2PERp12	2 年 12 月	接地	2PERp11	2PERn11
9	2PETp13	2PETn13	接地	2PERp13	2 年 13 月	接地	2PETp14	2PETn14
10	2PETp15	2PETn15	接地	2PERp15	2PERn15	接地	2PERp14	2 年 14 月

针	XP1 / XJ1 连接器
G GND	
传真 12V	
E 12 伏	
D GND	
C 5V	
B 3.3V	
A 接地	



4.10.3 PXI Express Hybrid Peripheral Slot

RULE: PXI Express Hybrid Peripheral Slots SHALL use the pin assignments in Table 4-12.

Table 4-12. Hybrid Peripheral Slot Pin Assignments

Pin	Z	A	B	C	D	E	F		
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4 / XJ4 Connector	
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND		
3	GND	12V	12V	GND	GND	GND	GND		
4	GND	GND	GND	3.3V	3.3V	3.3V	GND		
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND		
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND		
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND		
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND		
Pin	A	B	ab	C	D	cd	E	F	
1	PXle_CLK100+	PXle_CLK100-	GND	PXle_SYNC100+	PXle_SYNC100-	GND	PXle_DSTARC+	PXle_DSTARC-	
2	PRSN#	PWREN#	GND	PXle_DSTARB+	PXle_DSTARB-	GND	PXle_DSTARA+	PXle_DSTARA-	
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	
Pin	Z	A	B	C	D	E	F		
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1 / J1 Connector	
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND		
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND		
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND		
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND		
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND		
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND		
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND		
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND		
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND		
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND		
12-14				Key Area					
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND		
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND		
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND		
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND		
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND		
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND		
5	GND	BRSPV1A5	BRSPV1B5	RST#	GND	GNT#	GND		
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND		
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND		
2	GND	TCK	5V	TMS	TDO	TDI	GND		
1	GND	5V	-12V	TRST#	+12V	5V	GND		



4.10.4 PXI-1 Slot

RULE: PXI-1 Slots SHALL follow the pin assignments defined in the *PXI Hardware Specification*.

4.10.3 PXI Express 混合外设插槽

规则：PXI Express 混合外设插槽应使用表 4-12 中的引脚分配。

表 4-12.混合外设插槽引脚分配

XP4 / XJ4 连接器

引脚 Z	A	B	C	D	E	F
1	接地	GA4	GA3	GA2	GA1	GA0
2	接地	5 沃克斯	接地	系统#	唤醒#	接地
3	接地	12 伏	12 伏	接地	警报#	接地
4	接地	接地	接地	3.3 伏	接地	接地
5	接地	PXI_TRIGGER3	PXI_TRIGGER4	PXI_TRIGGER5	接地	PXI_TRIGGER6
6	接地	PXI_TRIGGER2	接地	ATNLED 的	PXI_STAR	PXI_CLK10
7	接地	PXI_TRIGGER1	PXI_TRIGGER0	ATNSW#	接地	PXI_TRIGGER7
8	接地	呼吸道合胞病毒	接地	呼吸道合胞病毒	PXI_LBL6	PXI_LBR6

XP3 / XJ3 连接器

引脚 A	B	血型	C	D	光盘	E	F	英孚
1	PXIe_CLK100+	PXIe_CLK100-	接地	PXIe_SYNC100+	PXIe_SYNC100-	接地	PXIe_DSTARC+	PXIe_DSTARC-
2	PRSN#	PWREN#	接地	PXIe_DSTARB+	PXIe_DSTARB-	接地	PXIe_DSTARA+	PXIe_DSTARA-
3	SMBDAT	三井住友国际	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒
4	MPWRGD	PERST#	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	1 参考 Clk+	1 参考 Clk-
5	1PETp0	1PETn0	接地	1PERp0	1PERn0	接地	1PETp1	1PETn1
6	1PETp2	1PETn2	接地	1PERp2	1PERn2	接地	1PERp1	1PERn1
7	1PETp3	1PETn3	接地	1PERp3	1PERn3	接地	1PETp4	1PETn4
8	1PETp5	1PETn5	接地	1PERp5	1PERn5	接地	1PETp7	1PETn7
9	1PETp6	1PETn6	接地	1PERp6	1PERn6	接地	1年 4 月	1年 7 月
10	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒

P1 / J1 连接器

针	Z	A	B	C	D	E	F
25	接地	5 伏	REQ64#	枚举#	3.3 伏	5 伏	接地
24	接地	公元[1]	5 伏	V (I/O)	公元[0]	ACK64#	接地
23	接地	3.3 伏	公元[4]	公元[3]	5 伏	公元[2]	接地
22	接地	公元[7]	接地	3.3 伏	公元[6]	公元[5]	接地
21	接地	3.3 伏	公元[9]	公元[8]	M66EN	C/BE[0]#	接地
20	接地	公元[12]	接地	V (I/O)	公元[11]	公元[10]	接地
19	接地	3.3 伏	公元[15]	公元[14]	接地	公元[13]	接地
18	接地	SERR#	接地	3.3 伏	由	C/BE[1]#	接地
17	接地	3.3 伏	IPMB_SCL	IPMB_SDA	接地	PERR#	接地
16	接地	开发#	接地	V (I/O)	停止#	锁#	接地
15	接地	3.3 伏	框架#	IRDY#	BD_SEL#	TRDY#	接地
12-14				关键领域			
11	接地	公元[18]	公元[17]	公元[16]	接地	C/BE[2]#	接地
10	接地	公元[21]	接地	3.3 伏	公元[20]	公元[19]	接地
9	接地	C/BE[3]#	IDSEL	公元[23]	接地	公元[22]	接地
8	接地	公元[26]	接地	V (I/O)	公元[25]	公元[24]	接地
7	接地	公元[30]	公元[29]	公元[28]	接地	公元[27]	接地
6	接地	要求#	接地	3.3 伏	时钟	公元[31]	接地
5	接地	BRSVP1A5	BRSVP1B5	RST#	接地	GNT#	接地
4	接地	IPMB_PWR	健康#	V (I/O)	国际特派	内联	接地
3	接地	INTA#	国际#	国际技术#	5 伏	国际#	接地
2	接地	TCK 的	5 伏	TMS 系统	TDO 的	TDI 的	接地
1	接地	5 伏	-12 伏	TRST#	+12 伏	5 伏	接地

4.10.4 PXI-1 插槽

规则：PXI-1 插槽应遵循 PXI 硬件规范中定义的引脚分配。

4.10.5 System Timing Slot

RULE: System Timing Modules and System Timing Slots SHALL use the pinouts in Table 4-13.

Table 4-13. PXI Express System Timing Slot/Module Pinout

Pin	Z	A	B	C	D	E	F		
1	GND	GA4	GA3	GA2	GA1	GA0	GND		
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND		
3	GND	12V	12V	GND	GND	GND	GND		
4	GND	GND	GND	3.3V	3.3V	3.3V	GND		
5	GND	PXI_TRIGGER3	PXI_TRIGGER4	PXI_TRIGGER5	GND	PXI_TRIGGER6	GND		
6	GND	PXI_TRIGGER2	GND	ATNLED	PXI_CLK10_IN	PXI_CLK10	GND		
7	GND	PXI_TRIGGER1	PXI_TRIGGER0	ATNSW#	GND	PXI_TRIGGER7	GND		
8	GND	PXIe_SYNC_CTRL	GND	RSV	PXI_LBL6	PXI_LBR6	GND		
Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND
2	PRSNT#*	PWREN#*	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND
Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_DSTARC0+	PXIe_DSTARC0-	GND	PXIe_DSTARC8+	PXIe_DSTARC8-	GND	PXIe_DSTARB8+	PXIe_DSTARB8-	GND
2	PXIe_DSTARA0+	PXIe_DSTARA0-	GND	PXIe_DSTARC9+	PXIe_DSTARC9-	GND	PXIe_DSTARA8+	PXIe_DSTARA8-	GND
3	PXIe_DSTARB0+	PXIe_DSTARB0-	GND	PXIe_DSTARC1+	PXIe_DSTARC1-	GND	PXIe_DSTARA9+	PXIe_DSTARA9-	GND
4	PXIe_DSTARB1+	PXIe_DSTARB1-	GND	PXI_STAR0	PXI_STAR1	GND	PXIe_DSTARB9+	PXIe_DSTARB9-	GND
5	PXIe_DSTARA1+	PXIe_DSTARA1-	GND	PXI_STAR2	PXI_STAR3	GND	PXIe_DSTARC10+	PXIe_DSTARC10-	GND
6	PXIe_DSTARC2+	PXIe_DSTARC2-	GND	PXI_STAR4	PXI_STAR5	GND	PXIe_DSTARA10+	PXIe_DSTARA10-	GND
7	PXIe_DSTARB2+	PXIe_DSTARB2-	GND	PXI_STAR6	PXI_STAR7	GND	PXIe_DSTARB10+	PXIe_DSTARB10-	GND
8	PXIe_DSTARA2+	PXIe_DSTARA2-	GND	PXI_STAR8	PXI_STAR9	GND	PXIe_DSTARC11+	PXIe_DSTARC11-	GND
9	PXIe_DSTARC3+	PXIe_DSTARC3-	GND	PXI_STAR10	PXI_STAR11	GND	PXIe_DSTARA11+	PXIe_DSTARA11-	GND
10	PXIe_DSTARB3+	PXIe_DSTARB3-	GND	PXIe_DSTARC16+	PXIe_DSTARC16-	GND	PXIe_DSTARB11+	PXIe_DSTARB11-	GND
Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_DSTARA3+	PXIe_DSTARA3-	GND	PXIe_DSTARC7+	PXIe_DSTARC7-	GND	PXIe_DSTARC12+	PXIe_DSTARC12-	GND
2	PXIe_DSTARC4+	PXIe_DSTARC4-	GND	PXI_STAR12	PXI_STAR13	GND	PXIe_DSTARA12+	PXIe_DSTARA12-	GND
3	PXIe_DSTARB4+	PXIe_DSTARB4-	GND	PXIe_DSTARA16+	PXIe_DSTARA16-	GND	PXIe_DSTARB12+	PXIe_DSTARB12-	GND
4	PXIe_DSTARA4+	PXIe_DSTARA4-	GND	PXIe_DSTARB7+	PXIe_DSTARB7-	GND	PXIe_DSTARC13+	PXIe_DSTARC13-	GND
5	PXIe_DSTARC5+	PXIe_DSTARC5-	GND	PXI_STAR14	PXI_STAR15	GND	PXIe_DSTARA13+	PXIe_DSTARA13-	GND
6	PXIe_DSTARB5+	PXIe_DSTARB5-	GND	PXIe_DSTARB16+	PXIe_DSTARB16-	GND	PXIe_DSTARB13+	PXIe_DSTARB13-	GND
7	PXIe_DSTARA5+	PXIe_DSTARA5-	GND	PXIe_DSTARA7+	PXIe_DSTARA7-	GND	PXIe_DSTARC14+	PXIe_DSTARC14-	GND
8	PXIe_DSTARC6+	PXIe_DSTARC6-	GND	PXI_STAR16	RSV	GND	PXIe_DSTARA14+	PXIe_DSTARA14-	GND
9	PXIe_DSTARB6+	PXIe_DSTARB6-	GND	PXIe_DSTARC15+	PXIe_DSTARC15-	GND	PXIe_DSTARB14+	PXIe_DSTARB14-	GND
10	PXIe_DSTARA6+	PXIe_DSTARA6-	GND	PXIe_DSTARB15+	PXIe_DSTARB15-	GND	PXIe_DSTARA15+	PXIe_DSTARA15-	GND

4.11 POWER

The power requirements for PXI Express Chassis and Modules include all requirements defined in the *CompactPCI Express Specification*, as well as additional rules that set minimum requirements for power provided by Chassis. These additional rules enhance the interoperability between Modules and Chassis.

4. 电气要求

4.10.5 系统时序插槽

规则：系统定时模块和系统定时插槽应使用表 4-13 中的引脚排列。

表 4-13.PXI Express 系统时序插槽/模块引脚排列

针	Z	A	B	C	D	E	F
1	接地	GA4	GA3	GA2	GA1	GA0	接地
2	接地	5 沃克斯	接地	西森 #	唤醒#	警报#	接地
3	接地	12 伏	12 伏	接地	接地	接地	接地
4	接地	接地	接地	3.3 伏	3.3 伏	3.3 伏	接地
5	接地	PXI_TRIGGER3	PXI_TRIGGER4	PXI_TRIGGER5	接地	PXI_TRIGGER6	接地
6	接地	PXI_TRIGGER2	接地	ATNLED 的	PXI_CLK10_IN	PXI_CLK10	接地
7	接地	PXI_TRIGGER1	PXI_TRIGGER0	新南威尔士州 #	接地	PXI_TRIGGER7	接地
8	接地	PXIe_SYNC_CTRL	接地	呼吸道合胞病毒	PXI_LBL6	PXI_LBR6	接地

针	A	B	血型	C	D	光盘	E	F	英孚
1	PXIe_CLK100+	PXIe_CLK100-	接地	PXIe_SYNC100+	PXIe_SYNC100-	接地	PXIe_DSTARC+	PXIe_DSTARC-	接地
2	PRSNT#*	PWREN#*	接地	PXIe_DSTARB+	PXIe_DSTARB-	接地	PXIe_DSTARA+	PXIe_DSTARA-	接地
3	SMBDAT	三井住友国际	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地
4	MPWRGD*	PERST#	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	1 参考 Clk+	1 参考 Clk-	接地
5	1PETp0	1PETn0	接地	1PERp0	1PERn0	接地	1PETp1	1PETn1	接地
6	1PETp2	1PETn2	接地	1PERp2	1PERn2	接地	1PERp1	1PERn1	接地
7	1PETp3	1PETn3	接地	1PERp3	1PERn3	接地	1PETp4	1PETn4	接地
8	1PETp5	1PETn5	接地	1PERp5	1PERn5	接地	1PERp4	1 年 4 月	接地
9	1PETp6	1PETn6	接地	1PERp6	1PERn6	接地	1PETp7	1PETn7	接地
10	呼吸道合胞病毒	呼吸道合胞病毒	接地	呼吸道合胞病毒	呼吸道合胞病毒	接地	1PERp7	1 年 7 月	接地

针	A	B	血型	C	D	光盘	E	F	英孚
1	PXIe_DSTARC0+	PXIe_DSTARC0-	接地	PXIe_DSTARC8+	PXIe_DSTARC8-	接地	PXIe_DSTARB8+	PXIe_DSTARB8-	接地
2	PXIe_DSTARA0+	PXIe_DSTARA0-	接地	PXIe_DSTARC9+	PXIe_DSTARC9-	接地	PXIe_DSTARA8+	PXIe_DSTARA8-	接地
3	PXIe_DSTARB0+	PXIe_DSTARB0-	接地	PXIe_DSTARC1+	PXIe_DSTARC1-	接地	PXIe_DSTARA9+	PXIe_DSTARA9-	接地
4	PXIe_DSTARB1+	PXIe_DSTARB1-	接地	PXI_STAR0	PXI_STAR1	接地	PXIe_DSTARB9+	PXIe_DSTARB9-	接地
5	PXIe_DSTARA1+	PXIe_DSTARA1-	接地	PXI_STAR2	PXI_STAR3	GND	PXIe_DSTARC10+ PXIe_DSTARC10-		接地
6	PXIe_DSTARC2+	PXIe_DSTARC2-	接地	PXI_STAR4	PXI_STAR5	GND	PXIe_DSTARA10+ PXIe_DSTARA10-		接地
7	PXIe_DSTARB2+	PXIe_DSTARB2-	接地	PXI_STAR6	PXI_STAR7	GND	PXIe_DSTARB10+ PXIe_DSTARB10-		接地
8	PXIe_DSTARA2+	PXIe_DSTARA2-	接地	PXI_STAR8	PXI_STAR9	GND	PXIe_DSTARC11+ PXIe_DSTARC11-		接地
9	PXIe_DSTARC3+	PXIe_DSTARC3-	接地	PXI_STAR10	PXI_STAR11	GND	PXIe_DSTARA11+ PXIe_DSTARA11-		接地
10	PXIe_DSTARB3+	PXIe_DSTARB3-	GND	PXIe_DSTARC16+ PXIe_DSTARC16-		GND	PXIe_DSTARB11+ PXIe_DSTARB11-		接地

引脚 A	B	血型	C	D	光盘	E	F	英孚
1	PXIe_DSTARA3+	PXIe_DSTARA3-	接地	PXIe_DSTARC7+	PXIe_DSTARC7-	GND	PXIe_DSTARC12+ PXIe_DSTARC12-	接地
2	PXIe_DSTARC4+	PXIe_DSTARC4-	接地	PXI_STAR12	PXI_STAR13	GND	PXIe_DSTARA12+ PXIe_DSTARA12-	接地
3	PXIe_DSTARB4+	PXIe_DSTARB4-	GND	PXIe_DSTARA16+ PXIe_DSTARA16-		GND	PXIe_DSTARB12+ PXIe_DSTARB12-	接地
4	PXIe_DSTARA4+	PXIe_DSTARA4-	接地	PXIe_DSTARB7+	PXIe_DSTARB7-	GND	PXIe_DSTARC13+ PXIe_DSTARC13-	接地
5	PXIe_DSTARC5+	PXIe_DSTARC5-	接地	PXI_STAR14	PXI_STAR15	GND	PXIe_DSTARA13+ PXIe_DSTARA13-	接地
6	PXIe_DSTARB5+	PXIe_DSTARB5-	GND	PXIe_DSTARB16+ PXIe_DSTARB16-		GND	PXIe_DSTARB13+ PXIe_DSTARB13-	接地
7	PXIe_DSTARA5+	PXIe_DSTARA5-	接地	PXIe_DSTARA7+	PXIe_DSTARA7-	GND	PXIe_DSTARC14+ PXIe_DSTARC14-	接地
8	PXIe_DSTARC6+	PXIe_DSTARC6-	接地	PXI_STAR16	呼吸道合胞病毒	GND	PXIe_DSTARA14+ PXIe_DSTARA14-	接地
9	PXIe_DSTARB6+	PXIe_DSTARB6-	GND	PXIe_DSTARC15+ PXIe_DSTARC15-		GND	PXIe_DSTARB14+ PXIe_DSTARB14-	接地
10	PXIe_DSTARA6+	PXIe_DSTARA6-	GND	PXIe_DSTARB15+	PXIe_DSTARB15-	GND	PXIe_DSTARA15+ PXIe_DSTARA15-	接地

4.11 权力

PXI Express 机箱和模块的电源要求包括 CompactPCI Express 规范中定义的所有要求，以及为机箱提供的电源设置最低要求的附加规则。这些附加规则增强了模块和机箱之间的互作性。

4.11.1 Power Requirements from CompactPCI Express

RULE: PXI Express Chassis and Modules SHALL meet all the rules relating to power defined within the CompactPCI Express specification. These rules include but are not limited to the following:

- Voltage rails
- Current capacity of the power pins for a slot
- Regulation
- Ripple and noise
- Backplane power decoupling
- Power rail timing
- Power supply signals to and from the System Module and the associated timing requirements

4.11.2 Chassis Requirements

Minimum power supply requirements are specified to ensure that Module designers can design Modules knowing that they will operate in any PXI Express Chassis regardless of the number of slots or form factor.

4.11.2.1 Minimum Required Continuous Current

RULE: The power supply in a PXI Express Chassis SHALL provide at least the required amounts of continuous current and total power per slot specified in Table 4-14.

Table 4-14. PXI Express Chassis Minimum Required Continuous Current

	5 V	3.3 V	+12 V	-12 V	5 V _{AUX}	Total Power	Notes
System Controller Slot with 2 or More Expansion Slots	9 A	9 A	11 A	N/A	1 A	140 W	1, 2
System Controller Slot with 1 Expansion Slot	2 A	6 A	4 A	N/A	1 A	60 W	1
System Controller Slot with no Expansion Slots	1 A	3 A	2 A	N/A	1 A	30 W	1
PXI Express Peripheral Slot / System Timing Slot	N/A	3 A	2 A	N/A	0 A	30 W	1, 3
Hybrid Slot	2 A	3 A	2 A	0.25 A	0 A	30 W	1, 3, 4
PXI-1 Peripheral Slot	2 A	2 A	0.5 A	0.25 A	N/A	25.6 W	1

Notes:

1. The PXI Express Chassis is required to provide only the combined power specified in the Total Power column.
2. The PXI Express Chassis is required to provide only a total of 61.5 W combined power on 3.3 V and 5 V a System Controller Slot with two or more expansion slots.
3. There SHALL be 0.5 A of 5V_{AUX} available for all PXI Express Peripheral Modules to share.
4. A Hybrid Slot SHALL provide the continuous current required for a PXI Express Peripheral Module OR a PXI-1 Peripheral Module (not both at the same time).

4.11.1 CompactPCI Express 的电源要求

规则：PXI Express 机箱和模块应满足 CompactPCI Express 规范中定义的与电源相关的所有规则。这些规则包括但不限于以下内容：

- 电压轨
- 插槽电源引脚的电流容量
- 调节
- 纹波和噪声
- 背板电源去耦
- 电源轨正时
- 进出系统模块的电源信号和相关的时序要求

4.11.2 机箱要求

指定了最低电源要求，以确保模块设计人员可以在设计模块时知道它们可以在任何 PXI Express 机箱中运行，无论插槽数量或外形尺寸如何。

4.11.2.1 所需的最小连续电流

规则：PXI Express 机箱中的电源应至少提供表 4-14 中指定的每个插槽所需的连续电流和总功率。

表 4-14.PXI Express 机箱所需的最小连续电流

	5 伏	3.3 伏	+12 伏	-12 伏	5 伏	总 权力	笔记
带有 2 个或更多扩展插槽的系统控制器插槽	9 安	9 安	11 安	不适用	1 安	140 瓦	1, 2
带 1 个扩展插槽的系统控制器插槽	2 安	6 安	4 安	不适用	1 安	60 瓦	1
没有扩展插槽的系统控制器插槽	1 安	3 安	2 安	不适用	1 安	30 瓦	1
PXI Express 外设插槽/系统时序插槽	不适用	3 安	2 安	不适用	0 安	30 瓦	1, 3
混合老虎机	2 安	3 安	2 安	0.25 安	0 安	30 瓦	1, 3, 4
PXI-1 外设插槽	2 安	2 安	0.5 安	0.25 安	不适用	25.6 瓦	1

笔记：

1. PXI Express 机箱只需要提供总功率列中指定的组合功率。
2. PXI Express 机箱只需在具有两个或多个扩展插槽的 3.3 V 和 5 V 系统控制器插槽上提供总共 61.5 W 的组合功率。
3. 应有 0.5 A 的 5V 电压可供所有 PXI Express 外设模块共享。
4. 混合插槽应提供 PXI Express 外设模块或 PXI-1 外设模块（不能同时提供两者）所需的连续电流。

4. Electrical Requirements

OBSERVATION: The minimum current for each voltage rail provided by a power supply in a PXI Express Chassis with X PXI Express Peripheral Slots, Y Hybrid Slots, and Z PXI-1 Peripheral Slots can be determined by the following formulas:

$$+12 \text{ V: } 11 \text{ A} + (X + Y) \times 2 \text{ A} + Z \times 0.5 \text{ A}$$

$$3.3 \text{ V: } 9 \text{ A} + (X + Y) \times 3 \text{ A} + Z \times 2 \text{ A}$$

$$5 \text{ V: } 9 \text{ A} + (Y + Z) \times 2 \text{ A}$$

$$-12 \text{ V: } (Y + Z) \times 0.25 \text{ A}$$

$$5 \text{ V}_{\text{AUX}}: 1.5 \text{ A if } (X + Y) > 0; \text{ else } 1 \text{ A}$$

For an 8-slot Chassis with one PXI Express System Timing Slot, two Hybrid Slots, and four PXI-1 Slots, the minimum current for each voltage rail for the entire Chassis would be as follows:

$$+12 \text{ V: } 11 \text{ A} + (1 + 2) \times 2 \text{ A} + 4 \times 0.5 \text{ A} = 11 \text{ A} + 6 \text{ A} + 2 \text{ A} = 19 \text{ A}$$

$$3.3 \text{ V: } 9 \text{ A} + (1 + 2) \times 3 \text{ A} + 4 \times 2 \text{ A} = 9 \text{ A} + 9 \text{ A} + 8 \text{ A} = 26 \text{ A}$$

$$5 \text{ V: } 9 \text{ A} + (2 + 4) \times 2 \text{ A} = 9 \text{ A} + 12 \text{ A} = 21 \text{ A}$$

$$-12 \text{ V: } (2 + 4) \times 0.25 \text{ A} = 1.5 \text{ A}$$

$$5 \text{ V}_{\text{AUX}}: 1.5 \text{ A}$$

For a 14-slot Chassis with one PXI Express System Timing Slot, two PXI Express Peripheral Slots, six Hybrid Slots, and four PXI-1 Slots, the minimum current for each voltage rail for the entire Chassis would be as follows:

$$+12 \text{ V: } 11 \text{ A} + (3 + 6) \times 2 \text{ A} + 4 \times 0.5 \text{ A} = 11 \text{ A} + 18 \text{ A} + 2 \text{ A} = 31 \text{ A}$$

$$3.3 \text{ V: } 9 \text{ A} + (3 + 6) \times 3 \text{ A} + 4 \times 2 \text{ A} = 9 \text{ A} + 27 \text{ A} + 8 \text{ A} = 44 \text{ A}$$

$$5 \text{ V: } 9 \text{ A} + (6 + 4) \times 2 \text{ A} = 9 \text{ A} + 20 \text{ A} = 29 \text{ A}$$

$$-12 \text{ V: } (6 + 4) \times 0.25 \text{ A} = 2.5 \text{ A}$$

$$5 \text{ V}_{\text{AUX}}: 1.5 \text{ A}$$

OBSERVATION: The minimum power provided by a power supply in a PXI Express Chassis with X PXI Express Peripheral Slots, Y Hybrid Slots, and Z PXI-1 Slots can be determined by the following formula:

$$140 \text{ W} + (X + Y) \times 30 \text{ W} + Z \times 25.6 \text{ W}$$

PERMISSION: PXI Express Chassis MAY provide additional current beyond what is required in Table 4-14.

OBSERVATION: Each generation of processors requires more power than the previous generation. Providing copious amounts of power and cooling to the System Slot of a Chassis can extend the product applicability in the future.

RULE: A PXI Express Chassis SHALL have its DC current output capability documented and available to the end users.

RULE: A PXI Express Chassis backplane and connectors SHALL be capable of transferring the amount of current specified in Table 4-15 to each slot.

4. 电气要求

观察：PXI Express 机箱中电源提供的每个电压轨的最小电流，具有 X PXI Express 外设插槽，Y 混合插槽和 Z PXI-1 外设插槽，可以通过以下公式确定：

$$+12 \text{ 伏: } 11 \text{ A} + (X + Y) \times 2 \text{ A} + Z \times 0.5 \text{ A}$$

$$3.3 \text{ 伏: } 9 \text{ A} + (X + Y) \times 3 \text{ A} + Z \times 2 \text{ A}$$

$$5 \text{ 伏: } 9 \text{ A} + (Y + Z) \times 2 \text{ A}$$

$$-12 \text{ 伏: } (Y + Z) \times 0.25 \text{ A}$$

5 V: 如果 $(X + Y) > 0$, 则为 1.5 A; 否则为 1 A

对于具有一个 PXI Express 系统时序插槽、两个混合插槽和四个 PXI-1 插槽的 8 插槽机箱，整个机箱每个电压轨的最小电流如下：

$$+12 \text{ 伏: } 11 \text{ A} + (1 + 2) \times 2 \text{ A} + 4 \times 0.5 \text{ A} = 11 \text{ A} + 6 \text{ A} + 2 \text{ A} = 19 \text{ A}$$

$$3.3 \text{ 伏: } 9 \text{ A} + (1 + 2) \times 3 \text{ A} + 4 \times 2 \text{ A} = 9 \text{ A} + 9 \text{ A} + 8 \text{ A} = 26 \text{ A}$$

$$5 \text{ 伏: } 9 \text{ A} + (2 + 4) \times 2 \text{ A} = 9 \text{ A} + 12 \text{ A} = 21 \text{ A}$$

$$-12 \text{ 伏: } (2 + 4) \times 0.25 \text{ A} = 1.5 \text{ A}$$

$$5 \text{ V: } 1.5 \text{ A}$$

对于具有 1 个 PXI Express 系统时序插槽、2 个 PXI Express 外设插槽、6 个混合插槽和 4 个 PXI-1 插槽的 14 插槽机箱，整个机箱每个电压轨的最小电流如下：


$$+12 \text{ 伏: } 11 \text{ A} + (3 + 6) \times 2 \text{ A} + 4 \times 0.5 \text{ A} = 11 \text{ A} + 18 \text{ A} + 2 \text{ A} = 31 \text{ A}$$

$$3.3 \text{ 伏: } 9 \text{ A} + (3 + 6) \times 3 \text{ A} + 4 \times 2 \text{ A} = 9 \text{ A} + 27 \text{ A} + 8 \text{ A} = 44 \text{ A}$$

$$5 \text{ 伏: } 9 \text{ A} + (6 + 4) \times 2 \text{ A} = 9 \text{ A} + 20 \text{ A} = 29 \text{ A}$$

$$-12 \text{ 伏: } (6 + 4) \times 0.25 \text{ A} = 2.5 \text{ A}$$

$$5 \text{ V: } 1.5 \text{ A}$$

观察：PXI Express 机箱中具有 X PXI Express 外设插槽、Y 混合插槽和 Z PXI-1 插槽的电源提供的最小功率可以通过以下公式确定：

$$140 \text{ W} + (X + Y) \times 30 \text{ W} + Z \times 25.6 \text{ W}$$

许可：PXI Express 机箱可以提供超出表 4-14 中要求的额外电流。

观察：每一代处理器都需要比上一代更多的功率。为机箱的系统插槽提供大量的电源和冷却可以扩展未来的产品适用性。

规则：PXI Express 机箱应记录其直流电流输出能力并可供最终用户使用。

规则：PXI Express 机箱背板和连接器应能够将表 4-15 中指定的电流量传输到每个插槽。

RULE: The backplane and connectors SHALL be capable of receiving as much return current as they are capable of delivering.

Table 4-15. PXI Express Backplane Continuous Current Capability

	5 V	V(I/O)	3.3 V	+12 V	-12 V	5 V _{AUX}	Notes
PXI Express System Controller Slot	15 A	0 A	15 A	30 A	0 A	1 A	1
PXI Express Peripheral Slot	0 A	0 A	3 A	2 A	0 A	1 A	
Hybrid Slot	6 A	5 A	6 A	2 A	1 A	1 A	
PXI-1 Peripheral Slot	6 A	11 A	6 A	1 A	1 A	0 A	

Notes:

1. Maximum combined current from 12 V, 3.3 V, and 5 V on the PXI Express System Controller Slot is 45 A.

4.11.2.2 Low-Power Chassis Power Supply Specifications

A Chassis designed for portable application or one with a DC power input may be constrained by the battery and operating hours. This may make meeting the minimum power requirements listed in Table 4-14 impractical, but minimum power requirements for this class of Chassis are still important for interoperability with Modules. The minimum power requirements for low-power Chassis are set to allow at least one PXI Express System Module that requires no expansion slots and two PXI Express Peripheral Modules to work in the Chassis, regardless of 3U/6U or the number of slots available.

PERMISSION: A low-power PXI Express Chassis MAY provide less power than is required in Table 4-14.

RULE: A low-power PXI Express Chassis with less power than is required in Table 4-14 SHALL provide at least the minimum output current necessary for a PXI Express System Module that requires no expansion slots and any two Peripheral Slots (PXI Express, Hybrid or PXI-1) that are in the Chassis.

RULE: PXI Express Chassis having less power than is required in Table 4-14 and meeting the power requirement for a low-power PXI Express Chassis SHALL have the text LOW POWER clearly visible with a character height of at least 4 mm on the front of the Chassis, as shown in Figure 4-12. Logo artwork can be obtained from the PXI Systems Alliance.



LOW POWER

Figure 4-12. Text Required for Low-Power Chassis

4.11.3 Module Requirements

The purpose of this section is to provide rules and recommendations for interoperability between the PXI Express System Controller and Peripheral Modules.

规则：背板和连接器应能够接收尽可能多的返回电流。

表 4-15.PXI Express 背板连续电流能力

	5 伏	V (I/O)	3.3 伏	+12 伏	-12 伏	5 伏	笔记
PXI Express 系统控制器插槽	15 安	0 安	15 安	30 安	0 安	1 安	1
PXI Express 外设插槽	0 安	0 安	3 安	2 安	0 安	1 安	
混合老虎机	6 安	5 安	6 安	2 安	1 安	1 安	
PXI-1 外设插槽	6 安	11 安	6 安	1 安	1 安	0 安	

笔记：

1. PXI Express 系统控制器插槽上 12 V、3.3 V 和 5 V 的最大组合电流为 45 A。

4.11.2.2 低功耗机箱电源规格

专为便携式应用设计的机箱或具有直流电源输入的机箱可能会受到电池和工作时间的限制。这可能会使满足表 4-14 中列出的最低功率要求变得不切实际，但此类机箱的最低功率要求对于与模块的互作性仍然很重要。低功耗机箱的最低功率要求设置为允许至少一个不需要扩展插槽的 PXI Express 系统模块和两个 PXI Express 外设模块在机箱中工作，无论 3U/6U 或可用插槽数量如何。



许可：低功耗 PXI Express 机箱提供的功率可以低于表 4-14 中所需的功率。

规则：功率低于表 4-14 中所需功率的低功耗 PXI Express 机箱应至少提供 PXI Express 系统模块所需的最小输出电流，该模块不需要扩展插槽和机箱中的任意两个外设插槽（PXI Express、混合或 PXI-1）。

规则：PXI Express 机箱的功率低于表 4-14 中要求的功率，并且满足低功耗 PXI Express 机箱的功率要求，机箱正面应清晰可见 LOW POWER 文本，字符高度至少为 4 mm，如图 4-12 所示。徽标图稿可从 PXI 系统联盟获得。

LOW POWER

图 4-12.低功耗机箱所需的文本

4.11.3 模块要求

本节的目的是提供 PXI Express 系统控制器和外设模块之间互作性的规则和建议。

4.11.3.1 Maximum Continuous Current Draw

PERMISSION: A PXI Express System Controller or Peripheral Module MAY draw more continuous current than the Chassis is required to provide in Table 4-14.

RULE: A PXI Express System Controller or Peripheral SHALL NOT draw more continuous current from the voltage rails of a slot than the maximum continuous current capabilities specified in Table 4-15.

RULE: A PXI Express System Controller or Peripheral Module SHALL publish its maximum continuous current requirements to the end user.

4.12 Chassis Grounding

Reference the *PXI Hardware Specification* for Chassis grounding requirements.



4.11.3.1 最大连续电流消耗

权限：PXI Express 系统控制器或外围设备模块消耗的连续电流可能比表 4-14 中机箱要求提供的更多。

规则：PXI Express 系统控制器或外围设备不得从插槽的电压轨中汲取超过表 4-15 中规定的最大连续电流能力。

规则：PXI Express 系统控制器或外围设备模块应向最终用户发布其最大连续电流要求。

4.12 机箱接地

请参阅 PXI 硬件规范，了解机箱接地要求。



5. Regulatory Requirements

The following standards assure uniform performance and international portability of PXI systems and Modules. All regulatory compliance information must be clearly documented for the user. Subsequently issued standards or amendments to these standards SHALL apply.

5.1 Requirements for EMC

RULE: Testing SHALL be performed for all PXI Express Modules and Chassis, either by the manufacturer or a competent laboratory, marked accordingly, and documented showing compliance to the following electromagnetic compatibility (EMC) standard(s). The latest released or accepted standard should be used. A competent laboratory should be qualified by a recognized accreditation body for EMC.

IEC 61326-1, *Electrical Equipment for Measurement, Control, and Laboratory Use—EMC Requirements—Part I, General Requirements*:

- Localized EMC standards may be substituted if sale and use are restricted accordingly.
- Use current edition of EN 55011, Group 1, Class A or Class B Limits, at 10 m for radiated emissions testing.

5.2 Requirements for Electrical Safety

RULE: Safety testing SHALL be performed for all PXI Express Modules and Chassis, either by an accredited safety organization¹ and marked accordingly (preferred), or tested by a qualified manufacturer, and documented showing compliance to the following electrical safety standard(s). Strictly safety extra low-voltage (SELV) devices do not need formal agency testing, though the basic requirements still apply, such as material flammability, DC power outputs fused or limited, and so on.

IEC 61010-1, Second Edition (2001), *Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory use—Part 1, General Requirements*:

- IEC 60950 and amendments are acceptable for applications restricted to the office use only.
- Localized safety standards may be substituted if sale and use are restricted accordingly, and laws allow.²
- All relevant safety laws and standards must be met for country(s) of use.



5.3 Additional Requirements for Chassis

RULE: A PXI Express Chassis SHALL be qualified for electrical safety as listed previously. Manufacturer claims of safety compliance are not sufficient without independent certification and regular inspection by a competent safety organization.

RULE: PXI Express Chassis manufacturers, or a designated party, SHALL demonstrate EMC compliance with a commonly available Controller. A reasonably common processor speed is sufficient for this test. The complete Controller system, including hard drive, floppy drive, serial, parallel, keyboard, mouse, and video ports (as offered with the Controller) will be exercised with typical Peripherals. Filling remaining slots, if any, is not required.

¹ Examples of accredited safety organizations are NRTLs in the U.S. and Notified Bodies in Europe.

² The use of localized EMC or safety standards must be clearly documented for the benefit of the user. The standards used may include standards in force during legally allowed transitional periods of new standards or amendments. Currently, manufacturer declarations must list all standards used for declaring compliance and conveniently meet this requirement when the declarations are included with the user documentation.

5. 监管要求

以下标准确保了 PXI 系统和模块的统一性能和国际便携性。所有法规遵从性信息必须为用户清楚地记录。随后发布的标准或这些标准的修订应适用。

5.1 EMC 要求

规则：应由制造商或主管实验室对所有 PXI Express 模块和机箱进行测试，并进行相应标记，并记录显示符合以下电磁兼容性（EMC）标准。应使用最新发布或接受的标准。合格的实验室应获得公认的 EMC 认证机构的资格。

IEC 61326-1，用于测量、控制和实验室使用的电气设备 - EMC 要求 - 第一部分，一般要求：

- 如果销售和使用受到相应限制，则可以替代本地化的 EMC 标准。
- 在 10 m 处使用当前版本的 EN 55011，第 1 组 A 类或 B 类限制进行辐射发射测试。

5.2 电气安全要求

规则：应由经认可的安全组织对所有 PXI Express 模块和机箱进行安全测试并进行相应标记（首选），或由合格的制造商进行测试，并记录显示符合以下电气安全标准。严格安全额外
低压（SELV）设备不需要正式的机构测试，但基本要求仍然适用，例如材料可燃性、直流电源输出熔断或受限等。

IEC 61010-1，第二版（2001），测量、控制和实验室使用电气设备的安全要求 - 第 1 部分，一般要求：

- IEC 60950 和修正案仅适用于仅限于办公室使用的应用。
- 如果销售和使用受到相应限制，并且法律允许，则可以替代本地化的安全标准。
- 必须满足使用国家/地区的所有相关安全法律和标准。

5.3 机箱的附加要求

规则：PXI Express 底盘应符合前面列出的电气安全条件。如果没有独立认证和主管安全组织的定期检查，制造商对安全合规性的声明是不够的。

规则：PXI Express 机箱制造商或指定方应证明 EMC 符合常用控制器的要求。合理通用的处理器速度足以进行此测试。完整的控制器系统，包括硬盘驱动器、软盘驱动器、串行、并行、键盘、鼠标和视频端口（控制器随附）将使用典型的外围设备进行测试。不需要填充剩余插槽（如果有）。

¹ 经认可的安全组织的例子包括美国的 NRTL 和欧洲的公告机构。

² 为了用户的利益，必须清楚地记录本地化 EMC 或安全标准的使用。使用的标准可能包括在法律允许的新标准或修正案过渡期间有效的标准。目前，制造商声明必须列出用于声明合规性的所有标准，并在声明包含在用户文档中时方便地满足此要求。

This Page Intentionally Left Blank



此页面故意留空



6. *PXI Express Software Specification* Compliance

RULE: PXI Express Modules, Chassis, and systems SHALL comply with the rules defined in the PXI-6: *PXI Express Software Specification* maintained by the PXI Systems Alliance.



6. PXI Express 软件规格 合规

规则：PXI Express 模块、机箱和系统应遵守 PXI 系统联盟维护的 PXI-6：PXI Express 软件规范中定义的规则。



This Page Intentionally Left Blank



此页面故意留空

