Table of contents

[1 GENERAL 2](#_Toc116893468)

[2 components information 2](#_Toc116893469)

[2.1 List of obsolete/single source components 2](#_Toc116893470)

[2.2 Where Used 2](#_Toc116893471)

[2.3 List of new identified components 3](#_Toc116893472)

[2.4 Testing Boards 3](#_Toc116893473)

[2.5 General information of identified components 3](#_Toc116893474)

[2.6 Critical parameter comparison 3](#_Toc116893475)

[3 Component validation 7](#_Toc116893476)

[3.1 Board #1 (KM51383820Gxx) 7](#_Toc116893477)

[3.1.1 Visual Check 7](#_Toc116893478)

[3.1.2 Functional Test 8](#_Toc116893479)

[3.1.3 Simulator / Test tower testing 11](#_Toc116893480)

[3.1.4 Reliability testing includes HALT, EMI/EMC, Climatic 11](#_Toc116893481)

[3.1.5 ICT/Flying Probe 11](#_Toc116893482)

[3.1.6 FCT 11](#_Toc116893483)

[3.1.7 Piloting 11](#_Toc116893484)

[3.1.8 Validation Test Summary 11](#_Toc116893485)

[4 Conclusion 12](#_Toc116893486)

[5 USED Instruments 12](#_Toc116893487)

[5.1 Periodically calibrated 12](#_Toc116893488)

[6 approvals and Version history 12](#_Toc116893489)

# GENERAL

This document contains the component validation report for the alternate/second source found for the FET, N-CH KM51414051 tested in, PCB, BRAKE CONTROL BOARD ESC PCBA.

# components information

Component KM number: KM51414051

Description of component: FET, N-CH-400V-1R-5.5A-TO220

## List of obsolete/single source components

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **#** | **Manufacturer** | **Part number** | **Obsolete/Single source/Lead time/Cost** | **Cost Information** | **Est. Life time Info.** | **Datasheet link** |
| 1 | VISHAY | IRF730APBF | Active | - | 6.4 Years |  |

## Where Used

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **#** | **Board KM** | **Description of board** | **Person in charge** | **Test needed YES/NO** | **Comments** |
| 1 | KM51383820Gxx | PCB, BRAKE CONTROL BOARD ESC | Sekar Rajkumar (keisraj) | Yes | - |

## List of new identified components

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **#** | **Manufacturer** | **Part number** | **Cost Information** | **Est. Life time Info.** | **Datasheet link** |
| 1 | ST microelectronics | STP6N62K3 | - | 8.1 Years |  |
| 2 | Silan microelectronics | SVF740T | - | - |  |

## Testing Boards

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **#** | **Board KM** | **Description of board** | **Testing Responsibility** | **Comments** |
| 1 | KM51383820Gxx | PCB, BRAKE CONTROL BOARD ESC | - | - |

## General information of identified components

## Critical parameter comparison

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | Unit | Existing | New | New |
|  | MPN |  | IRF730APBF | STP6N62K3 | SVF740T |
|  | Manufacturer |  | Vishay | STMicroelectronics | Silan Microelectronics |
|  | Cost |  | $1.71 | $2.04 | - |
|  | Lead Time |  | 63 Weeks | 52 Weeks | - |
|  | Country of Origin |  | China,Israel,Mexico,Taiwan | China,Italy,Morocco,Philippines,Singapore | China |
|  | Life Cycle |  | Active | Active | Active |
|  | ROHS |  | Yes | Yes | Yes |
|  | Description |  | Trans MOSFET N-CH 400V 5.5A 3-Pin(3+Tab) TO-220AB | Trans MOSFET N-CH 620V 5.5A 3-Pin(3+Tab) TO-220AB Tube | 10A,400V N-channel enhancement mode FET |
|  | Channel Mode |  | Enhancement | Enhancement | Enhancement |
|  | Channel Type |  | N-Channel | N-Channel | N-Channel |
|  | Drain-source voltage, VDS | V | 400 | 620 | 400 |
|  | Gate-source voltage,VGS | V | ± 30 | ± 30 | ± 30 |
|  | Continuous drain current,ID | A | 5.5 at TC = 25 °C,VGS at 10 V | 5.5 at TC = 25 °C | 10 A |
|  | Pulsed drain current,IDM | A | 22 | 22 | 40 A |
|  | Linear derating factor | W/°C | 0.6 | - | - |
|  | Single pulse avalanche energy , EAS | mJ | 290 | 140 | 517mJ |
|  | Repetitive avalanche current , IAR | A | 5.5 | 5.5 | - |
|  | Repetitive avalanche energy, EAR | mJ | 7.4 | - | - |
|  | Maximum power dissipation,PD | W | 74 at TC = 25 °C | 90 at TC = 25 °C | 130 at TC = 25 °C |
|  | Peak diode recovery, dV/dt | V/ns | 4.6 | 12 | - |
|  | Operating junction temperature range,TJ | °C | -55 to +150 | -55 to +150 | -55 to +150 |
| Static | Drain-source breakdown voltage ,VDS | V | 400(min) at VGS = 0 V, ID = 250 μA | 620(min) at ID = 1 mA, VGS = 0 | 400 at VGS=0V，ID=250µA |
| VDS temperature coefficient, ΔVDS/TJ | V/°C | 0.5(typ) at Reference to 25 °C, ID = 1 mA | - | - |
| Gate-source threshold voltage, VGS(th) | V | 2.0(min),4.5(max) at VDS = VGS, ID = 250 μA | 3(min),3.75(typ),4.5(max) | 2.0(min),4.0(max) at VGS= VDS，ID=250µA |
| Gate-source leakage,IGSS | nA | ± 100(max) at VGS = ± 30 V | ± 9 µA at VGS = ± 20 V | ± 100(max) at VGS = ± 30 V,VDS=0V |
| Zero gate voltage drain current, IDSS | μA | 25(max) at VDS = 400 V, VGS = 0 V | 0.8 µA at VGS = 0,VDS = 620 V | 1.0(max) at VDS=400V，VGS=0V |
| Drain-source on-state resistance, RDS(on) | Ω | 1.0(max) at VGS = 10 V, ID = 3.3 A | 0.95(typ),1.2(max) at VGS = 10 V, ID = 2.8 A | 0.45(typ),0.60(max) at VGS=10V，ID=5.0A |
| Forward transconductance ,gfs | S | 3.1 at VDS = 50 V, ID = 3.3 A | - | - |
| Dynamic | Input capacitance,Ciss | pF | 600(typ) at VGS = 0 V, VDS = 25 V, f = 1.0 MHz | 875(typ) at VDS = 50 V, f = 1 MHz, VGS = 0 | 801(typ) at VDS=25V，VGS=0V，f=1.0MHz |
| Output capacitance ,Coss | pF | 103(typ) at VGS = 0 V, VDS = 25 V, f = 1.0 MHz | 100(typ) at VDS = 50 V, f = 1 MHz, VGS = 0 | 118.5(typ) at VDS=25V，VGS=0V，f=1.0MHz |
| Reverse transfer capacitance, Crss | pF | 4.0(typ) at VGS = 0 V, VDS = 25 V, f = 1.0 MHz | 17(typ) at VDS = 50 V, f = 1 MHz, VGS = 0 | 5.06(typ) at VDS=25V，VGS=0V，f=1.0MHz |
| Output capacitance ,Coss | pF | 890(typ) at VDS = 1.0 V, f = 1.0 MHz,VGS = 0 V | - | - |
| Effective output capacitance, Coss eff. | pF | 45(typ) at VGS = 0 V, VDS = 0 V to 320 V | - | - |
| Total gate charge,Qg | nC | 22(max) at VGS = 10 V,ID = 3.5 A, VDS = 320 V | 34(typ) at VDD = 496 V, ID = 5.5 A, VGS = 10 V | 16.18(typ) at VDD=320V，ID=10A， VGS=10V |
| Gate-source charge, Qgs | nC | 5.8(max) at VGS = 10 V,ID = 3.5 A, VDS = 320 V | 4(typ) at VDD = 496 V, ID = 5.5 A, VGS = 10 V | 4.77(typ) at VDD=320V，ID=10A， VGS=10V |
| Gate-drain charge, Qgd | nC | 9.3(max) at VGS = 10 V,ID = 3.5 A, VDS = 320 V | 22(typ) at VDD = 496 V, ID = 5.5 A, VGS = 10 V | 7.18(typ) at VDD=320V，ID=10A， VGS=10V |
| Turn-on delay time,td(on) | ns | 10(typ) at VDD = 200 V, ID = 3.5 A  Rg = 12 Ω, RD = 57 Ω | 22(typ) VDD = 310 V, ID = 2.75 A,  RG = 4.7 Ω, VGS = 10 V | 15.44(typ) at VDD=200V，RG=25Ω，ID =10A |
| Rise time,tr | ns | 22(typ) at VDD = 200 V, ID = 3.5 A  Rg = 12 Ω, RD = 57 Ω | 12(typ) at VDD = 310 V, ID = 2.75 A,  RG = 4.7 Ω, VGS = 10 V | 38.60(typ) at VDD=200V，RG=25Ω，ID =10A |
| Turn-off delay time,td(off) | ns | 20(typ) at VDD = 200 V, ID = 3.5 A  Rg = 12 Ω, RD = 57 Ω | 49(typ) at VDD = 310 V, ID = 2.75 A,  RG = 4.7 Ω, VGS = 10 V | 35.12(typ) at VDD=200V，RG=25Ω，ID =10A |
| Fall time, tf | ns | 16(typ) at VDD = 200 V, ID = 3.5 A  Rg = 12 Ω, RD = 57 Ω | 20(typ) at VDD = 310 V, ID = 2.75 A,  RG = 4.7 Ω, VGS = 10 V | 28.16(typ) at VDD=200V，RG=25Ω，ID =10A |
| Gate input resistance,Rg | Ω | 2.7(min),10.9(max) at f = 1 MHz, open drain | 3.5(typ) at f = 1 MHz open drain |  |
| Drain-Source Body Diode Characteristics | Continuous source-drain diode current, IS | A | 5.5(max) | 5.5(max) | 10(max) |
| Pulsed diode forward current,ISM | A | 22(max) | 27(max) | 40(max) |
| Body diode voltage,VSD | V | 1.6(max) at TJ = 25 °C, IS = 5.5 A, VGS = 0 V | 1.5(max) at ISD = 5.5 A, VGS = 0 | 1.4(max) at IS=10A，VGS=0V |
| Body diode reverse recovery time, trr | ns | 370(typ),550(max) at TJ = 25 °C, IF = 3.5 A, dI/dt = 100 A/μs | 290(typ) at ISD = 5.5 A, di/dt = 100 A/µs VDD = 60 V | 255.6(typ) at IS=10A，VGS=0V，dIF/dt=100A/µs |
| Body diode reverse recovery charge ,Qrr | μC | 1.6(typ),2.4(max) at TJ = 25 °C, IF = 3.5 A, dI/dt = 100 A/μs | 1.9(typ) at ISD = 5.5 A, di/dt = 100 A/µs VDD = 60 V | 2.15(typ) at IS=10A，VGS=0V，dIF/dt=100A/µs |
|  | Schematic Pin Matching Status |  | Matching with others | Matching with others | Matching with others |
|  | Schematic Symbol |  |  |  |  |
|  | Package Type |  | TO-220 | TO-220 | TO-220 |
|  | Package Match Status |  | Matching with others | Matching with others | Matching with others |
|  | Package Length | mm | 9.96(min),10.52(max) | 10(min),10.40(max) | 9.60(min),9.90(nom),10.40(max) |
|  | Package Width | mm | 4.24(min),4.65(max) | 4.40(min),4.60(max) | 4.30(min),4.50(nom),4.70(max) |
|  | Package Height | mm | 14.33(min),15.85(max) | 15.25(min),15.75(max) | 15.10(min),15.70(nom),16.10(max) |
|  | Pin Length | mm | 13.36(min),14.40(max) | 13(min),14(max) | 12.60(min),13.08(nom),13.60(max) |
|  | Pin Pitch | mm | 2.41(min),2.92(max) | 2.40(min),2.70(max) | 2.54 |
|  | Package |  |  |  |  |

# Component validation

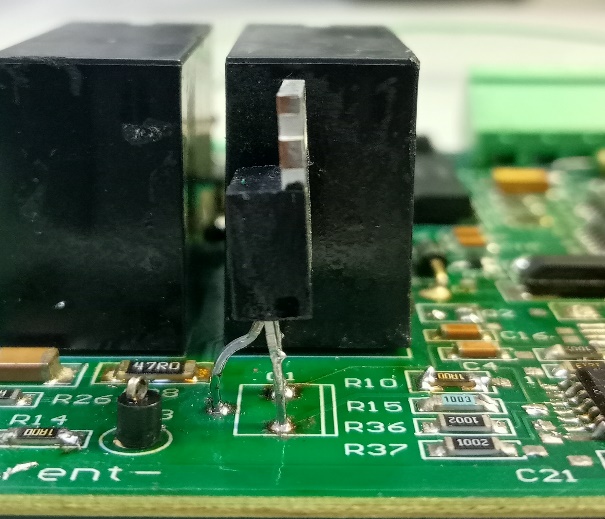
## Board #1 (KM51383820Gxx)

### Visual Check

**Alternate#1 STP6N62K3 @ ST Micro Alternate#2 SVF740T @ Silan**

* Fitment photo

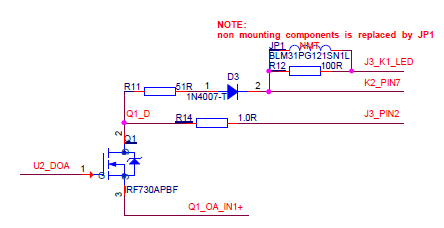
**Alternate#1 STP6N62K3 @ ST Micro Alternate#2 SVF740T @ Silan**

### Functional Test

##### **Description of testing**

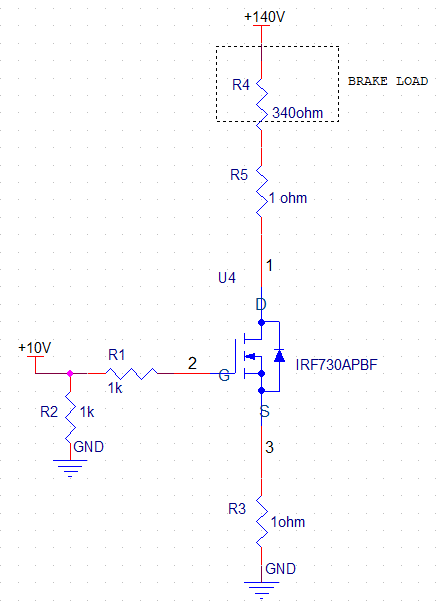
The purpose of the document is to verify operation of planned second source of n-channel MoSFET which is used in PCB, BRAKE CONTROL BOARD ESC (51383820D02), with following components STP6N62K3 @ST microelectronics and SVF740T @Silan microelectronics are tested at Q1 position in PCB, BRAKE CONTROL BOARD ESC.

##### **Circuit Diagram**



##### **Test Plan**

The below circuit built manually to test the MoSFET Q1 for alternate validation purpose.



| **S.No** | **Action** | **Expected** | **Result** | **Conclusion** |
| --- | --- | --- | --- | --- |
| 1 | Connect the +140V DC power supply across R4 pin1 and GND |  |  | PASS /FAIL |
| 2 | Connect the Function generator in Q1.1 with pulse of  Frequency 20Hz, Amplitude 5Vpp, offset +2.5V, pulse width 21ms. |  |  |  |
| 3 | Connect the Resistive load of 340 ohm in series with +140V |  |  |  |
| 4 | MoSFET Q1 is active.   * Measure Gate threshold Voltage * Measure Drain to source voltage * Measure turn on delay time. * Measure turn off delay time. * Measure drain current. |  |  | PASS /FAIL |
| 5 | Temperature test:  Connect the Gate to 10V and measure the temperature after 20min of continuous run | Temperature after 20min.=  Delta temp = <20 °C |  | PASS /FAIL |

##### **Existing (IRF730APBF) component measurement**

| **S.No** | **Action** | **Expected** | **Result** | **Conclusion** |
| --- | --- | --- | --- | --- |
| 1 | Connect the +140V DC power supply across R4 pin1 and GND |  |  | PASS |
| 2 | Connect the Function generator in Q1.1 with pulse of  Frequency 20Hz, Amplitude 5Vpp, offset +2.5V, pulse width 21ms. |  |  | PASS |
| 3 | Connect the Resistive load of 340 ohm in series with +140V |  |  | PASS |
| 4 | MoSFET Q1 is active.   * Measure Gate threshold Voltage * Measure Drain to source voltage. * Measure drain current. * Measure turn on delay time. * Measure turn off delay time. |  | VGS (th) = 3.8 V  VDS = 138.3 V  IDS = 405 mA  Turn ON delay time = 1.871 µs  Turn OFF delay time = 1.5889 µs | PASS |
| 5 | Temperature test:  Connect the Gate to 10V and measure the temperature after 20min of continuous run | Temperature after 20min.=  Delta temp = <20 °C | Tamb = 24.8°C  Temperature after 20min.= 38.2°C  Delta temp = 13.4 °C | PASS |



**Existing (IRF730APBF) Gate threshold voltage**



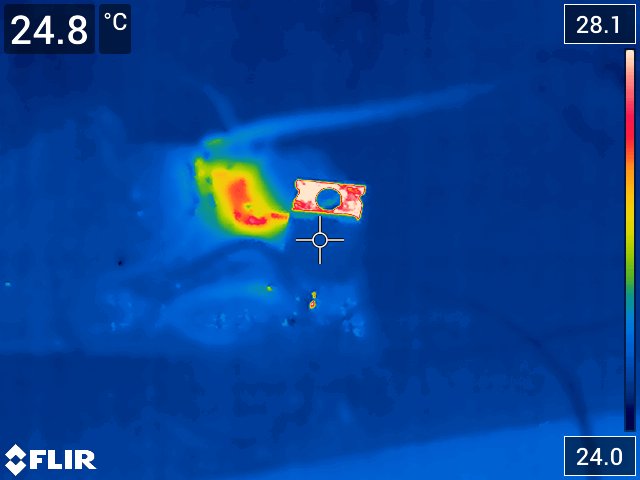
**Existing (IRF730APBF) During Gate ON/OFF**



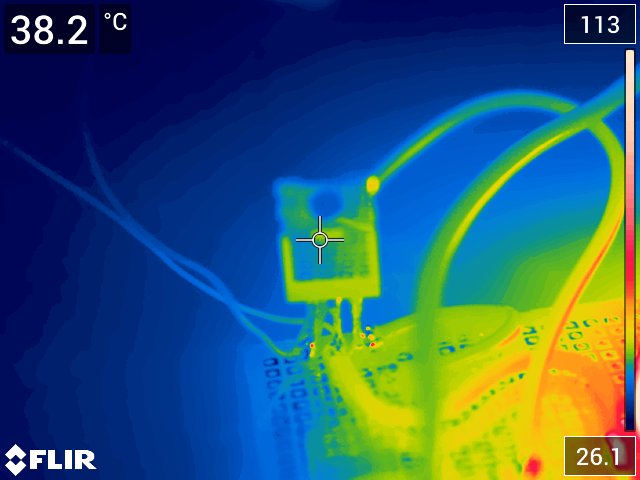
**Existing (IRF730APBF)**  **Drain delay time when Gate is ON**



**Existing (IRF730APBF)**  **Drain delay time when Gate is OFF**



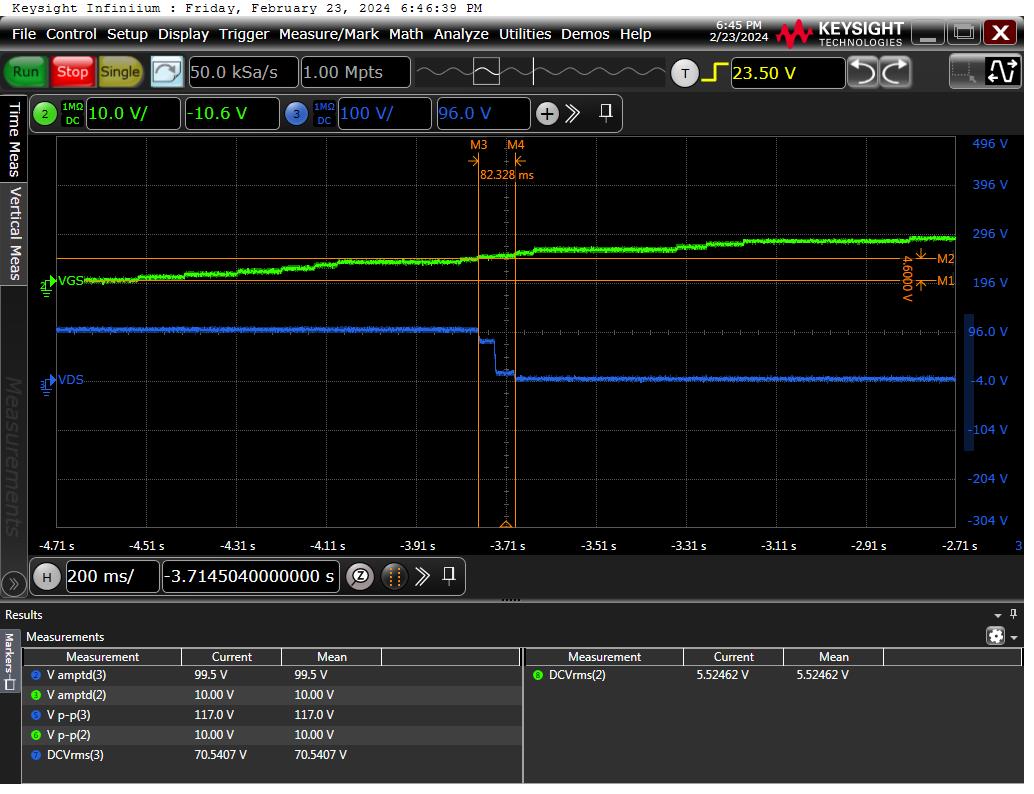
**Existing (IRF730APBF) Ambient temperature**

****

**Existing (IRF730APBF) temperature after 20min of continuous run**

##### **Alternate#1 (STP6N62K3) component measurement**

| **S.No** | **Action** | **Expected** | **Result** | **Conclusion** |
| --- | --- | --- | --- | --- |
| 1 | Connect the +140V DC power supply across R4 pin1 and GND |  |  | PASS |
| 2 | Connect the Function generator in Q1.1 with pulse of  Frequency 20Hz, Amplitude 5Vpp, offset +2.5V, pulse width 21ms. |  |  | PASS |
| 3 | Connect the Resistive load of 340 ohm in series with +140V |  |  | PASS |
| 4 | MoSFET Q1 is active.   * Measure Gate threshold Voltage * Measure Drain to source voltage. * Measure drain current. * Measure turn on delay time. * Measure turn off delay time. |  | VGS (th) = 4.6 V  VDS = 136.6 V  IDS = 396 mA  Turn ON delay time = 3.1136 µs  Turn OFF delay time = 3.444 µs | PASS |
| 5 | Temperature test:  Connect the Gate to 10V and measure the temperature after 20min of continuous run | Temperature after 20min.=  Delta temp = <20 °C | Tamb = 28.2°C  Temperature after 20min.= 47°C  Delta temp = 18.8 °C | PASS |



**Alternate#1 (STP6N62K3) Gate threshold voltage**

****

**Alternate#1 (STP6N62K3) During Gate ON/OFF**

****

**Alternate#1 (STP6N62K3)** **Drain delay time when Gate is ON**

**A computer screen shot of a graph

Description automatically generated**

**Alternate#1 (STP6N62K3)** **Drain delay time when Gate is OFF**

****

**Alternate#1 (STP6N62K3)** **Ambient temperature**

**A screenshot of a computer

Description automatically generated**

**Alternate#1 (STP6N62K3) Temperature after 20min of continuous run**

##### **Alternate#2 (SVF740T) component measurement**

| **S.No** | **Action** | **Expected** | **Result** | **Conclusion** |
| --- | --- | --- | --- | --- |
| 1 | Connect the +140V DC power supply across R4 pin1 and GND |  |  | PASS |
| 2 | Connect the Function generator in Q1.1 with pulse of  Frequency 20Hz, Amplitude 5Vpp, offset +2.5V, pulse width 21ms. |  |  | PASS |
| 3 | Connect the Resistive load of 340 ohm in series with +140V |  |  | PASS |
| 4 | MoSFET Q1 is active.   * Measure Gate threshold Voltage * Measure Drain to source voltage. * Measure drain current. * Measure turn on delay time. * Measure turn off delay time. |  | VGS (th) = 3.4 V  VDS = 136.6 V  IDS = 396 mA  Turn ON delay time = 866.67 ns  Turn OFF delay time = 1.911 µs | PASS |
| 5 | Temperature test:  Connect the Gate to 10V and measure the temperature after 20min of continuous run | Temperature after 20min.=  Delta temp = <20 °C | Tamb = 28°C  Temperature after 20min.= 40.7°C  Delta temp = 12.7 °C | PASS |



**Alternate#2 (SVF740T) Gate threshold voltage**

**A screenshot of a computer

Description automatically generated**

**Alternate#2 (SVF740T) During Gate ON/OFF**

****

**Alternate#2 (SVF740T) Drain delay time when Gate is ON**

A screenshot of a computer

Description automatically generated

**Alternate#2 (SVF740T) Drain delay time when Gate is OFF**

A computer screen with a colorful image

Description automatically generated with medium confidence

**Alternate#2 (SVF740T) Ambient temperature**

**A close-up of a computer

Description automatically generated**

**Alternate#2 (SVF740T) Temperature after 20 mins of continuous run**

### Simulator / Test tower testing

### Reliability testing includes HALT, EMI/EMC, Climatic

### ICT/Flying Probe

### FCT

### Piloting

### Test result comparison table

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameters** | **Existing** | **STP6N62K3** | **SVF740T** |
| Drain – source voltage | 138.3V | 136.6 V | 136.6 |
| Drain current | 405mA | 396mA | 396mA |
| Turn ON delay time | 1.8711 µs | 3.1136 µs | 866.67ns |
| Turn OFF delay time | 1.5889 µs | 3.444 µs | 1.9111 µs |
| Gate-source threshold voltage | 3.8 V | 4.6 V | 3.4 V |

### Validation Test Summary

|  |  |  |
| --- | --- | --- |
| Test Type | Result (PASS/FAIL) | Comments |
| Visual Check | PASS |  |
| Functional Test | PASS |  |
| Simulator Test | NA |  |
| Reliability test | NA |  |
| ICT/Flying Probe | NA |  |
| FCT | NA |  |
| Piloting | NA |  |
| **Summary** | **PASS** |  |

# Conclusion

Based on the above fitment test and functional test STP6N62K3 @ STMicro and SVF740T @ Silan can be added as alternate for KM51414051

|  |  |  |  |
| --- | --- | --- | --- |
| **#** | **Board name with KM** | **Test Result**  **(**PASS/FAIL) | **Comments** |
| 1 | KM51383820Gxx(PCB, BRAKE CONTROL BOARD ESC) | **PASS** |  |

# USED Instruments

## Periodically calibrated

|  |  |  |
| --- | --- | --- |
| Instrument | Serial number | Calibration due date |
| Mixed Signal Oscilloscope | MY55510160 | 14/11/2024 |

# approvals and Version history

Compiled by: Hariharan Raja

Checked by: Uvaraj / Suresh Kumar T

Approved by Matti Naapuri

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Issue** | **Date** | **Description of Change** | **Ref CR** | **Approved By** |
| **-** | 2024-02-26 | New Alternate test report added |  | Matti Naapuri |
|  |  |  |  |  |
|  |  |  |  |  |