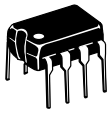
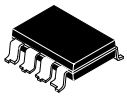
1000 V SenseFET Integrated Power Switch

FSL4110LR



PDIP−7 (PDIP−8 LESS PIN 6)
(7−DIP)
CASE 626A



PDIP7 MINUS PIN 6 GW
(7−LSOP)
CASE 707AA

Description

The FSL4110LR is an integrated pulse width modulation (PWM) controller and 1000 V avalanche rugged SenseFET specifically designed for high input voltage offline Switching Mode Power Supplies (SMPS) with minimal external components. V_{CC} can be supplied through integrated high−voltage power regulator without auxiliary bias winding.

The integrated PWM controller includes a fixed−frequency oscillator, Under−Voltage Lockout (UVLO), Leading−Edge Blanking (LEB), optimized gate driver, soft−start, temperature−compensated precise current sources for loop−compensation, and variable protection circuitry.

Compared with a discrete MOSFET and PWM controller solution, the FSL4110LR reduces total cost, component count, PCB size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost−effective design of a flyback converter.

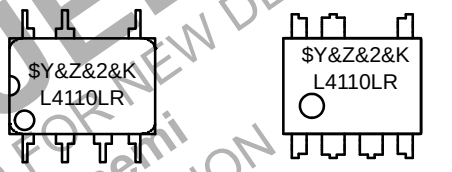
Features

- Built−in Avalanche Rugged 1000 V SenseFET
- Precise Fixed Operating Frequency: 50 kHz
- V_{CC} can be Supplied from either Bias−winding or Self−biasing
- Soft Burst−Mode Operation Minimizing Audible Noise
- Random Frequency Fluctuation for Low EMI
- Pulse−by−Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over−Voltage Protection (OVP), Abnormal Over−Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis. Under−Voltage Lockout (UVLO) and Line Over−Voltage Protection (LOVP) with Hysteresis.
- Built−in Internal Startup and Soft−Start Circuit
- Fixed 1.6 s Restart Time for Safe Auto−Restart Mode of All Protections
- These are Pb−Free Devices

Applications

- SMPS for Electric Metering
- Auxiliary Power Supply for 3−Phase Input Industrial Systems

MARKING DIAGRAM



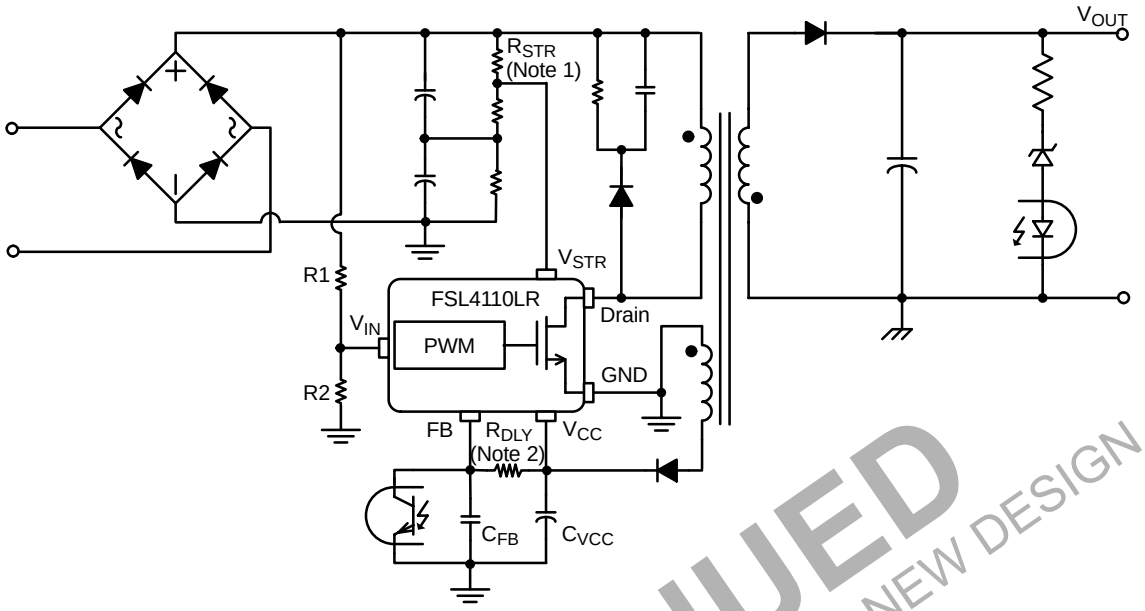
FSL4110LRN FSL4110LRLX

$Y	= Logo
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code
L4110LR	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

TYPICAL APPLICATION CIRCUIT



NOTES:
1. R_{STR}: See the functional description Startup and High−Voltage Regulator.
2. R_{DLY}: See the functional description Overload Protection (OLP).

Figure 1. Typical Application Circuit

INTERNAL BLOCK DIAGRAM

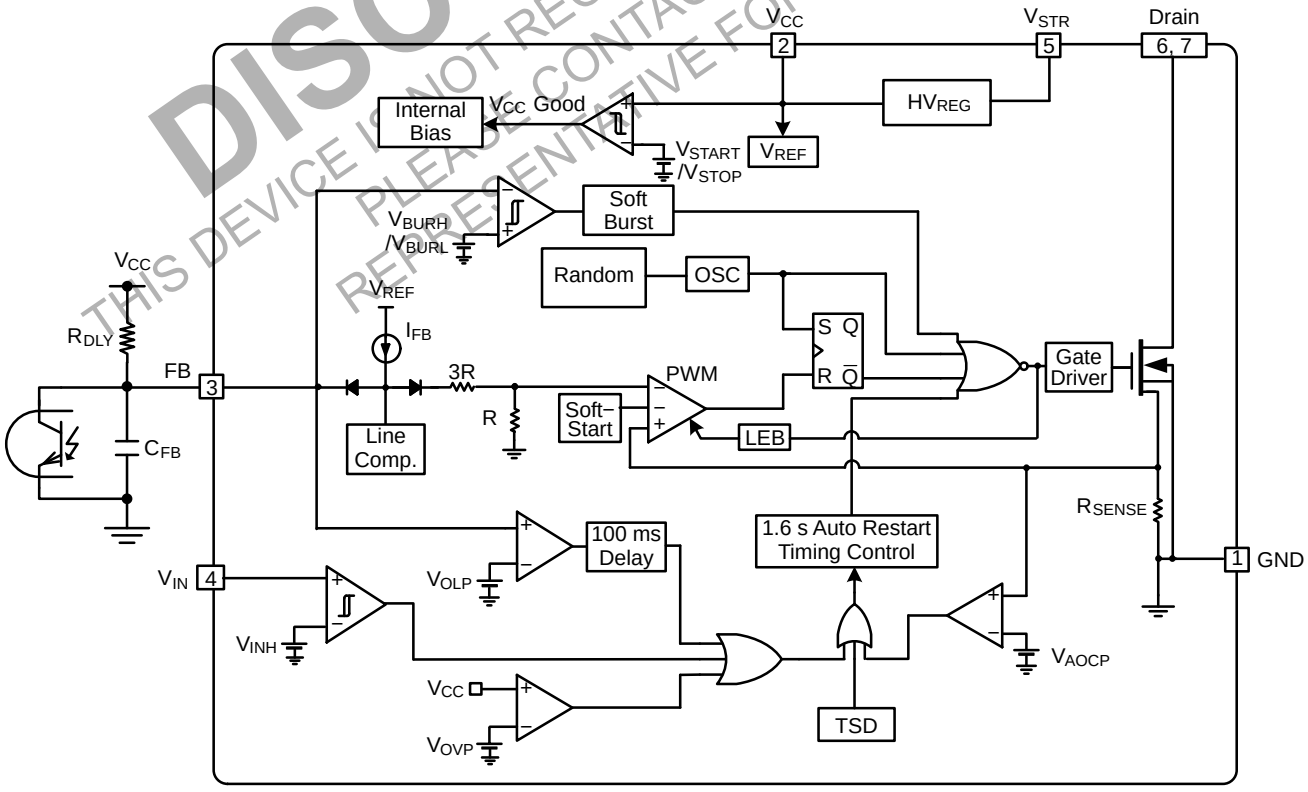


Figure 2. Internal Block Diagram

PIN CONFIGURATION

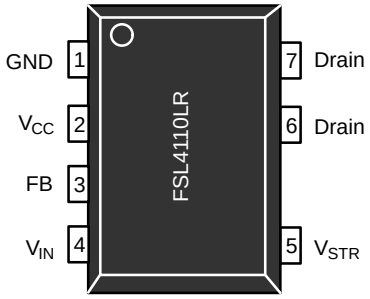


Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

Pin #	Name	Description
1	GND	Ground. The SenseFET source terminal on primary side and the internal PWM control ground.
2	V_{CC}	Power Supply Voltage Input. This pin is the positive supply input, which provides the internal operating current for startup and steady−state operation. This voltage is supplied from internal high−voltage regulator via pin 5 (V_{STR}) during startup (*see Figure 2*). When the external bias voltage is higher than 10 V, internal high voltage regulator is disable. A ceramic capacitor need to be placed as close as possible between this pin and pin 1 (GND). Recommended distance is less than 3 mm.
3	FB	Feedback. This pin is internally connected to the inverting input to the PWM comparator. This pin has a 100 μA current source internally. The collector of an opto−coupler is typically tied to this pin. A capacitor should be placed between this pin and GND. A resitor should be connected between this pin and pin 2 (V_{CC}) to generate delay current (I_{DELAY}) for overload protection delay time. The resistance should not be exceed 5 MΩ in self−biasing.
4	V_{IN}	Line Over−Voltage Input. This pin is the input of divided line voltage. The voltage is devided by resistors. When this voltage is higher than 2 V, the FSL4110LR is not operationed. If this pin is not used, it should be connected to the ground.
5	V_{STR}	Startup. Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between V_{CC} pin and ground. Once V_{CC} reaches 12 V, all internal blocks are activated. The internal high−voltage regulator turns on and off to maintain V_{CC} at 10 V without auxiliary bias winding.
6, 7	Drain	Drain. Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 1000 V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{STR}	V_{STR} Pin Voltage		−	700	V
V_{DS}	Drain Pin Voltage		−	1000	V
V_{CC}	V_{CC} Pin Voltage		−	27	V
V_{FB}	Feedback Pin Voltage (Note 3)		−0.3	12.0	V
V_{IN}	V_{IN} Pin Voltage (Note 3)		−0.3	12.0	V
I_{DM}	Drain Current Pulsed		−	4	A
I_{DS}	Continuous Switching Drain Current (Note 4)	T_C = 25°C	−	1	A
		T_C = 100°C	−	0.6	A
E_{AS}	Single Pulsed Avalanche Energy (Note 5)		−	51	mJ
P_D	Total Power Dissipation (T_C = 25°C) (Note 6)		−	1.5	W
T_J	Maximum Junction Temperature		−	150	°C
	Operating Junction Temperature (Note 7)		−40	+125	°C
TSTG	Storage Temperature		−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. V_{FB} and V_{IN} are clamped by internal clamping diode (11 V, I_{CLAMP_MAX} < 100 μA).
4. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX} = 0.73) and junction temperature *(see Figure 4)*.
5. I_{AS} = 3.2 A, L = 10 mH, starting T_J = 25°C.
6. Infinite cooling condition *(refer to the SEMI G30−88)*.
7. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

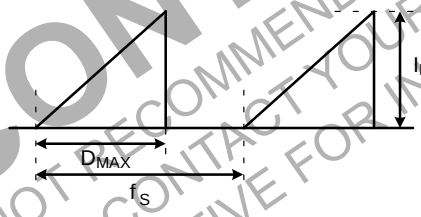


Figure 4. Repetitive Peak Switching Current

THERMAL IMPEDANCE

Symbol	Parameter	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Impedance (Note 8)	85	°C/W

8. JEDEC recommended environment, JESD51−2, and test board, JESD51−3, with minimum land pattern.

ESD CAPABILITY

Symbol	Parameter	Value	Unit
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	5.0	KV
	Charged Device Model, JESD22−C101	2.0	

ELECTRICAL CHARACTERISTICS (T_J = −40°C to 125°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SenseFET SECTION						
BV_{DSS}	Drain−Source Breakdown Voltage (Note 9)	V_{GS} = 0 V, I_D = 250 μA	1000	−	−	V
I_{DSS}	Zero−Gate−Voltage Drain Current (Note 9)	V_{DS} = 1000 V, V_{GS} = 0 V	−	−	250	μA
$R_{DS(ON)}$	Drain−Source On−State Resistance (Note 9)	V_{GS} = 10 V, I_D = 1.0 A	−	−	10	Ω
C_{ISS}	Input Capacitance (Note 9) (Note 10)	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	−	367	477	pF
C_{OSS}	Output Capacitance (Note 9) (Note 10)		−	37.5	48.8	pF
$t_{d(on)}$	Turn−On Delay Time (Note 9)	V_{DD} = 500 V, I_D = 1.0 A, V_{GS} = 10 V, R_g = 25 Ω	−	13.7	−	ns
t_r	Rise Time (Note 9)		−	14	−	ns
$t_{d(off)}$	Turn−Off Delay Time (Note 9)		−	33	−	ns
t_f	Fall Time (Note 9)		−	45	−	ns
CONTROL SECTION						
f_S	Switching Frequency (Note 9)	V_{CC} = 14 V, V_{FB} = 4 V	46.5	50.0	53.5	kHz
f_M	Frequency Modulation (Note 10)		−	±1.5	−	kHz
D_{MAX}	Maximum Duty Ratio	V_{CC} = 14 V, V_{FB} = 4 V	61	67	73	%
I_{FB}	Feedback Source Current (Note 9)	V_{FB} = 0 V	70	100	130	μA
V_{START}	UVLO Threshold Voltage	V_{FB} = 0 V, V_{CC} Sweep	11	12	13	V
V_{STOP}		After Turn−on, V_{FB} = 0 V	7	8	9	
$t_{S/S}$	Internal Soft−Start Time	V_{STR} = 40 V, V_{CC} Sweep	−	20	−	ms
BURST−MODE SECTION						
V_{BURH}	Burst−Mode Voltage (Note 9)	V_{CC} = 14 V, V_{FB} Sweep	0.45	0.50	0.55	V
V_{BURL}			0.35	0.40	0.45	V
V_{HYS}			−	100	−	mV
PROTECTION SECTION						
I_{LIM}	Peak Drain Current Limit (Note 9)	di/dt = 240 mA/μs	0.45	0.52	0.59	A
V_{OLP}	Overload Protection (Note 9)	V_{CC} = 14 V, V_{FB} Sweep	4.0	4.4	4.8	V
V_{AOCP}	Abnormal Over−Current Protection (Note 10)		−	1.0	−	V
t_{LEB}	Leading−Edge Blanking Time (Note 10) (Note 11)		−	250	−	ns
t_{CLD}	Current Limit Delay Time (Note 10)		−	−	200	ns
V_{OVP}	Over−Voltage Protection	V_{CC} Sweep	23.0	24.5	26.0	V
V_{INH}	Line Over−Voltage Protection Threshold Voltage	V_{CC} = 14 V, V_{IN} Sweep	1.9	2.0	2.1	V
V_{INHYS}	Line Over−Voltage Protection Hysteresis (Note 9)	V_{CC} = 14 V, V_{IN} Sweep	−	100	−	mV
t_{DELAY}	Overload Protection Delay		−	100	−	ms
$t_{RESTART}$	Restart Time After Protection (Note 10)		−	1.6	−	s
TSD	Thermal Shutdown Temperature (Note 10)	Shutdown Temperature	130	140	150	°C
T_{HYS}		Hysteresis (FSL4110LRN)	−	60	−	
T_{HYS}		Hysteresis (FSL4110LRLX)	−	30	−	
HIGH VOLTAGE REGULATOR SECTION						
V_{HVREG}	HV Regulator Voltage	V_{FB} = 0 V, V_{STR} = 40 V	9	10	11	V

ELECTRICAL CHARACTERISTICS (T_J = −40°C to 125°C unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TOTAL DEVICE SECTION						
I_{OP}	Operating Supply Current, (Control Part in Burst Mode) (Note 9)	V_{CC} = 14 V, V_{FB} = 0 V	−	0.40	0.50	mA
I_{OPS}	Operating Switching Current, (Control Part and SenseFET Part) (Note 9)	V_{CC} = 14 V, V_{FB} = 2 V	−	1.00	1.35	mA
I_{START}	Start Current (Note 9)	V_{CC} = 11 V (Before V_{CC} Reaches V_{START})	−	160	240	μA
I_{CH}	Startup Charging Current (Note 9)	V_{CC} = V_{FB} = 0 V, V_{STR} = 40 V	1.5	2.0	−	mA
V_{STR}	Minimum V_{STR} Supply Voltage	C_{VCC} = 0.1 μF, V_{STR} Sweep	−	−	26	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. T_J = 25°C.
10. Although these parameters are guaranteed, they are not 100% tested in production.
11. t_{LEB} includes gate turn−on time.

TYPICAL PERFORMANCE CHARACTERISTICS

(Characteristic graphs are normalized at T_A = 25°C.)

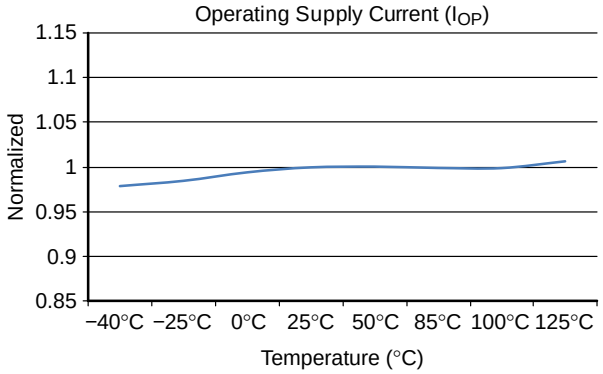


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

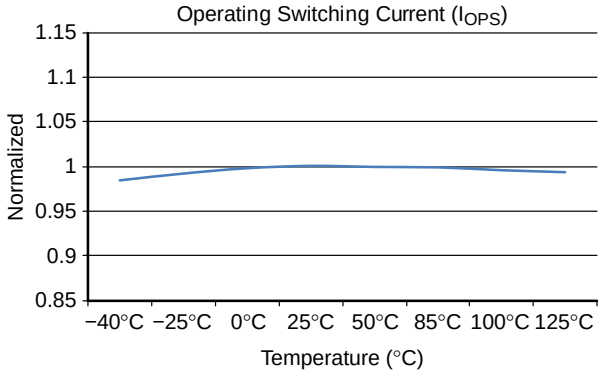


Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

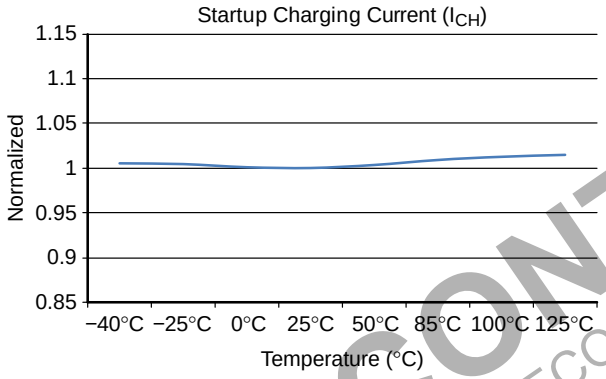


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

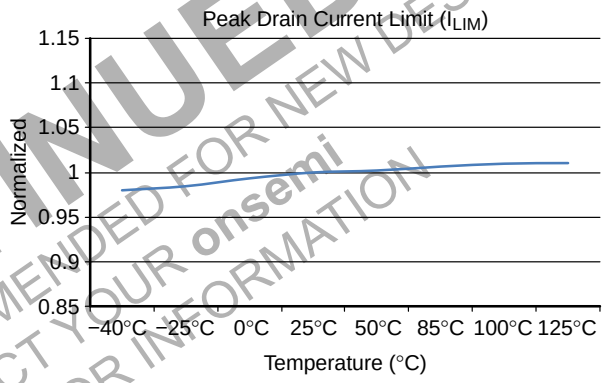


Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

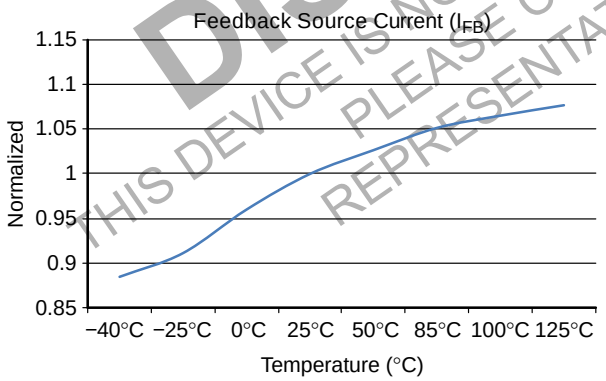


Figure 9. Feedback Source Current (I_{FB}) vs. T_A

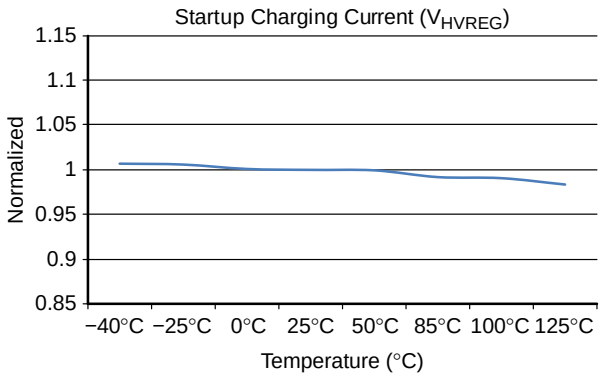


Figure 10. HV Regulator Voltage (V_{HVREG}) vs. T_A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(Characteristic graphs are normalized at T_A = 25°C.)

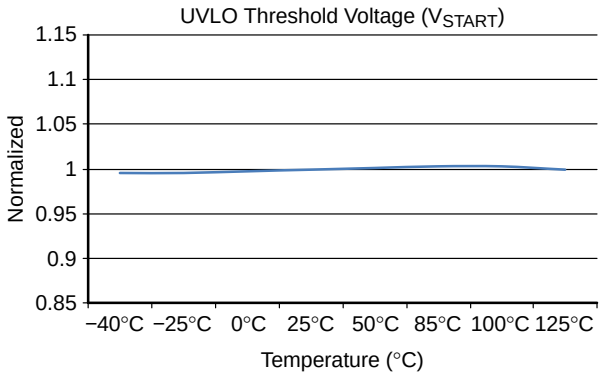


Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

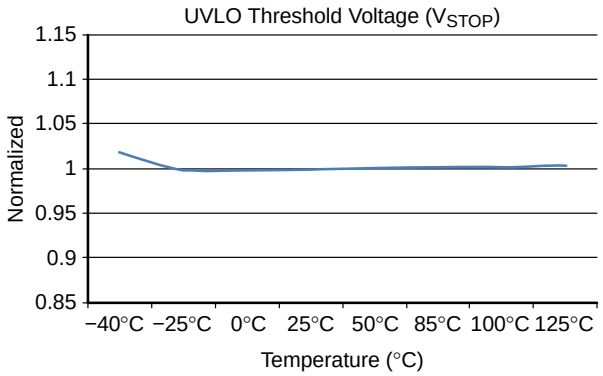


Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

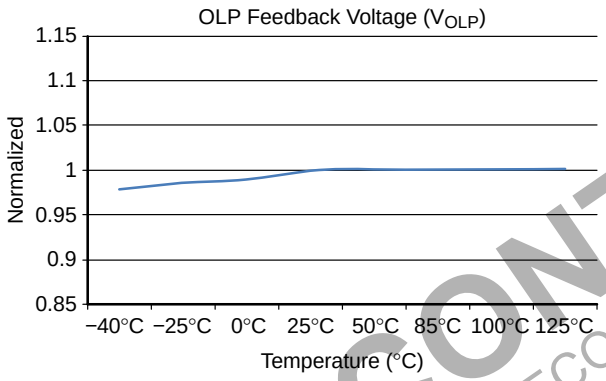


Figure 13. OLP Feedback Voltage (V_{OLP}) vs. T_A

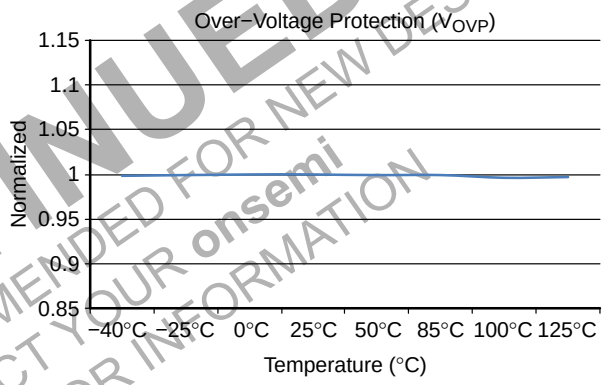


Figure 14. Over−Voltage Protection (V_{OVP}) vs. T_A

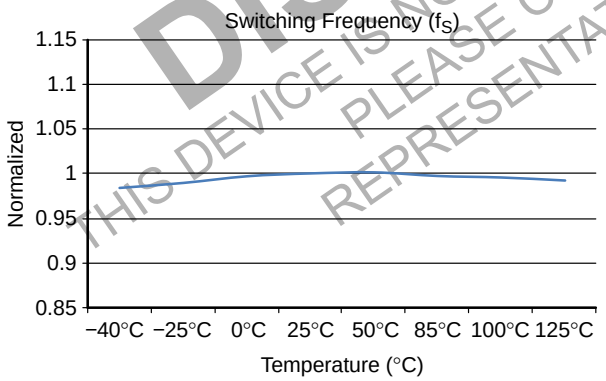


Figure 15. Switching Frequency (f_S) vs. T_A

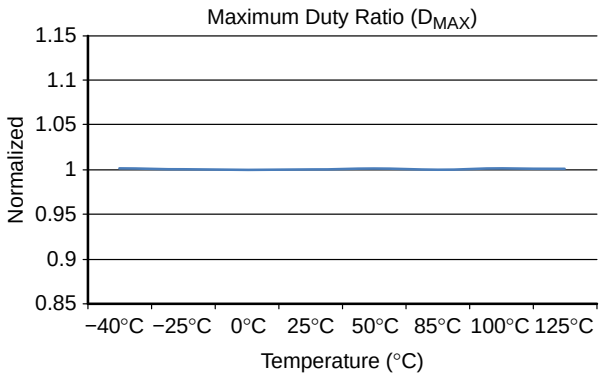


Figure 16. Maximum Duty Ratio (D_{MAX}) vs. T_A

FUNCTIONAL DESCRIPTION

Startup and High−Voltage Regulator

During startup, an internal high−voltage current source (I_{CH}) of the high−voltage regulator (HV_{REG}) supplies the internal bias current (I_{START}) and charges the external capacitor (C_{VCC}) connected to V_{CC} pin, as shown in Figure 17. This internal high−voltage current source is enabled until V_{CC} reaches V_{START} (12 V). During steady−state operation, this internal high−voltage regulator (HV_{REG}) maintains the V_{CC} with 10 V and provides operating switching current (I_{OPS}) for all internal circuits. Therefore, FSL4110LR needs no external bias circuit. The high−voltage regulator is disabled when V_{CC} supplied by the external bias is higher than 10 V. However in the case of self−biasing, power consumption is increased.

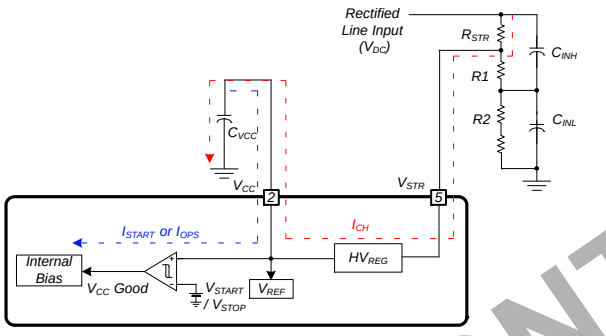


Figure 17. Startup and HV_{REG} Block

The startup resistor (R_{STR}) can be calculated by the following equation (1).

$$R_{STR} \le \frac{V_{DC\_MIN} - V_{START}}{I_{CH}} \quad \text{(eq. 1)}$$

where, $I_{OPS} < I_{CH} < 2$ mA, $R_{STR} + R1 = R2 + R3$

Feedback Control

FSL4110LR employs current−mode control scheme. An opto−coupler (such as FOD817) and shunt regulator (such as KA431) in secondary−side are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across R_{SENSE} resistor makes it possible to control the switching duty cycle. When the input voltage is increased or the output load is decreased, reference input voltage of shunt regulator is increased. If this voltage exceeds internal reference voltage of shunt regulator, opto−diode's current of the opto−coupler increases, pulling down the feedback voltage and reducing drain current.

Pulse−by−Pulse Current Limit

Because current−mode control is employed, the peak current flowing through the SenseFET is limited by the inverting input of PWM comparator, as shown in Figure 18. Assuming that 100 μA current source (I_{FB}) flows only through the internal resistors (3R + R = 24 kΩ), the cathode voltage of diode D2 is about 2.4 V. Since D1 is blocked when feedback voltage (V_{FB}) exceeds 2.4 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current of the SenseFET is limited at:

$$\frac{2.4\ \text{V}}{R_{SENSE}} \times \text{Sense Ratio} \quad \text{(eq. 2)}$$

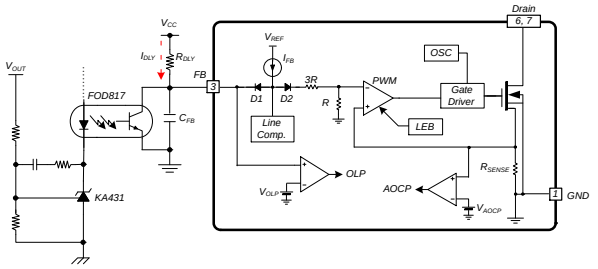


Figure 18. Pulse Width Modulation Circuit

Leading Edge Blanking (LEB)

At the instant, the internal SenseFET is turned on, a high−current spike usually occurs through the SenseFET, caused by primary−side capacitance and secondary−side rectifier reverse recovery. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the current−mode PWM control. To counter this effect, FSL4110LR employs a leading−edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for t_{LEB} (250 ns) after the SenseFET is turned on.

Protection Circuits

The protective functions include Overload Protection (OLP), Over−Voltage Protection (OVP), Under−Voltage Lockout (UVLO), Abnormal Over−Current Protection (AOCP), and Thermal Shutdown (TSD). All of the protections operate in auto−restart mode as shown in Figure 19. Since these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost and PCB space. If a fault condition occurs, switching is terminated and the SenseFET remains off. At the same time, internal protection timing control is activated to decrease power consumption and stress on passive and active components during auto−restart. When internal protection timing control is activated, V_{CC} is regulated with 10 V through the internal high−voltage regulator while switching is terminated. This internal protection timing control continues until restart time (1.6 s) duration is finished. After counting to 1.6 s, the internal high−voltage regulator is disabled and V_{CC} is decreased. When V_{CC} reaches the UVLO stop voltage, V_{STOP} (8 V), the protection is reset and the internal high−voltage current source charges the V_{CC} capacitor via the high voltage startup pin (V_{STR}) again. When V_{CC} reaches the UVLO start voltage, V_{START} (12 V), the FSL4110LR resumes normal operation. In this manner, auto−restart function can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

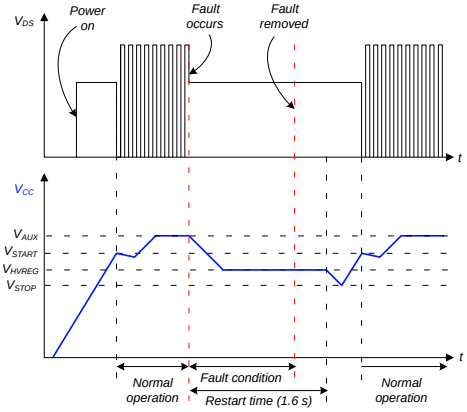


Figure 19. Auto−Restart Protection Waveforms

Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse−by−pulse current−limit capability, the maximum peak current through the SenseFET is limited. If the output consumes more than this maximum power, the output voltage decreases below the set voltage. This reduces the current through the opto−diode, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4 V, internal diode D1 is blocked and the current (I_{DLY}) by R_{DLY} starts to charge C_{FB}. If feedback voltage reaches 4.4 V, internal fixed delay time (t_{DELAY}) starts counting. If feedback voltage maintains over 4.4 V after t_{DELAY} (100 ms), the switching operation is terminated *(see Figure 20)*. The internal OLP circuit is shown in Figure 21.

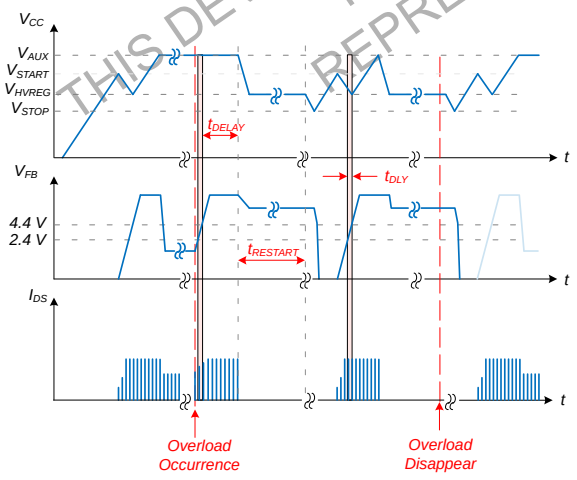


Figure 20. OLP Waveforms

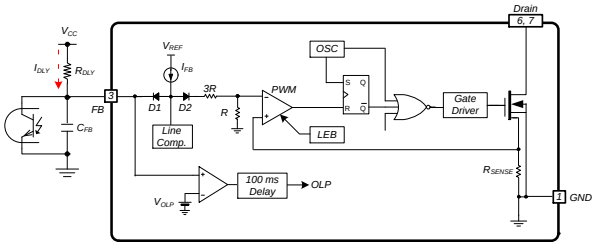


Figure 21. OLP Circuit

Recommended the R_{DLY} value is less than 5 MΩ in self−biasing. The delay time (t_{DLY}) can be calculated by equation (3).

$$t_{DLY} = -R_{DLY} \times C_{FB} \times \ln\left(1 - \frac{2}{V_{CC} - 2.4}\right) \quad \text{(eq. 3)}$$

Example:

When, R_{DLY} = 3 MΩ, C_{FB} = 68 nF, V_{CC} = 15 V,
t_{DLY} = 35 ms

∴ Total delay time for OLP: 135 ms

Abnormal Over−Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn−on time. Overload protection is not enough to protect the FSL4110LR in that abnormal case *(see Figure 22)*; since severe current stress is imposed on the SenseFET until OLP is triggered. The internal AOCP circuit is shown in Figure 23. When the gate turn−on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing−resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the high signal is applied to input of the NOR gate, resulting in the shutdown of the SMPS.

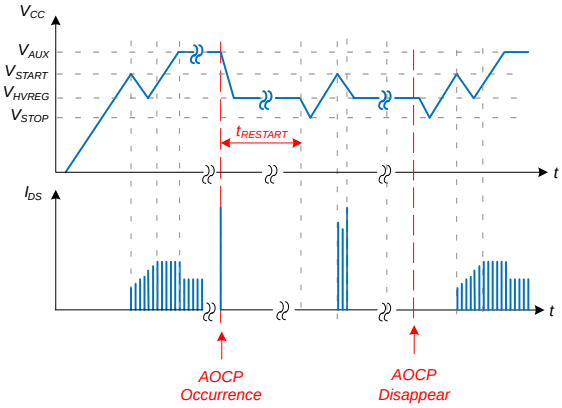


Figure 22. AOCP Waveforms

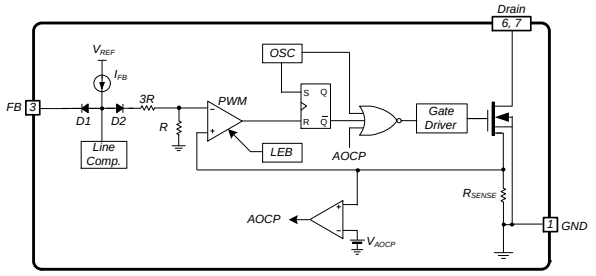


Figure 23. AOCP Circuit

Over−Voltage Protection (OVP)

If the secondary−side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto−coupler transistor becomes almost zero. Then V_{FB} climbs in a similar manner to the overload situation, forcing the preset maximum drain current to flow until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage when the bias−winding is used and the FSL4110LR uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5 V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5 V in the normal conditions. The internal OVP circuit is shown in Figure 24.

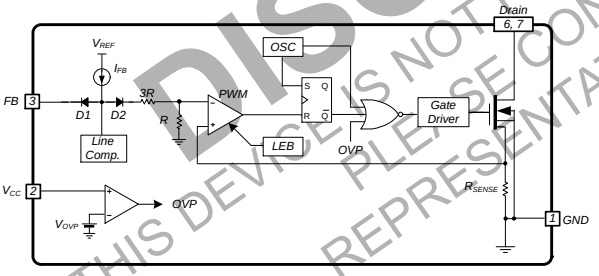


Figure 24. OVP Circuit

Thermal Shutdown (TSD)

The SenseFET and control IC integrated on the same package makes it easier to detect the temperature of the SenseFET. When the junction temperature exceeds 140°C, thermal shutdown is activated. The FSL4110LR is restarted when the temperature decreases by 60°C within $t_{RESTART}$ (1.6 s).

Line Over−Voltage Protection (LOVP)

If the line input voltage is increased to an undesirable level, high line input voltage creates high−voltage stress on the entire system. To protect the SMPS from this abnormal condition, LOVP is included. It is comprised of detecting V_{IN} voltage by using divided resistors. When voltage of V_{IN} voltage is higher than 2.0 V, this condition is recognized as an abnormal error and PWM switching shuts down until voltage of V_{IN} voltage decreases to around 1.9 V within $t_{RESTART}$ (*see Figure 25*). The internal LOVP circuit is shown in Figure 26.

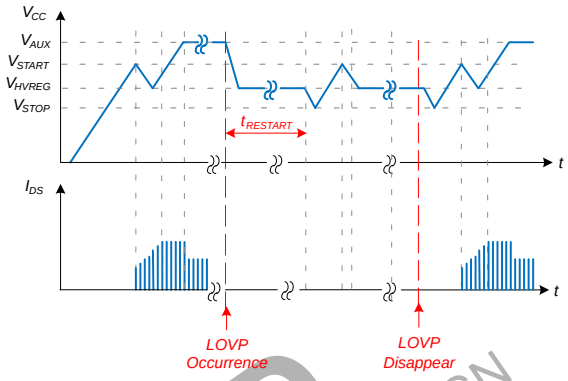


Figure 25. LOVP Waveforms

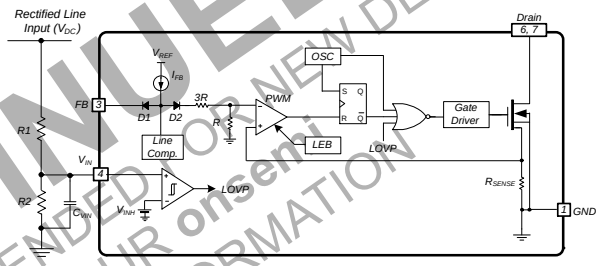


Figure 26. LOVP Circuit

Equation (4) calculates the level of input over−voltage to RMS value.

$$R2 = \frac{V_{INH} \times R1}{V_{DC} - V_{INH}} \quad \text{(eq. 4)}$$

The resistance of divided resistor can be adjusted as necessary. Small resistance can bring relatively large stand−by power consumption at light−load condition. To avoid this situation, a several MΩ resistor is recommended. For stable operation, a several MΩ resistor should accompany a capacitor (C_{VIN}) with hundreds of pF capacitance between the V_{IN} pin and GND.

Oscillator Block

The oscillator frequency is set internally and the FSL4110LR has a random frequency fluctuation function as shown in Figure 27. Fluctuation of the switching frequency can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of an external feedback voltage and an internal free−running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise near switching frequency and allows the use of a cost−effective inductor instead of an AC input line filter to satisfy world−wide EMI requirements.

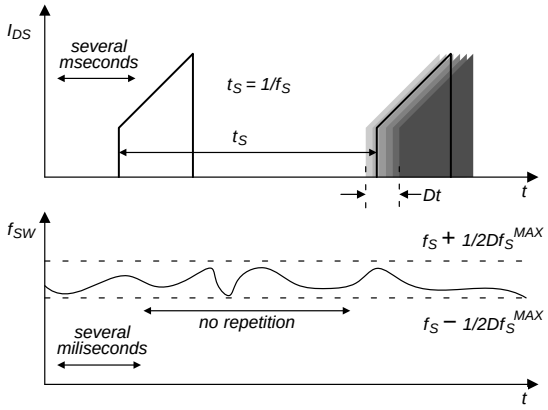


Figure 27. Frequency Fluctuation Waveforms

Soft−Start

The internal soft−start circuit slowly increases the SenseFET current after it starts. The typical soft−start time is 20 ms, as shown in Figure 28, where progressive increments of the SenseFET current are allowed during startup. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is gradually increased to smoothly establish the required output voltage. Soft−start also helps to prevent transformer saturation and reduces stress on the secondary diode.

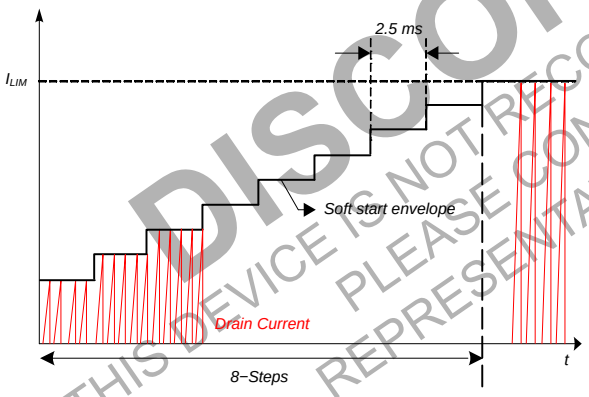


Figure 28. Internal Soft−Start

Burst Mode Operation

To minimize power dissipation in standby mode, the FSL4110LR enters burst mode. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL} (400 mV), as shown in Figure 29. At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes VBURH (500 mV), switching resumes. Feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET, reducing switching loss in standby mode. Additionally to reduce the audible noise soft−burst is implemented.

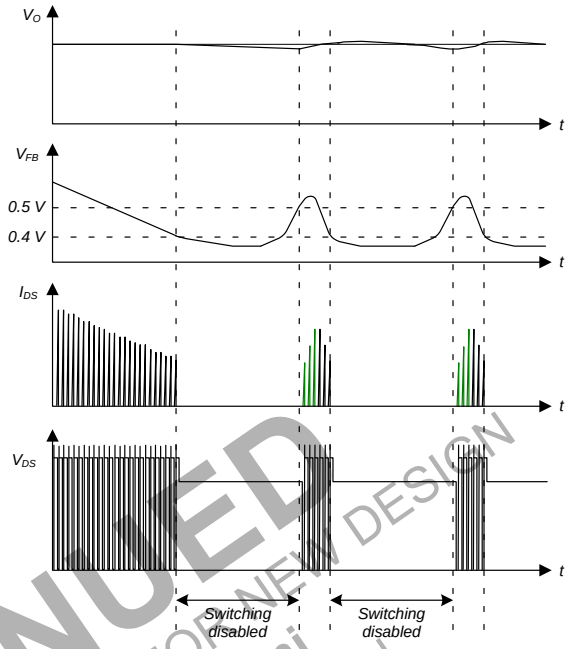


Figure 29. Burst Mode Operation

Line Compensation

All of switching devices have their own inherent propagation delays. This propagation delay will cause a current limit delay defined as t_{CLD}. Because there is a current limit delay, t_{CLD}, there is a difference in the current peak between low and high input voltage. The variance in the current peak is related to the difference between the input voltages, a wider gap in input voltage will result in a greater variance of the current peak.

In order to have a constant current peak regardless of the input voltage, line compensation is required. FSL4110LR has line compensation, so the real peak value of high input voltage is similar to that of low input voltage. t_{CLD} effect could be neglected as showed Figure 30.

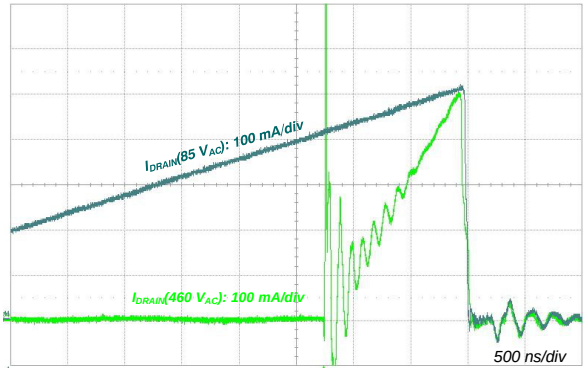


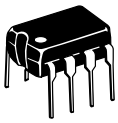
Figure 30. I_{LIMIT} Waveforms (85 V_{AC} vs. 460 V_{AC})

ORDERING INFORMATION

Part Number	Package	Operating Junction Temperature	Current Limit	$R_{DS(ON)}$ (Max)	Output Power Table (Note 12)		Shipping†
					45~460 V_{AC} (Note 13)	85~460 V_{AC} (Note 13)	
FSL4110LRN	PDIP−7 (PDIP−8 LESS PIN 6) (7−DIP) (Pb−Free)	−40°C~125°C	0.52 A	10 Ω	4 W (Note 14)	9 W (Note 14)	3000 Units / Tube
FSL4110LRLX	PDIP7 MINUS PIN 6 GW (7−LSOP) (Pb−Free)						1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

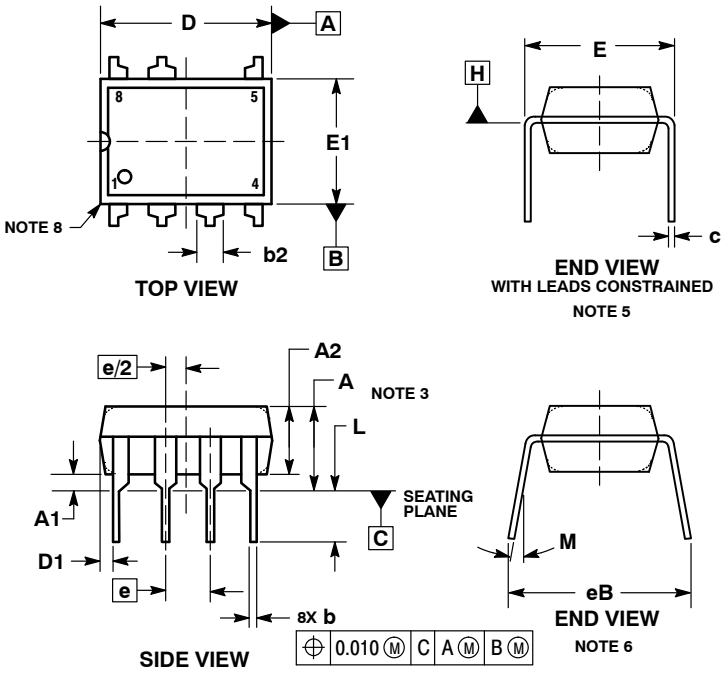
12. The junction temperature can limit the maximum output power.
13. Maximum practical continuous power in an open−frame design at 50°C ambient temperatures.
14. Bias winding condition.



PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

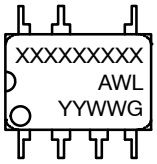
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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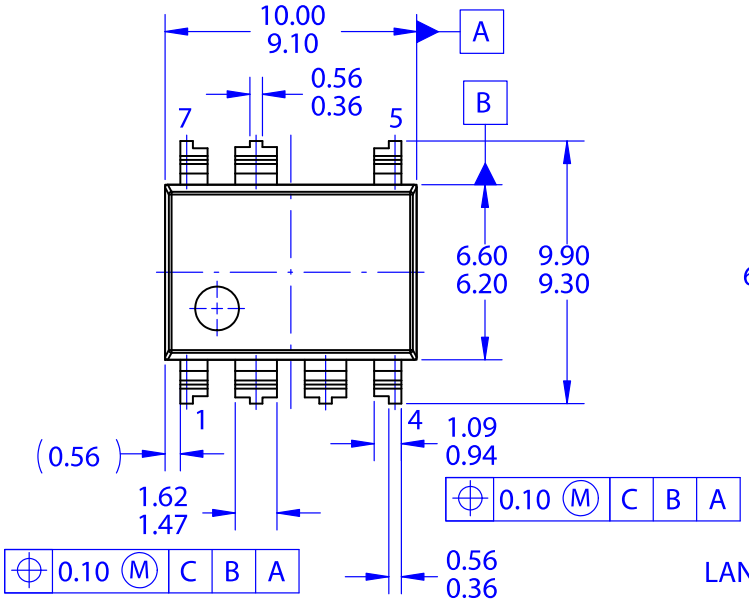
PDIP7 MINUS PIN 6 GW
CASE 707AA
ISSUE O

DATE 31 JAN 2017



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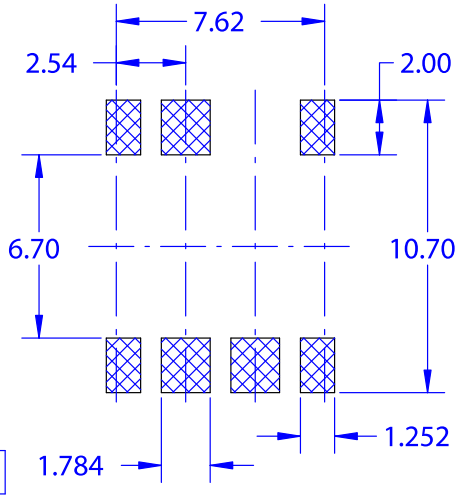
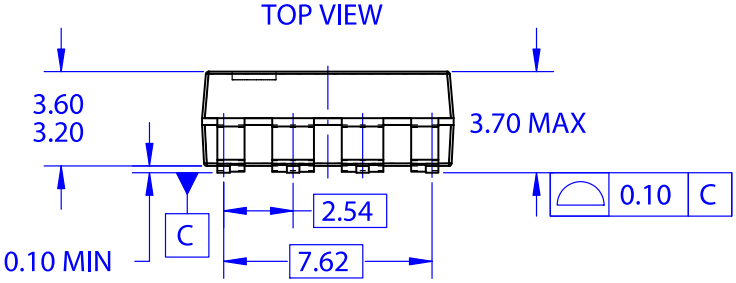


LAND PATTERN RECOMMENDATION



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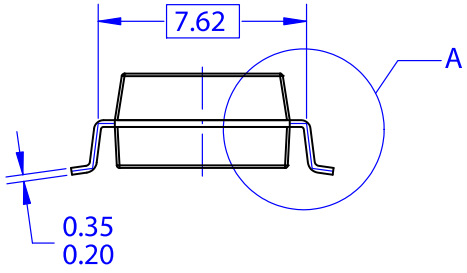
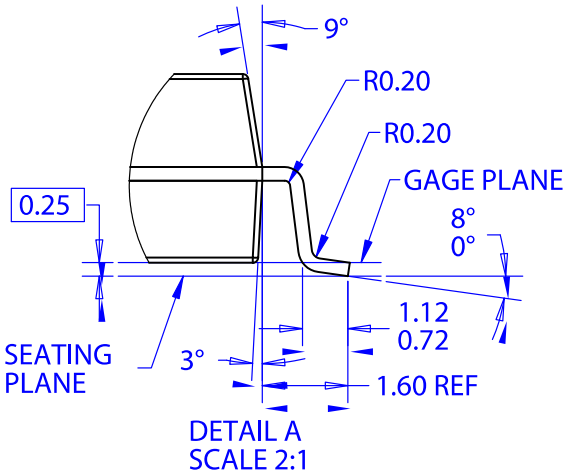


SIDE VIEW



DETAIL A
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C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009

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