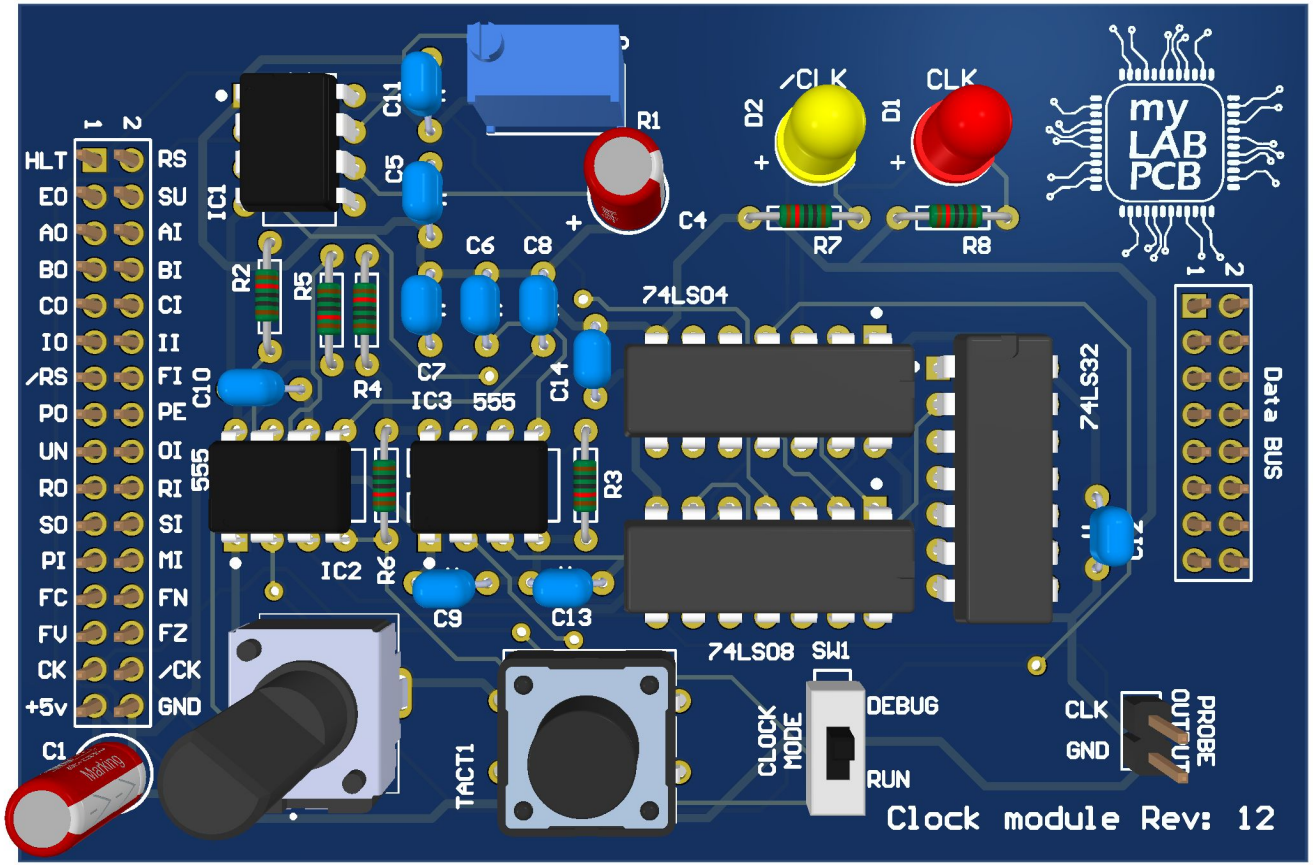
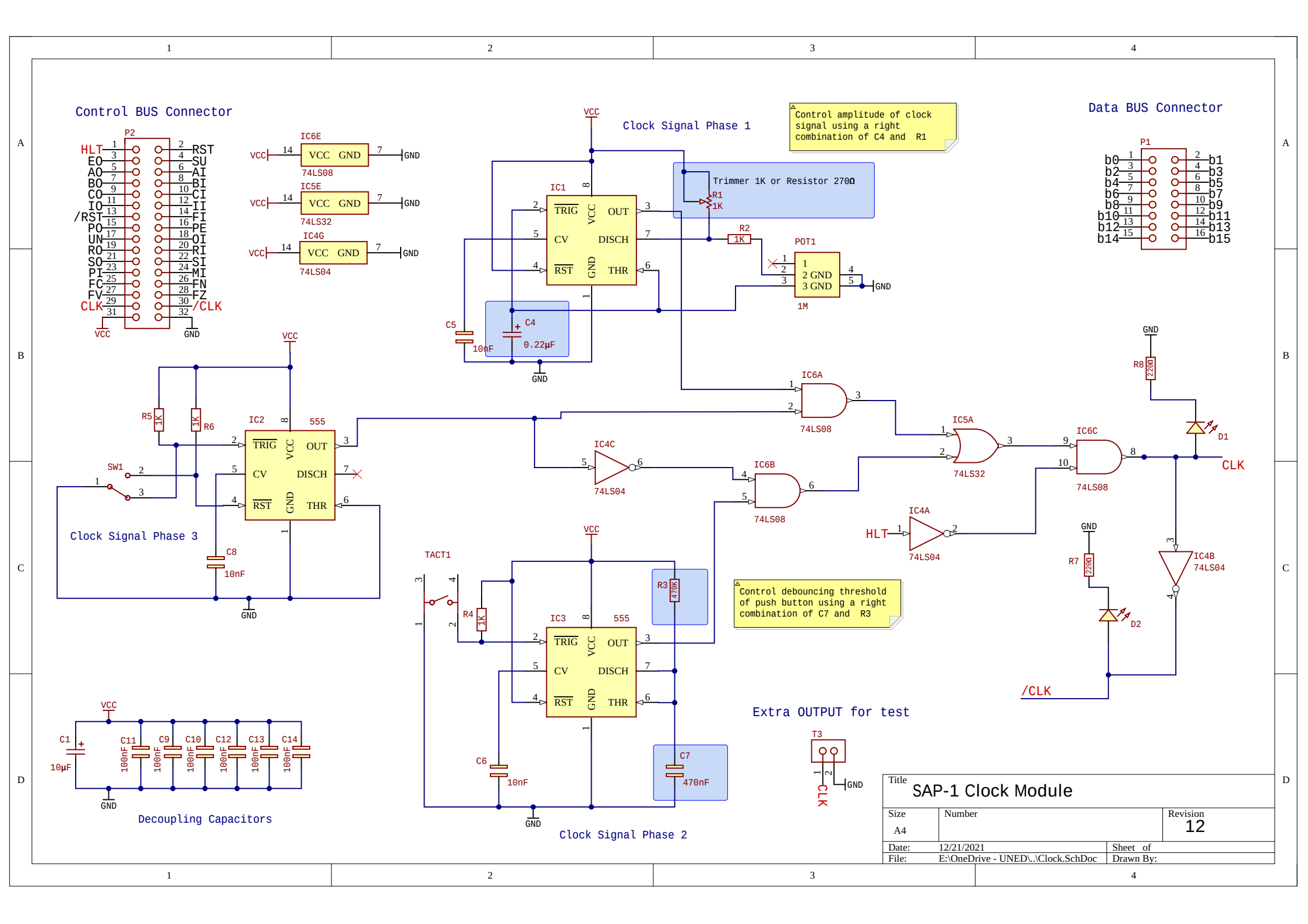
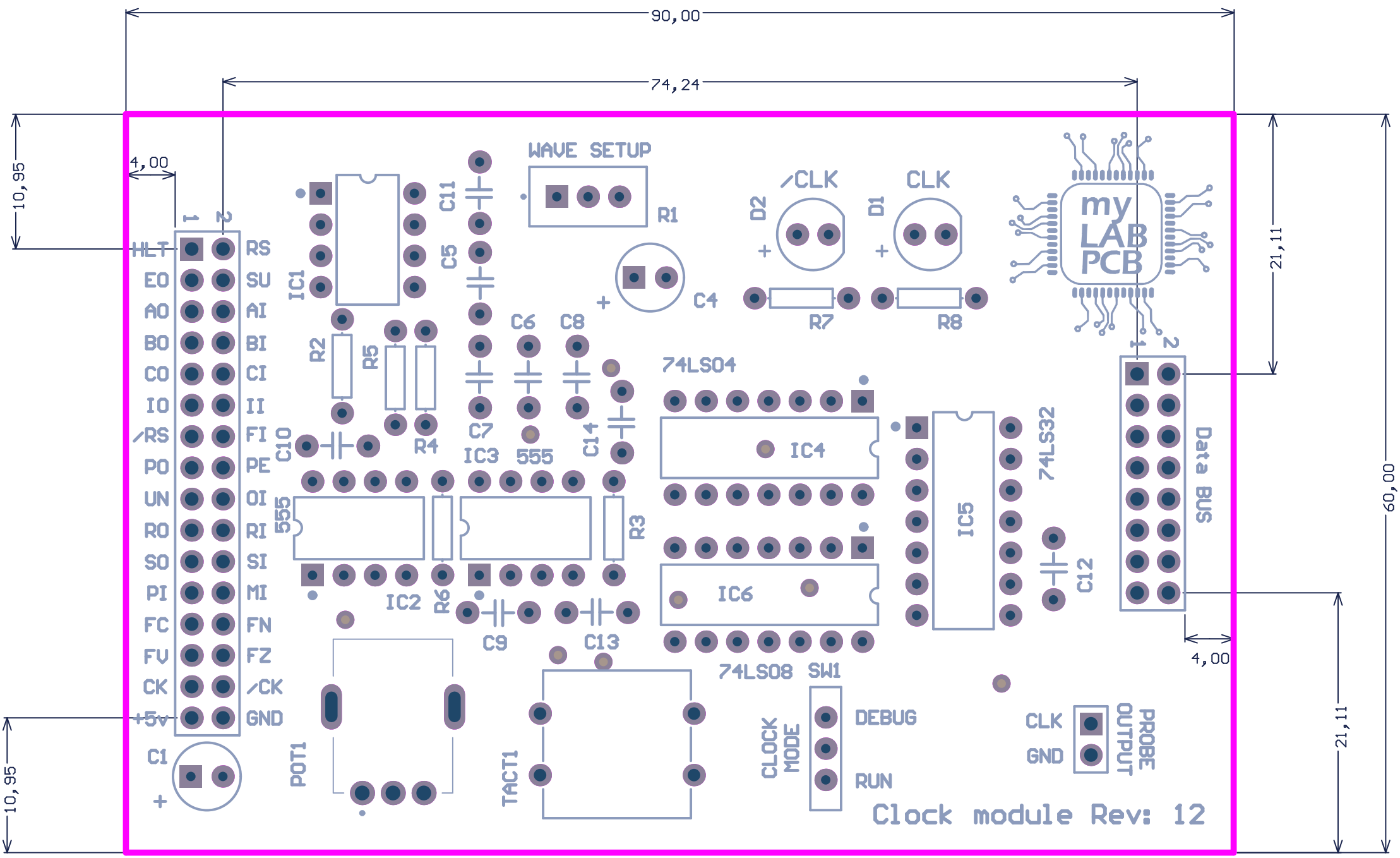

HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
IC1
C11
C5
R1
C4
D2
/CLK
D1
CLK
R7
R8
my LAB PCB
C6
C8
R2
R5
R4
C7
C10
IC3
555
C14
74LS04
74LS32
555
IC2
R6
R3
C9
C13
74LS08
SW1
DEBUG
RUN
CLOCK MODE
TACT1
CLK
GND
PROBE OUTPUT
Data BUS
Clock module Rev: 12


Control BUS Connector
P2
HLT 1 2 RST
EO 3 4 SU
AO 5 6 AI
BO 7 8 BI
CO 9 10 CI
IO 11 12 II
/RST 13 14 FI
PO 15 16 PE
UN 17 18 OI
RO 19 20 RI
SO 21 22 SI
PI 23 24 MI
FC 25 26 FN
FV 27 28 FZ
CLK 29 30 /CLK
31 32
VCC
GND
IC6E
VCC 14 VCC GND 7 GND
74LS08
IC5E
VCC 14 VCC GND 7 GND
74LS32
IC4G
VCC 14 VCC GND 7 GND
74LS04
Clock Signal Phase 1
Control amplitude of clock signal using a right combination of C4 and R1
Trimmer 1K or Resistor 270Ω
R1
1K
IC1
TRIG
CV
RST
VCC
GND
OUT
DISCH
THR
R2
1K
POT1
1
2 GND
3 GND
1M
C5
10nF
C4
0.22µF
Data BUS Connector
P1
b0 1 2 b1
b2 3 4 b3
b4 5 6 b5
b6 7 8 b7
b8 9 10 b9
b10 11 12 b11
b12 13 14 b13
b14 15 16 b15
IC6A
74LS08
IC5A
74LS32
IC6C
74LS08
R8
220Ω
D1
CLK
R5
1K
R6
1K
IC2
555
SW1
Clock Signal Phase 3
C8
10nF
IC4C
74LS04
IC6B
74LS08
IC4A
HLT
74LS04
R7
220Ω
D2
IC4B
74LS04
/CLK
TACT1
R4
1K
R3
470K
IC3
555
C6
10nF
C7
470nF
Control debouncing threshold of push button using a right combination of C7 and R3
Extra OUTPUT for test
T3
CLK
GND
C1
10µF
C11
C9
C10
C12
C13
C14
100nF
Decoupling Capacitors
Clock Signal Phase 2
Title
SAP-1 Clock Module
Size
A4
Number
Revision
12
Date:
12/21/2021
File:
E:\OneDrive - UNED\..\Clock.SchDoc
Sheet of
Drawn By:


90,00
74,24
10,95
4,00
21,11
60,00
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
IC1
C11
C5
WAVE SETUP
R1
C4
/CLK
CLK
D2
D1
R7
R8
my LAB PCB
Data BUS
R2
R5
R4
C10
C6
C8
C7
IC3
555
C14
74LS04
IC4
74LS32
IC5
C12
555
R3
IC2
R6
C9
C13
IC6
74LS08
SW1
POT1
TACT1
CLOCK MODE
DEBUG
RUN
CLK
GND
PROBE OUTPUT
Clock module Rev: 12