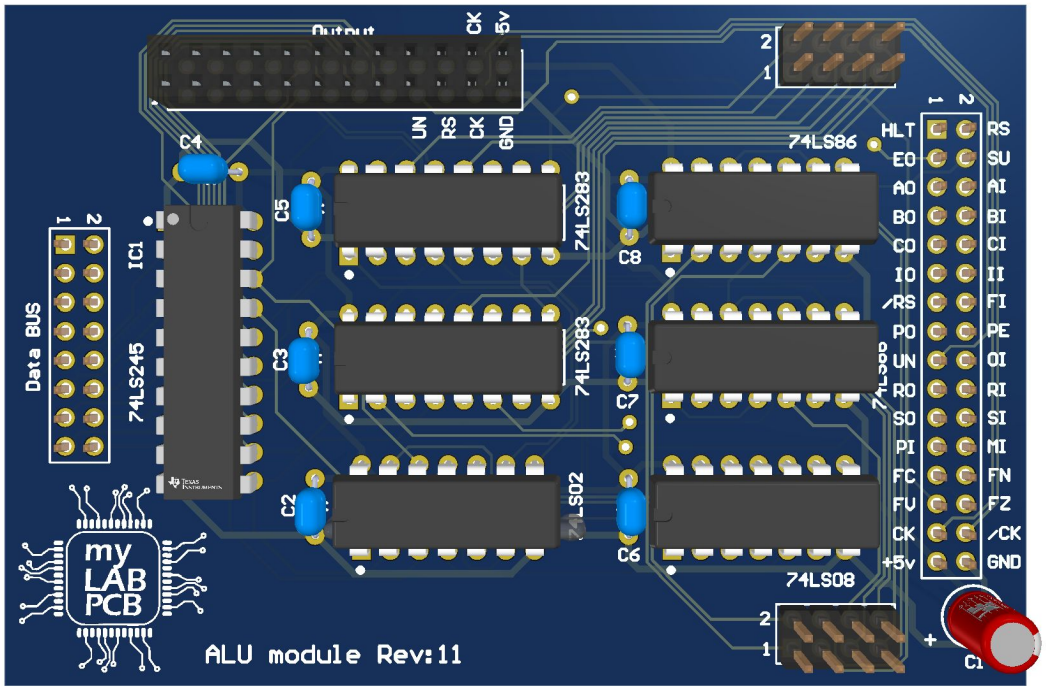
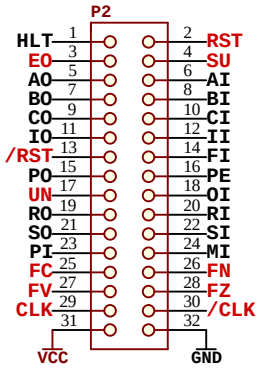
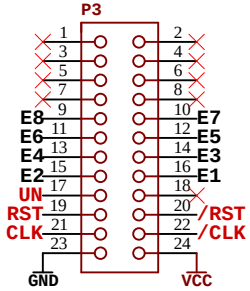

Output
CK
5v
UN
RS
CK
GND
2
1
1
2
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
74LS86
74LS283
74LS283
74LS02
74LS08
74LS245
IC1
Data BUS
C1
C2
C3
C4
C5
C6
C7
C8
my
LAB
PCB
ALU module Rev:11

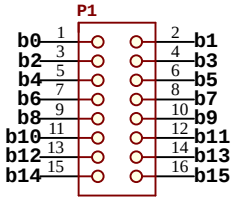
Control BUS Connector



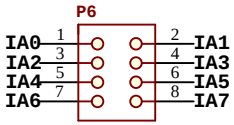
OUTPUT Connector



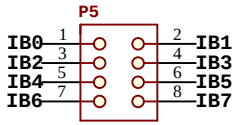
Data BUS Connector

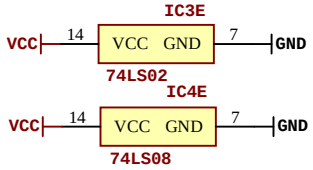


Register A input

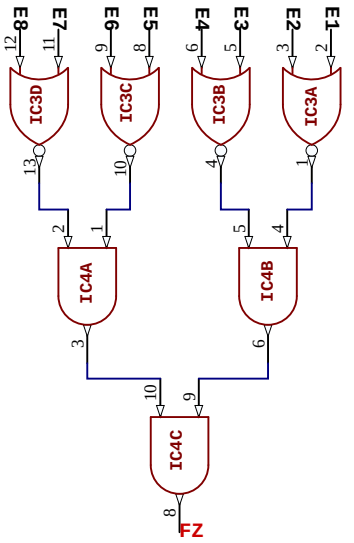


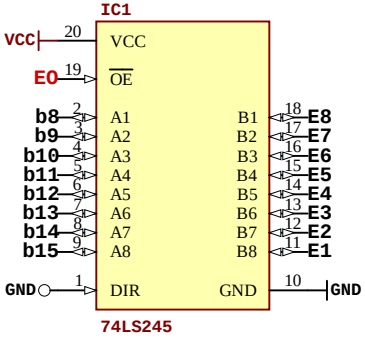
Register B Input



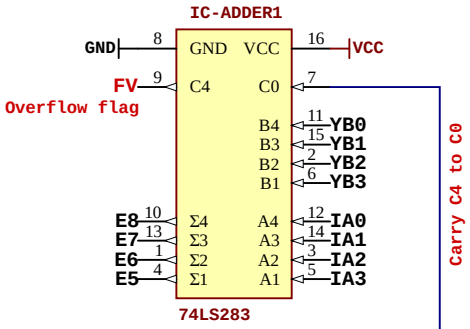


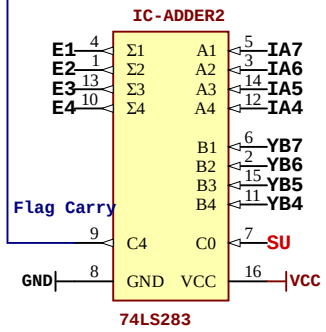
Zero Flag



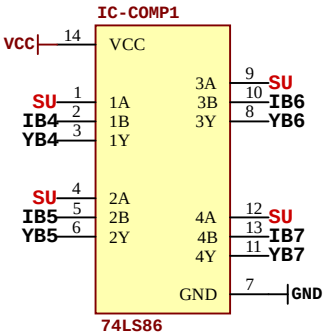


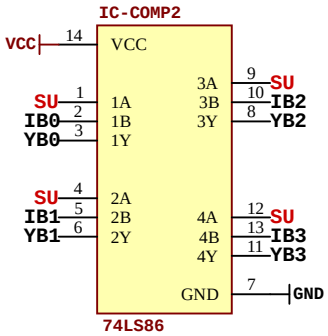
Input significative bit weigh goes from IA7 or YB7 (lower)

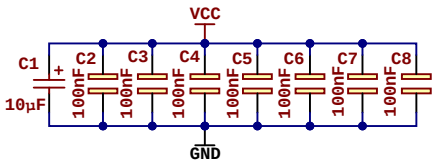




Add operation goes from E1 to E4 and carry is passed from C4 to C0. Then SUM inputs order goes from A1,B1 to A4,B4
Cascade is from IC-ADDER2 to IC-ADDER1.



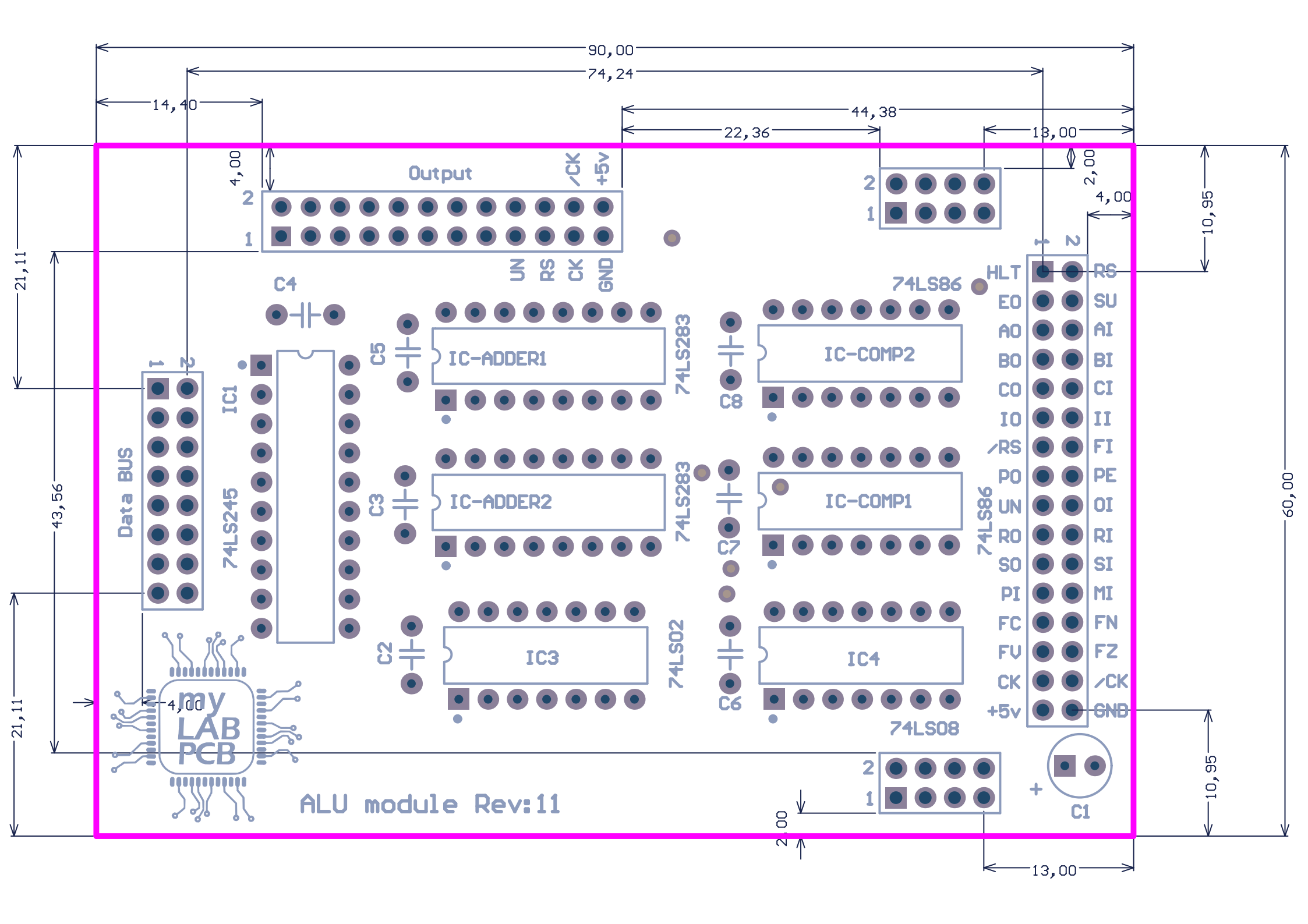


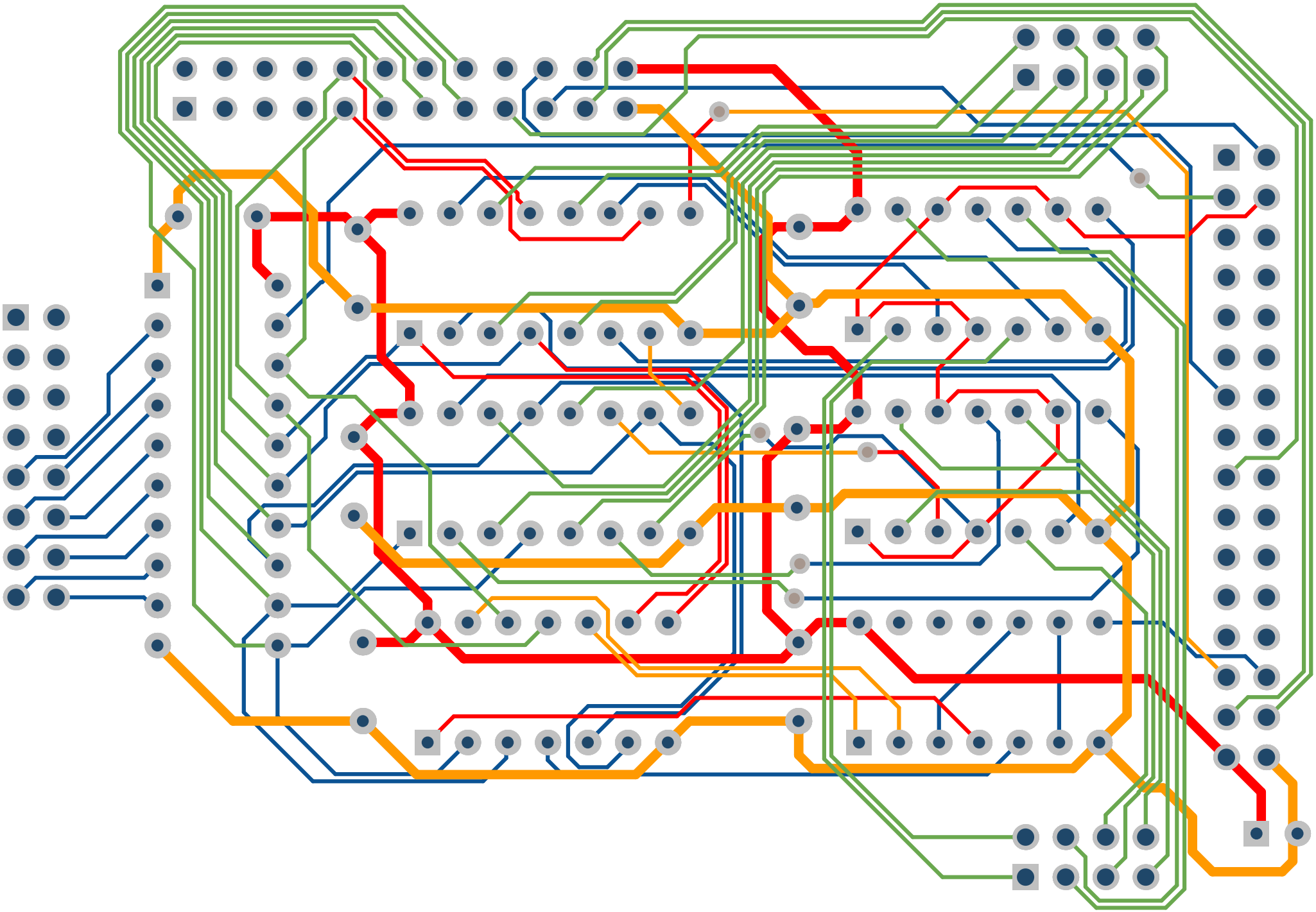


Decoupling Capacitors

CO, first carry should set to SU signal. On ADD operation SU is LOW and Carry is 0, for SUB operation SU is HIGH and Carry is 1.

Project: myCPU ALU module	
Revision: 11	**Date:** 05/10/2021
Author: Rafa Hernández	


90,00
74,24
14,40
44,38
22,36
13,00
4,00
2,00
4,00
10,95
21,11
43,56
60,00
Output
/CK
+5v
UN
RS
CK
GND
C4
C5
C3
C2
C8
C7
C6
IC-ADDER1
IC-ADDER2
IC3
IC-COMP2
IC-COMP1
IC4
74LS283
74LS283
74LS02
74LS86
74LS08
IC1
74LS245
Data BUS
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
my
LAB
PCB
ALU module Rev:11



Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C2, C3, C4, C5, C6, C7, C	Ceramic or tantalum capacitor	100nF	7
IC1	Non inverting bus transceiver	74LS245	1
IC3	Quad 2-input NOR gates	74LS02	1
IC4	Quad 2-input AND gates	74LS08	1
IC-ADDER1, IC-ADDER2	4-Bits Full adder with fast carry	74LS283	2
IC-COMP1, IC-COMP2	Quad 2-input XOR gates	74LS86	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p	1
P5, P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	2

Assembly List

Desig.	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
C6	Ceramic or tantalum capacitor	100nF
C7	Ceramic or tantalum capacitor	100nF
C8	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC3	Quad 2-input NOR gates	74LS02
IC4	Quad 2-input AND gates	74LS08
IC-ADDER1	4-Bits Full adder with fast carry	74LS283
IC-ADDER2	4-Bits Full adder with fast carry	74LS283
IC-COMP1	Quad 2-input XOR gates	74LS86
IC-COMP2	Quad 2-input XOR gates	74LS86
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p