Data sheet acquired from Harris Semiconductor
SCHS211

# CD74HC4094, CD74HCT4094

## High Speed CMOS Logic
## 8-Stage Shift and Store Bus Register, Three-State

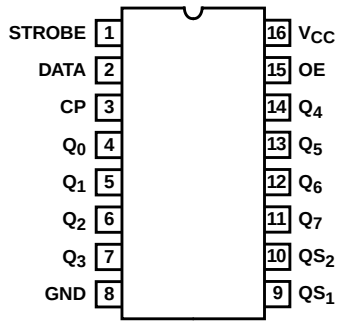
November 1997

### Features

- Buffered Inputs
- Separate Serial Outputs Synchronous to Both Positive and Negative Clock Edges For Cascading
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55$^{o}$C to 125$^{o}$C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$

### Pinout

**CD74HC4094, CD74HCT4094**
**(PDIP, SOIC)**
TOP VIEW



## Description

The Harris CD74HC4094 and CD74HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input to parallel buffered three-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the Strobe input is high. Data in the storage register appears at the outputs whenever the Output-Enable signal is high.

Two serial outputs are available for cascading a number of these devices. Data is available at the $QS_1$ serial output terminal on positive clock edges to allow for high-speed operation in cascaded system in which the clock rise time is fast. The same serial information, available at the $QS_2$ terminal on the next negative clock edge, provides a means for cascading these devices when the clock rise time is slow.

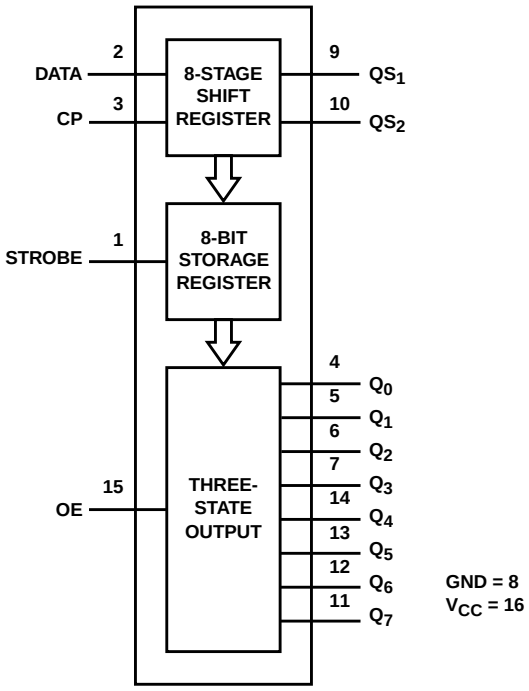
## Ordering Information

| PART NUMBER | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD74HC4094E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74HCT4094E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74HC4094M | -55 to 125 | 16 Ld SOIC | M16.15 |
| CD74HCT4094M | -55 to 125 | 16 Ld SOIC | M16.15 |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

## Functional Diagram




**TRUTH TABLE**

| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|---|---|---|---|---|---|---|---|
| CP | OE | STR | D | $Q_0$ | $Q_n$ | $QS_1$ (NOTE 4) | $QS_2$ |
| ↑ | L | X | X | Z | Z | Q'6 | NC |
| ↓ | L | X | X | Z | Z | NC | $Q_7$ |
| ↑ | H | L | X | NC | NC | Q'6 | NC |
| ↑ | H | H | L | L | $Q_n$ -1 | Q'6 | NC |

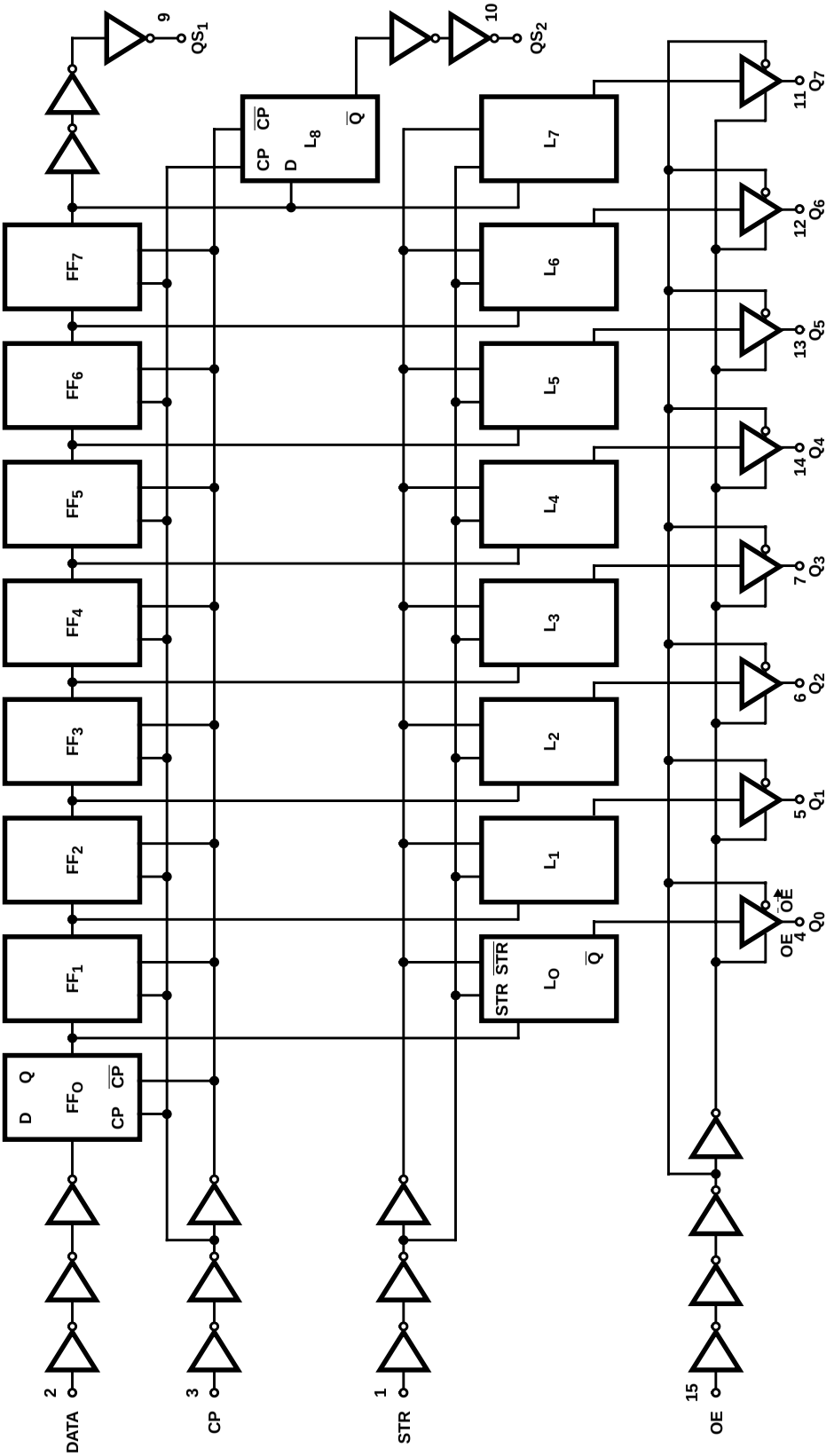
**TRUTH TABLE**

| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|---|---|---|---|---|---|---|---|
| **CP** | **OE** | **STR** | **D** | $Q_0$ | $Q_n$ | $QS_1$ (NOTE 4) | $QS_2$ |
| ↑ | H | H | H | H | $Q_n$ -1 | Q'6 | NC |
| ↓ | H | H | H | NC | NC | NC | $Q_7$ |

NOTES:

3. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, NC = No charge, Z = High Impedance Off-state, ↑ = Transition from Low to High Level, ↓ = Transition from High to Low.
4. At the positive clock edge the information in the seventh register stage is transferred to the 8th register stage and $QS_1$ output.

## Logic Diagram



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

Thermal Resistance (Typical, Note 5) $\theta_{JA}$ (°C/W)
PDIP Package . . . . . 90
SOIC Package . . . . . 160
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

5. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE: For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| D | 0.4 |
| CP, OE | 1.5 |
| STR | 1.0 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

## Prerequisite for Switching Specifications

| CHARACTERISTIC | SYMBOL | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | |
| CP Pulse Width | $t_W$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| STR Pulse Width | $t_{WH}$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |

## Prerequisite for Switching Specifications (Continued)

| CHARACTERISTIC | SYMBOL | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Data Set-up Time | $t_{SU}$ | 2 | 50 | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | 11 | - | 13 | - | ns |
| Data Hold Time | $t_H$ | 2 | 3 | - | 3 | - | 3 | - | ns |
| | | 4.5 | 3 | - | 3 | - | 3 | - | ns |
| | | 6 | 3 | - | 3 | - | 3 | - | ns |
| STR Set-up Time | $t_{SU}$ | 2 | 100 | - | 125 | - | 150 | - | ns |
| | | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| | | 6 | 17 | - | 21 | - | 26 | - | ns |
| STR Hold Time | $t_H$ | 2 | 0 | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | 0 | - | 0 | - | ns |
| Maximum CP Frequency | $f_{CL\ (MAX)}$ | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| **HCT TYPES** | | | | | | | | | |
| CP Pulse Width | $t_W$ | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| STR Pulse Width | $t_{WH}$ | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| Data Set-up Time | $t_{SU}$ | 4.5 | 10 | - | 13 | - | 15 | - | ns |
| Data Hold Time | $t_H$ | 4.5 | 4 | - | 4 | - | 4 | - | ns |
| STR Set-up Time | $t_{SU}$ | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| STR Hold Time | $t_H$ | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Maximum CP Frequency | $f_{CL\ (MAX)}$ | 4.5 | 30 | - | 24 | - | 20 | - | MHz |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay Time (Figure 1) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 150 | - | 190 | - | 225 | ns |
| CP to $QS_1$ | | | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| | | $C_L$ =15pF | 5 | - | 12 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 26 | - | 33 | - | 38 | ns |
| CP to $QS_2$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 135 | - | 170 | - | 205 | ns |
| | | | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | $C_L$ =15pF | 5 | - | 11 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 23 | - | 29 | - | 35 | ns |
| CP to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 195 | - | 245 | - | 295 | ns |
| | | | 4.5 | - | - | 39 | - | 49 | - | 59 | ns |
| | | | 5 | - | 16 | - | - | - | - | - | ns |
| | | | 6 | - | - | 33 | - | 42 | - | 50 | ns |
| STR to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 180 | - | 225 | - | 270 | ns |
| | | | 4.5 | - | - | 36 | - | 45 | - | 54 | ns |
| | | | 6 | - | - | 31 | - | 38 | - | 46 | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Output Enable to $Q_n$ | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| | | | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | | 6 | - | - | 30 | - | 37 | - | 45 | ns |
| Output Disable to $Q_n$ | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| | | | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Output Disabling Time | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ =15pF | 5 | - | 10 | - | - | - | - | - | ns |
| Maximum CP Frequency | $f_{MAX}$ | $C_L$ =15pF | 5 | - | 60 | - | - | - | - | - | MHz |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 6, 7) | $C_{PD}$ | $C_L$ =15pF | 5 | - | 90 | - | - | - | - | - | pF |
| Three-State Output Capacitance | $C_O$ | $C_L$ = 50pF | - | - | - | 15 | - | 15 | - | 15 | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay Time (Figure 1) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 39 | - | - | - | - | ns |
| CP to $QS_1$ | | $C_L$ =15pF | 5 | - | 16 | - | - | - | - | - | ns |
| CP to $QS_2$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 36 | - | - | - | - | ns |
| | | $C_L$ =15pF | 5 | - | 15 | - | - | - | - | - | ns |
| CP to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 43 | - | - | - | - | ns |
| | | $C_L$ =15pF | 5 | - | 18 | - | - | - | - | - | ns |
| STR to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 39 | - | - | - | - | ns |
| Output Enable to $Q_n$ | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 4.5 | - | - | 35 | - | - | - | - | ns |
| Output Disable to $Q_n$ | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 4.5 | - | - | 35 | - | - | - | - | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | - | - | - | ns |
| Output Disabling Time | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ =15pF | 5 | - | 14 | - | - | - | - | - | ns |
| Maximum CP Frequency | $f_{MAX}$ | $C_L$ =15pF | 5 | - | 60 | - | - | - | - | - | MHz |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 6, 7) | $C_{PD}$ | $C_L$ =15pF | 5 | - | 110 | - | - | - | - | - | pF |
| Three-State Output Capacitance | $C_O$ | $C_L$ = 50pF | - | - | - | 15 | - | 15 | - | 15 | pF |

NOTES:

6. $C_{PD}$ is used to determine the dynamic power consumption, per register.
7. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

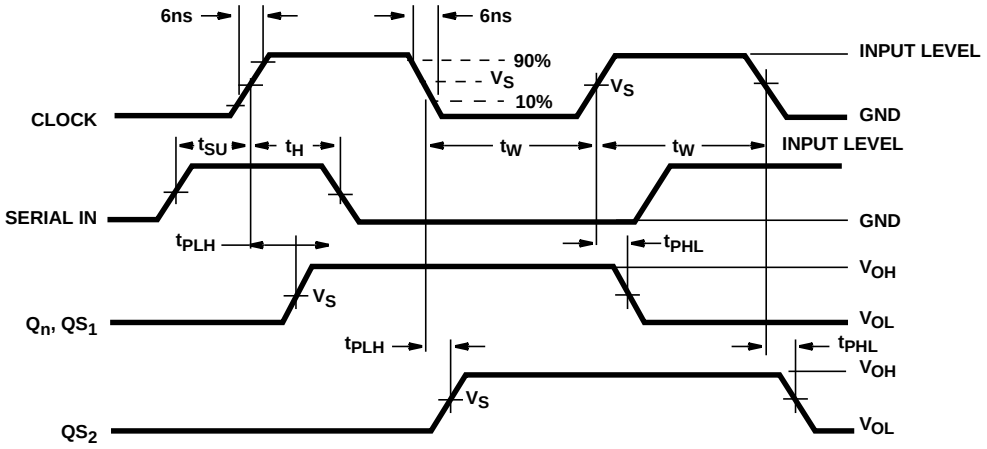



FIGURE 1. DATA PROPAGATION DELAYS, SET-UP AND HOLD TIMES

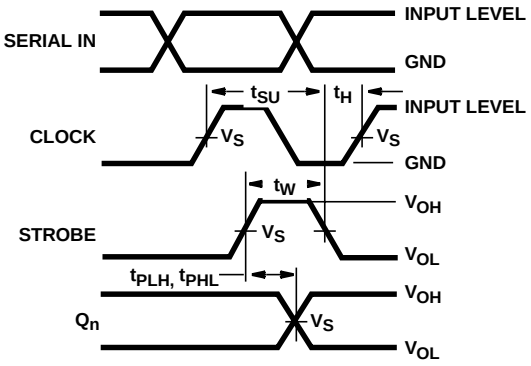



FIGURE 2. STROBE PROPAGATION DELAYS AND SET-UP AND HOLD TIMES

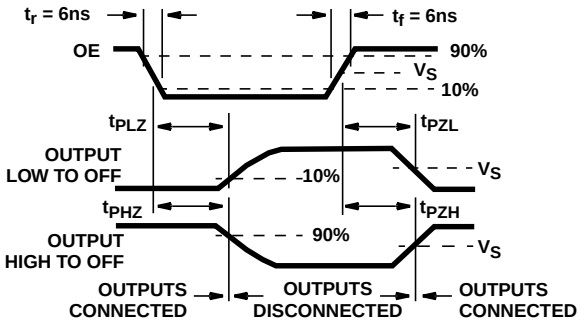



FIGURE 3. ENABLE AND DISABLE TIMES

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