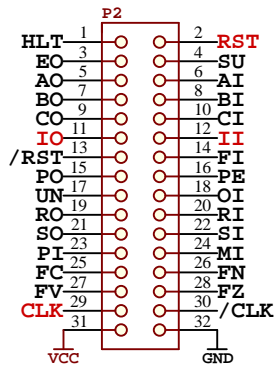
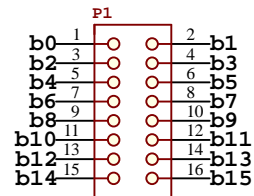


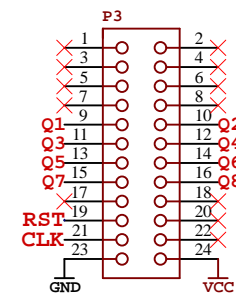
Control BUS Connector



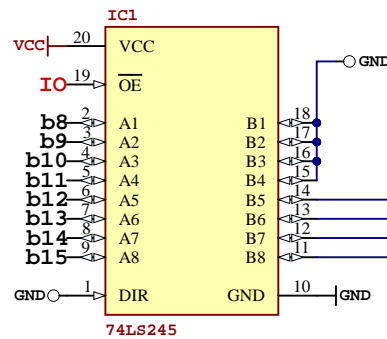
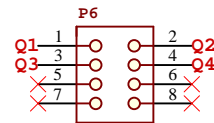
Data BUS Connector



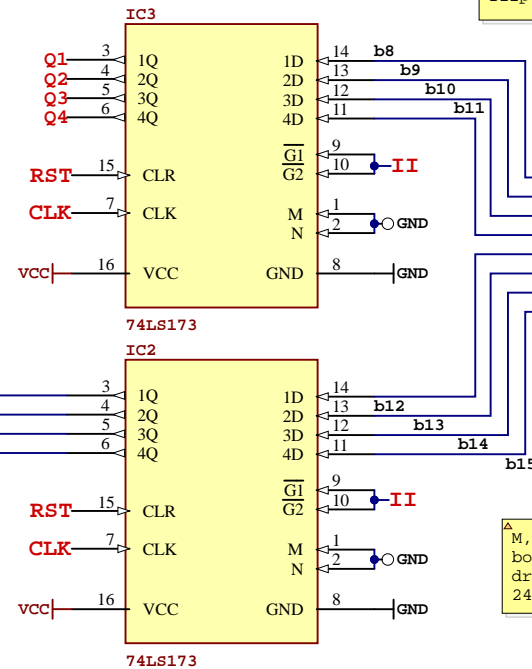
OUTPUT Connector



Instruction Decoder Connector

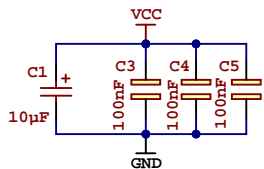


A 4+4 bits register module. Most significative word correspond to instruction opcode and is shared with Instruction decoder, less significative word correspond to operand and is exposed to data BUS when an IO signal is received. Bit weigh goes from Q8 (less) to Q1.



G1, G2 input control. Set both to LOW to load all inputs into flip-flops

M, N output control. Set both to LOW allow driving all outputs to 245.



Decoupling Capacitors

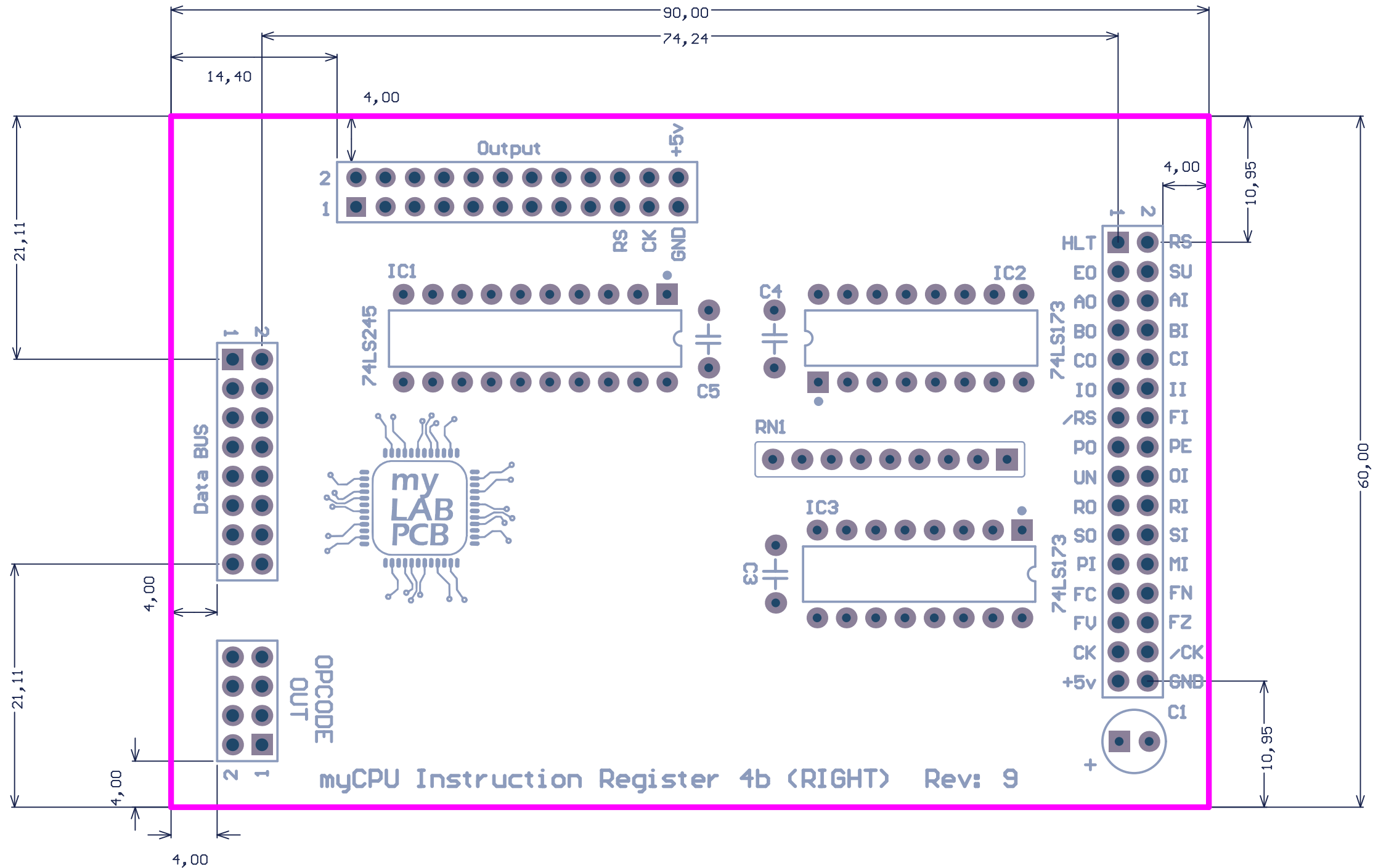


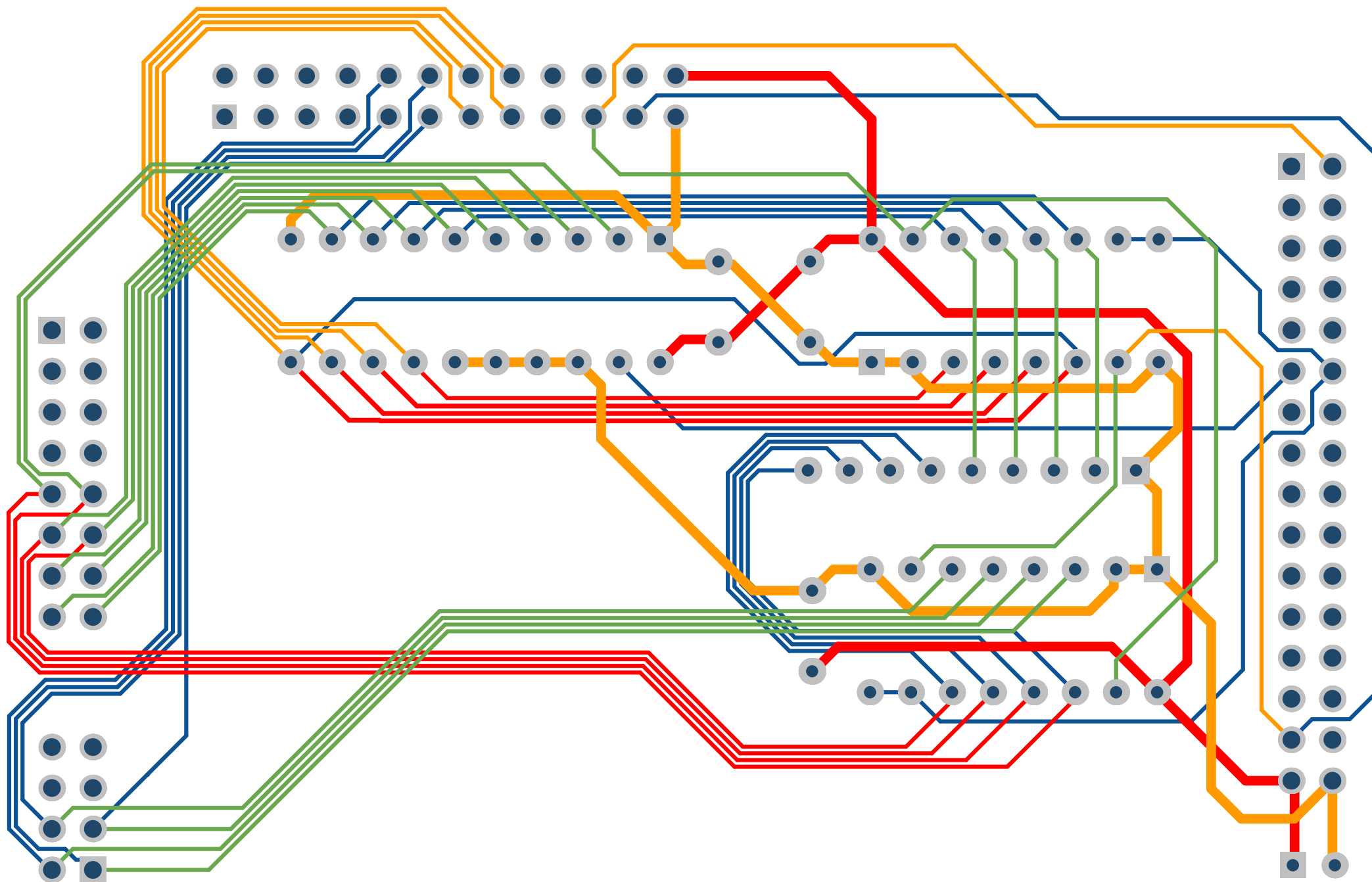
Project: myCPU Instruction Register 4+4 bit R

Revision: 9

Date: 12/10/2022

Author: Rafa Hernández







Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C3, C4, C5	Ceramic or tantalum capacitor	100nF	3
IC1	Non inverting bus transceiver	74LS245	1
IC2, IC3	4-bit D-Type Register with 3 state outputs	74LS173	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical,	24p	1
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	1
RN1	Resistor array 8 elements, 9 pins	1K	1



Assembly List

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10 μ F
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC2	4-bit D-Type Register with 3 state outputs	74LS173
IC3	4-bit D-Type Register with 3 state outputs	74LS173
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
RN1	Resistor array 8 elements, 9 pins	1K