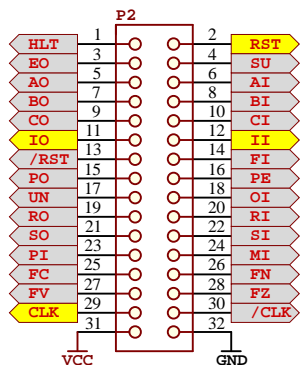
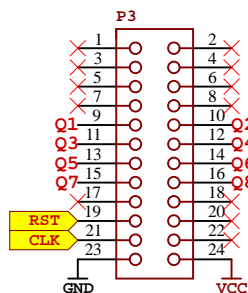




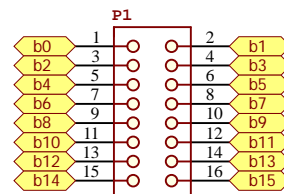
## Control BUS Connector



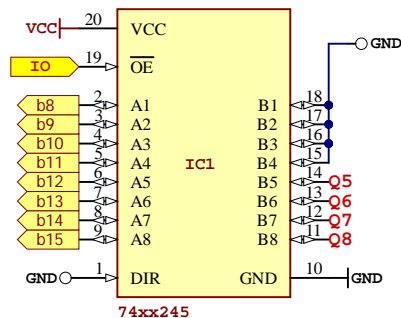
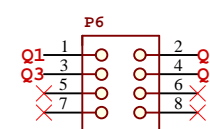
## OUTPUT Connector



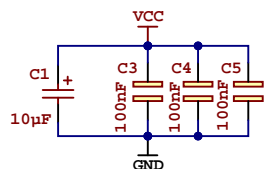
## Data BUS Connector



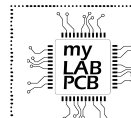
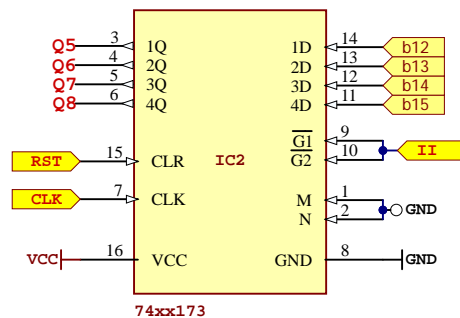
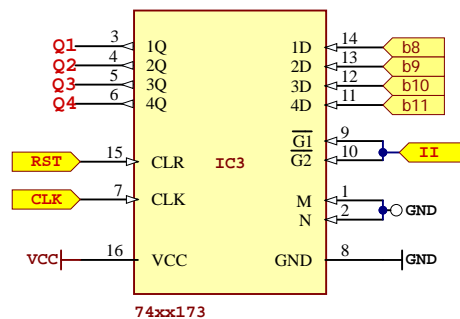
## Instruction Decoder Connector



A 4+4 bits register module. Most significative word correspond to instruction opcode and is shared with Instruction decoder, less significative word correspond to operand and is exposed to data BUS when an IO signal is received. Bit weight goes from Q8 (less) to Q1 (most)



Decoupling Capacitors

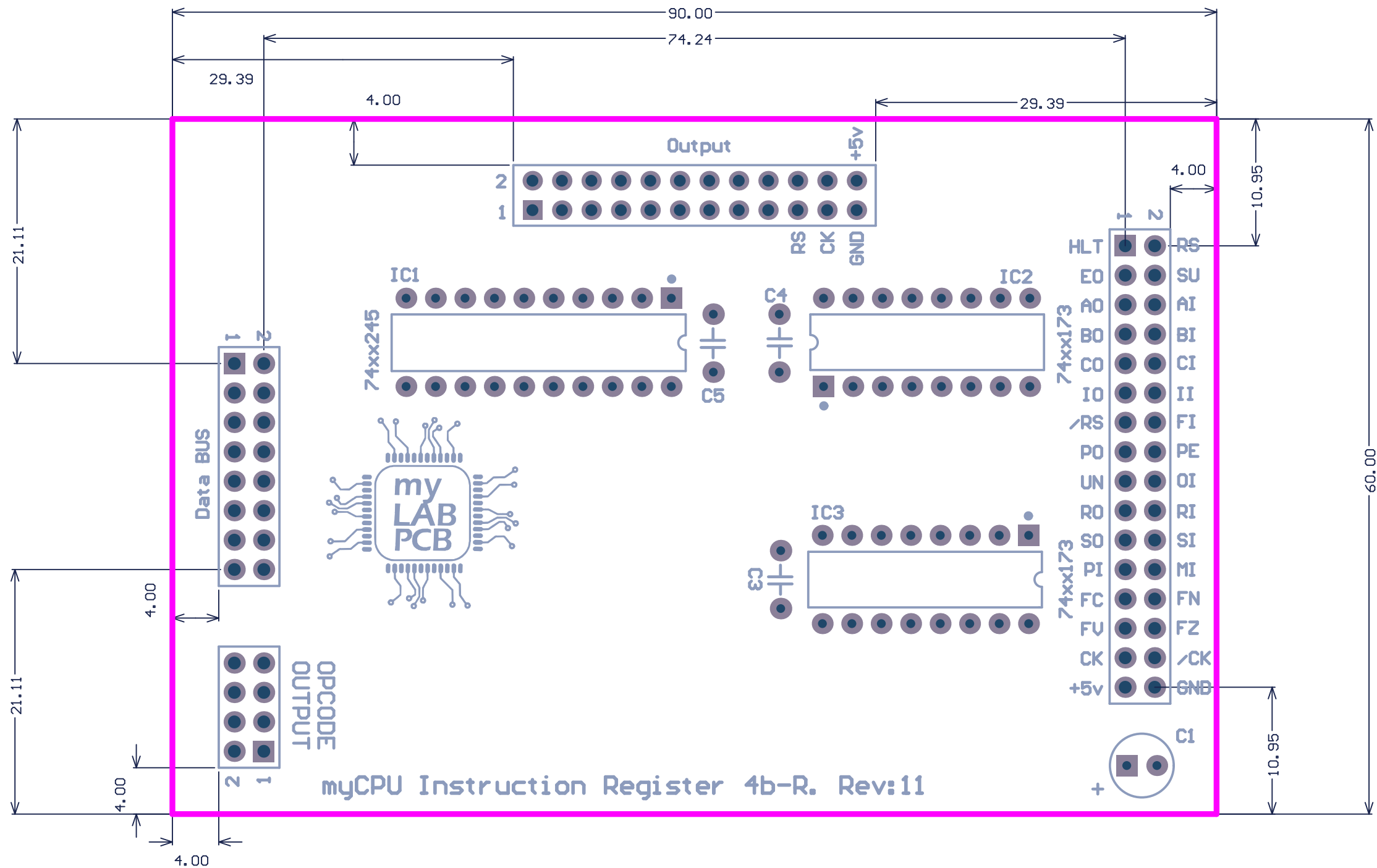


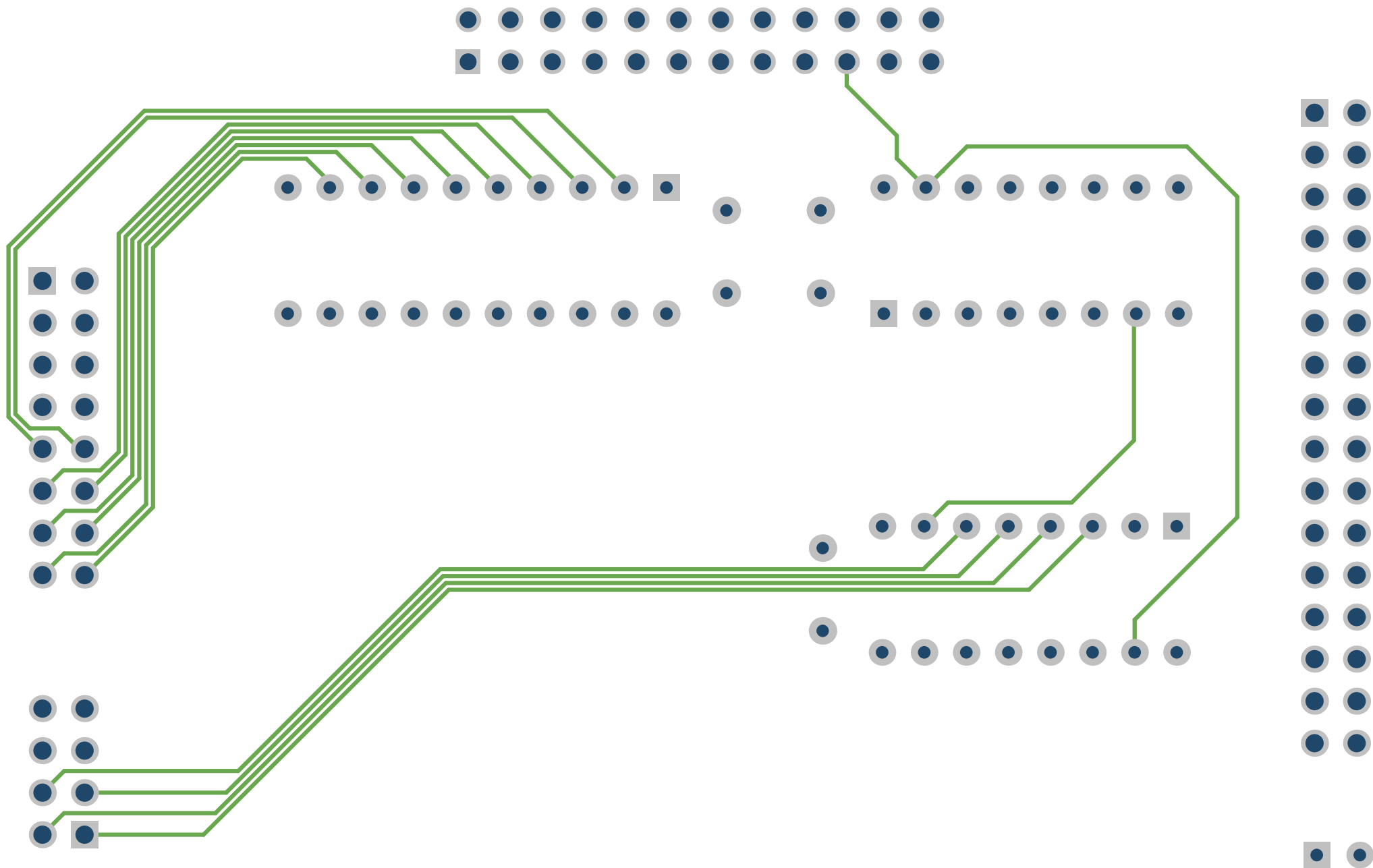
**Project:** myCPU Instruction Register 4+4 bit R

**Revision:** 11

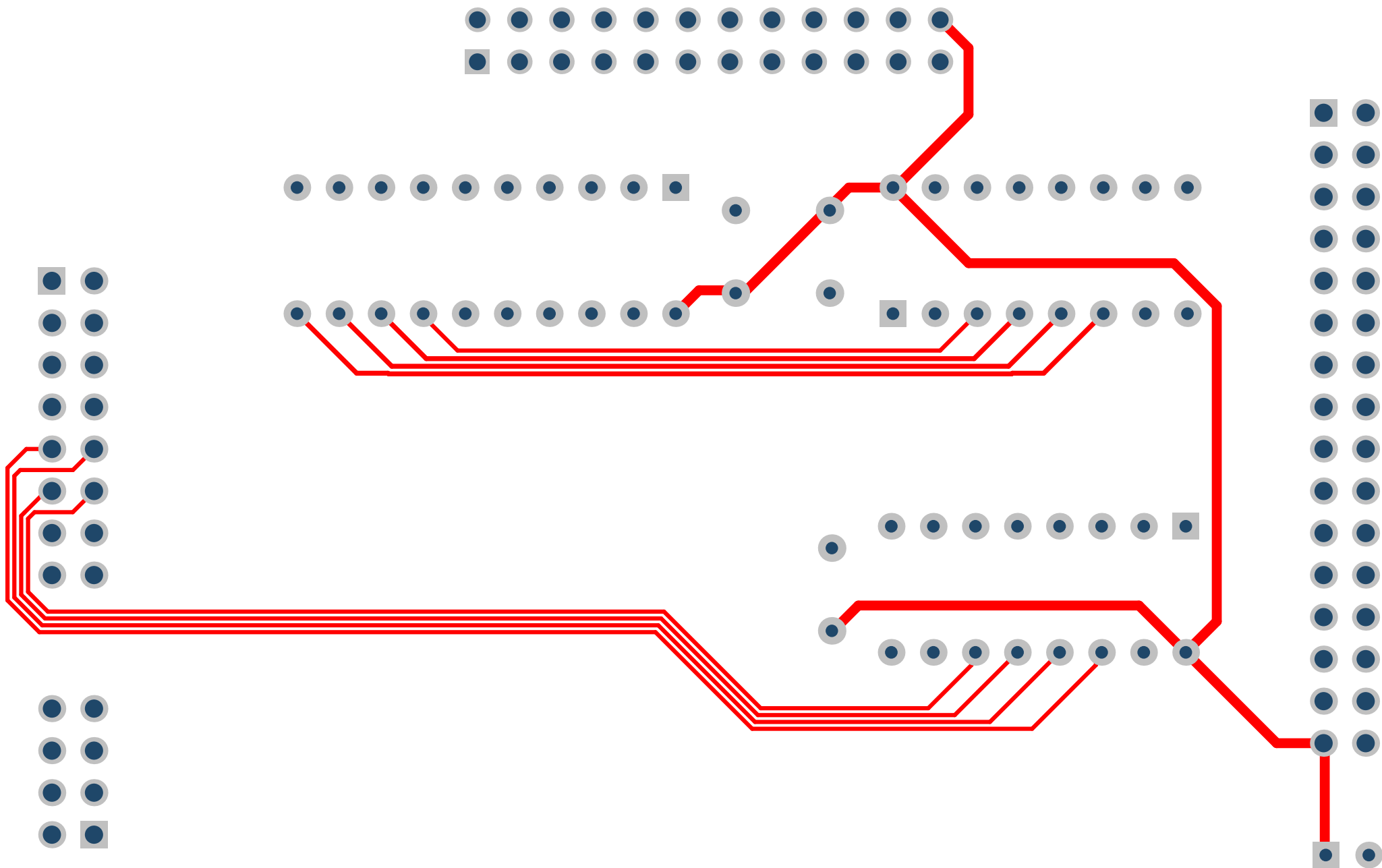
**Date:** 15-Jul-24

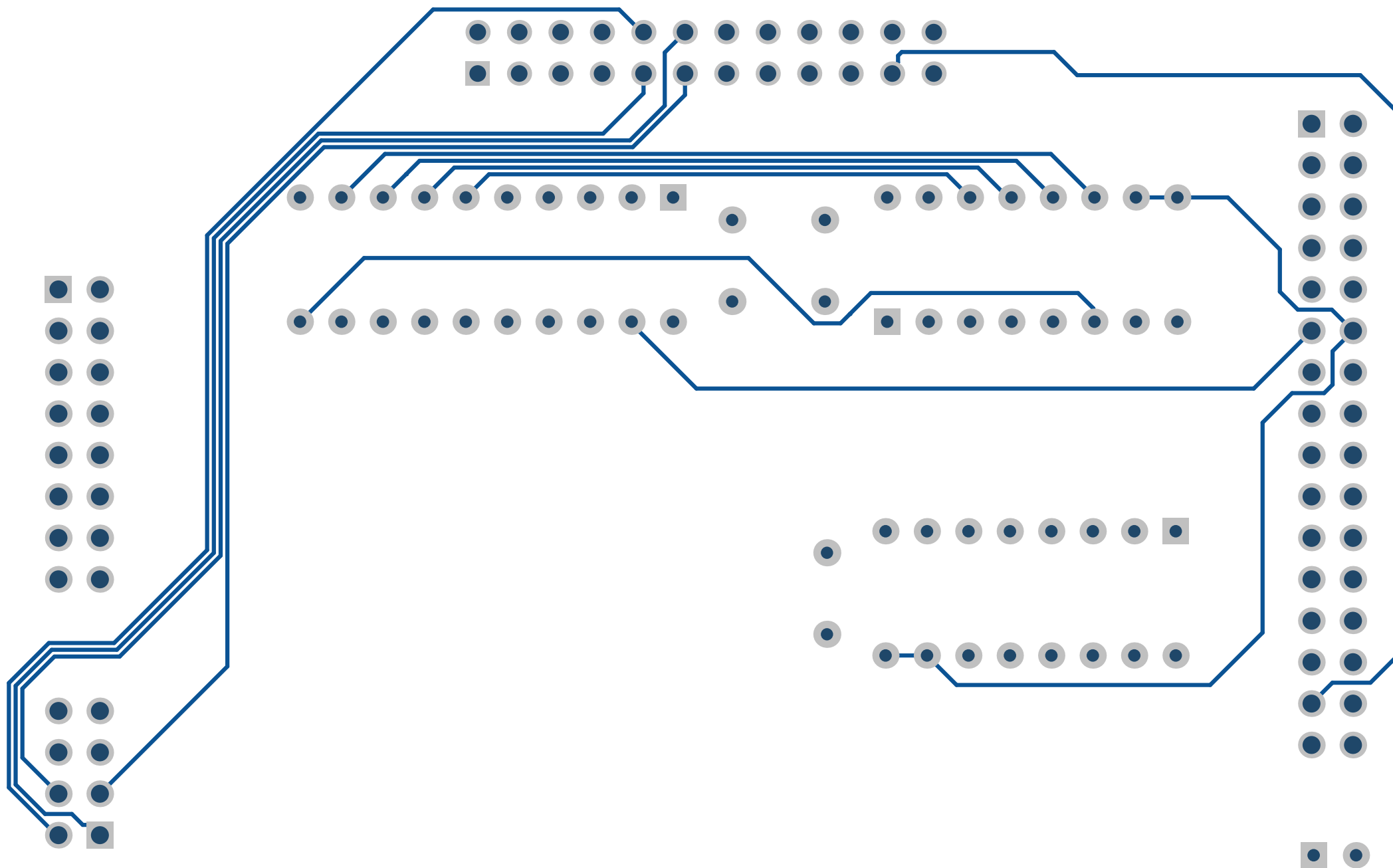
**Author:** Rafa Hernández















# Bill of Materials

## myCPU Instruction Register 4+4 bit

Description	Value	Q
Electrolytic capacitor 16v/50v	10µF	1
Ceramic capacitor	100nF	3
Non inverting bus transceiver	74xx245	1
4-bit D-Type Register with 3 state outputs	74xx173	2
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p	1
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p	1
Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p	1
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	8p	1



# Assembly List

## myCPU Instruction Register 4+4 bit

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10 $\mu$ F
C3	Ceramic capacitor	100nF
C4	Ceramic capacitor	100nF
C5	Ceramic capacitor	100nF
IC1	Non inverting bus transceiver	74xx245
IC2	4-bit D-Type Register with 3 state outputs	74xx173
IC3	4-bit D-Type Register with 3 state outputs	74xx173
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	8p