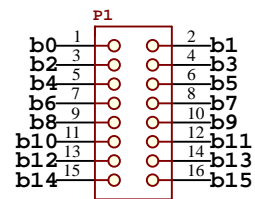
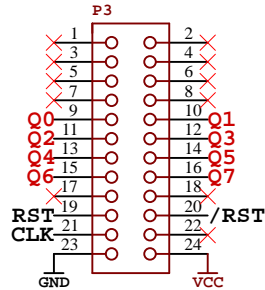
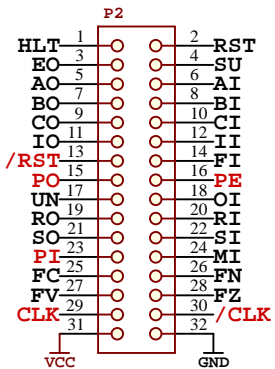
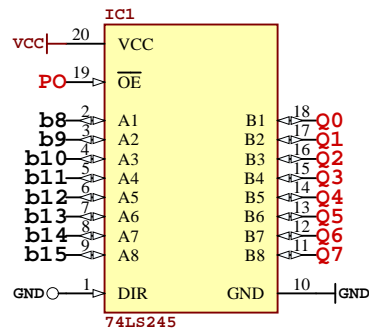




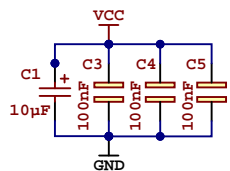
# Control BUS Connector OUTPUT Connector Data BUS Connector



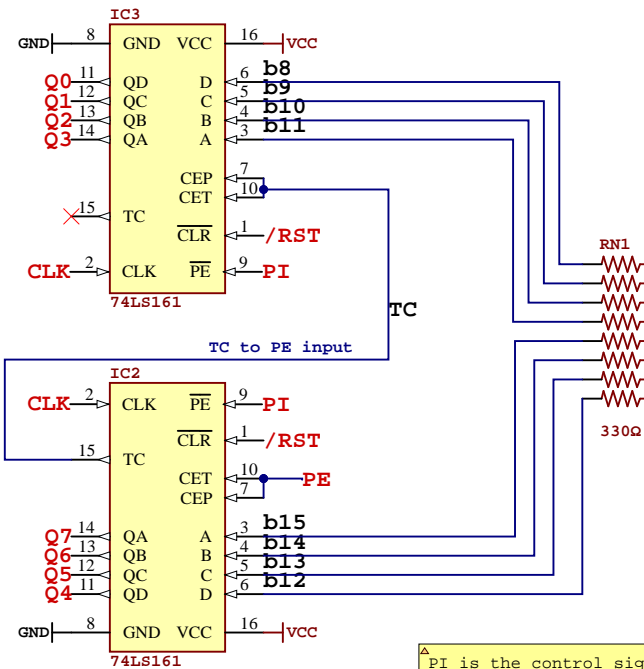
Counts operation goes from QA to QD, A is less significative bit.



Pin DIR to GND means data flow from B >> A when a low PO signal comes.



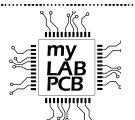
Decoupling Capacitors



\*\*PE signal is not related to /PE pin

Cascade goes from IC2 to IC3 through pin TC (Terminal Count Output) to pin CET/CEP (10) forcing a count step.

PI is the control signal to load the current value from the DATABUS to the counters.

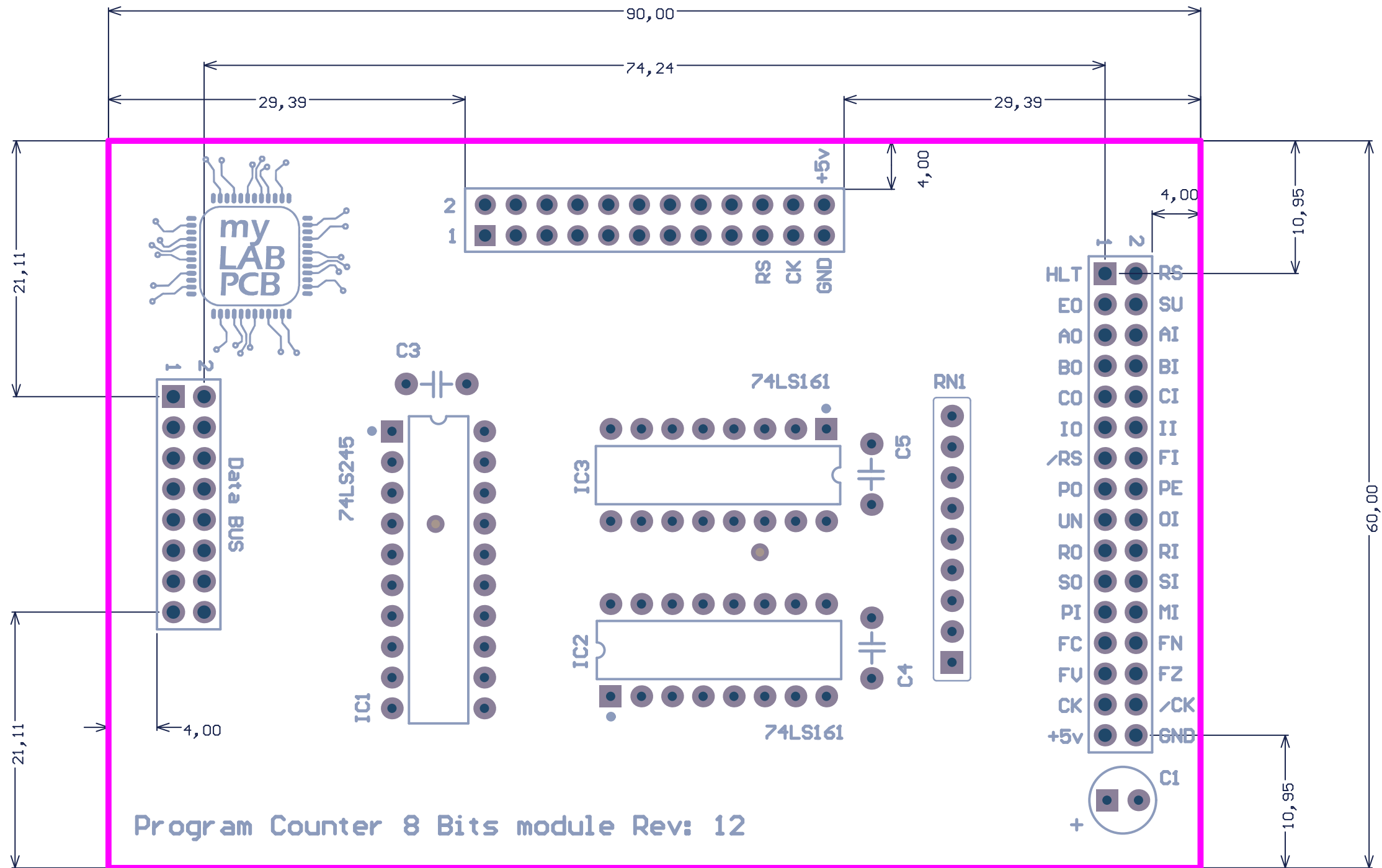


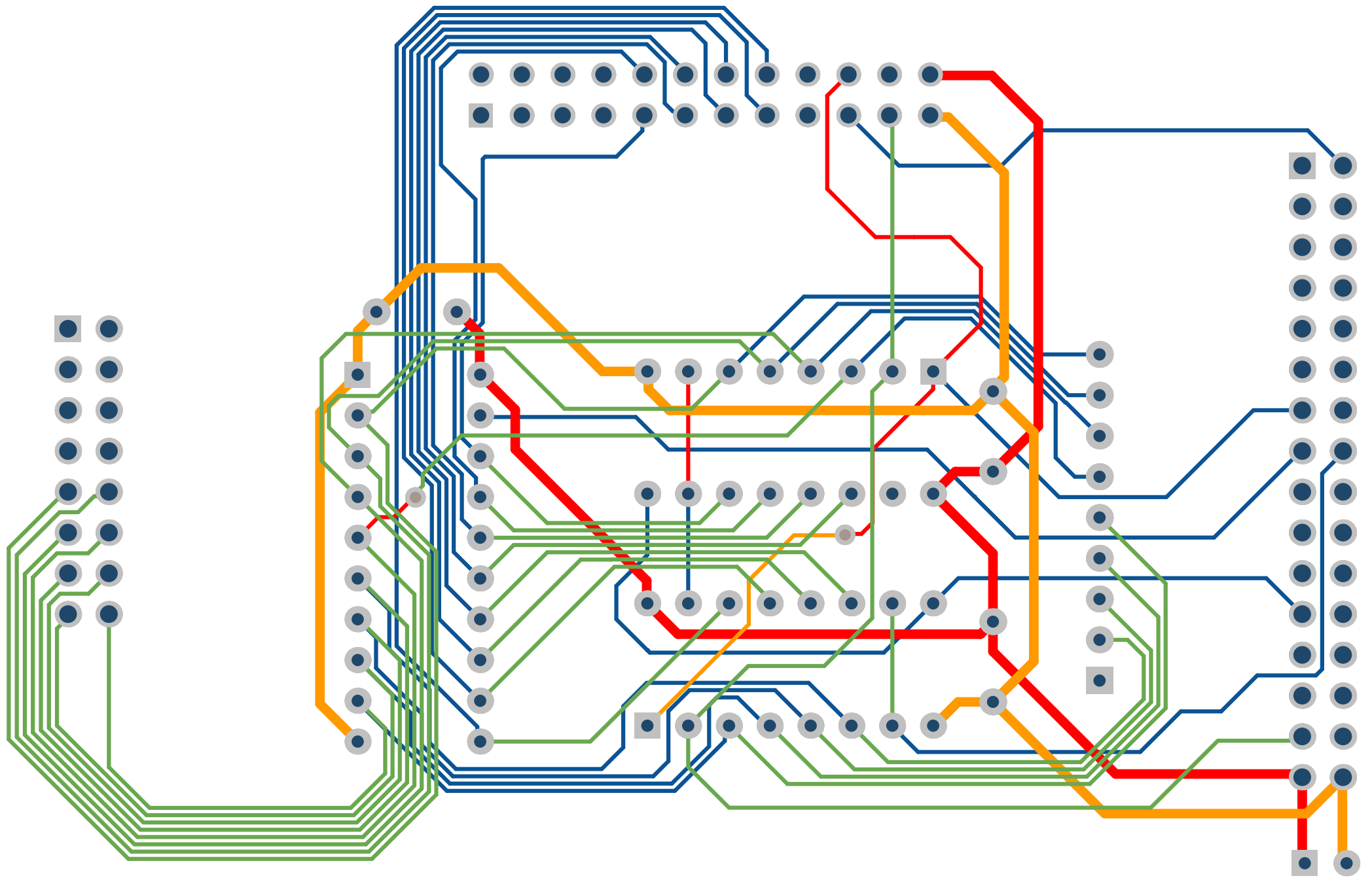
Project: myCPU Program Counter module

Revision: 12

Date: 31/5/2022

Author: Rafa Hernández









# Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10 $\mu$ F	1
C3, C4, C5	Ceramic or tantalum capacitor	100nF	3
IC1	Non inverting bus transceiver	74LS245	1
IC2, IC3	4-Bit sync counter	74LS161	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p	1
RN1	Resistor array 8 elements,9 pins	330 $\Omega$	1



# Assembly List

Desig.	Description	Value
C1	Electrolytic capacitor 16v/50v	10 $\mu$ F
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC2	4-Bit sync counter	74LS161
IC3	4-Bit sync counter	74LS161
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p
RN1	Resistor array 8 elements,9 pins	330 $\Omega$