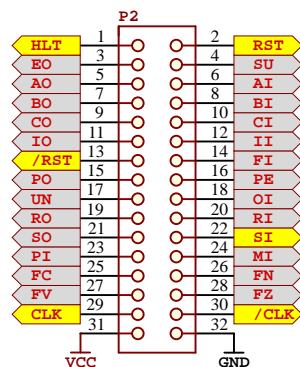
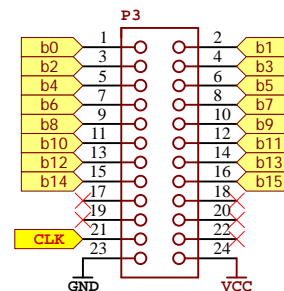




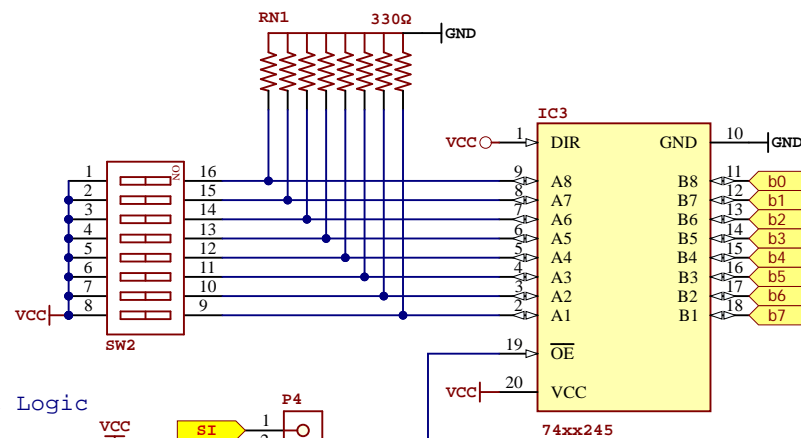
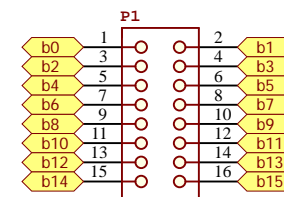
## Control BUS Connector



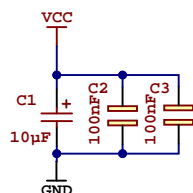
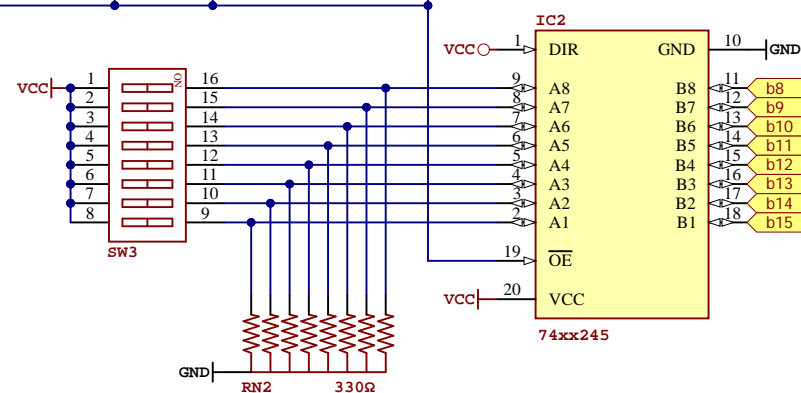
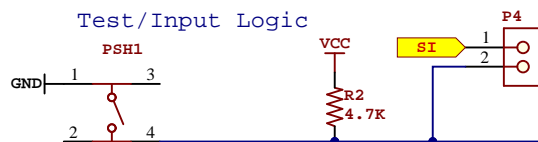
## OUTPUT Connector



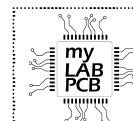
## Data BUS Connector



## Test/Input Logic



## Decoupling Capacitors

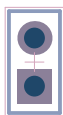
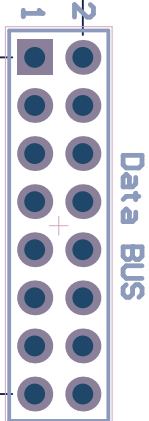
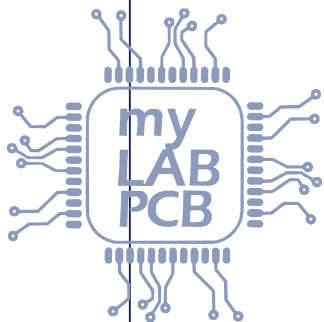


**Project:** myCPU BUS Manager

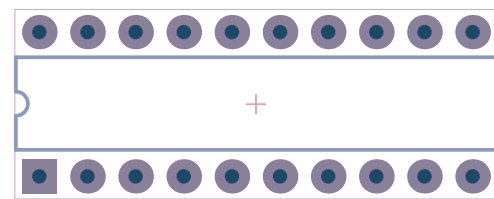
**Revision:** 9

**Date:** 20-Jun-24

**Author:** Rafa Hernández



ENABLE INPUT

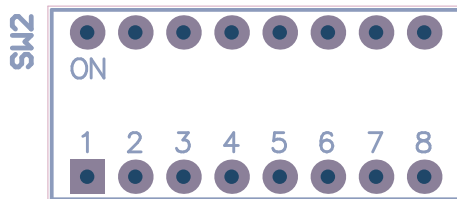


IC3

74xx245

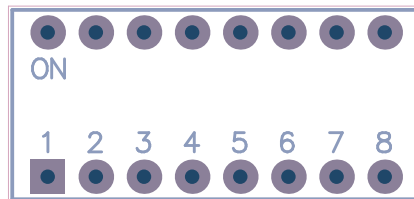


RN1



SW2

ON

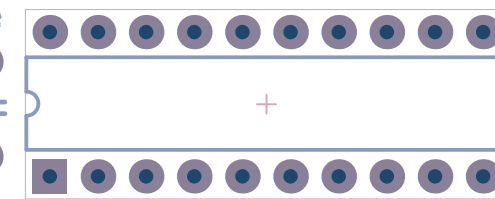


SW3

ON



TEST SWITCHES



IC2

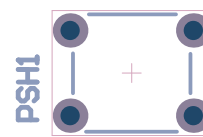
74xx245



RN2



R2

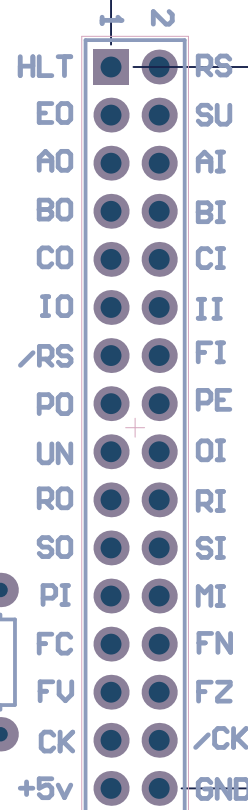


PSH1

TEST



C1



HLT

EO

AO

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II

FI

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/CK

GND

RS

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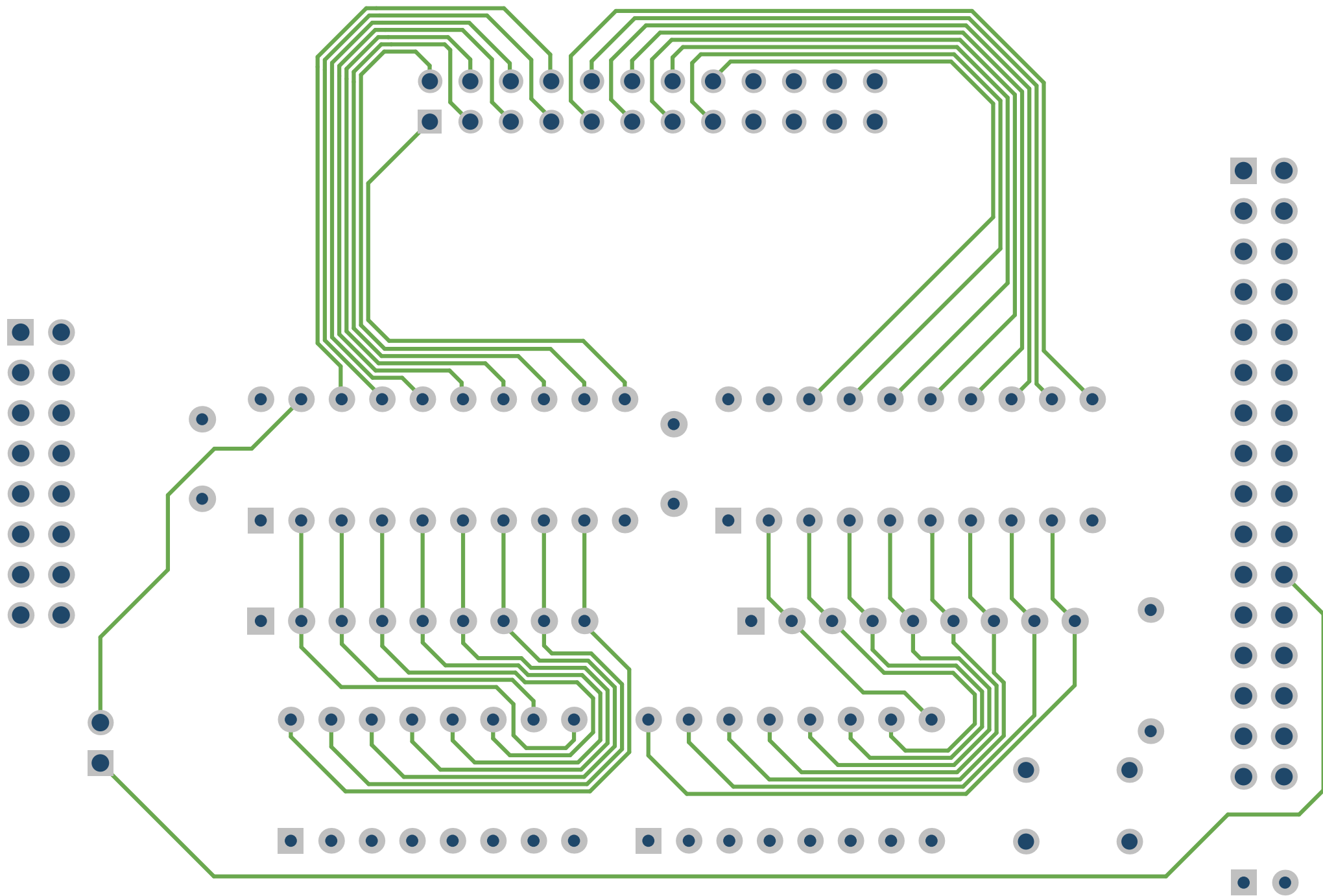
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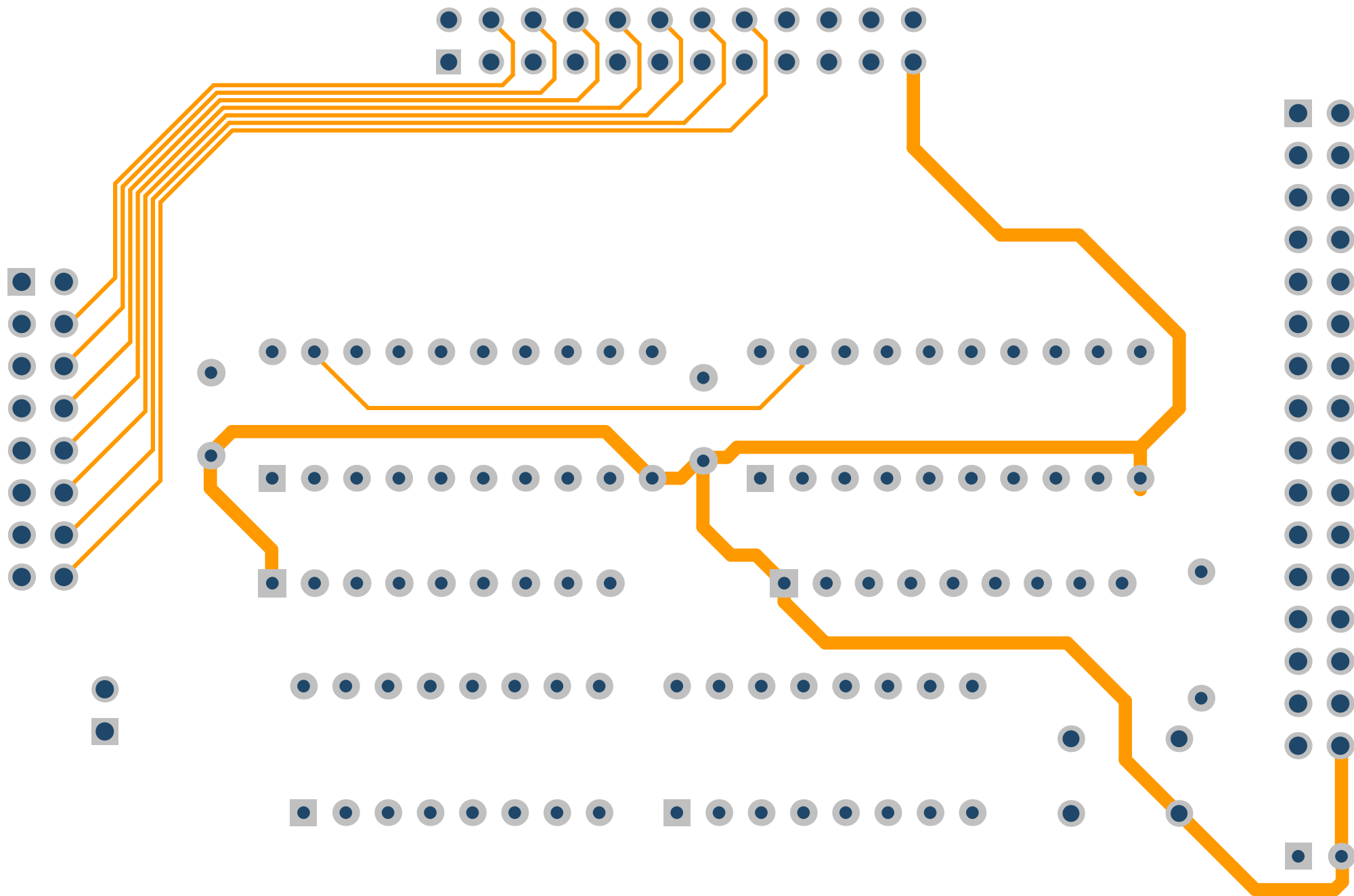
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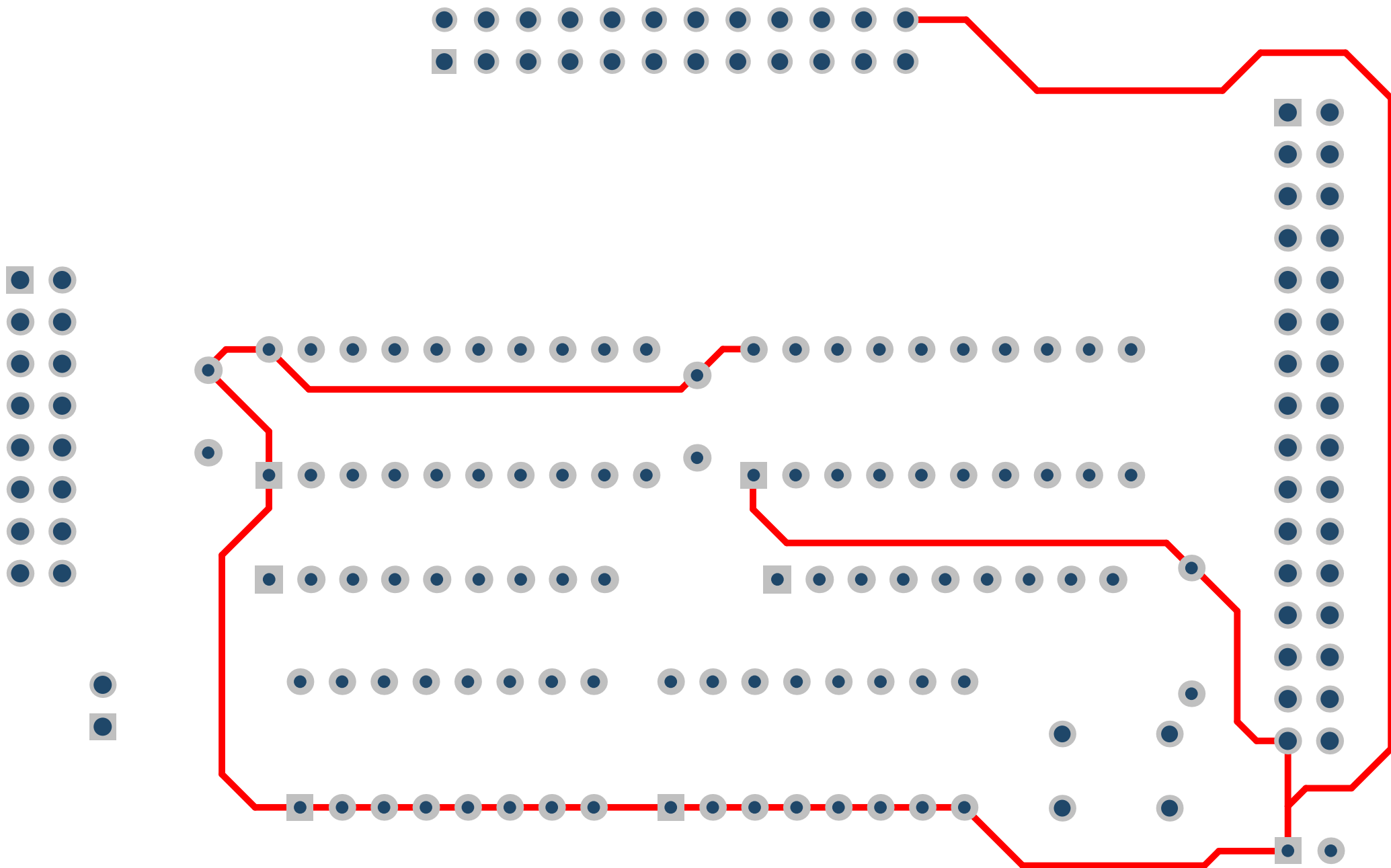
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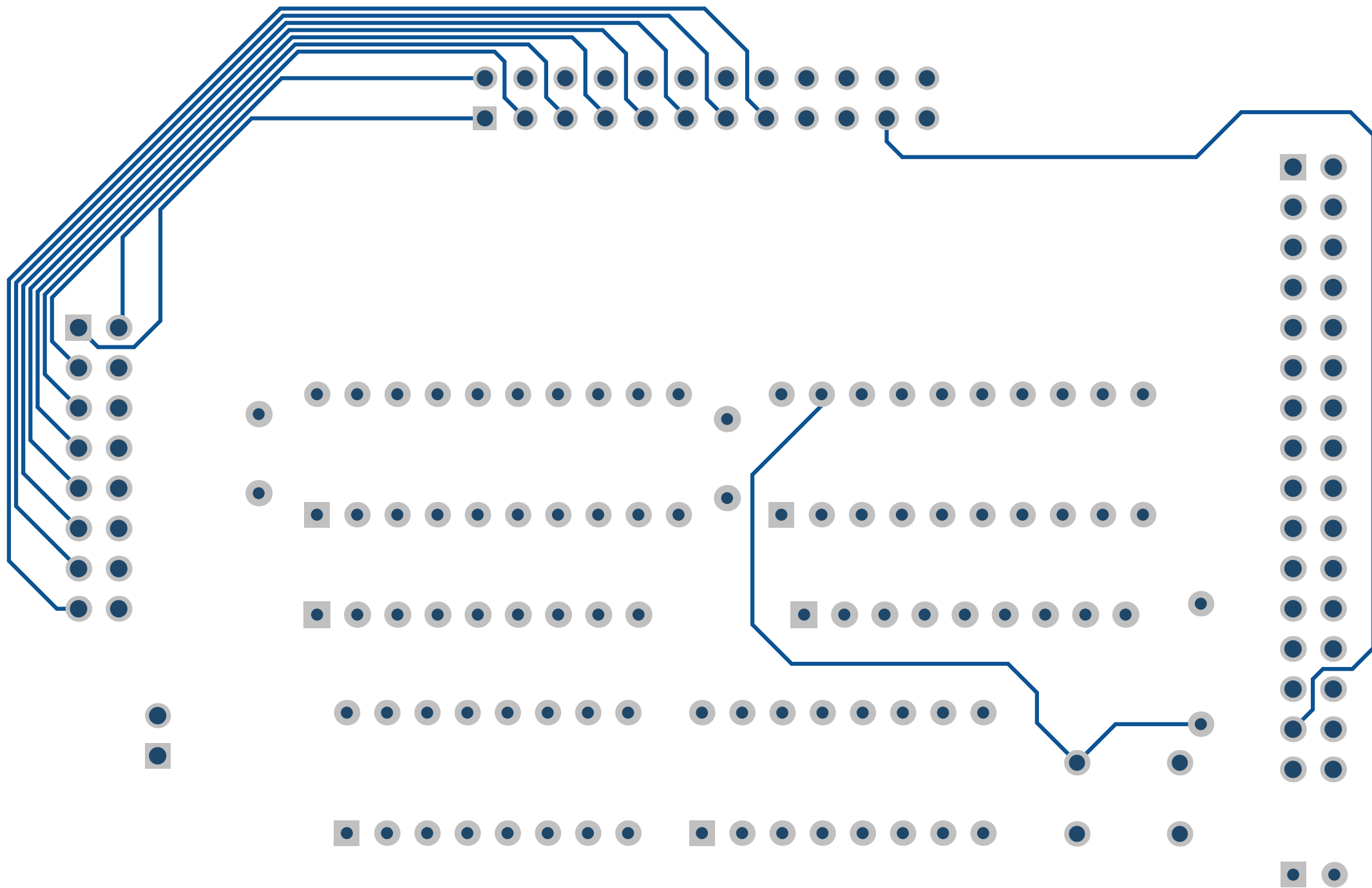
BI

CI













# Bill of Materials

## myCPU BUS Manager

Description	Value	Q
Electrolytic capacitor 16v/50v	10 $\mu$ F	1
Ceramic capacitor	100nF	2
Non inverting bus transceiver	74xx245	2
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p	1
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p	1
Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p	1
Pin Header, THT, pitch 2.54mm, Single Row, Vertical	2p	1
Tactile button 6 mm	6mm	1
Resistor Axial	4.7K	1
Resistor array 8 elements,9 pins	330	2
DIP switch 8 positions	8p	2



# Assembly List

## myCPU BUS Manager

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10 $\mu$ F
C2	Ceramic capacitor	100nF
C3	Ceramic capacitor	100nF
IC2	Non inverting bus transceiver	74xx245
IC3	Non inverting bus transceiver	74xx245
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p
P4	Pin Header, THT, pitch 2.54mm, Single Row, Vertical	2p
PSH1	Tactile button 6 mm	6mm
R2	Resistor Axial	4.7K
RN1	Resistor array 8 elements,9 pins	330
RN2	Resistor array 8 elements,9 pins	330
SW2	DIP switch 8 positions	8p
SW3	DIP switch 8 positions	8p