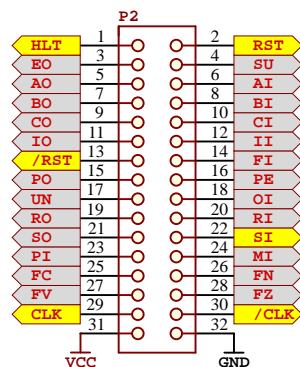
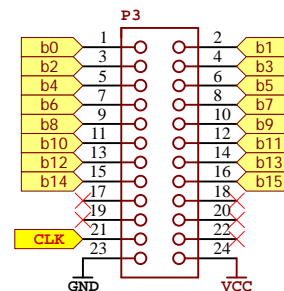


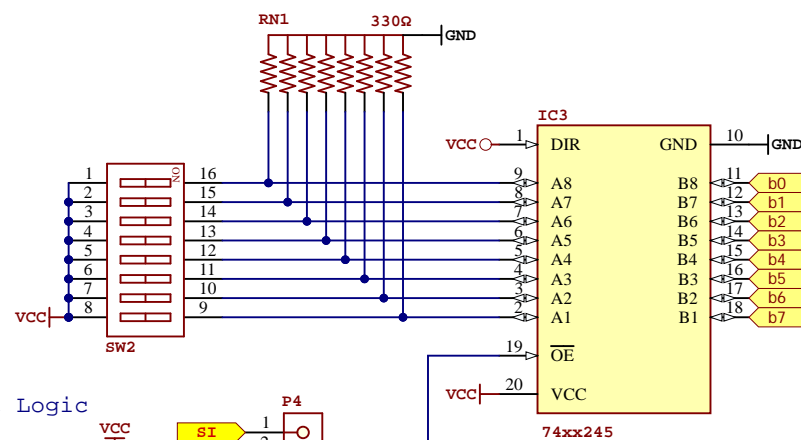
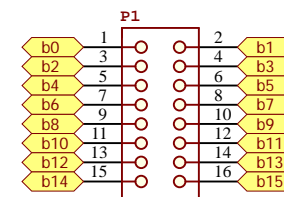
Control BUS Connector



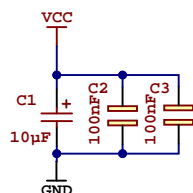
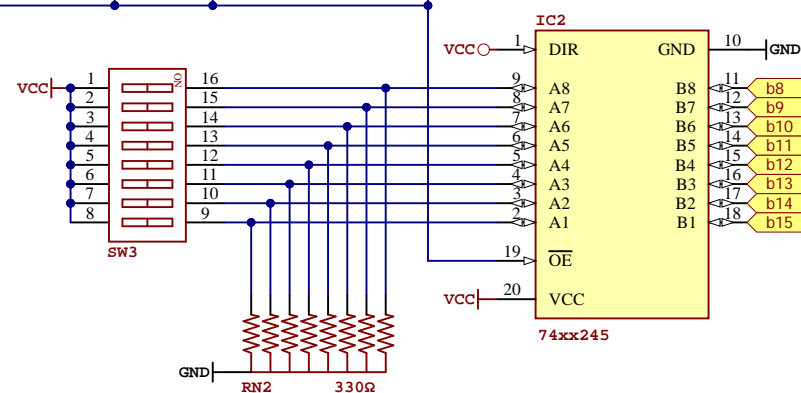
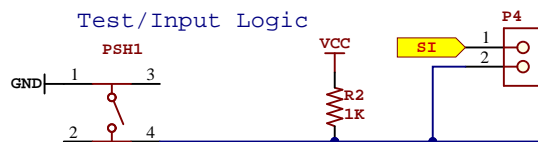
OUTPUT Connector



Data BUS Connector

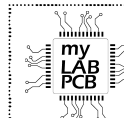


Test/Input Logic



Decoupling Capacitors

"74xx" Indicates the use LS (TTL) or HC(CMOS) ICs as your prefer for your build.

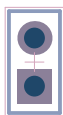
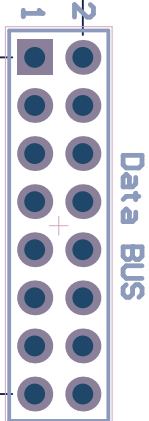
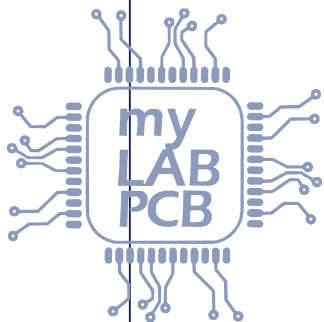


Project: myCPU BUS Manager

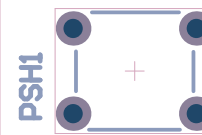
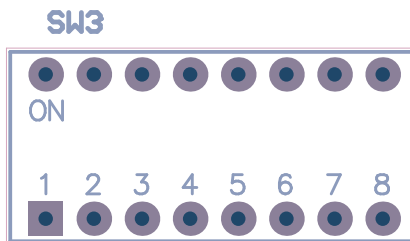
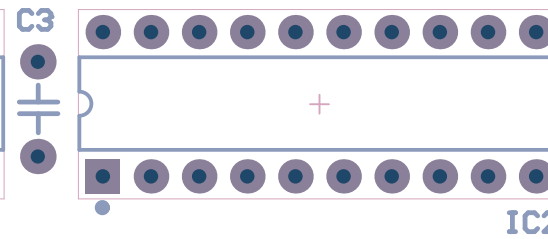
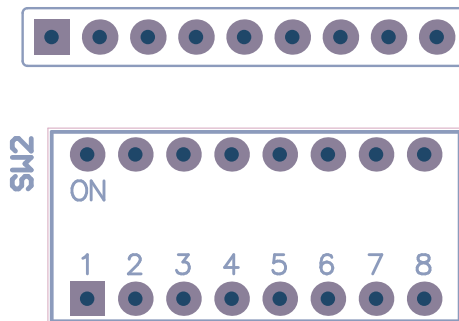
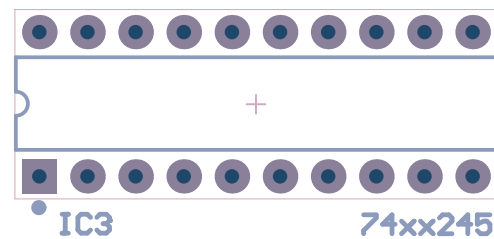
Revision: 9

Date: 06-Feb-24

Author: Rafa Hernández

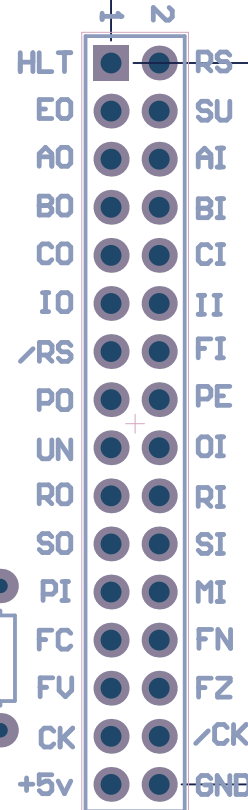


ENABLE INPUT



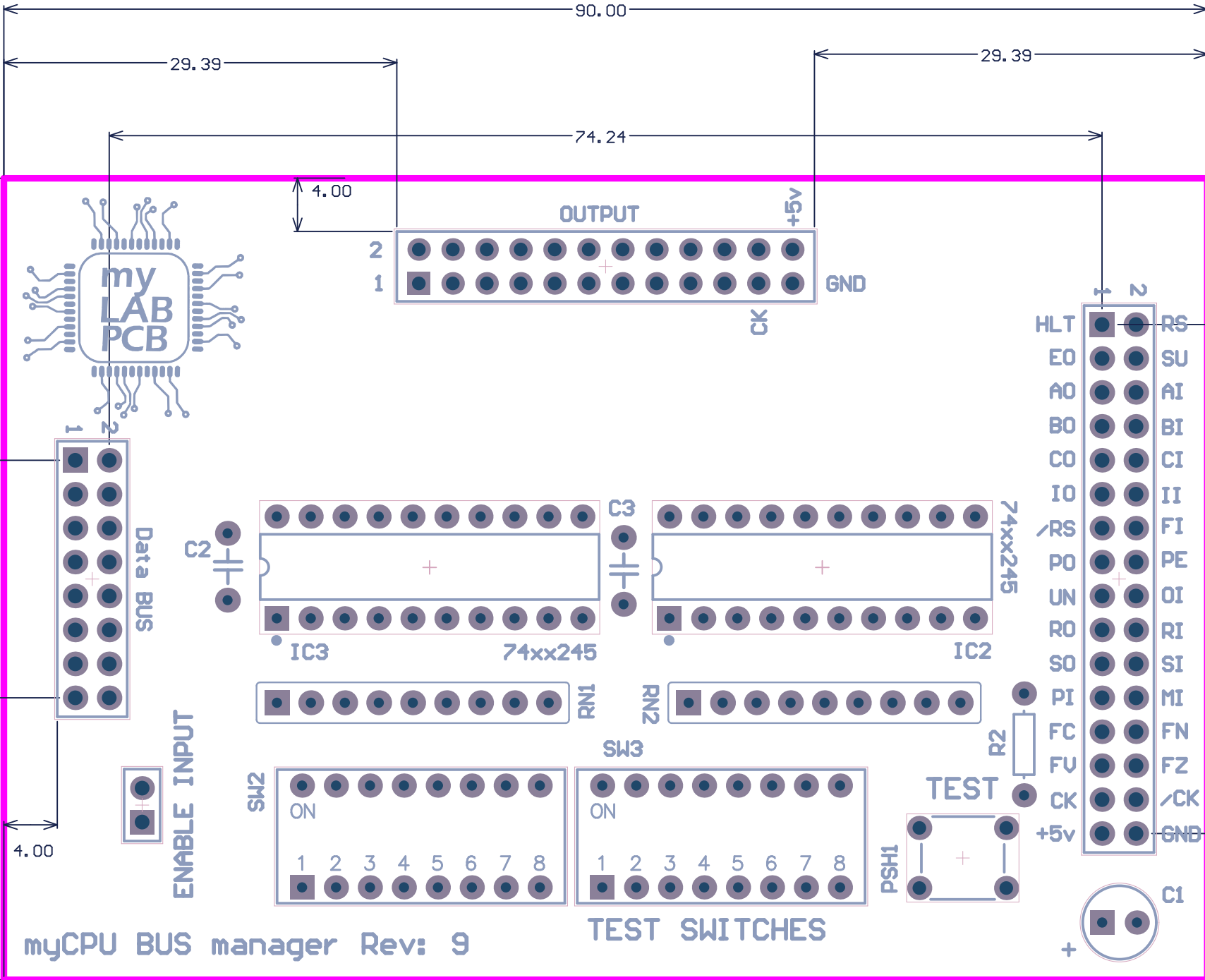
74xx245

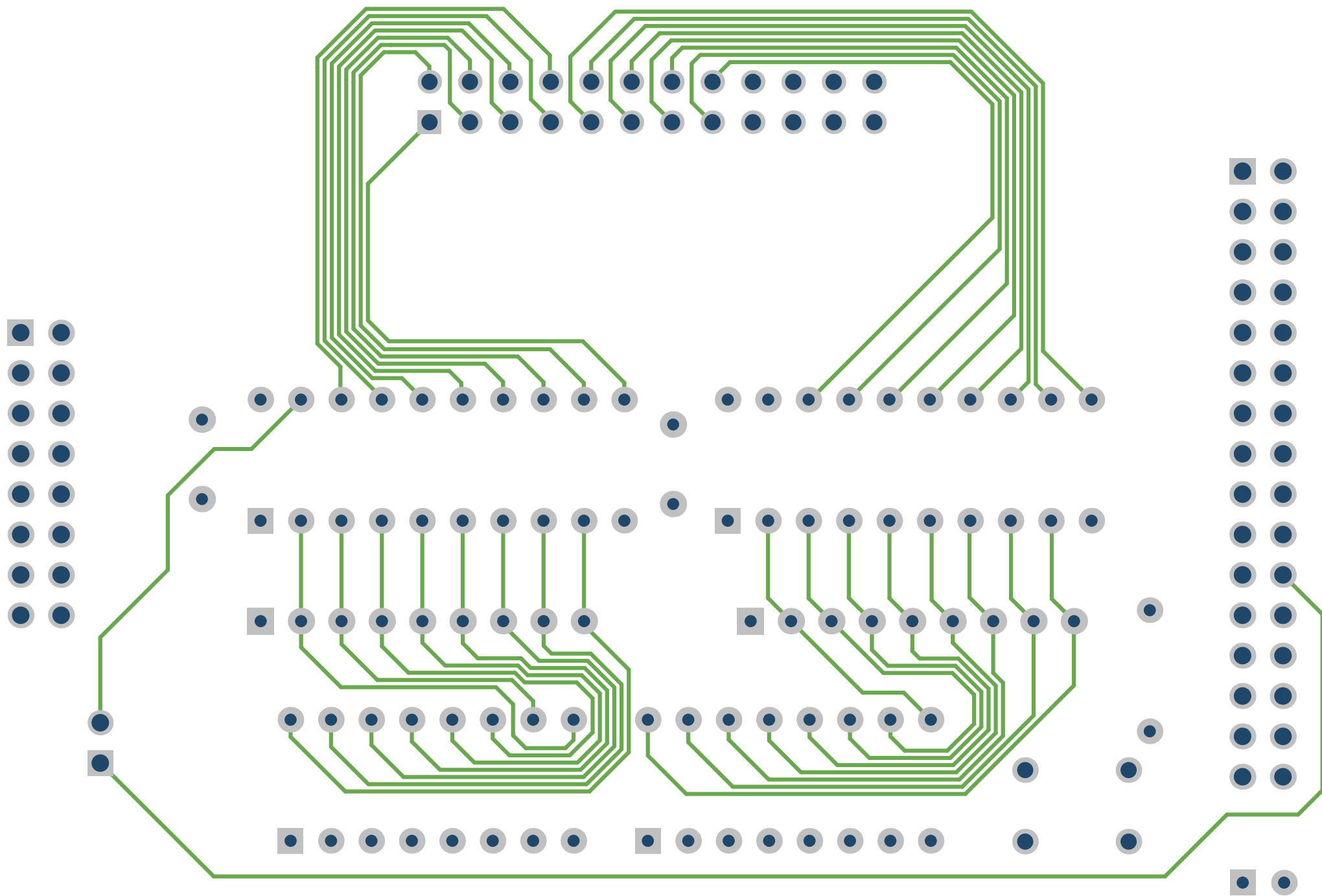
R2

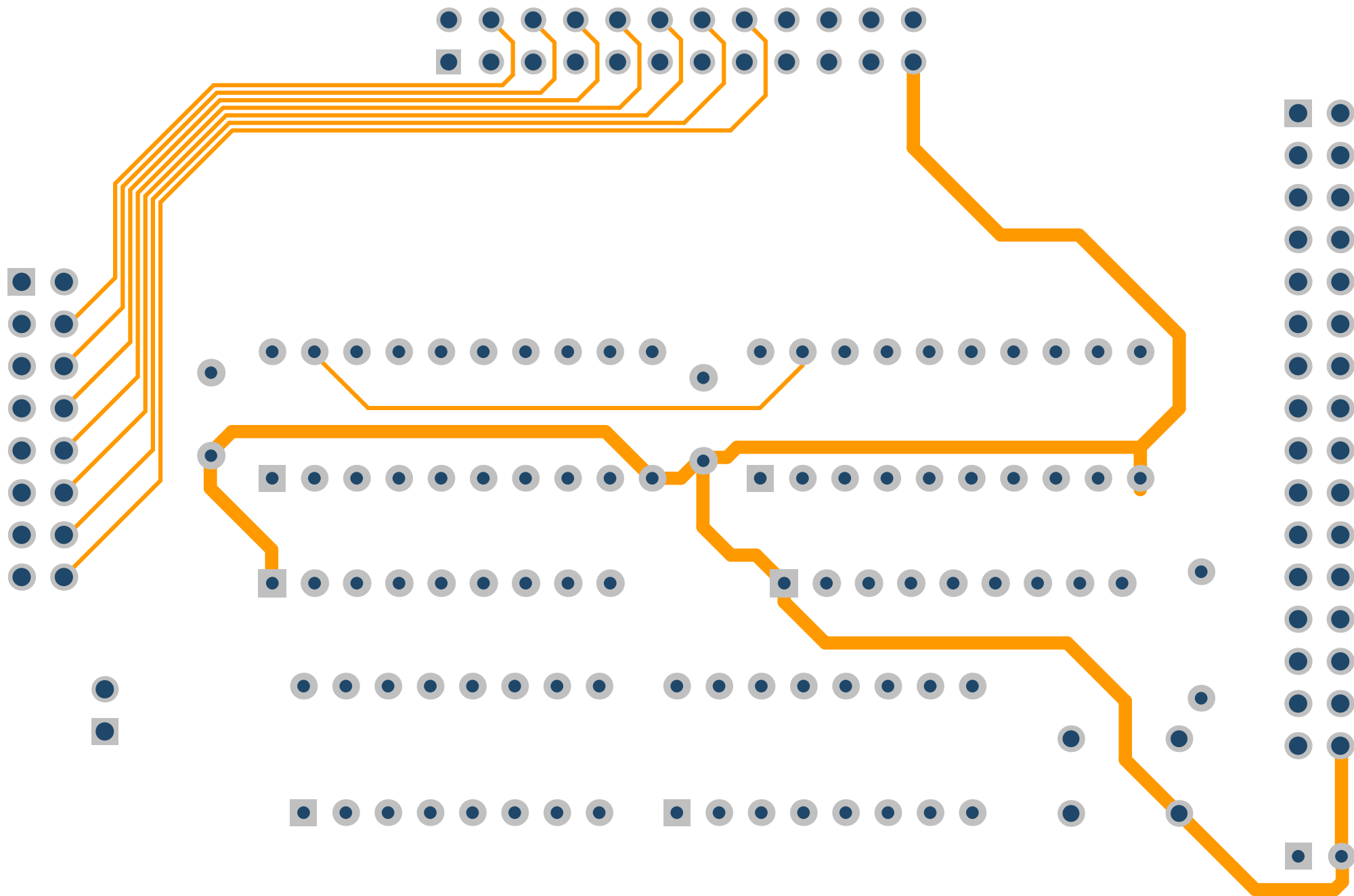


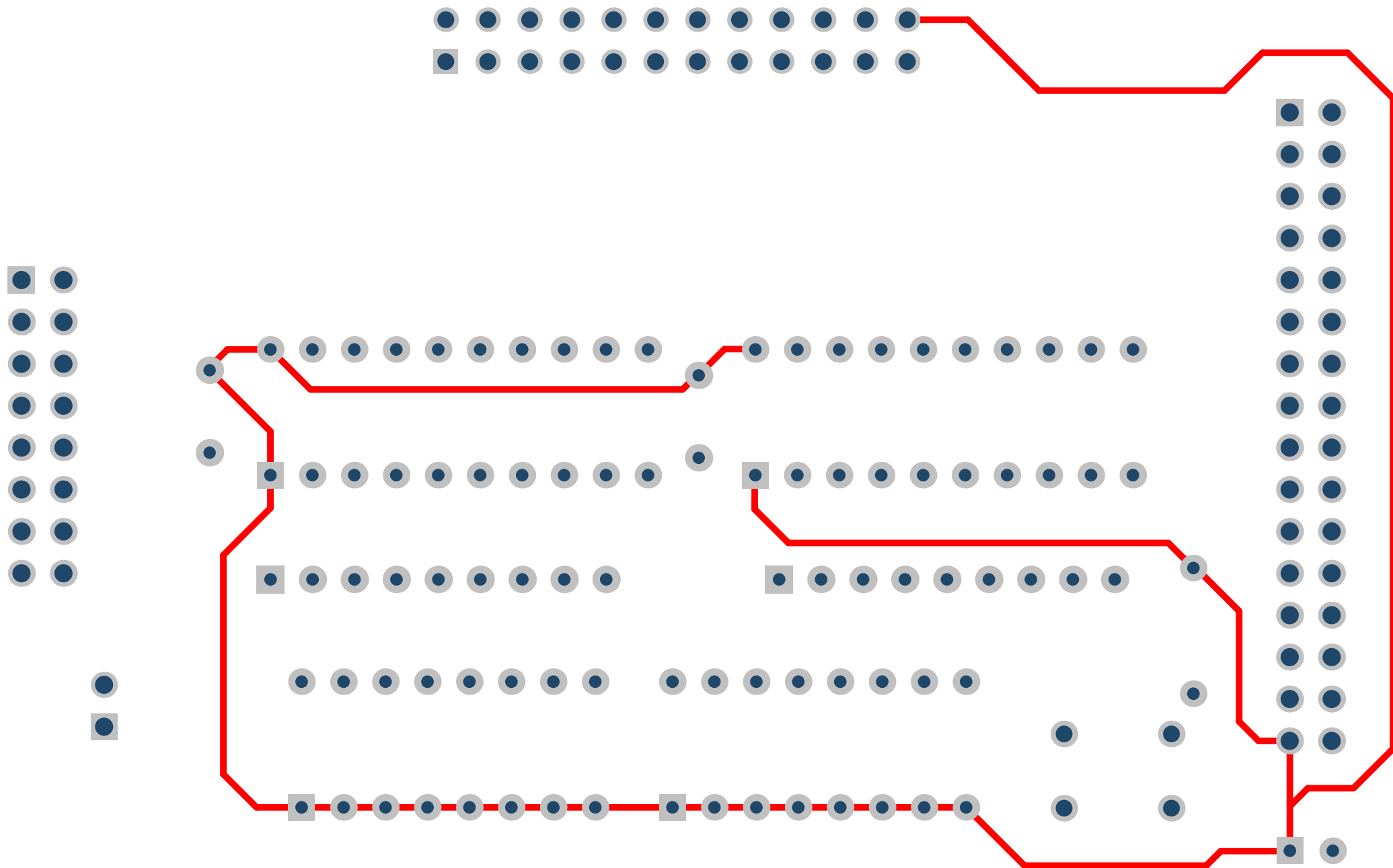
myCPU BUS manager Rev: 9

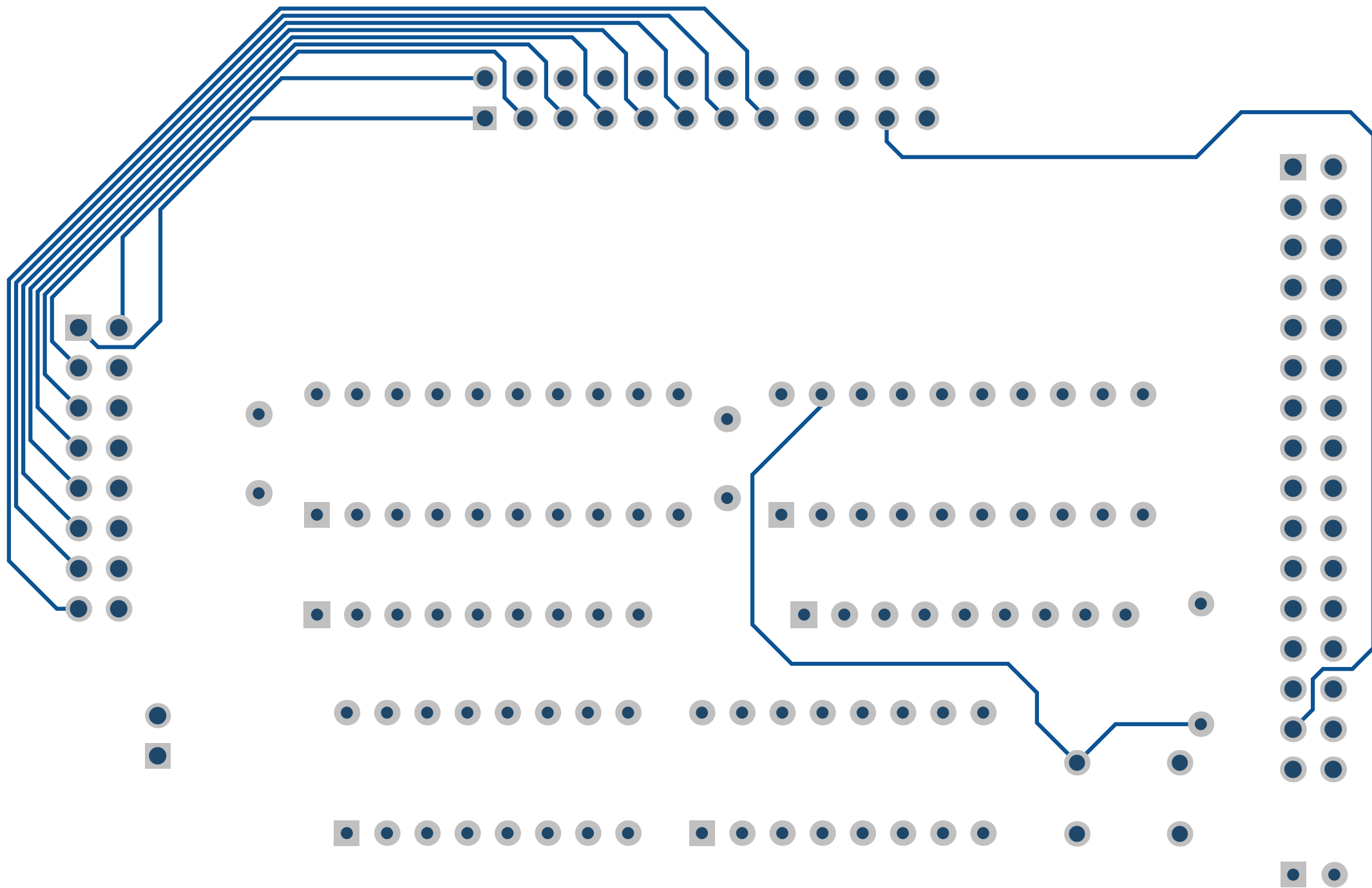
TEST SWITCHES













Bill of Materials

myCPU BUS Manager

Description	Value	Q
Electrolytic capacitor 16v/50v	10 μ F	1
Ceramic or tantalum capacitor	100nF	2
Non inverting bus transceiver	74xx245	2
Pin Header, pitch 2.54mm, Dual Row, Vertical	16p	1
Pin Header, pitch 2.54mm, Dual Row, Vertical	32p	1
Socket Header, pitch 2.54mm, Dual Row, Vertical	24p	1
Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 2p	2p	1
Tactile button 6 mm	6mm	1
Resistor Axial	1K	1
Resistor array 8 elements,9 pins	330 Ω	2
DIP switch 8 positions	8p	2



Assembly List

myCPU BUS Manager

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10 μ F
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
IC2	Non inverting bus transceiver	74xx245
IC3	Non inverting bus transceiver	74xx245
P1	Pin Header, pitch 2.54mm, Dual Row, Vertical	16p
P2	Pin Header, pitch 2.54mm, Dual Row, Vertical	32p
P3	Socket Header, pitch 2.54mm, Dual Row, Vertical	24p
P4	Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 2p	2p
PSH1	Tactile button 6 mm	6mm
R2	Resistor Axial	1K
RN1	Resistor array 8 elements,9 pins	330 Ω
RN2	Resistor array 8 elements,9 pins	330 Ω
SW2	DIP switch 8 positions	8p
SW3	DIP switch 8 positions	8p