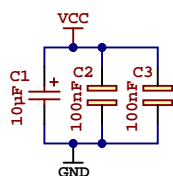
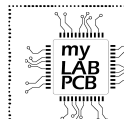


△ G1, G2 input control.  
Set both to LOW to load  
all bit on inputs into  
flip-flops



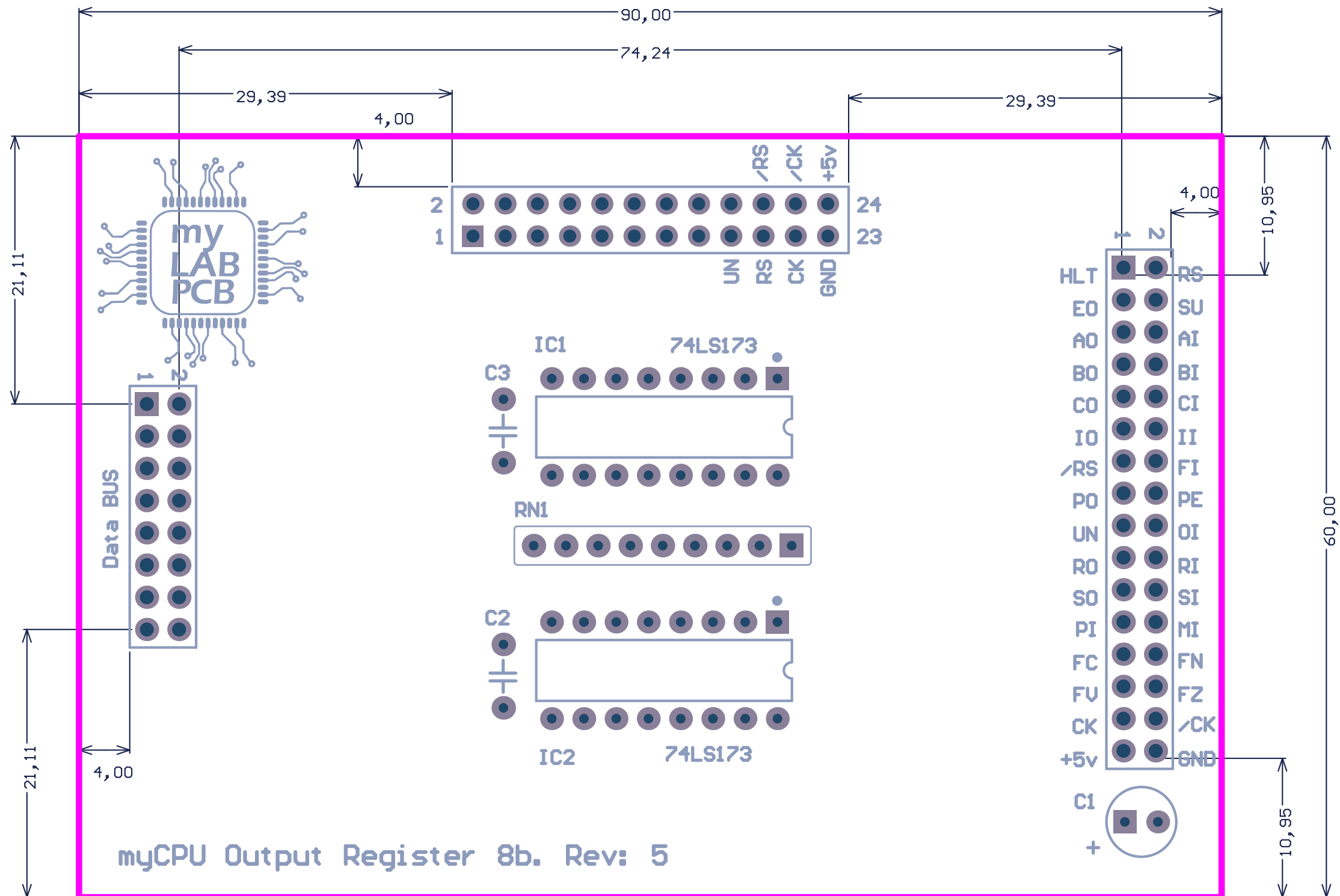
## Decoupling Capacitors

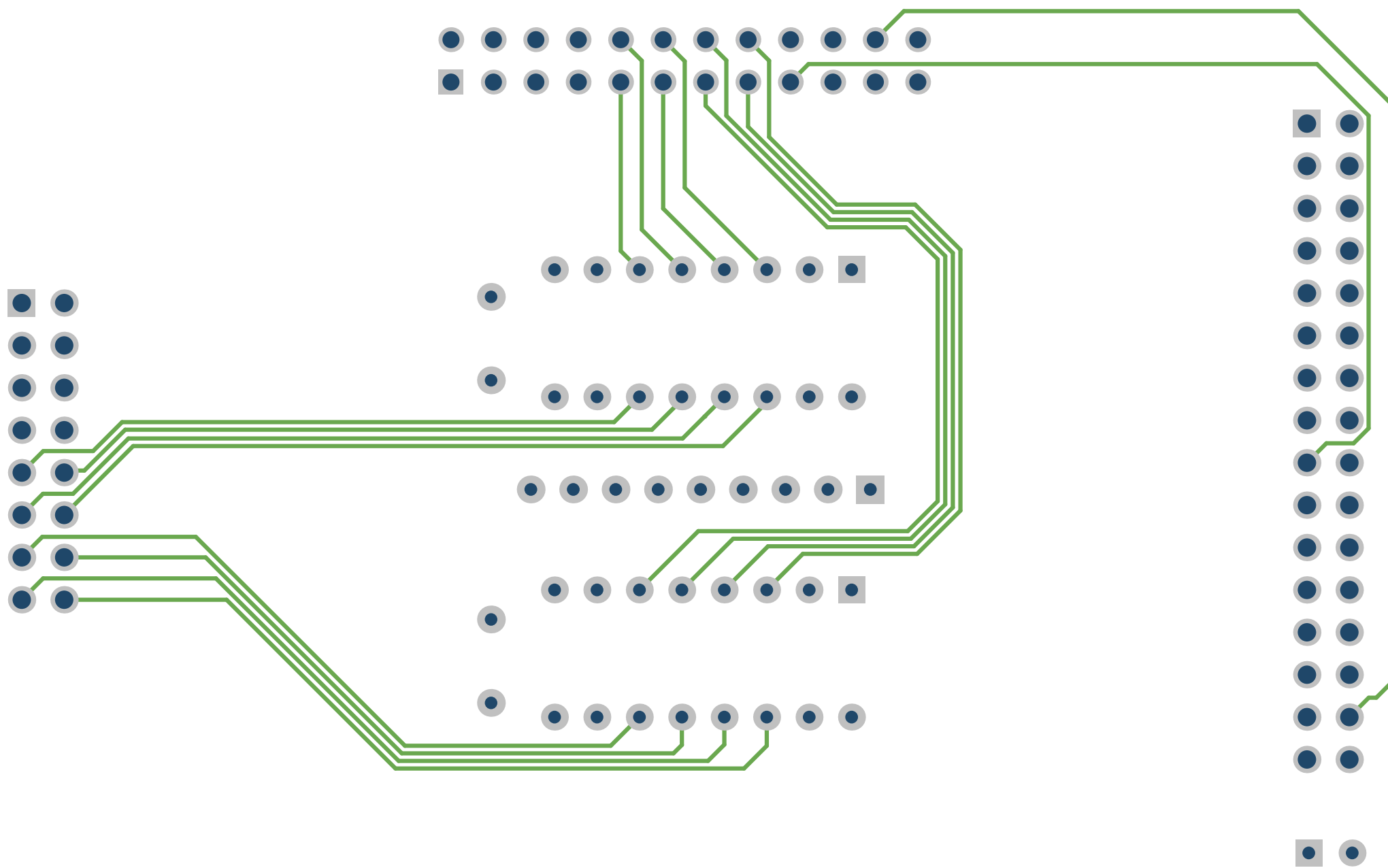


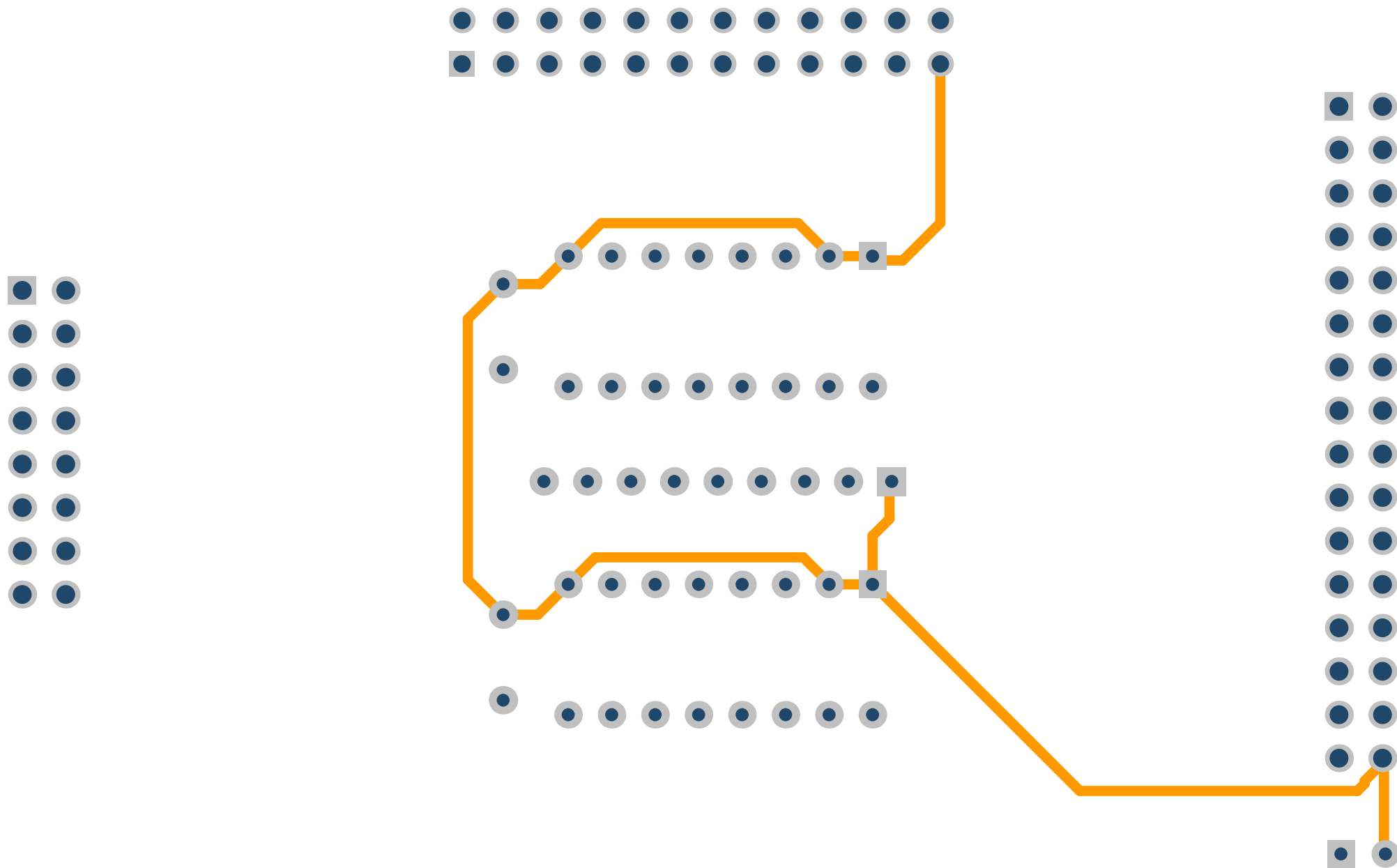
**Project:** myCPU Output Register 8 bit

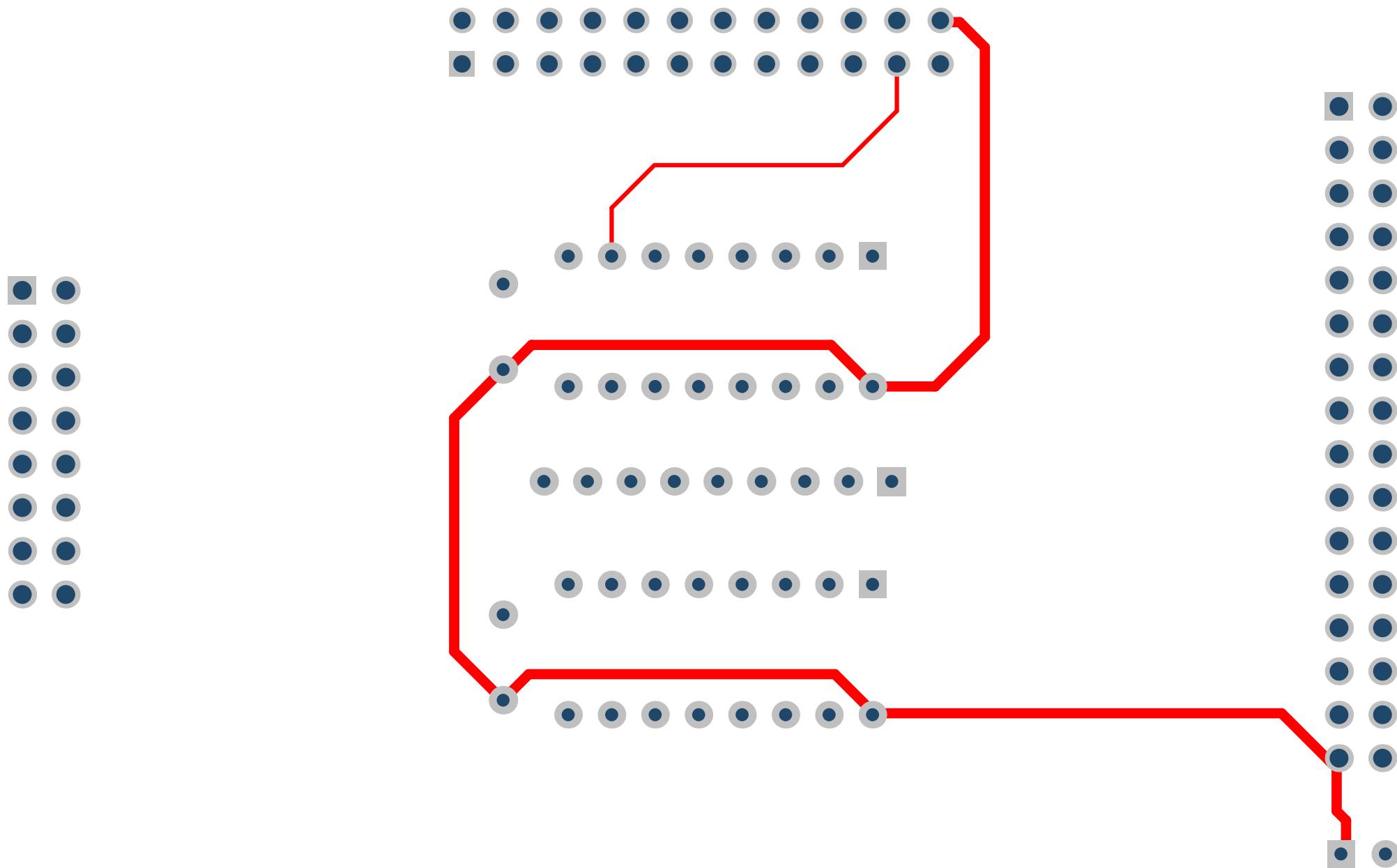
Date: 10/01/2023

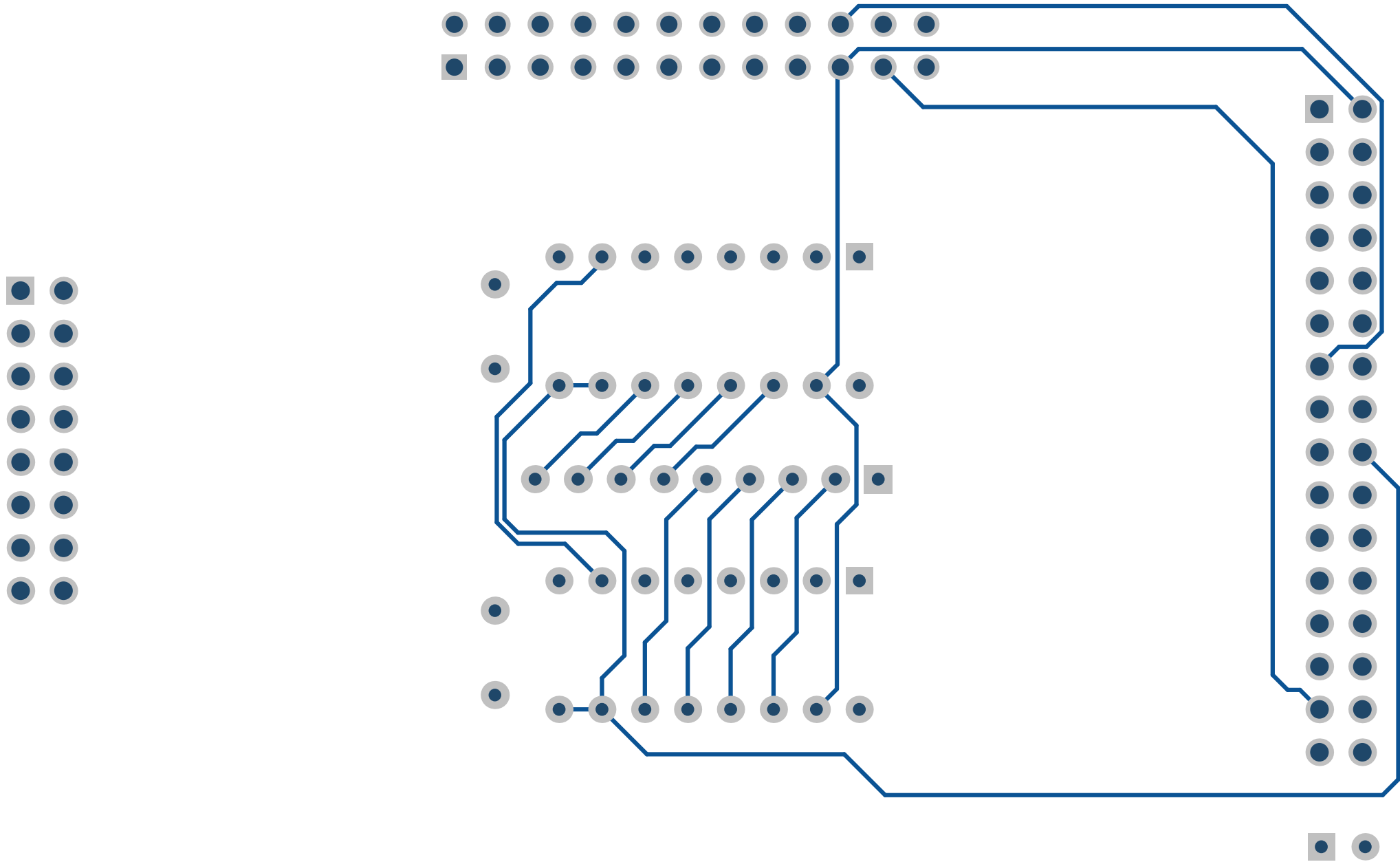
**Author:** Rafa Hernández



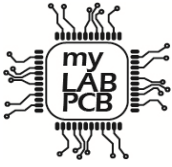












# Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10μF	1
C2, C3	Ceramic or tantalum capacitor	100nF	2
IC1, IC2	4-bit D-Type Register with 3 state outputs	74LS173	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical,	24p	1
RN1	Resistor array 8 elements,9 pins	1K	1



# Assembly List

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10 $\mu$ F
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
IC1	4-bit D-Type Register with 3 state outputs	74LS173
IC2	4-bit D-Type Register with 3 state outputs	74LS173
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
RN1	Resistor array 8 elements, 9 pins	1K