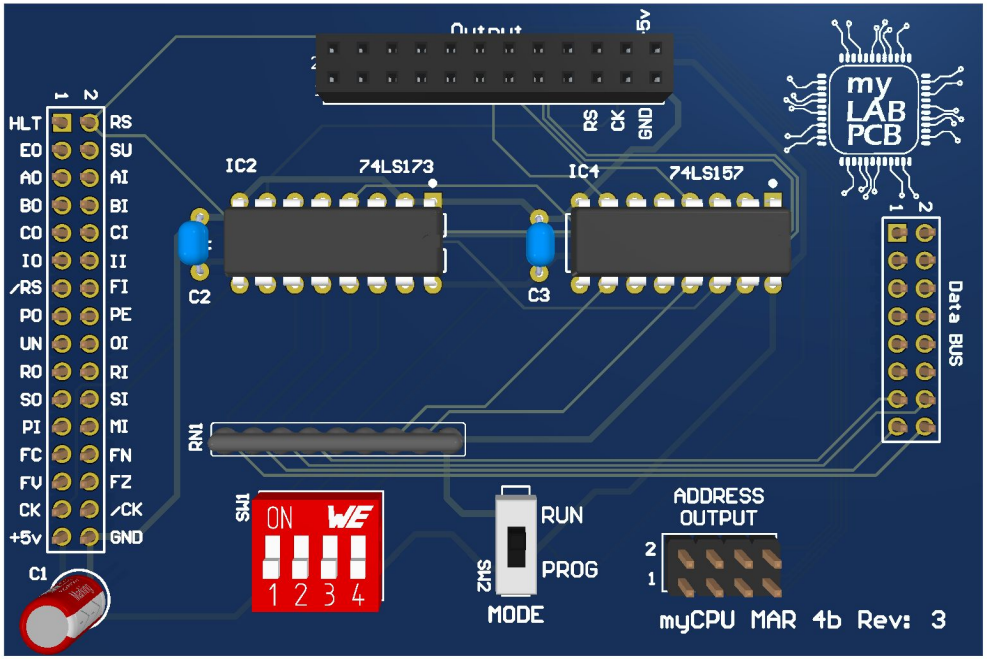
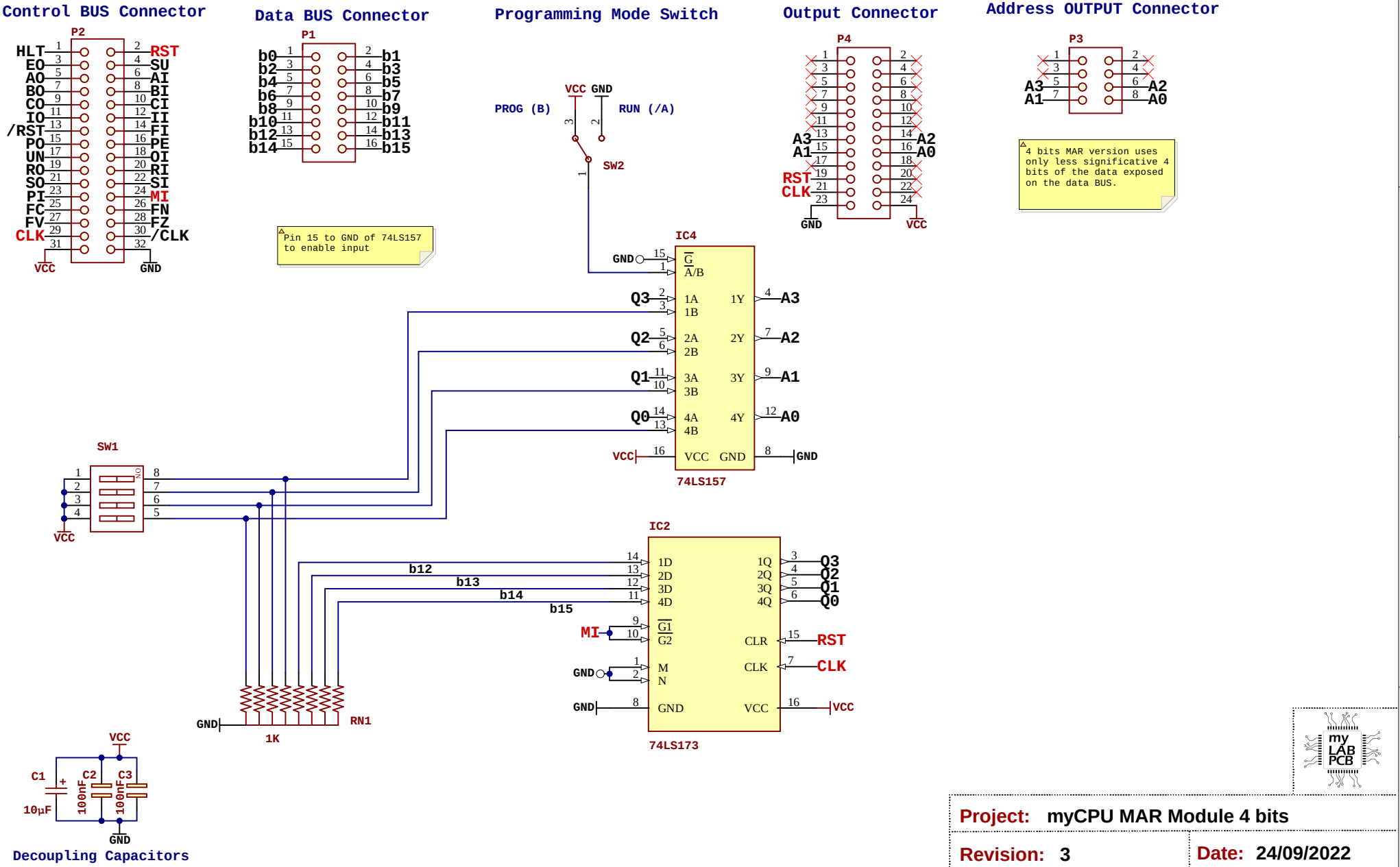
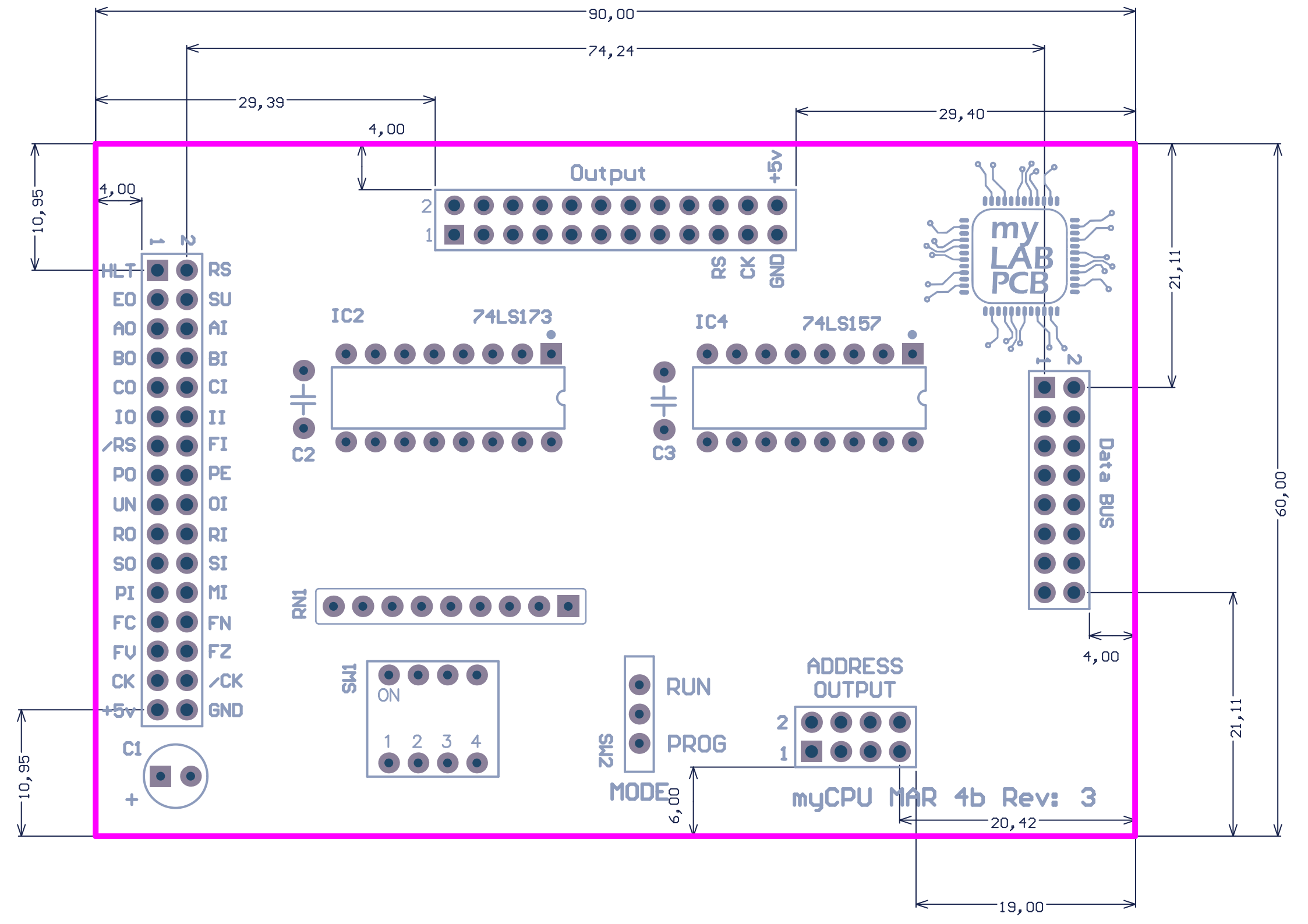
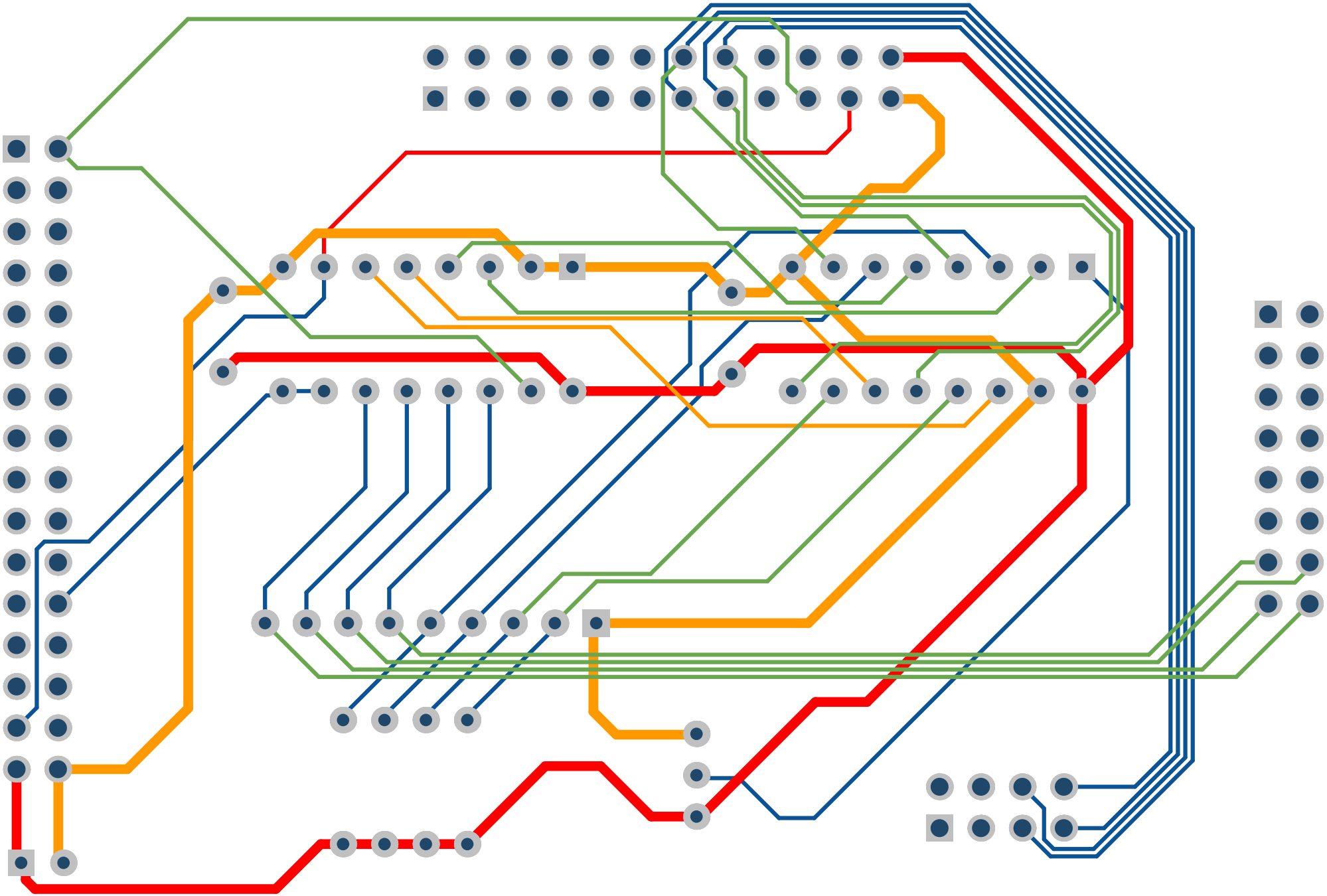

Output
+5v
RS
CK
GND
my
LAB
PCB
IC2
74LS173
IC4
74LS157
C2
C3
1
2
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Data BUS
RN1
C1
SW1
ON
WE
1 2 3 4
SW2
RUN
PROG
MODE
ADDRESS
OUTPUT
2
1
myCPU MAR 4b Rev: 3


Control BUS Connector
P2
HLT 1 2 RST
EO 3 4 SU
AO 5 6 AI
BO 7 8 BI
CO 9 10 CI
IO 11 12 II
/RST 13 14 FI
PO 15 16 PE
UN 17 18 OI
RO 19 20 RI
SO 21 22 SI
PI 23 24 MI
FC 25 26 FN
FV 27 28 FZ
CLK 29 30 /CLK
31 32
VCC
GND
Data BUS Connector
P1
b0 1 2 b1
b2 3 4 b3
b4 5 6 b5
b6 7 8 b7
b8 9 10 b9
b10 11 12 b11
b12 13 14 b13
b14 15 16 b15
Programming Mode Switch
VCC GND
PROG (B)
RUN (/A)
3
2
1
SW2
Output Connector
P4
A3 13 16 A2
A1 15 18 A0
RST 19 20
CLK 21 22
23 24
GND
VCC
Address OUTPUT Connector
P3
A3 1 2
A1 3 4
5 6 A2
7 8 A0
4 bits MAR version uses only less significative 4 bits of the data exposed on the data BUS.
Pin 15 to GND of 74LS157 to enable input
IC4
GND 15 G
1 A/B
Q3 2 1A 1Y 4 A3
3 1B
Q2 5 2A 2Y 7 A2
6 2B
Q1 11 3A 3Y 9 A1
10 3B
Q0 14 4A 4Y 12 A0
13 4B
VCC 16 VCC GND 8 GND
74LS157
SW1
VCC
IC2
b12
b13
b14
b15
1D 1Q 3 Q3
2D 2Q 4 Q2
3D 3Q 5 Q1
4D 4Q 6 Q0
MI 9 G1
10 G2
CLR 15 RST
GND 1 M
2 N
CLK 7 CLK
GND 8 GND
VCC 16 VCC
74LS173
GND
1K
RN1
VCC
C1 10µF
C2 100nF
C3 100nF
GND
Decoupling Capacitors
my LAB PCB
Project: myCPU MAR Module 4 bits
Revision: 3
Date: 24/09/2022
Author: Rafa Hernández


90,00
74,24
29,39
4,00
29,40
10,95
4,00
Output
+5v
2
1
RS
CK
GND
my
LAB
PCB
21,11
60,00
IC2
74LS173
IC4
74LS157
C2
C3
1
2
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Data BUS
RN1
4,00
SW1
ON
1 2 3 4
ZMS
RUN
PROG
MODE
ADDRESS
OUTPUT
2
1
C1
+
10,95
6,00
myCPU MAR 4b Rev: 3
20,42
19,00



Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C2, C3	Ceramic or tantalum capacitor	100nF	2
IC2	4-bit D-Type Register with 3 state outputs	74LS173	1
IC4	4-Bits 2-Line to 1 Line data selector	74LS157	1
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	1
P4	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical,	24p	1
RN1	Resistor array 8 elements,9 pins	1K	1
SW1	DIP switch 4 positions	4 pos	1
SW2	Mini slide switch 2 pos, 3 pins		1

Assembly List

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
IC2	4-bit D-Type Register with 3 state outputs	74LS173
IC4	4-Bits 2-Line to 1 Line data selector	74LS157
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
P4	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
RN1	Resistor array 8 elements,9 pins	1K
SW1	DIP switch 4 positions	4 pos
SW2	Mini slide switch 2 pos, 3 pins	