HM6264B Series

64 k SRAM (8-kword × 8-bit)

HITACHI

ADE-203-454B (Z)
Rev. 2.0
Nov. 1997

Description

The Hitachi HM6264B is 64k-bit static RAM organized 8-kword × 8-bit. It realizes higher performance and low power consumption by 1.5 μm CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, 300 mil plastic DIP, is available for high density mounting.

Features

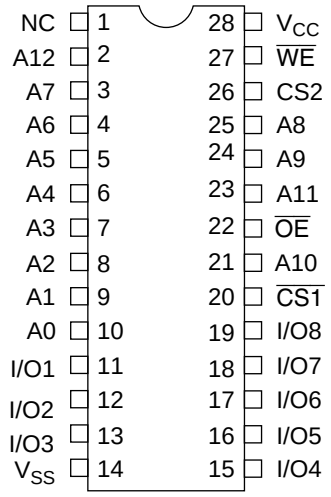
- High speed
  Fast access time: 85/100 ns (max)
- Low power
  Standby: 10 μW (typ)
  Operation: 15 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- Directly TTL compatible
  All inputs and outputs
- Battery backup operation capability

Ordering Information

Type No.	Access time	Package
HM6264BLP-8L HM6264BLP-10L	85 ns 100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264BLSP-8L HM6264BLSP-10L	85 ns 100 ns	300-mil, 28-pin plastic DIP(DP-28N)
HM6264BLFP-8LT HM6264BLFP-10LT	85 ns 100 ns	450-mil, 28-pin plastic SOP(FP-28DA)

Pin Arrangement

HM6264BLP/BLSP/BLFP Series

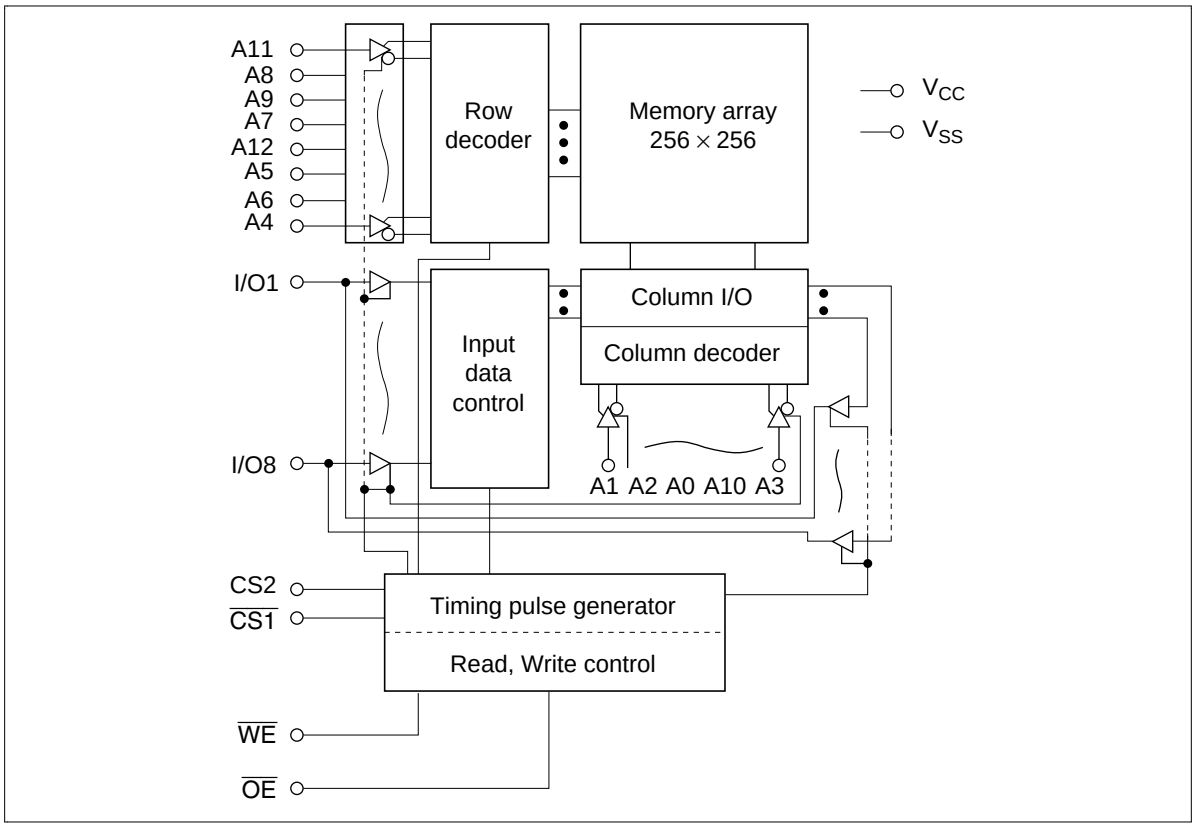


(Top view)

Pin Description

Pin name	Function	Pin name	Function
A0 to A12	Address input	$\overline{WE}$	Write enable
I/O1 to I/O8	Data input/output	$\overline{OE}$	Output enable
$\overline{CS1}$	Chip select 1	NC	No connection
CS2	Chip select 2	V_{CC}	Power supply
		V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
×	H	×	×	Not selected (power down)	I_{SB}, I_{SB1}	High-Z	—
×	×	L	×	Not selected (power down)	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage[*1]	V_{CC}	–0.5 to +7.0	V
Terminal voltage[*1]	V_T	–0.5[*2] to V_{CC} + 0.3[*3]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. Relative to V_{SS}
2. V_T min: –3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3[*1]	—	0.8	V

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CCDC}	—	7	15	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA others = V_{IH}/V_{IL}
Average operating power supply current	I_{CC1}	—	30	45	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA others = V_{IH}/V_{IL}
	I_{CC2}	—	3	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IL}
	I_{SB1}	—	2	50	µA	$\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V, 0 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance[*1]	Cin	—	—	5	pF	Vin = 0 V
Input/output capacitance[*1]	$C_{I/O}$	—	—	7	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

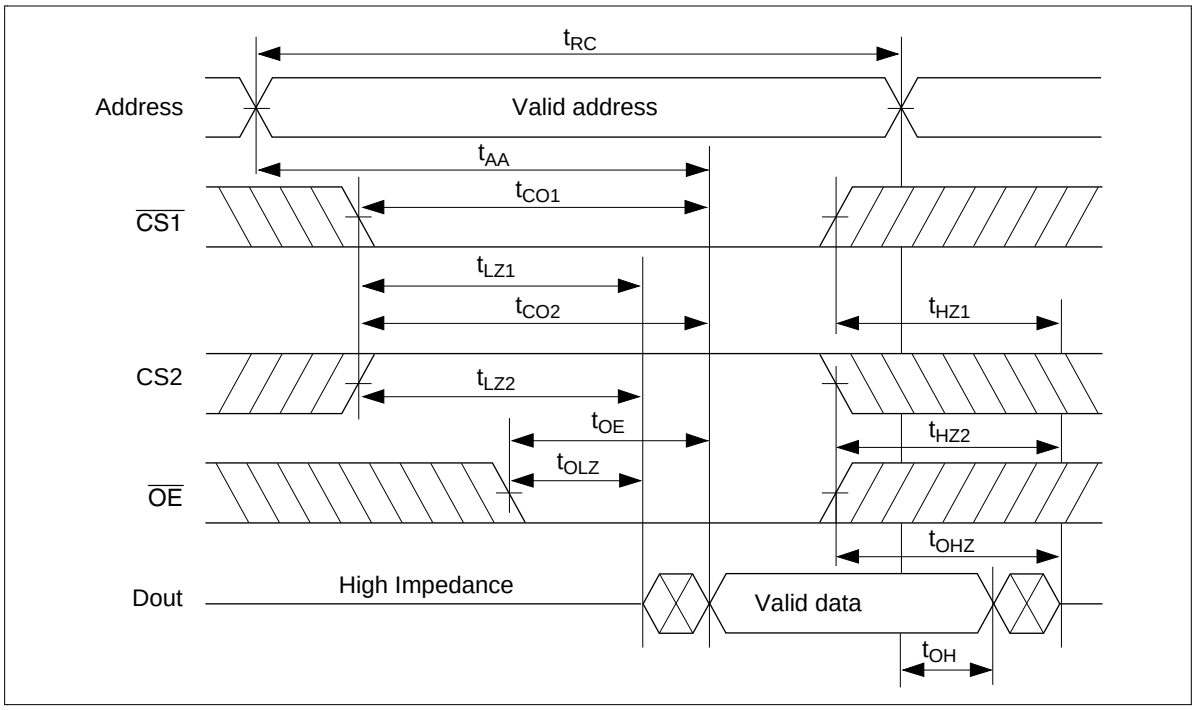
Read Cycle

			HM6264B-8L		HM6264B-10L			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time		t_{RC}	85	—	100	—	ns	
Address access time		t_{AA}	—	85	—	100	ns	
Chip select access time	$\overline{CS1}$	t_{CO1}	—	85	—	100	ns	
	CS2	t_{CO2}	—	85	—	100	ns	
Output enable to output valid		t_{OE}	—	45	—	50	ns	
Chip selection to output in low-Z	$\overline{CS1}$	t_{LZ1}	10	—	10	—	ns	2
	CS2	t_{LZ2}	10	—	10	—	ns	2
Output enable to output in low-Z		t_{OLZ}	5	—	5	—	ns	2
Chip deselection in to output in high-Z	$\overline{CS1}$	t_{HZ1}	0	30	0	35	ns	1, 2
	CS2	t_{HZ2}	0	30	0	35	ns	1, 2
Output disable to output in high-Z		t_{OHZ}	0	30	0	35	ns	1, 2
Output hold from address change		t_{OH}	10	—	10	—	ns	

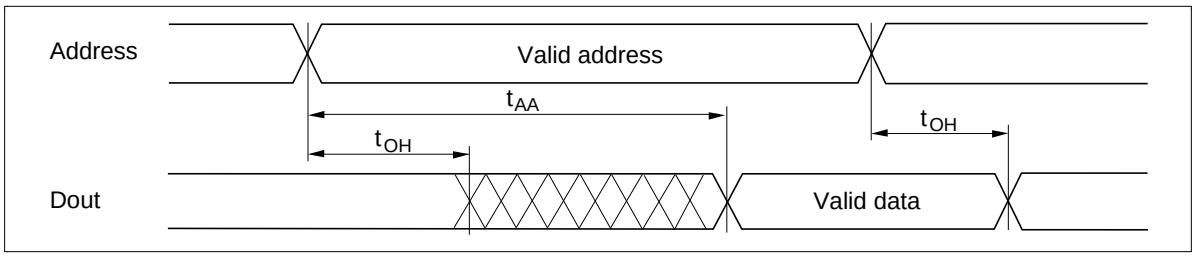
Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

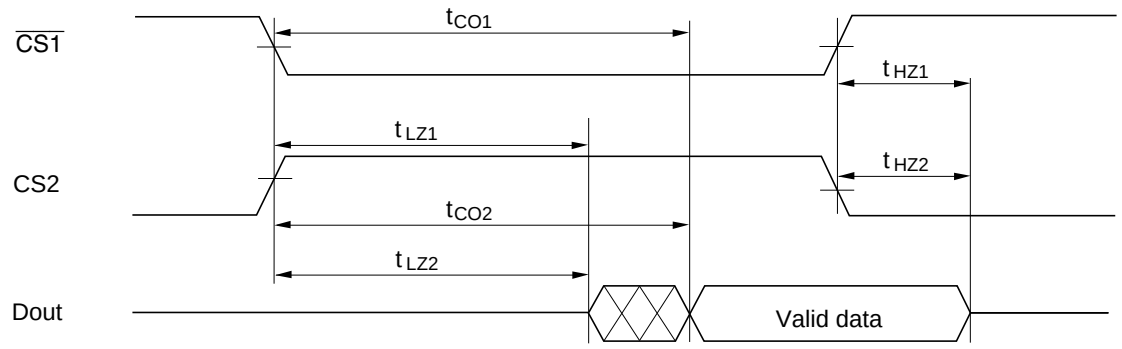
Read Timing Waveform (1) ($\overline{WE}$ = V_{IH})



Read Timing Waveform (2) ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})



Read Timing Waveform (3) ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})[*1]



Note: 1. Address must be valid prior to or simultaneously with $\overline{CS1}$ going low or CS2 going high.

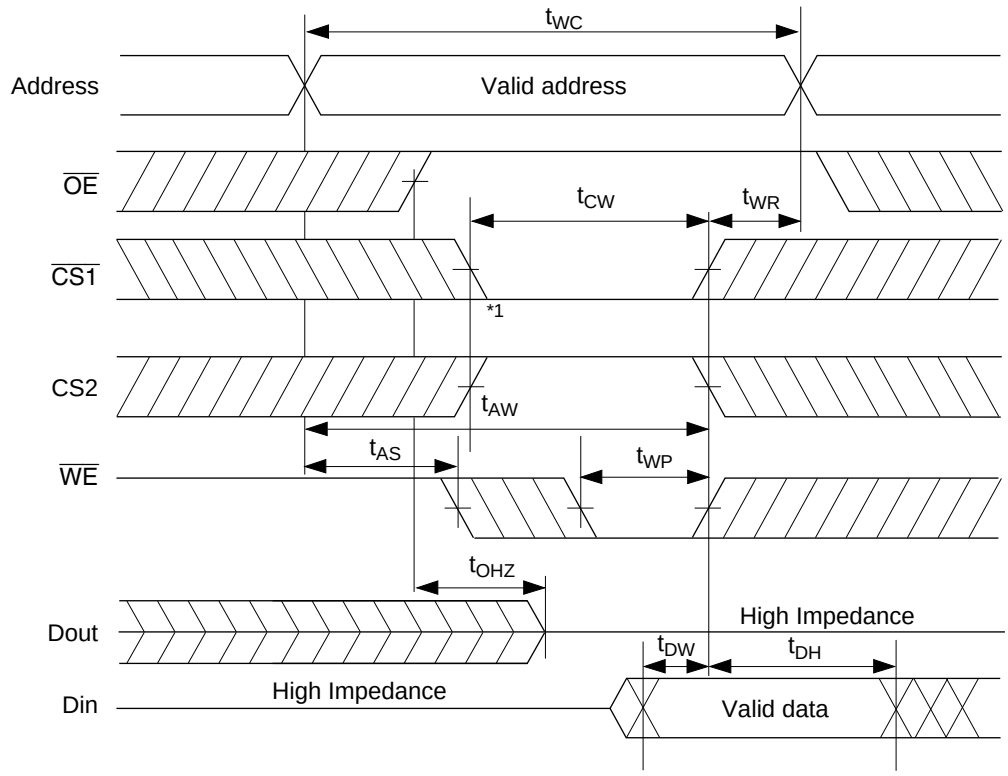
Write Cycle

		HM6264B-8L		HM6264B-10L			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	ns	2
Address setup time	t_{AS}	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	ns	
Write pulse width	t_{WP}	55	—	60	—	ns	1, 6
Write recovery time	t_{WR}	0	—	0	—	ns	4
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	ns	5
Data to write time overlap	t_{DW}	40	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	5

Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, and high CS2, and a high $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low,CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high CS2 going low and $\overline{WE}$ going high. Time t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
6. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention

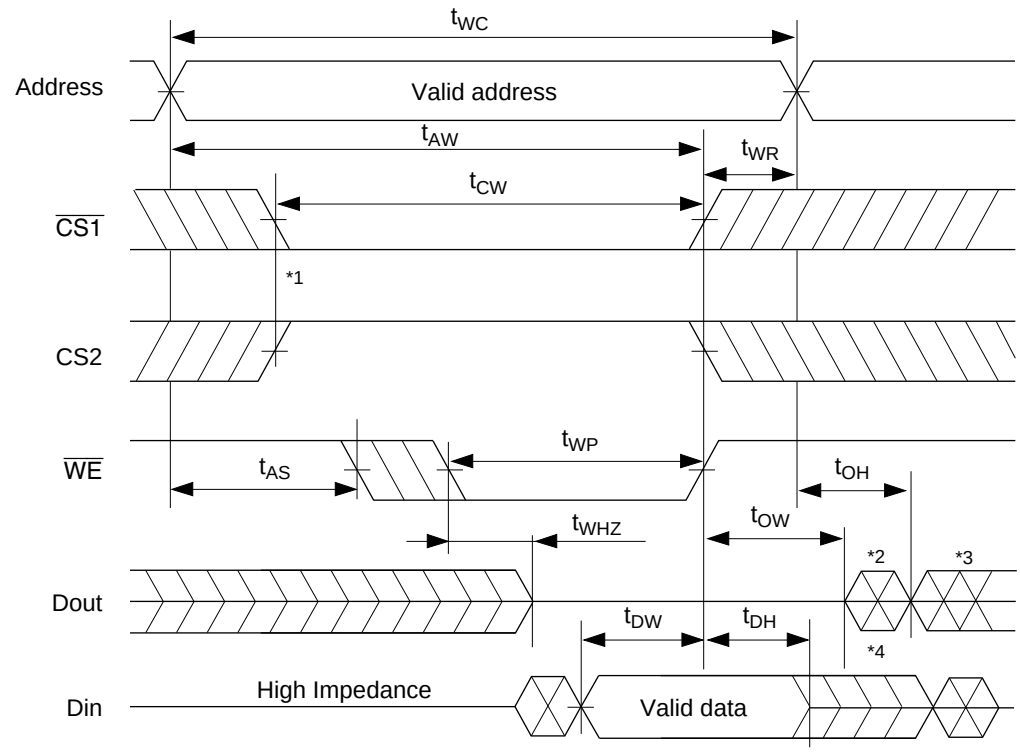
   $t_{WP} \geq t_{WHZ}$ max + t_{DW} min.

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Note: 1. If $\overline{CS1}$ goes low or CS2 goes high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance.state.

Write Timing Waveform (2) ($\overline{OE}$ Low Fixed) ($\overline{OE}$ = V_{IL})



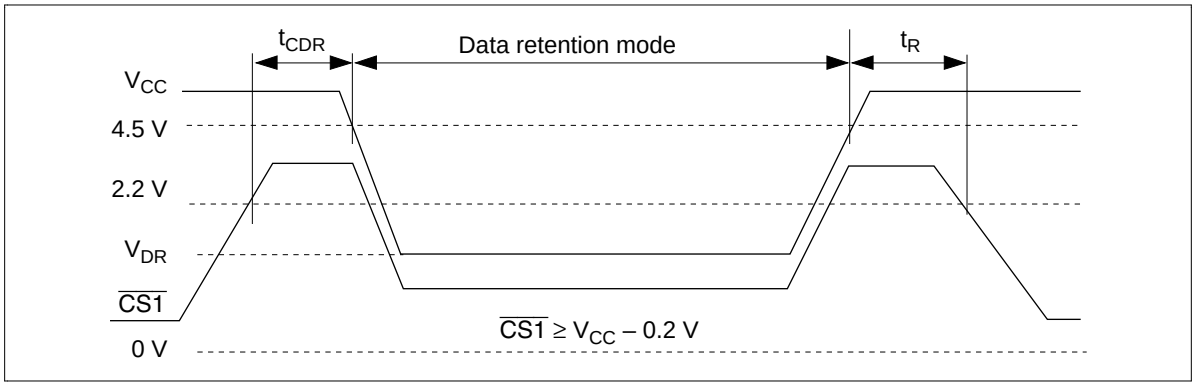
Notes:
1. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ goes low, the outputs remain in high impedance state.
2. Dout is the same phase of the written data in this write cycle.
3. Dout is the read data of the next address.
4. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied to I/O pins.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

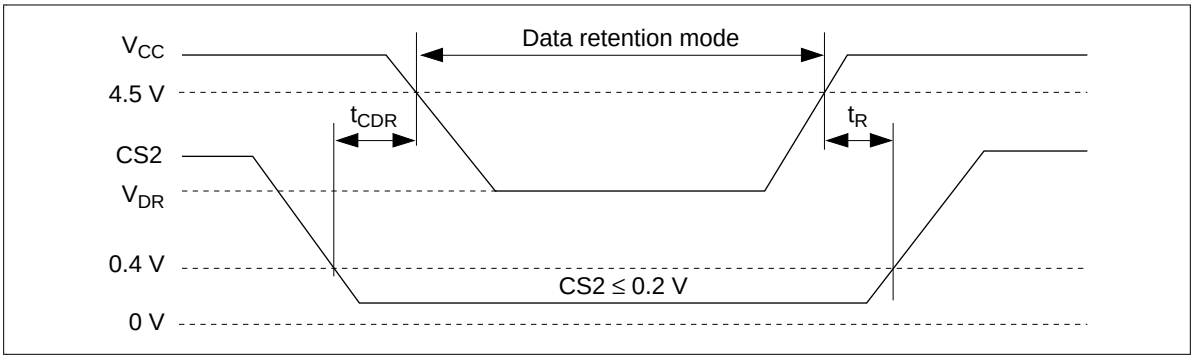
Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions[*4]
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} –0.2 V or CS2 ≤ 0.2 V
Data retention current	I_{CCDR}	—	1[*1]	25[*2]	µA	V_{CC} = 3.0 V, 0 V ≤ Vin ≤ V_{CC} $\overline{CS1} \geq V_{CC}$ –0.2 V, CS2 ≥ V_{CC} –0.2 V or 0 V ≤ CS2 ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[*3]	—	—	ns	

Notes: 1. Reference data at Ta = 25°C.
2. 10 µA max at Ta = 0 to + 40°C.
3. t_{RC} = read cycle time.
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



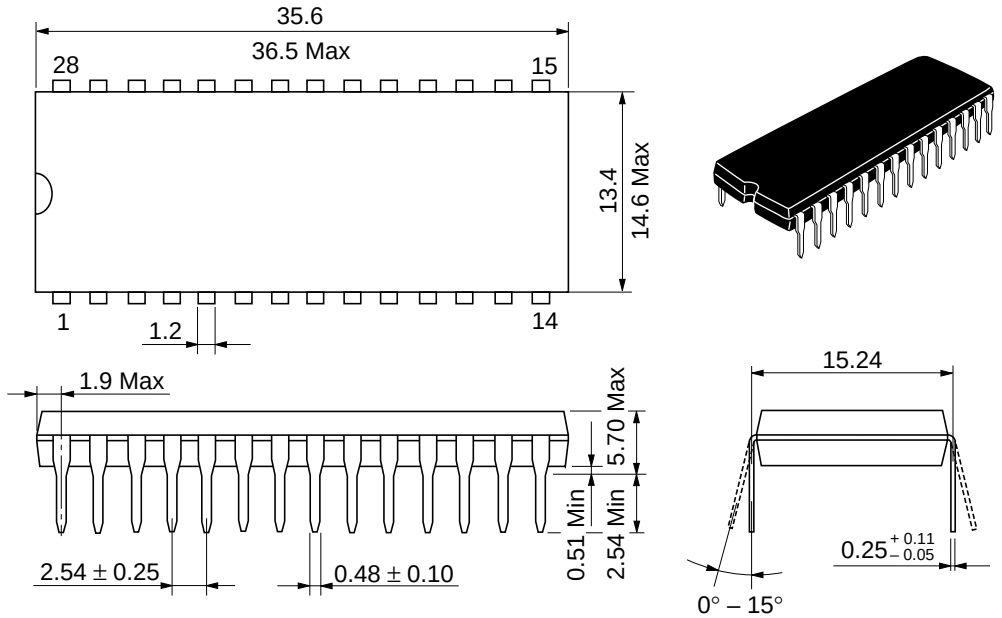
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM6264BLP Series (DP-28)

Unit: mm

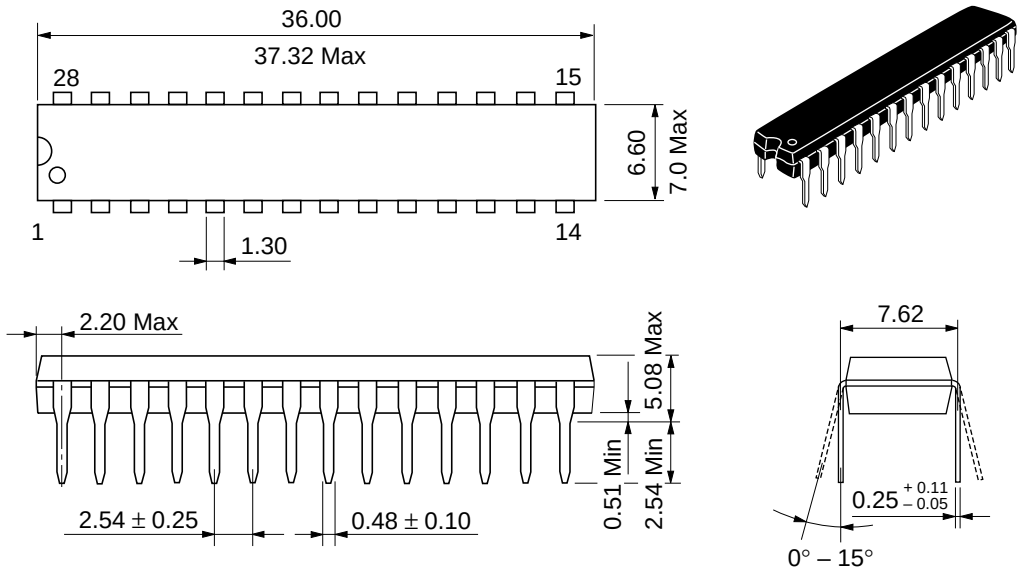


Hitachi Code	DP-28
JEDEC	—
EIAJ	Conforms
Weight (reference value)	4.6 g

Package Dimensions (cont)

HM6264BLSP Series (DP-28N)

Unit: mm

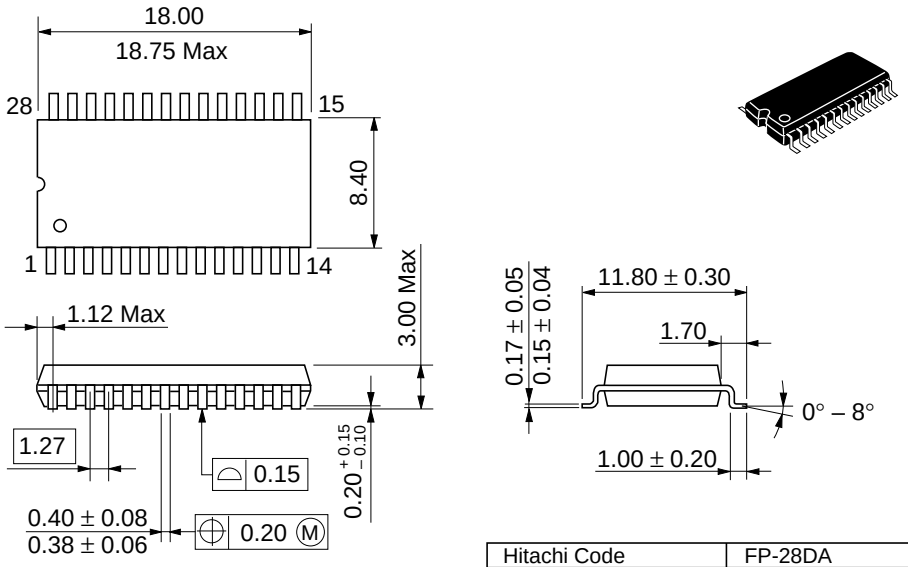


Hitachi Code	DP-28N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	2.04 g

Package Dimensions (cont)

HM6264BLFP Series (FP-28DA)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-28DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.82 g

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A
Tel: 800-285-1601
Fax:303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 5, 1995	Initial issue	I. Ogiwara	K. Yoshizaki
1.0	Dec. 6, 1995	Deletion of Preliminary	I. Ogiwara	K. Yoshizaki
2.0	Nov. 1997	Change of Subtitle Change of FP-28DA		