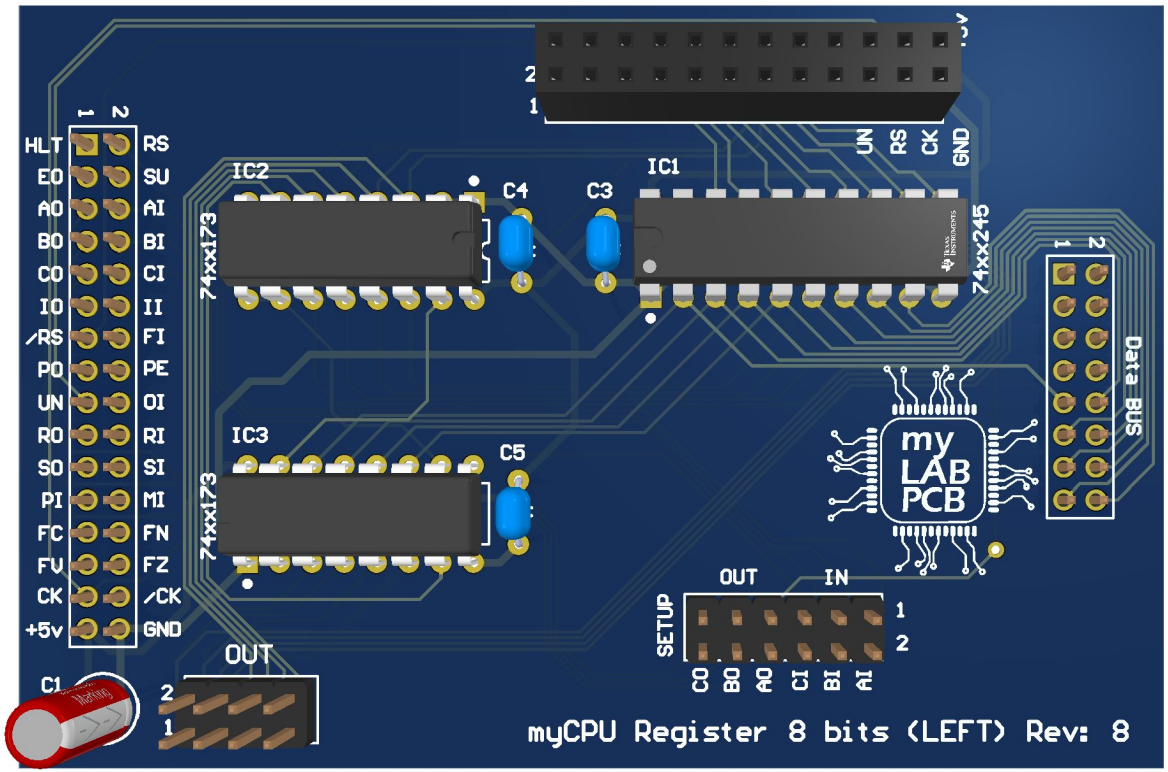
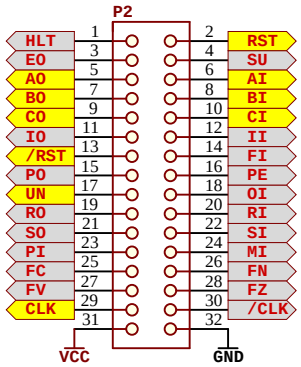
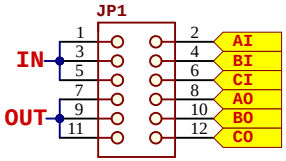

HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
IC1
IC2
IC3
74xx173
74xx245
C1
C3
C4
C5
OUT
IN
SETUP
CO BO AO CI BI AI
UN RS CK GND
Data BUS
my LAB PCB
myCPU Register 8 bits (LEFT) Rev: 8

## Control BUS Connector

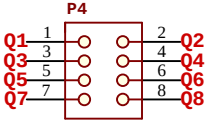



Register board setup.
Setting up which are the active signals for the register. Define the register role A, B or C.

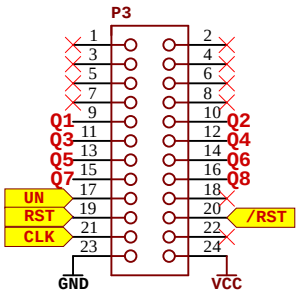
## REGISTER SETUP



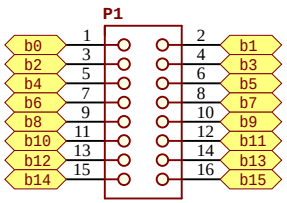

## Direct Data OUT

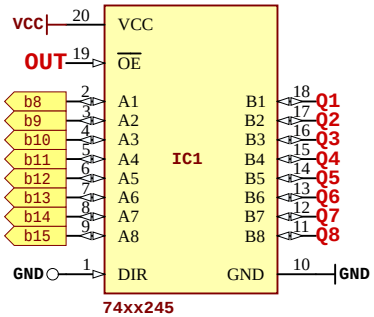


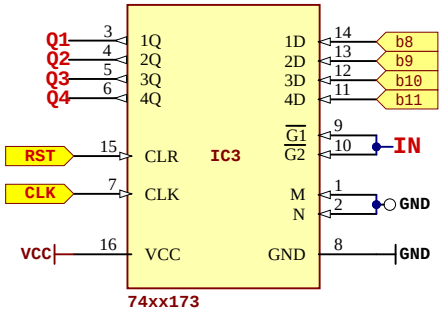

## OUTPUT Connector

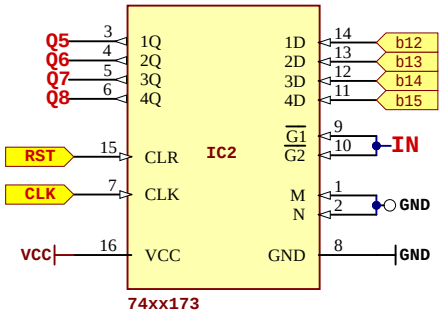


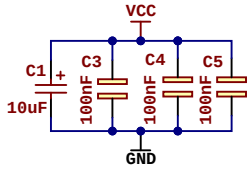

## Data BUS Connector




Decoupling Capacitors

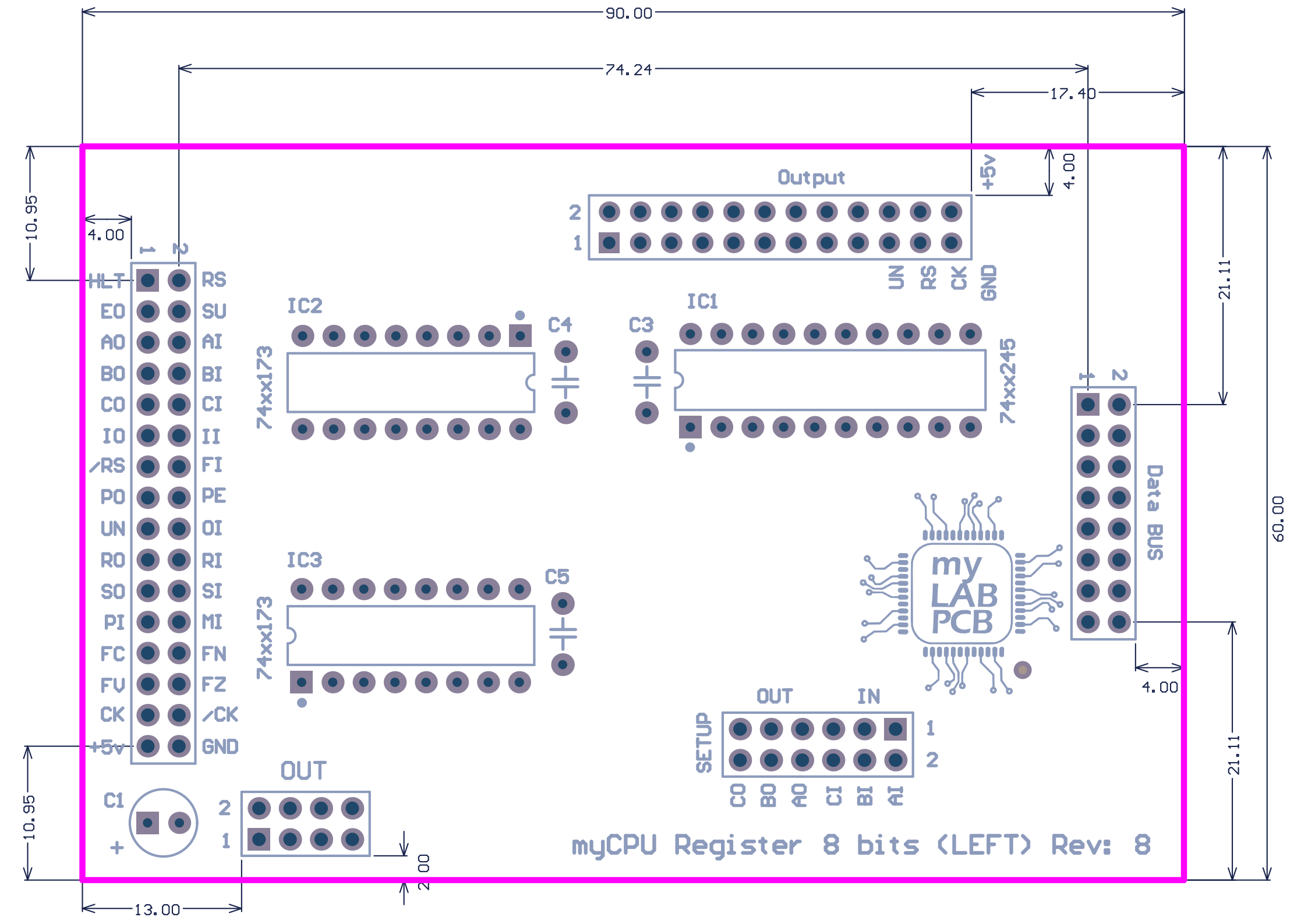
"74xx" Indicates the use LS (TTL) or HC(CMOS) ICs as your prefer for your build.

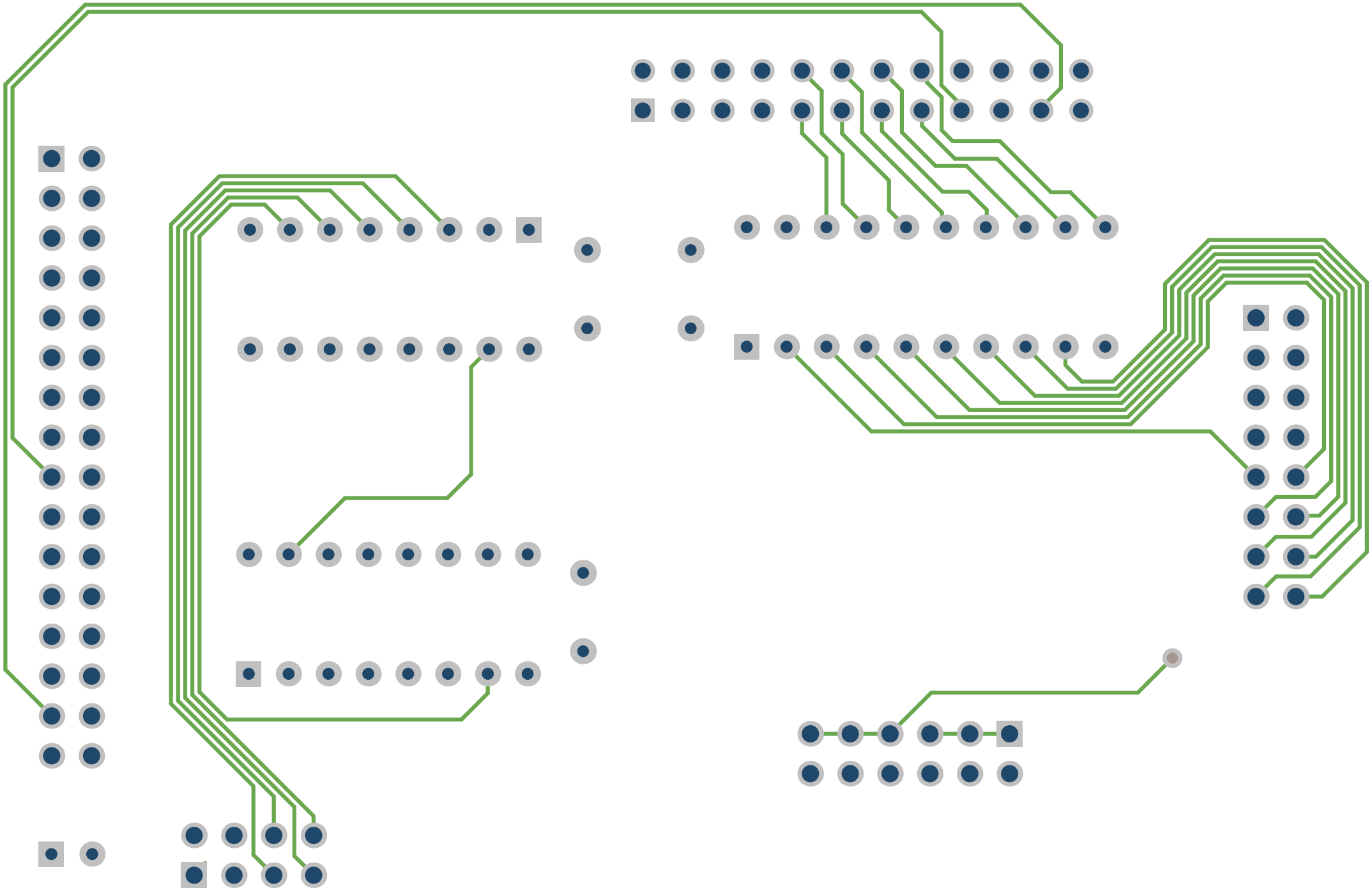
my LAB PCB

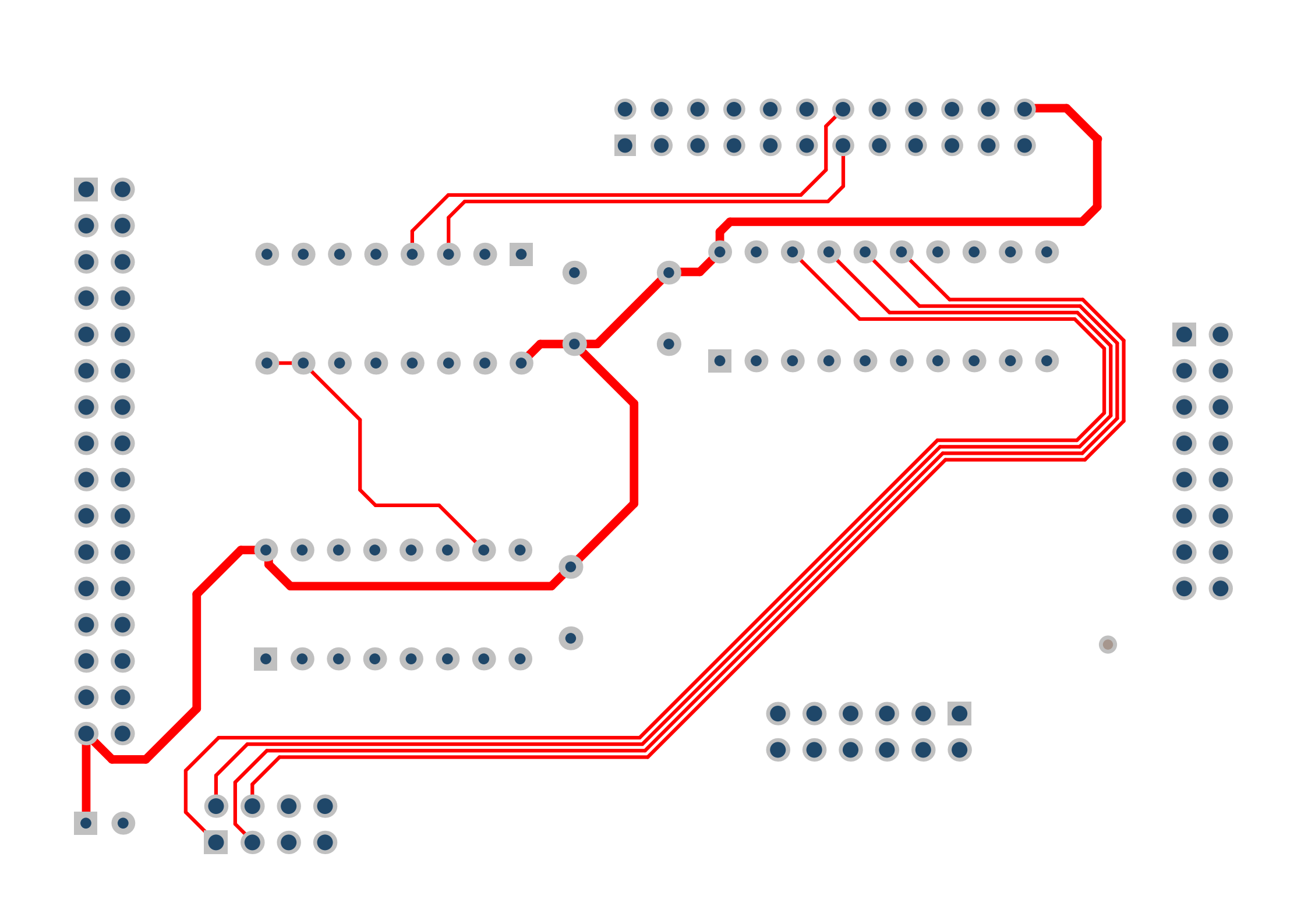
**Project:** myCPU Register 8 bit LEFT

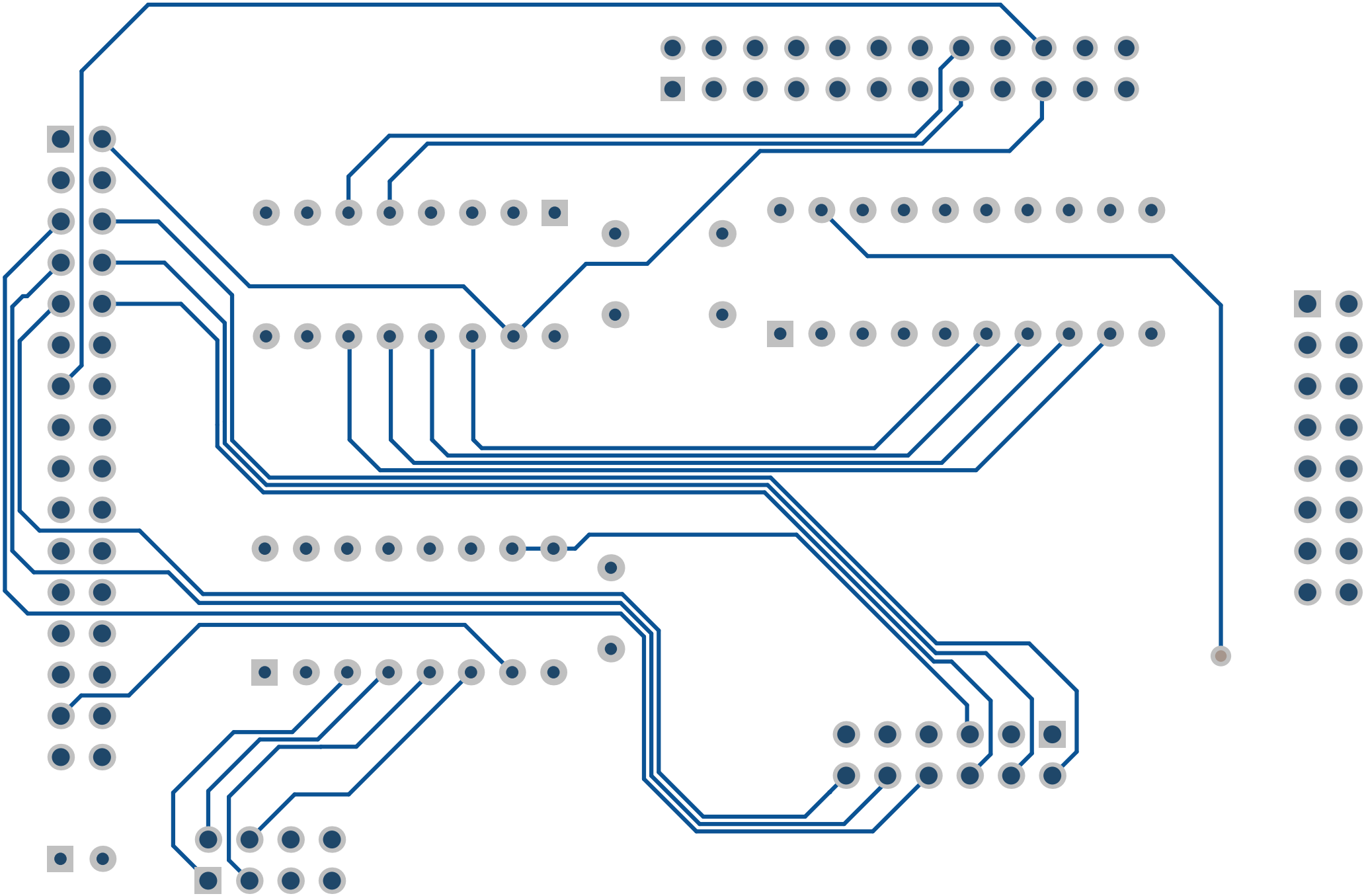
**Revision:** 8 **Date:** 27-Feb-24

**Author:** Rafa Hernández


90.00
74.24
17.40
10.95
4.00
21.11
60.00
+5v
Output
2
1
UN
RS
CK
GND
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
IC2
74xx173
C4
IC1
C3
74xx245
IC3
C5
Data BUS
my
LAB
PCB
OUT
IN
SETUP
CO
BO
AO
CI
BI
AI
C1
+
OUT
2.00
13.00
myCPU Register 8 bits (LEFT) Rev: 8







# Bill of Materials

## myCPU Register 8 bit

| Description | Value | Q |
|---|---|---|
| Electrolytic capacitor 16v/50v | 10uF | 1 |
| Ceramic or tantalum capacitor | 100nF | 3 |
| Non inverting bus transceiver | 74xx245 | 1 |
| 4-bit D-Type Register with 3 state outputs | 74xx173 | 2 |
| Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 12p | 12p | 1 |
| Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p | 16p | 1 |
| Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p | 32p | 1 |
| Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p | 24p | 1 |
| Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p | 8p | 1 |

# Assembly List

## myCPU Register 8 bit

| Designator | Description | Value |
|---|---|---|
| C1 | Electrolytic capacitor 16v/50v | 10uF |
| C3 | Ceramic or tantalum capacitor | 100nF |
| C4 | Ceramic or tantalum capacitor | 100nF |
| C5 | Ceramic or tantalum capacitor | 100nF |
| IC1 | Non inverting bus transceiver | 74xx245 |
| IC2 | 4-bit D-Type Register with 3 state outputs | 74xx173 |
| IC3 | 4-bit D-Type Register with 3 state outputs | 74xx173 |
| JP1 | Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 12p | 12p |
| P1 | Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p | 16p |
| P2 | Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p | 32p |
| P3 | Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p | 24p |
| P4 | Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p | 8p |