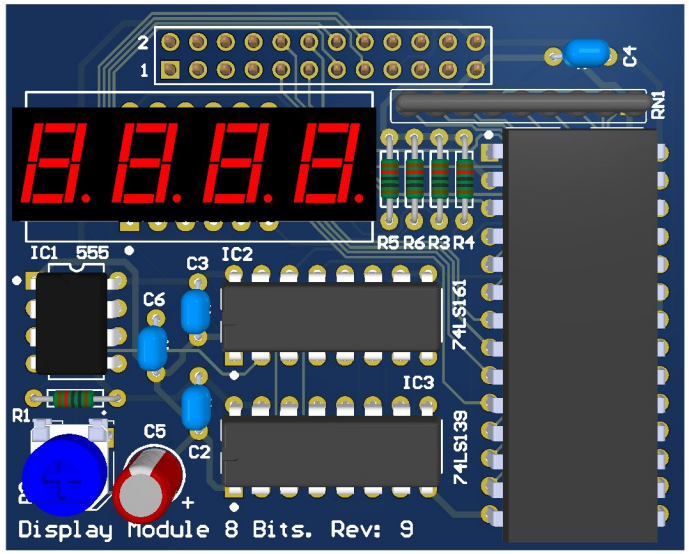
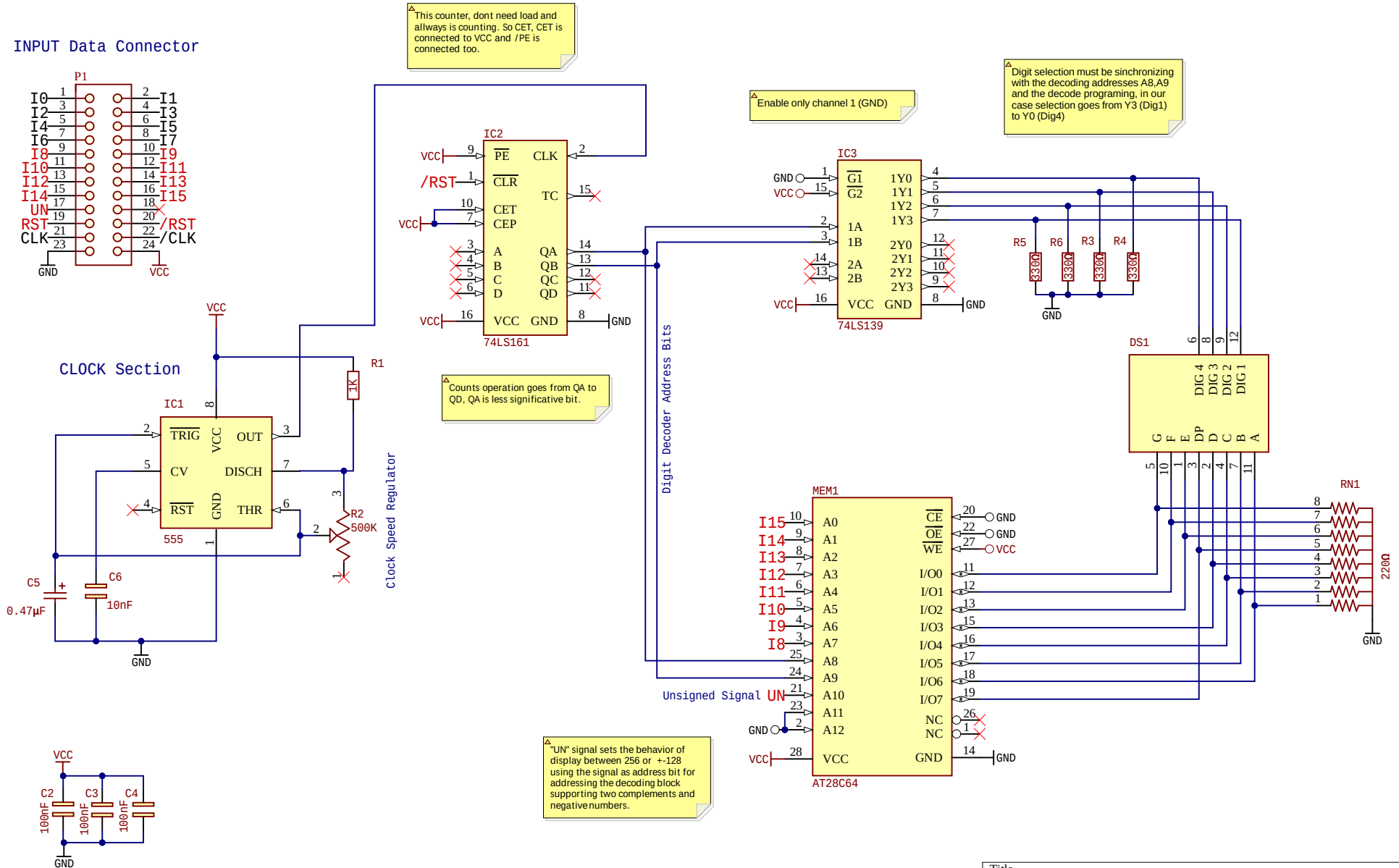
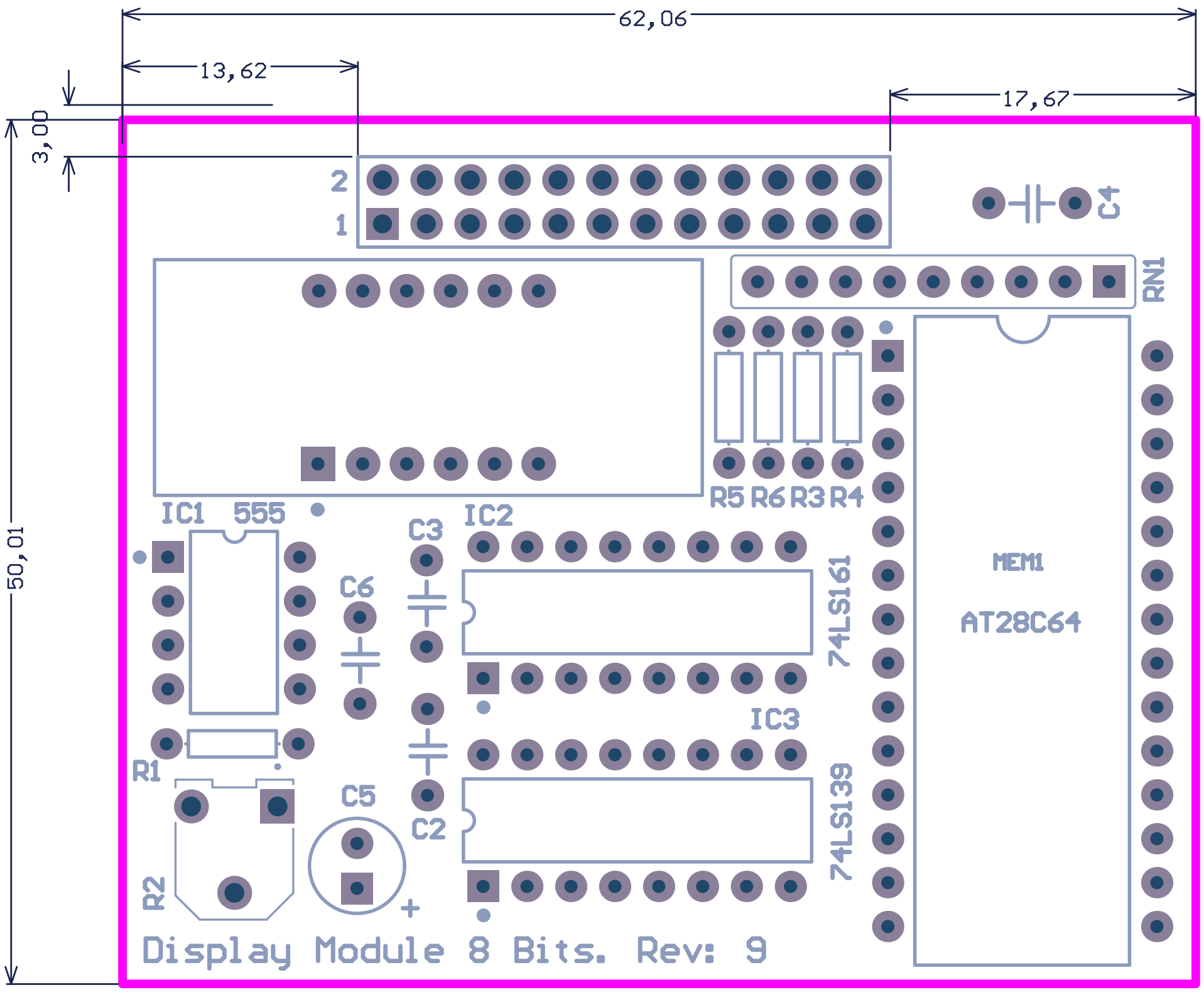

2
1
C4
RN1
R5 R6 R3 R4
IC1 555
C3
IC2
C6
74LS161
IC3
R1
C5
C2
74LS139
Display Module 8 Bits. Rev: 9


INPUT Data Connector
P1
I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14 I15 UN /RST CLK /CLK
GND VCC
This counter, dont need load and allways is counting. So CET, CET is connected to VCC and /PE is connected too.
IC2
PE CLK CLR TC CET CEP A QA B QB C QC D QD VCC GND
74LS161
/RST
Enable only channel 1 (GND)
IC3
G1 G2 1A 1B 2A 2B 1Y0 1Y1 1Y2 1Y3 2Y0 2Y1 2Y2 2Y3
74LS139
Digit selection must be sinchronizing with the decoding addresses A8,A9 and the decode programing, in our case selection goes from Y3 (Dig1) to Y0 (Dig4)
R5 R6 R3 R4 330Ω
DS1
DIG 4 DIG 3 DIG 2 DIG 1
G F E DP D C B A
RN1
220Ω
CLOCK Section
IC1
TRIG OUT CV DISCH RST GND THR
555
R1 1K
R2 500K
C5 0.47µF
C6 10nF
Clock Speed Regulator
Counts operation goes from QA to QD, QA is less significative bit.
Digit Decoder Address Bits
Unsigned Signal UN
MEM1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
CE OE WE I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 NC NC VCC GND
AT28C64
"UN" signal sets the behavior of display between 256 or +-128 using the signal as address bit for addressing the decoding block supporting two complements and negative numbers.
C2 C3 C4 100nF
Decoupling Capacitors
Title
Display 8 Bits Submodule (AT28C64)
Size A4
Number
Revision 9
Date: 12/21/2021
Sheet of
File: E:\OneDrive - UNED\..\DisplayAT28C64.SchDoc
Drawn By:


62,06
13,62
17,67
3,00
50,01
2
1
C4
RN1
R5
R6
R3
R4
IC1
555
C3
IC2
C6
74LS161
MEM1
AT28C64
IC3
R1
C5
C2
74LS139
R2
+
Display Module 8 Bits. Rev: 9