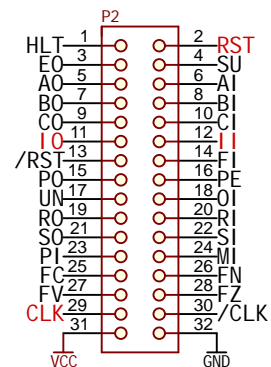
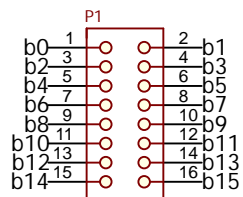


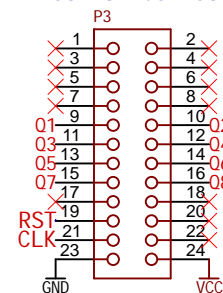
Control BUS Connector



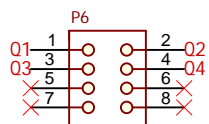
Data BUS Connector



OUTPUT Connector



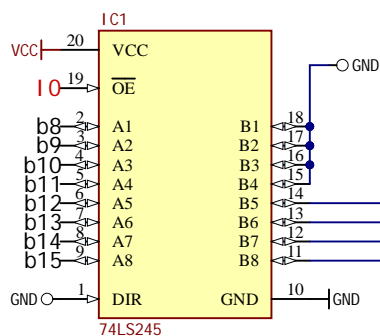
Direct Data Output



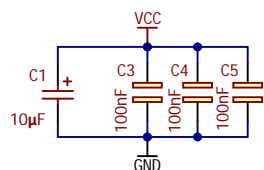
Most significant bits from Q4 to Q1 are not exposed to data BUS, only a 4 bits address is supported in the SAP-1 release.

G1, G2 input control. Set both to LOW to load all inputs to flip-flops

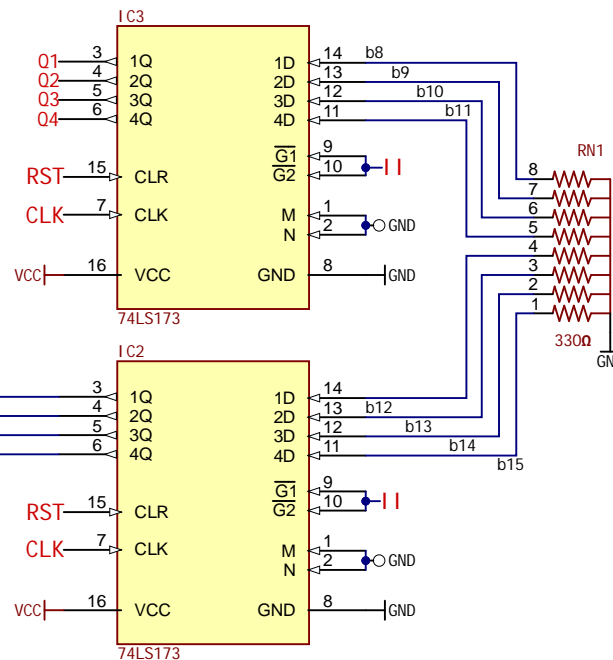
M,N output control. Set both to LOW allow driving all outputs to 245.



DIR to GND, set data flow direction from B to A



Decoupling Capacitors



Title		
Instruction Register 8 bits (RIGHT)		
Size	Number	Revision
A4		9
Date:	12/21/2021	Sheet of
File:	E:\OneDrive - UNED\...InstructionRegister8Right.Sch.Doc	1

