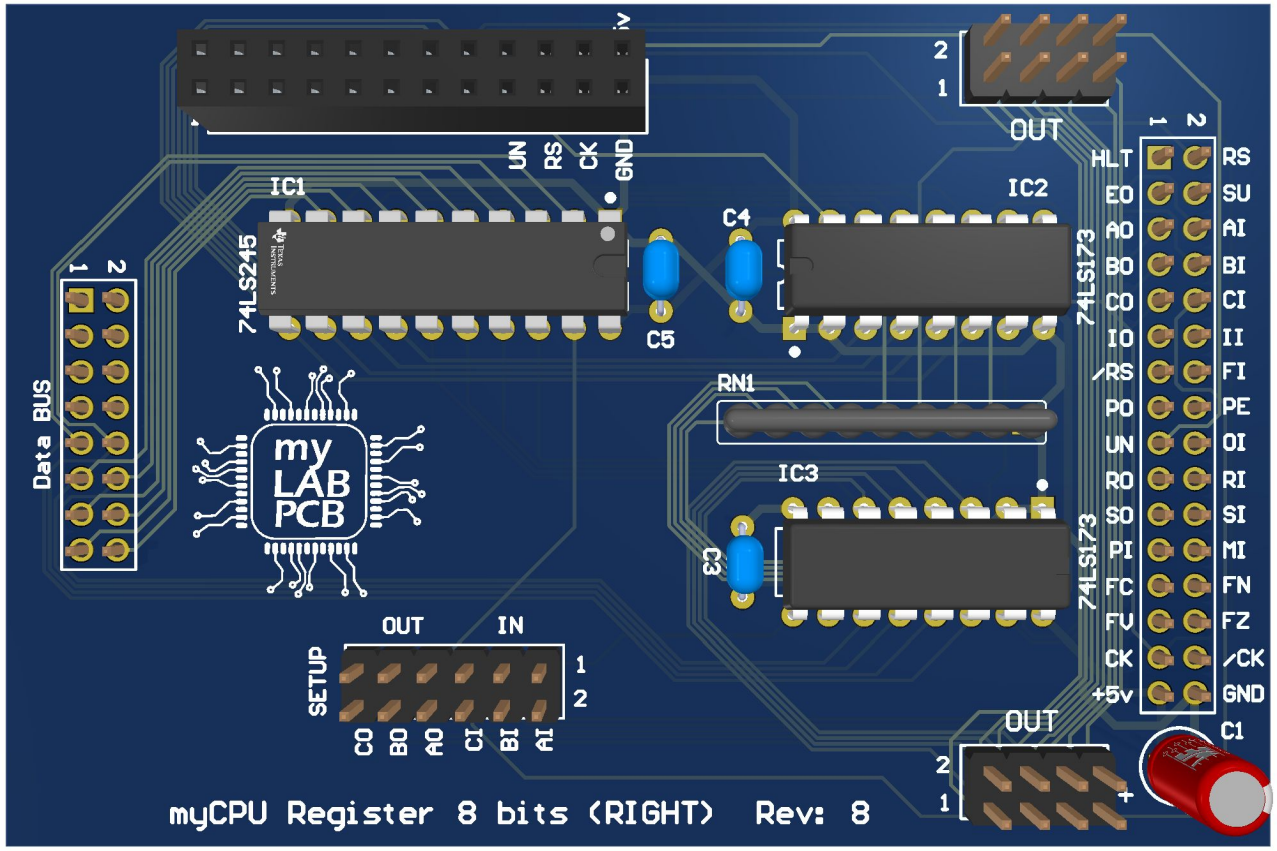
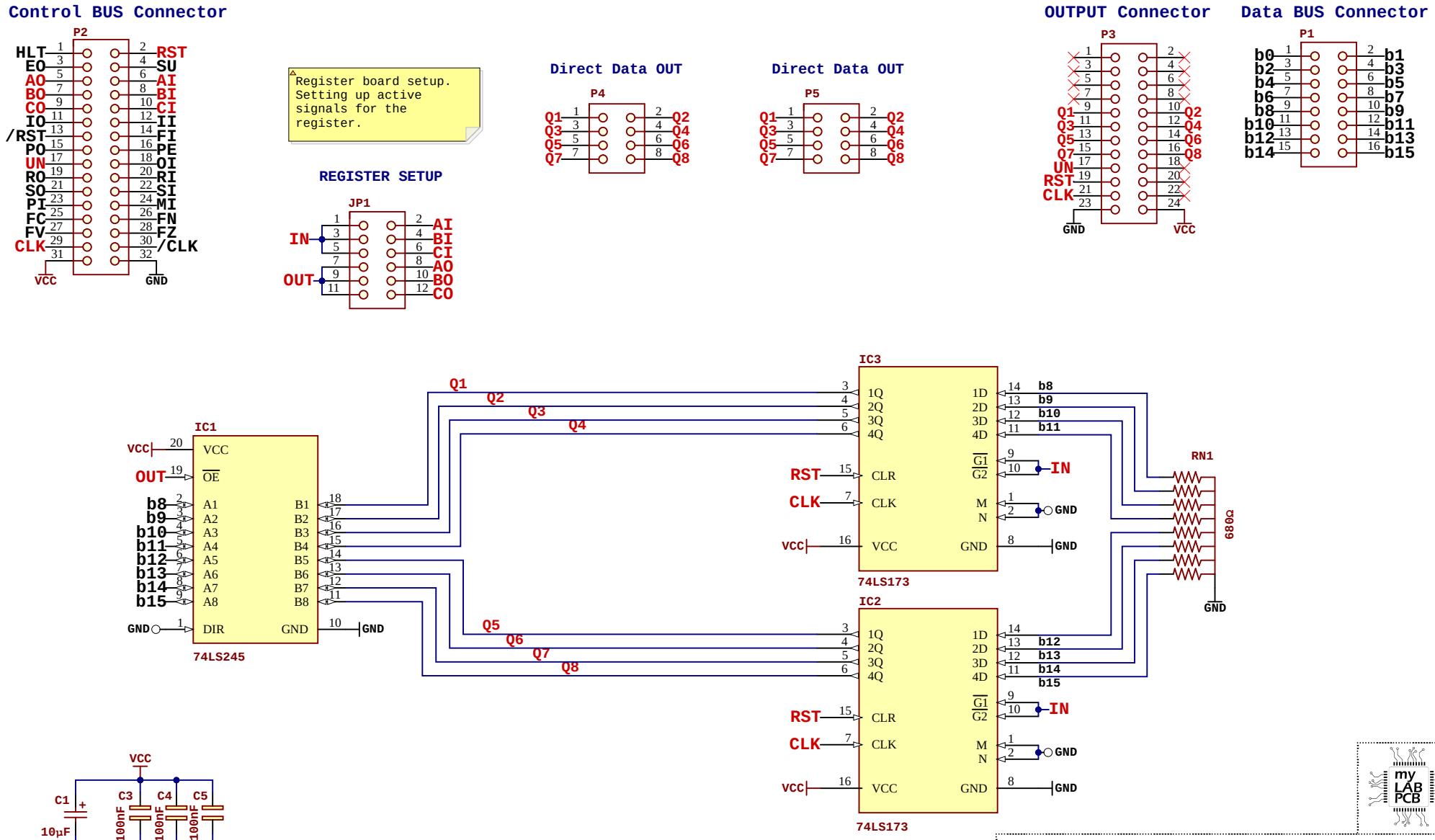
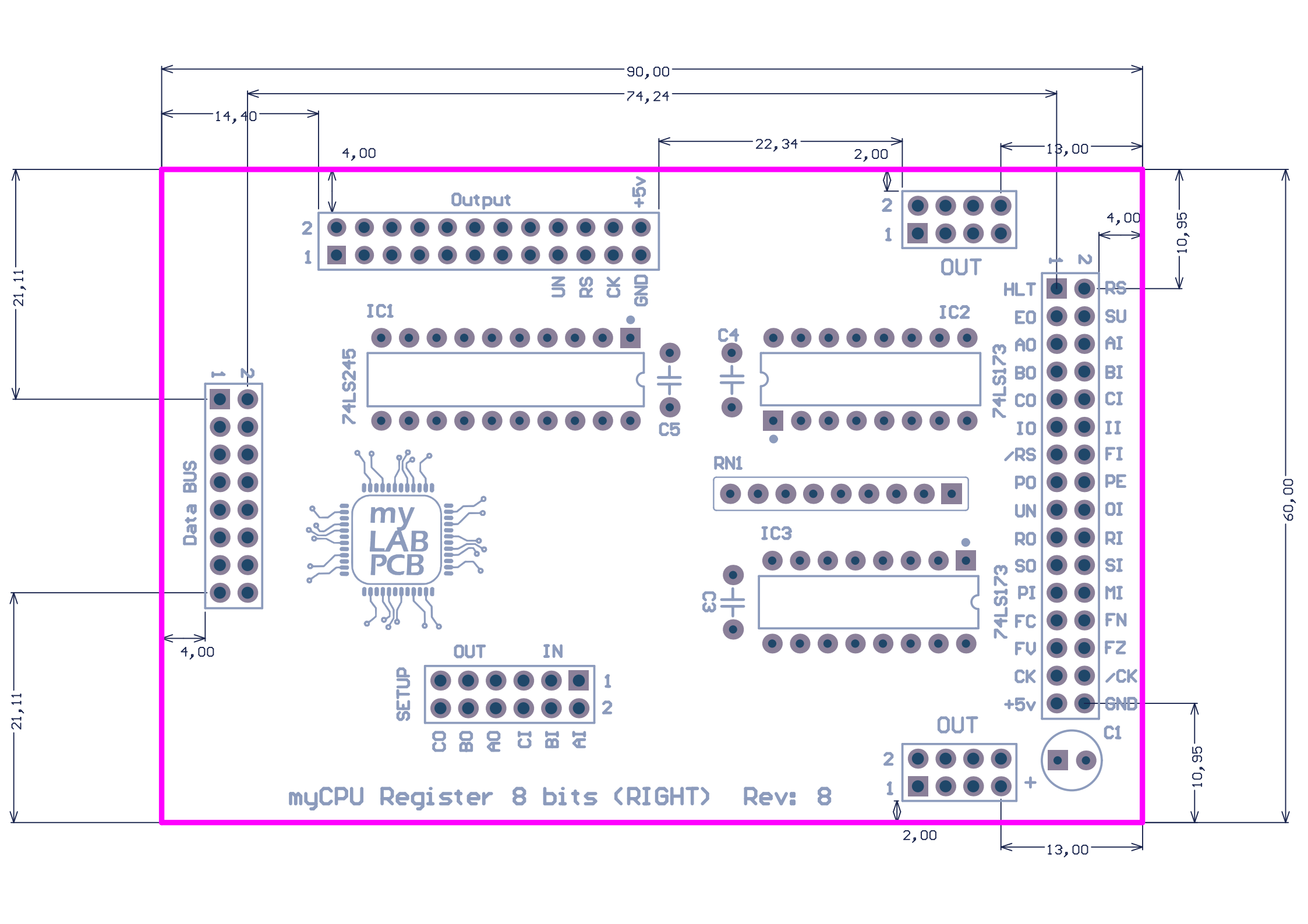

UN
RS
CK
GND
IC1
74LS245
C5
C4
IC2
74LS173
OUT
2
1
HLT
EO
AO
BO
CO
IO
\RS
PO
UN
RO
SO
PI
FC
FZ
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
Data BUS
RN1
IC3
C3
my
LAB
PCB
SETUP
OUT
IN
CO
BO
AO
CI
BI
AI
myCPU Register 8 bits (RIGHT) Rev: 8


Control BUS Connector
P2
HLT 1 2 RST
EO 3 4 SU
AO 5 6 AI
BO 7 8 BI
CO 9 10 CI
IO 11 12 II
/RST 13 14 FI
PO 15 16 PE
UN 17 18 OI
RO 19 20 RI
SO 21 22 SI
PI 23 24 MI
FC 25 26 FN
FV 27 28 FZ
CLK 29 30 /CLK
31 32
VCC
GND
Register board setup.
Setting up active
signals for the
register.
REGISTER SETUP
JP1
IN
OUT
1 2 AI
3 4 BI
5 6 CI
7 8 AO
9 10 BO
11 12 CO
Direct Data OUT
P4
Q1 1 2 Q2
Q3 3 4 Q4
Q5 5 6 Q6
Q7 7 8 Q8
Direct Data OUT
P5
Q1 1 2 Q2
Q3 3 4 Q4
Q5 5 6 Q6
Q7 7 8 Q8
OUTPUT Connector
P3
Q1 1 2
3 4
5 6
Q3 7 8
9 10 Q2
Q5 11 12 Q4
13 14 Q6
Q7 15 16 Q8
UN 17 18
RST 19 20
CLK 21 22
23 24
GND
VCC
Data BUS Connector
P1
b0 1 2 b1
b2 3 4 b3
b4 5 6 b5
b6 7 8 b7
b8 9 10 b9
b10 11 12 b11
b12 13 14 b13
b14 15 16 b15
IC1
VCC 20 VCC
OUT 19 OE
b8 2 A1 B1 18
b9 3 A2 B2 17
b10 4 A3 B3 16
b11 5 A4 B4 15
b12 6 A5 B5 14
b13 7 A6 B6 13
b14 8 A7 B7 12
b15 9 A8 B8 11
GND 1 DIR GND 10 GND
74LS245
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
IC3
3 1Q 1D 14 b8
4 2Q 2D 13 b9
5 3Q 3D 12 b10
6 4Q 4D 11 b11
9 G1
10 G2 IN
RST 15 CLR
CLK 7 CLK
M 1 GND
N 2 GND
VCC 16 VCC GND 8 GND
74LS173
IC2
3 1Q 1D 14
4 2Q 2D 13 b12
5 3Q 3D 12 b13
6 4Q 4D 11 b14
b15
9 G1
10 G2 IN
RST 15 CLR
CLK 7 CLK
M 1 GND
N 2 GND
VCC 16 VCC GND 8 GND
74LS173
RN1
680Ω
GND
VCC
C1 10µF
C3 100nF
C4 100nF
C5 100nF
GND
Decoupling Capacitors
my LAB PCB
Project: myCPU Register 8 bit RIGHT
Revision: 8
Date: 09/01/2023
Author: Rafa Hernández


90,00
74,24
14,40
4,00
22,34
2,00
13,00
21,11
10,95
60,00
Output
+5v
2
1
UN
RS
CK
GND
OUT
IC1
74LS245
C5
C4
IC2
74LS173
HLT
EO
AO
BO
CO
IO
\RS
PO
UN
RO
SO
PI
FC
FU
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
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Data BUS
my
LAB
PCB
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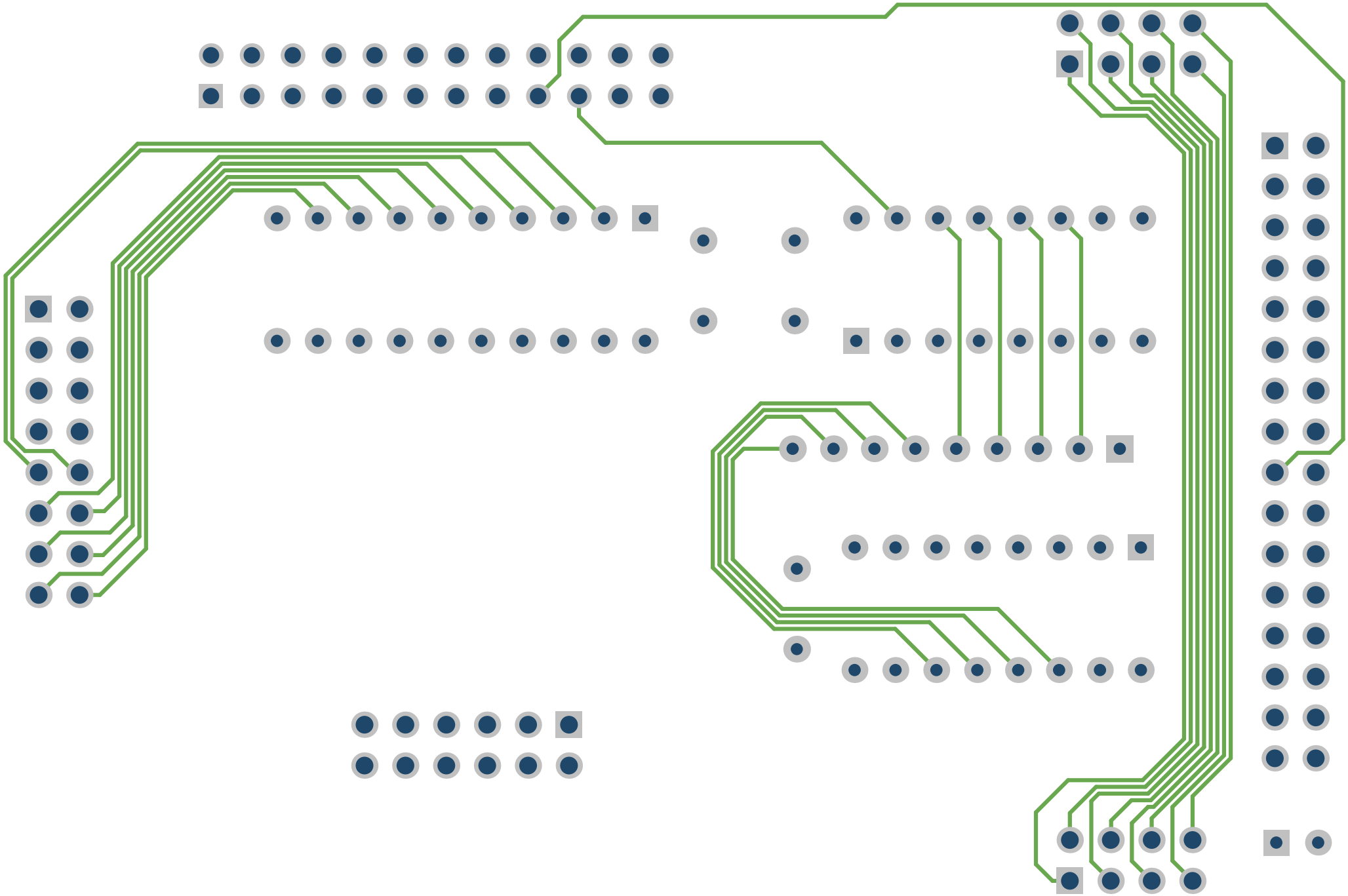
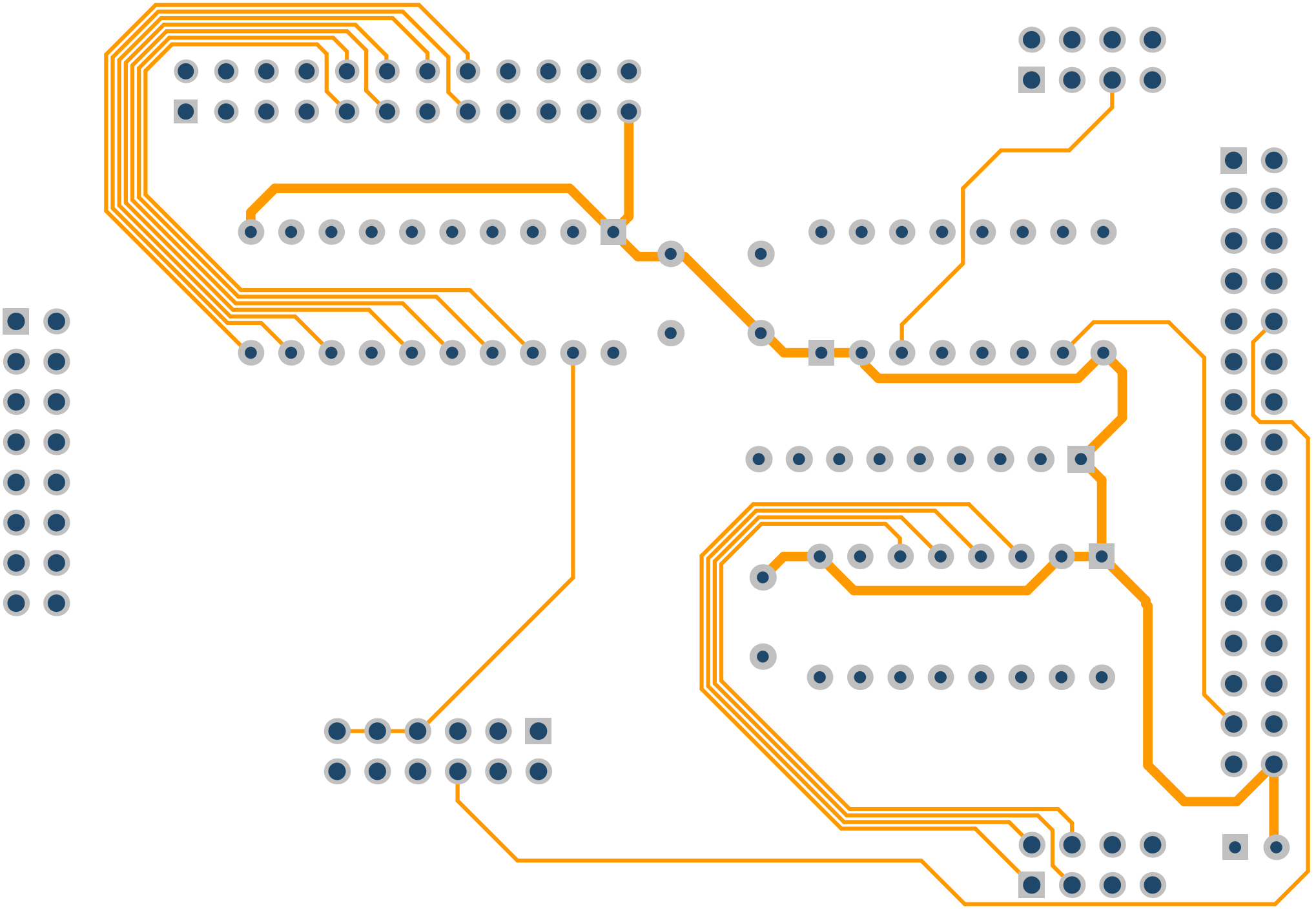
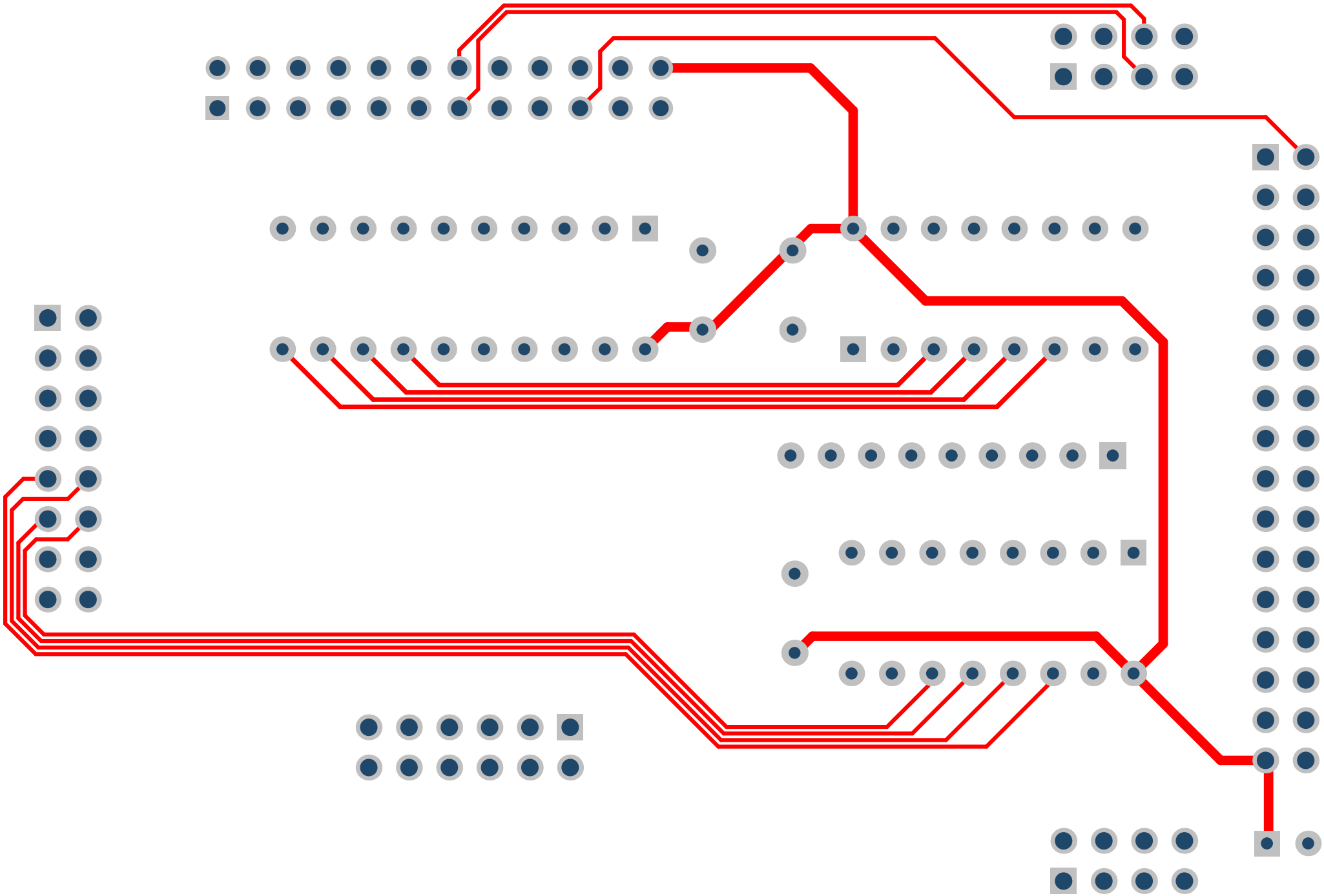
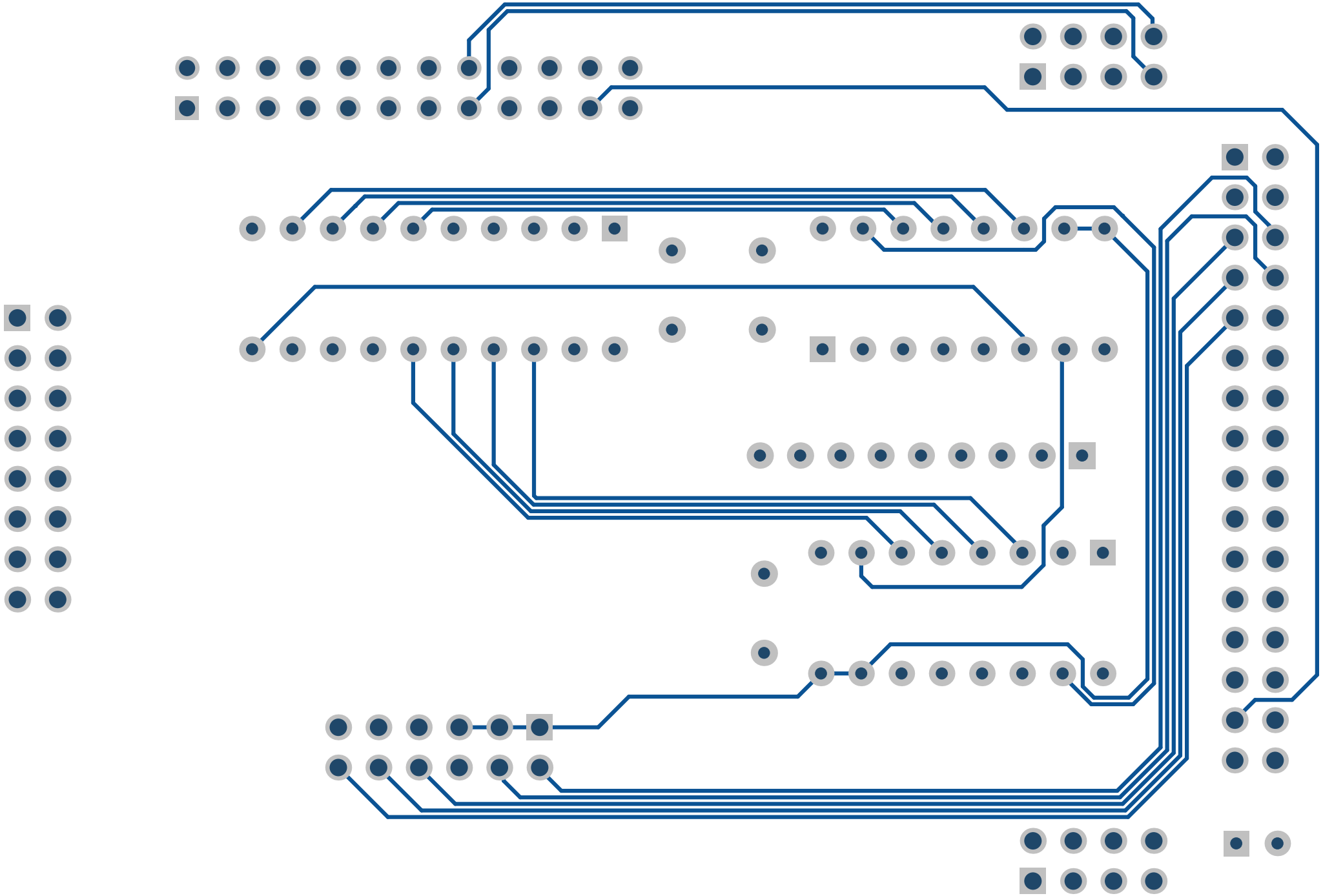
OUT
IN
CO
BO
AO
CI
BI
AI
myCPU Register 8 bits (RIGHT) Rev: 8









Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C3, C4, C5	Ceramic or tantalum capacitor	100nF	3
IC1	Non inverting bus transceiver	74LS245	1
IC2, IC3	4-bit D-Type Register with 3 state outputs	74LS173	2
JP1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 12p	12p	1
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical,	24p	1
P4, P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	2
RN1	Resistor array 8 elements,9 pins	680Ω	1

Assembly List

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC2	4-bit D-Type Register with 3 state outputs	74LS173
IC3	4-bit D-Type Register with 3 state outputs	74LS173
JP1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 12p	12p
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P4	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
RN1	Resistor array 8 elements,9 pins	680Ω