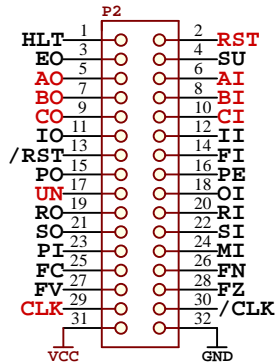


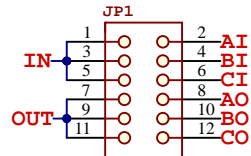


## Control BUS Connector

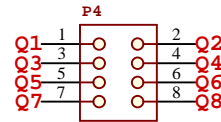


Register board setup.  
Setting up active  
signals for the  
register.

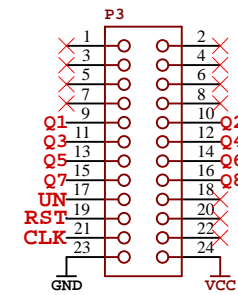
## REGISTER SETUP



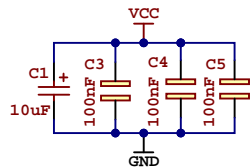
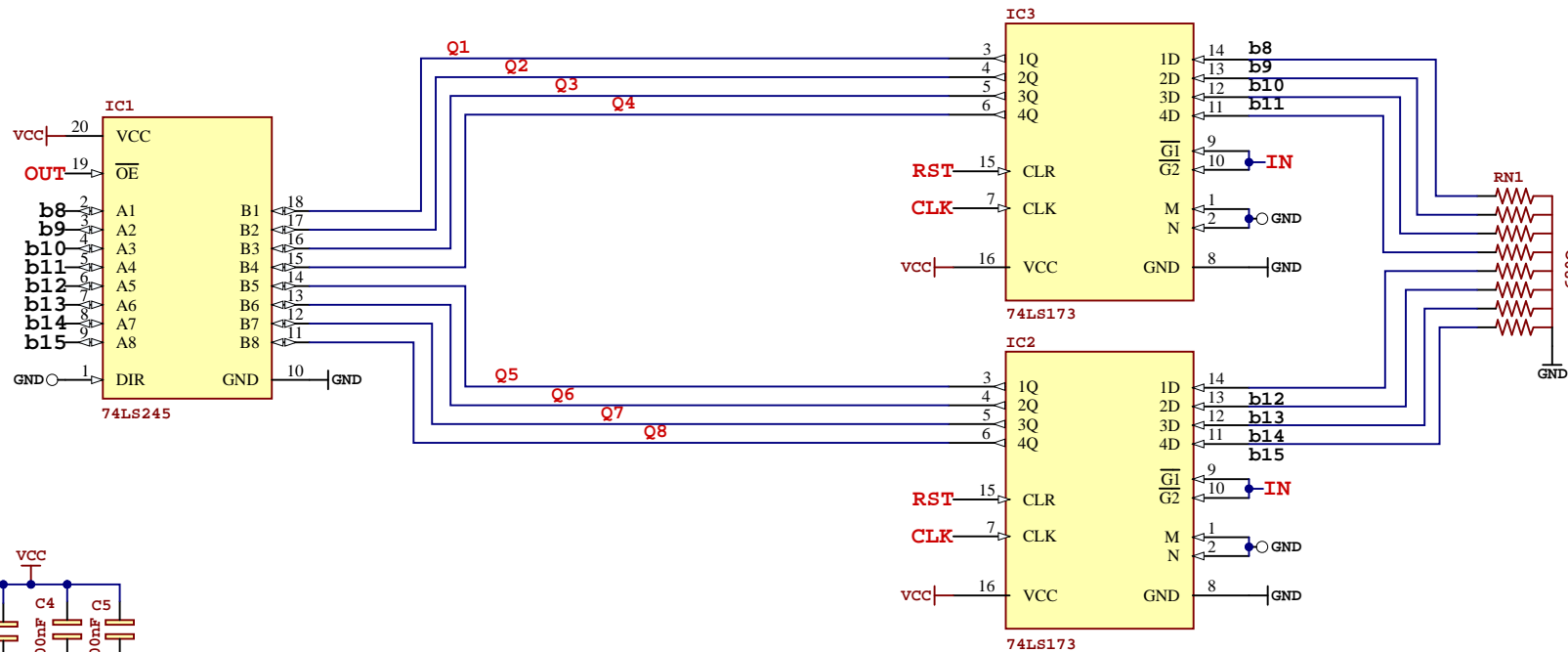
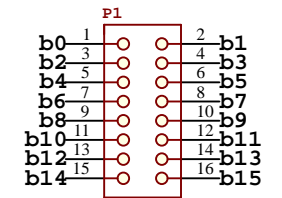
## Direct Data OUT



## OUTPUT Connector



## Data BUS Connector



Decoupling Capacitors

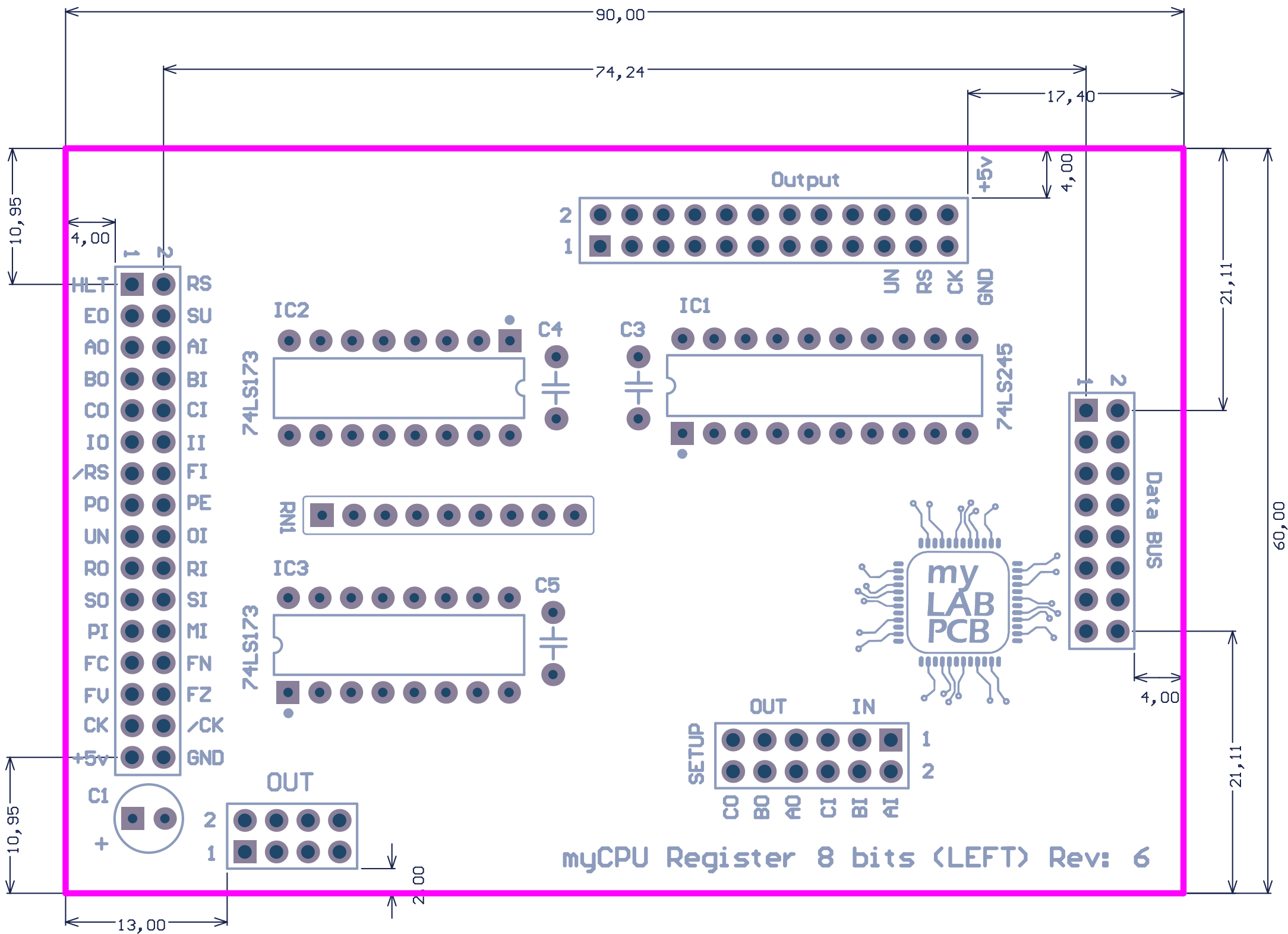


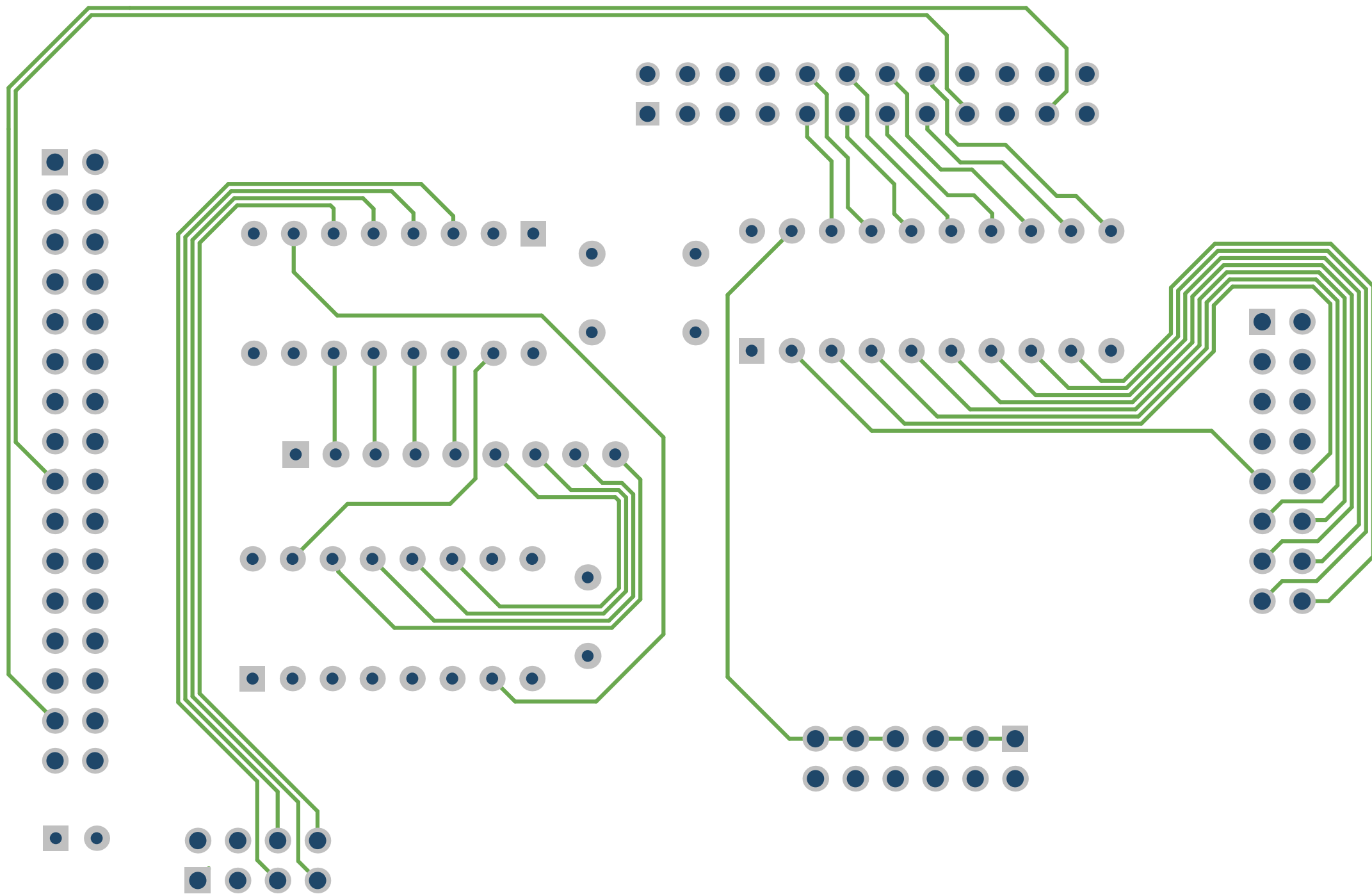
Project: myCPU Register 8 bit LEFT

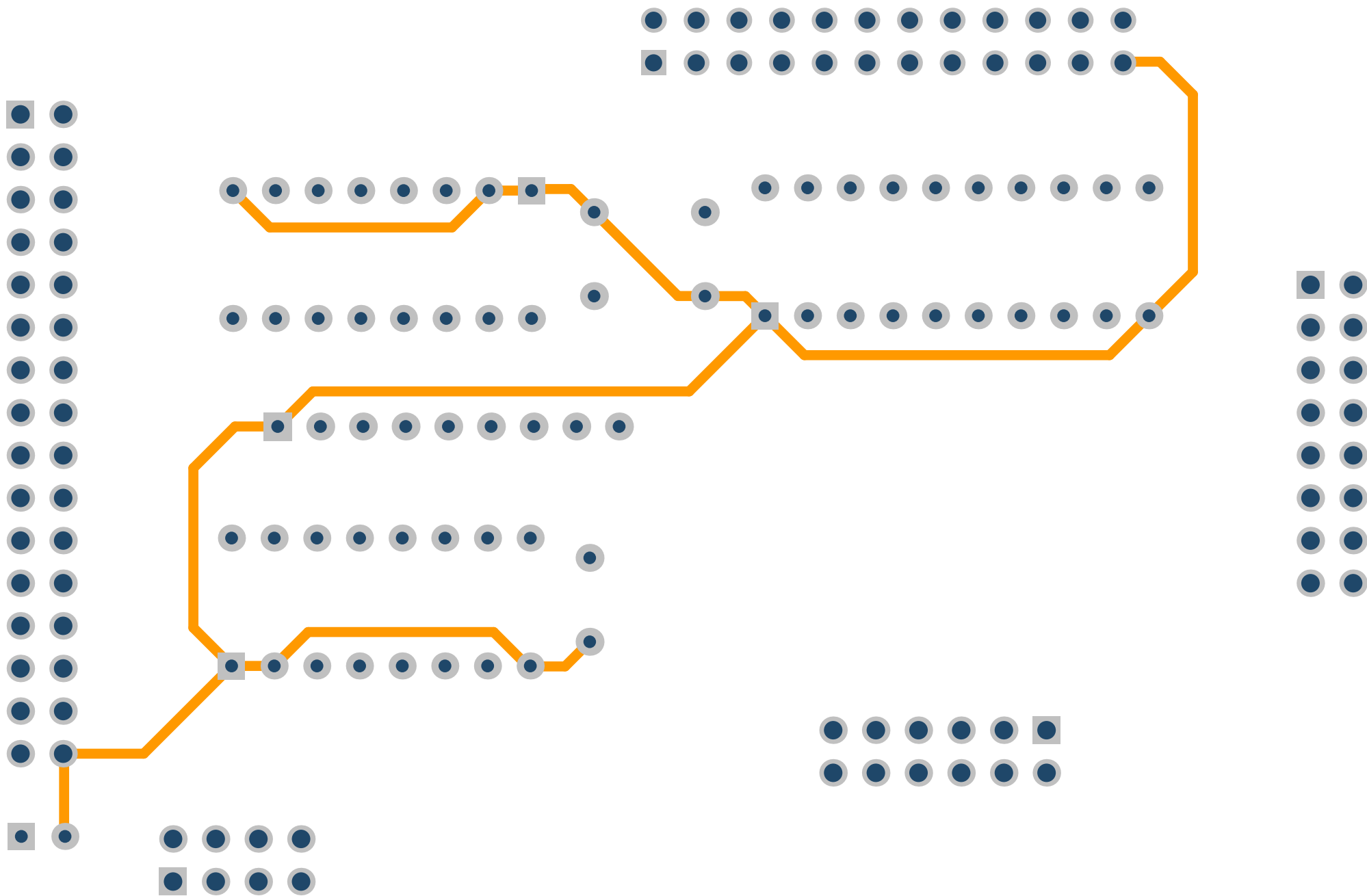
Revision: 6

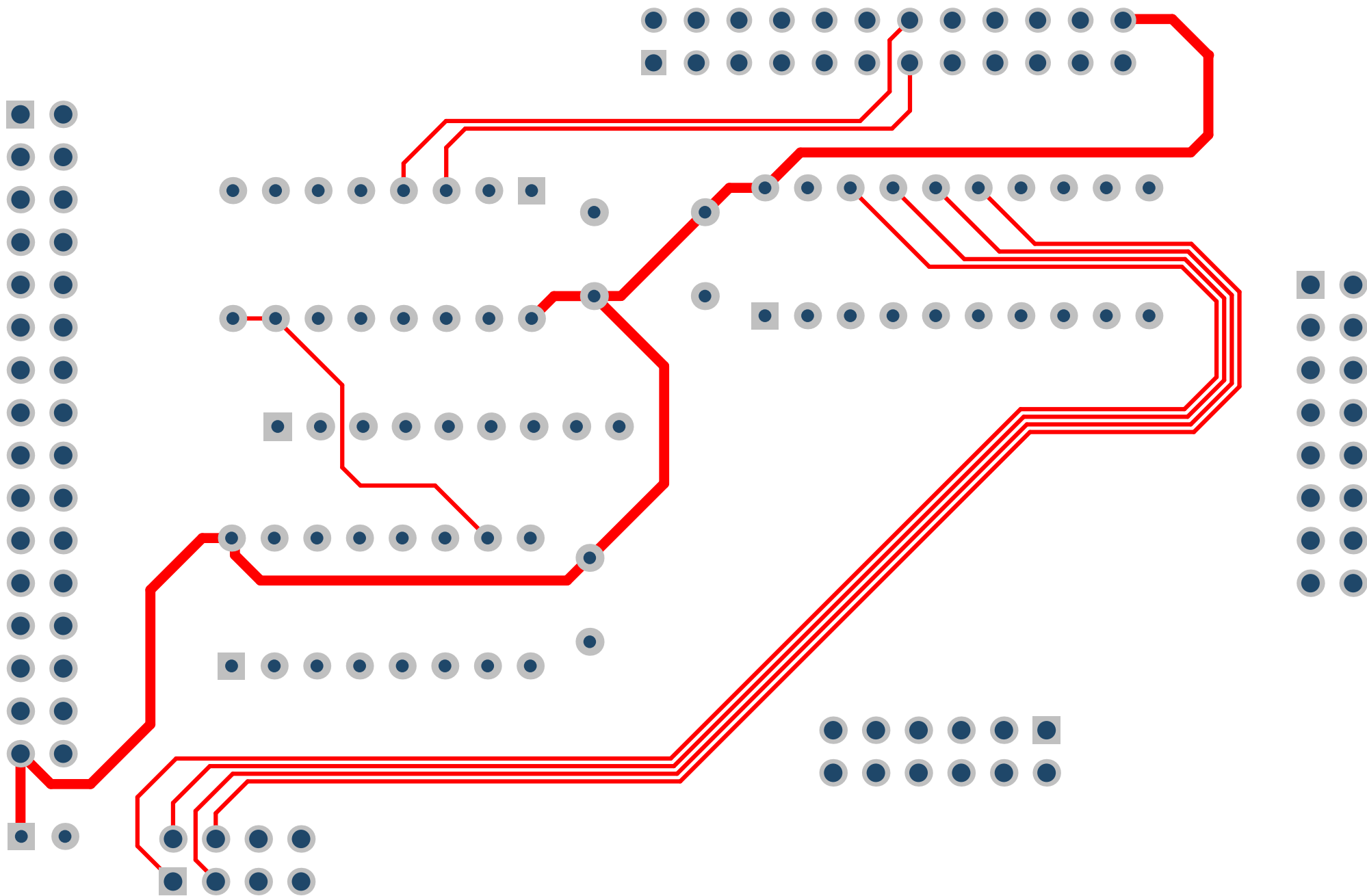
Date: 09/01/2023

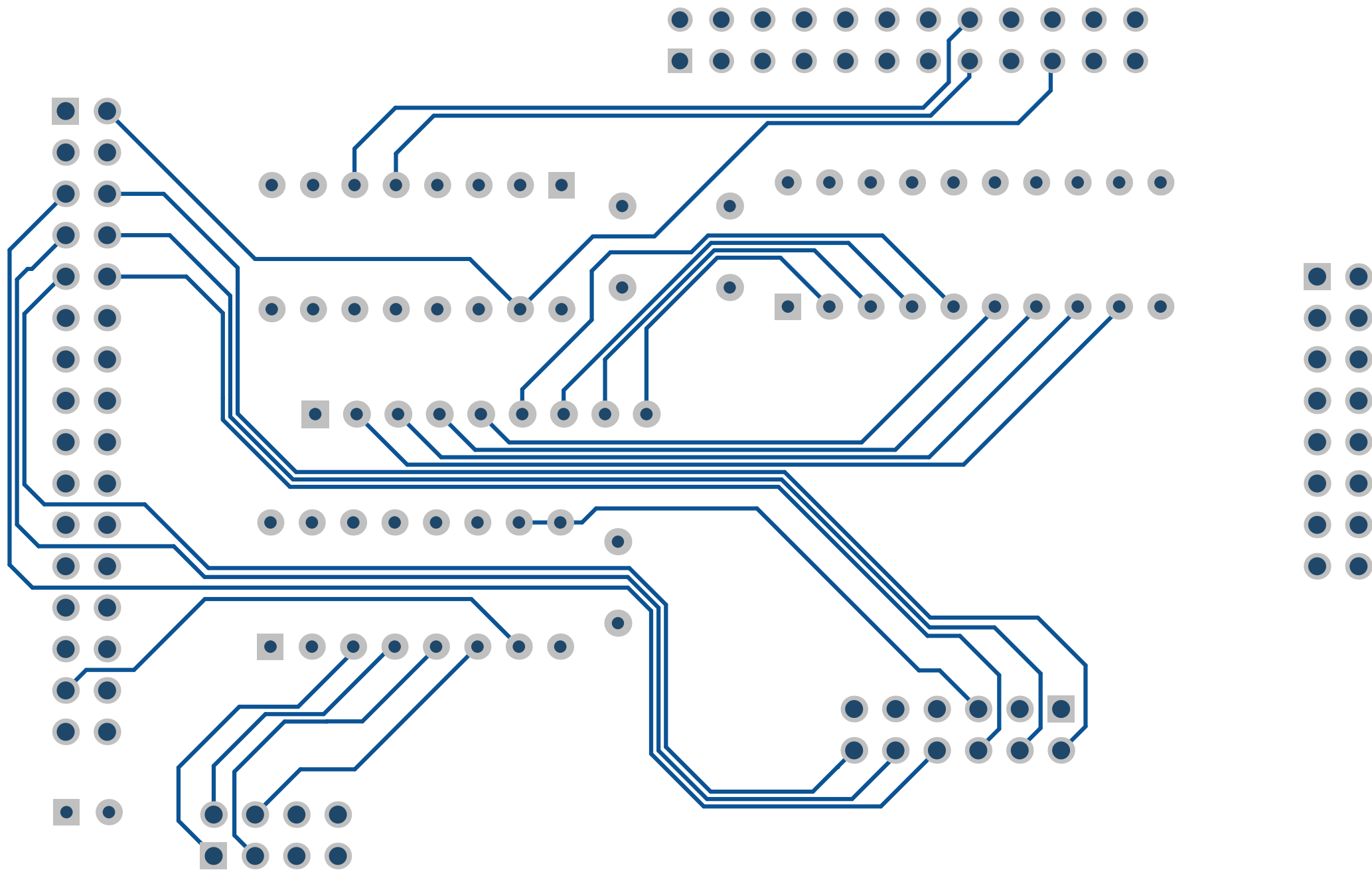
Author: Rafa Hernández















# Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10uF	1
C3, C4, C5	Ceramic or tantalum capacitor	100nF	3
IC1	Non inverting bus transceiver	74LS245	1
IC2, IC3	4-bit D-Type Register with 3 state outputs	74LS173	2
JP1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 12p	12p	1
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical,	24p	1
P4	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	1
RN1	Resistor array 8 elements,9 pins	680Ω	1



# Assembly List

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10uF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC2	4-bit D-Type Register with 3 state outputs	74LS173
IC3	4-bit D-Type Register with 3 state outputs	74LS173
JP1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 12p	12p
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P4	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
RN1	Resistor array 8 elements, 9 pins	680Ω