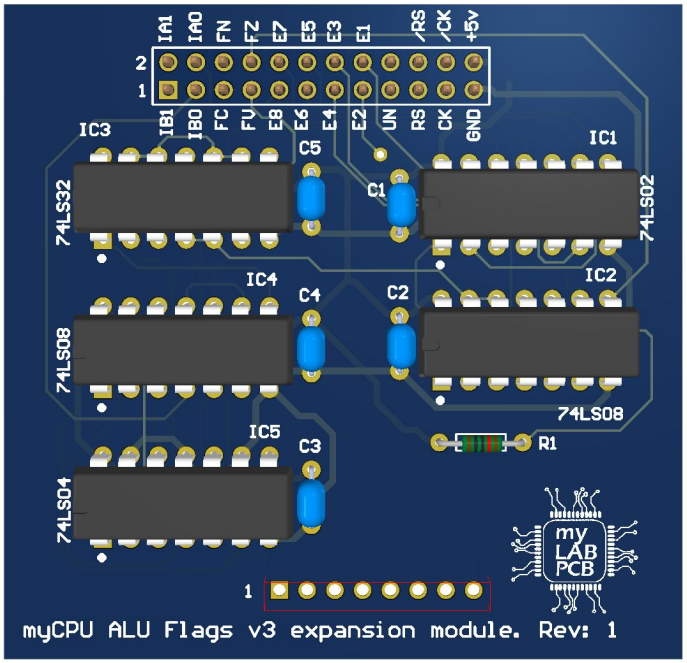
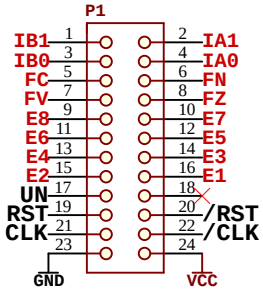
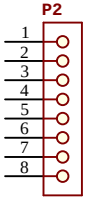

IA1
IA0
FN
FZ
E7
E5
E3
E1
/RS
/CK
+5v
2
1
IB1
IB0
FC
FV
E8
E6
E4
E2
UN
RS
CK
GND
IC3
74LS32
C5
C1
IC1
74LS02
IC4
74LS08
C4
C2
IC2
74LS08
IC5
74LS04
C3
R1
1
my LAB PCB
myCPU ALU Flags v3 expansion module. Rev: 1

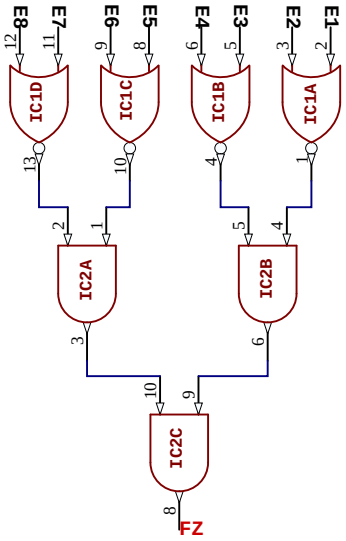
INPUT Data Connector



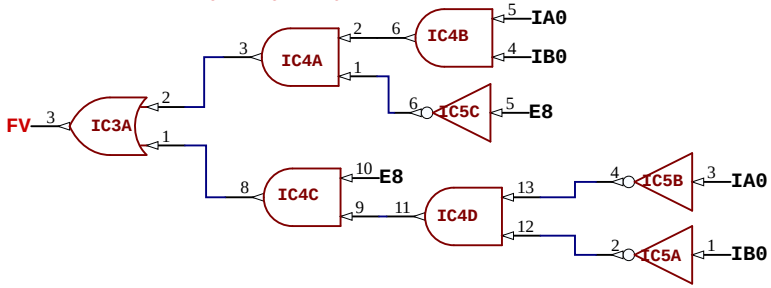


Overflow flag logic. Cover the cases when SUM result sign is different than sign of operands (A,B). It means SUM result is 2's complement overflow.
Out of range (-128, 127).

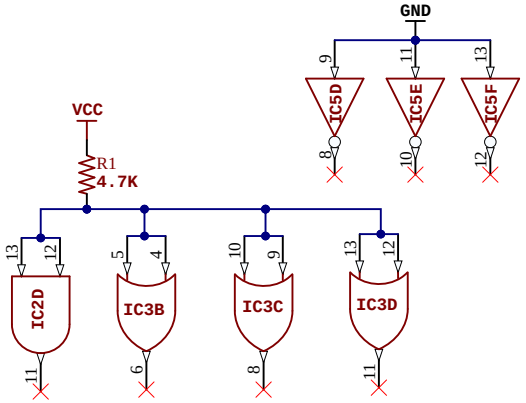
ZERO FLAG

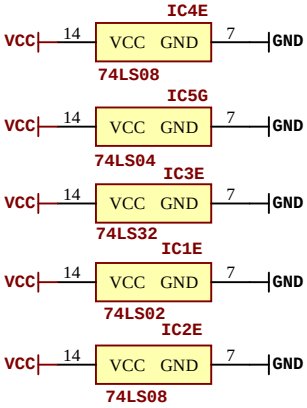


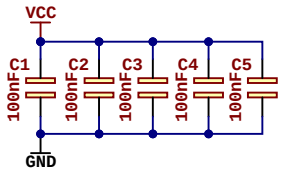
OVERFLOW FLAG



Unused TTL Inputs

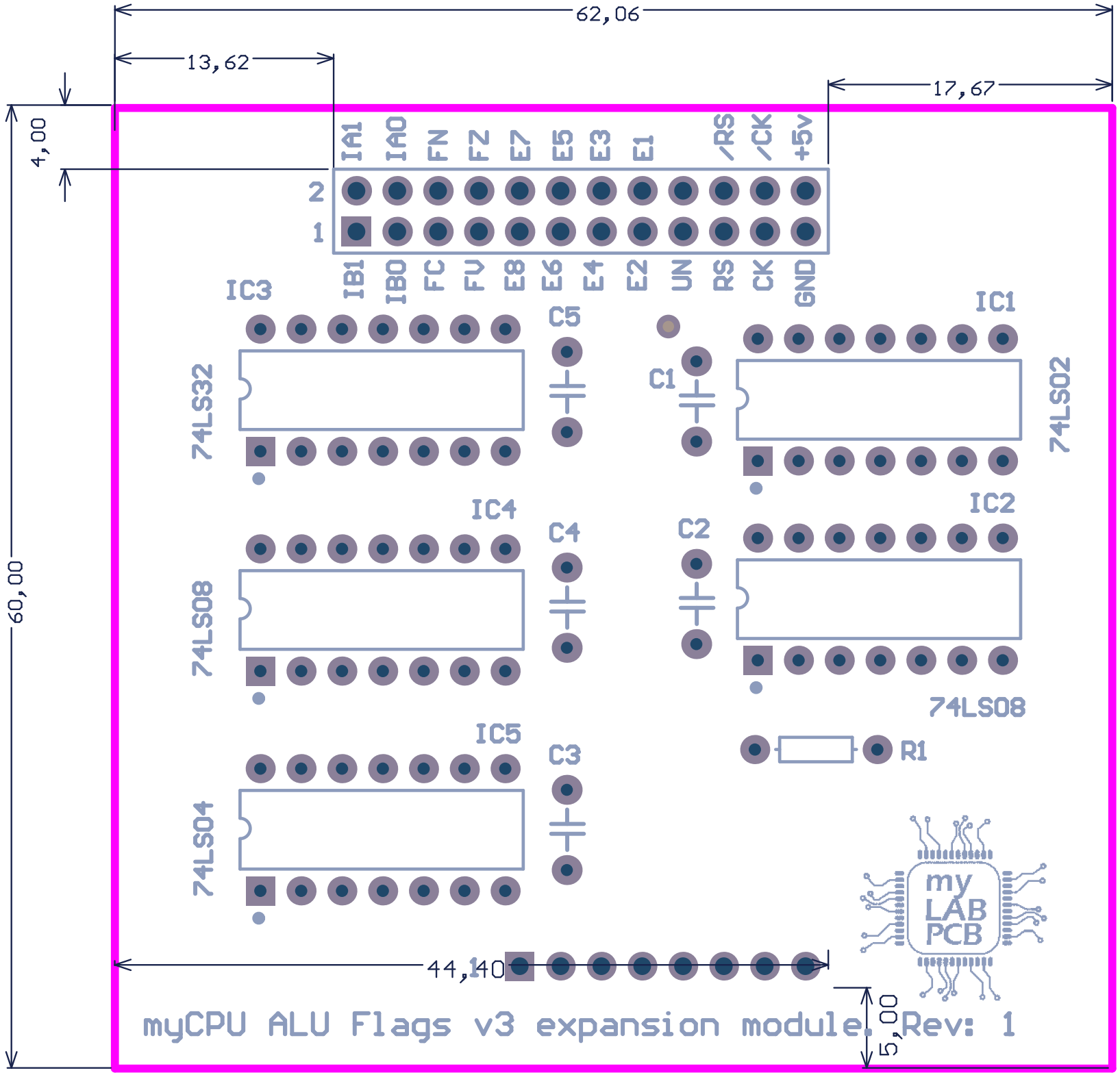


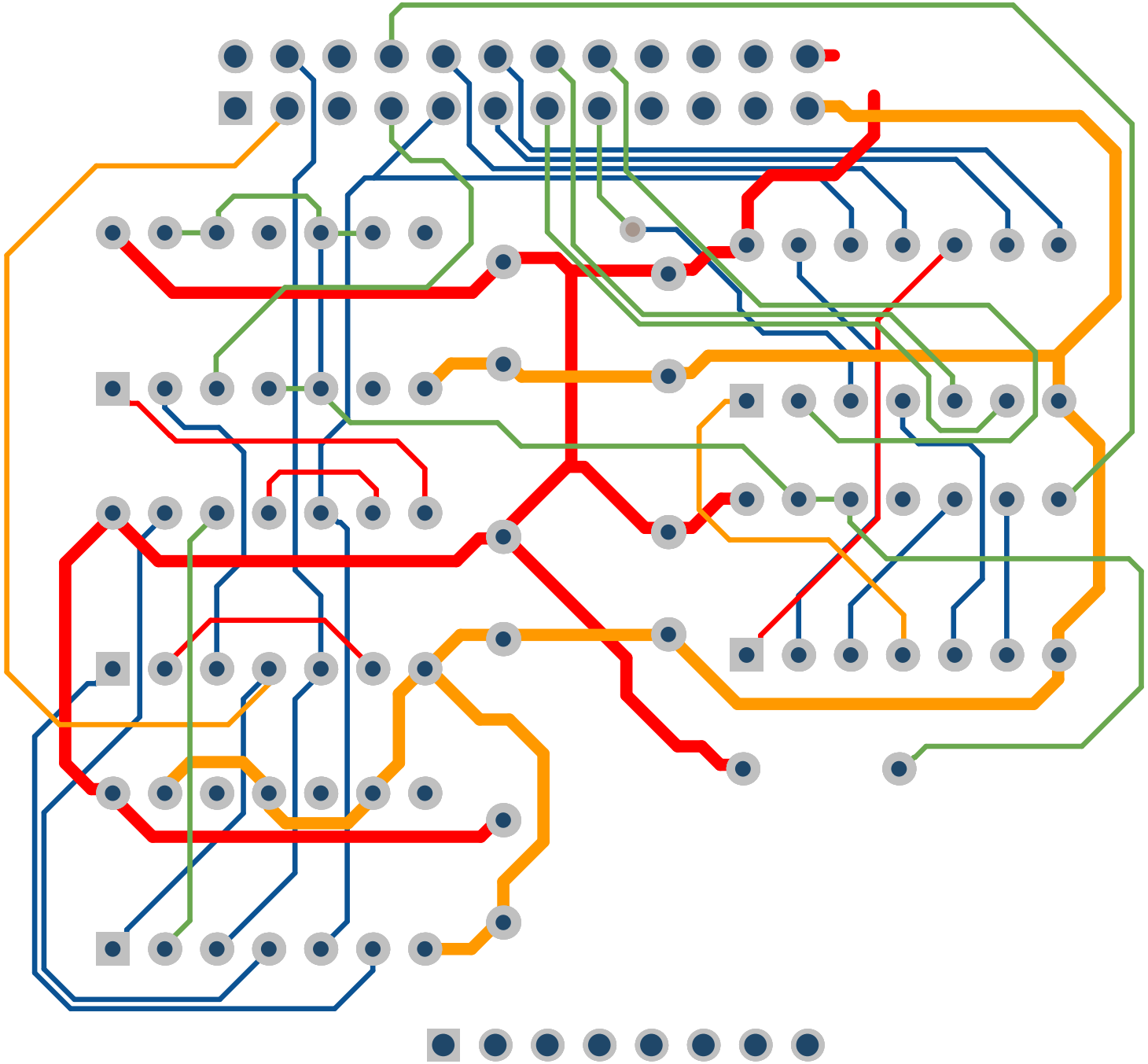




Decoupling Capacitors

Project: myCPU Expansion module	
Revision: 1	**Date:** 22/11/2022
Author: Rafa Hernández	


62,06
13,62
17,67
4,00
60,00
IA1
IA0
FN
FZ
E7
E5
E3
E1
/RS
/CK
+5v
2
1
IB1
IB0
FC
FV
E8
E6
E4
E2
UN
RS
CK
GND
IC3
74LS32
C5
C1
IC1
74LS02
IC4
74LS08
C4
C2
IC2
74LS08
R1
IC5
74LS04
C3
44,40
5,00
myCPU ALU Flags v3 expansion module, Rev: 1
my
LAB
PCB



Bill of Materials

Designator	Description	Value	Q
C1, C2, C3, C4, C5	Ceramic or tantalum capacitor	100nF	5
IC1	Quad 2-input NOR gates	74LS02	1
IC2, IC4	Quad 2-input AND gates	74LS08	2
IC3	Quad 2-input OR gates.	74LS32	1
IC5	Hex inverters	74LS04	1
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p	1
P2	Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 8	8p	1
R1	Resistor Axial	4.7K	1

Assembly List

Designator	Description	Value
C1	Ceramic or tantalum capacitor	100nF
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Quad 2-input NOR gates	74LS02
IC2	Quad 2-input AND gates	74LS08
IC3	Quad 2-input OR gates.	74LS32
IC4	Quad 2-input AND gates	74LS08
IC5	Hex inverters	74LS04
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P2	Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 8p	8p
R1	Resistor Axial	4.7K