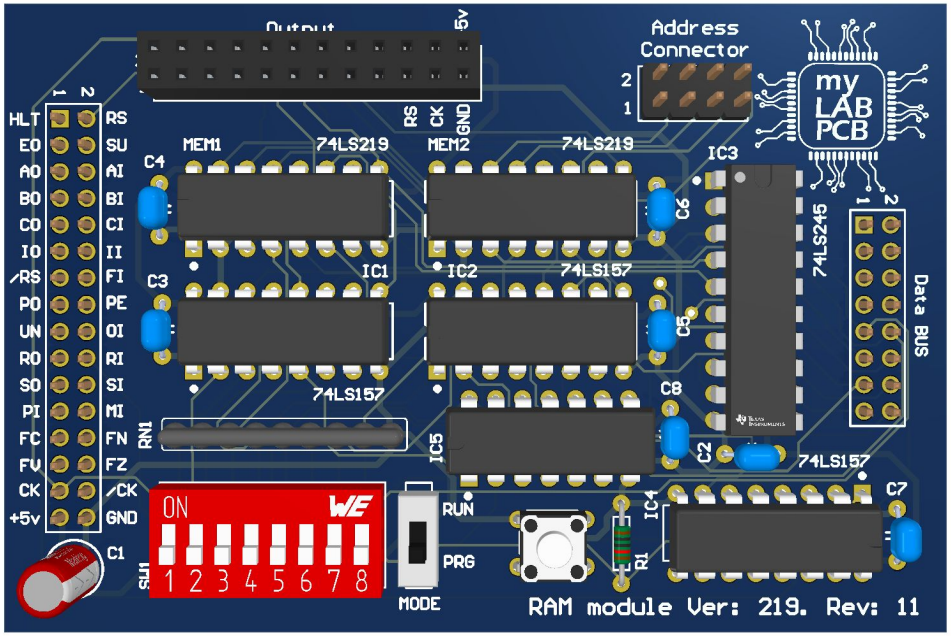
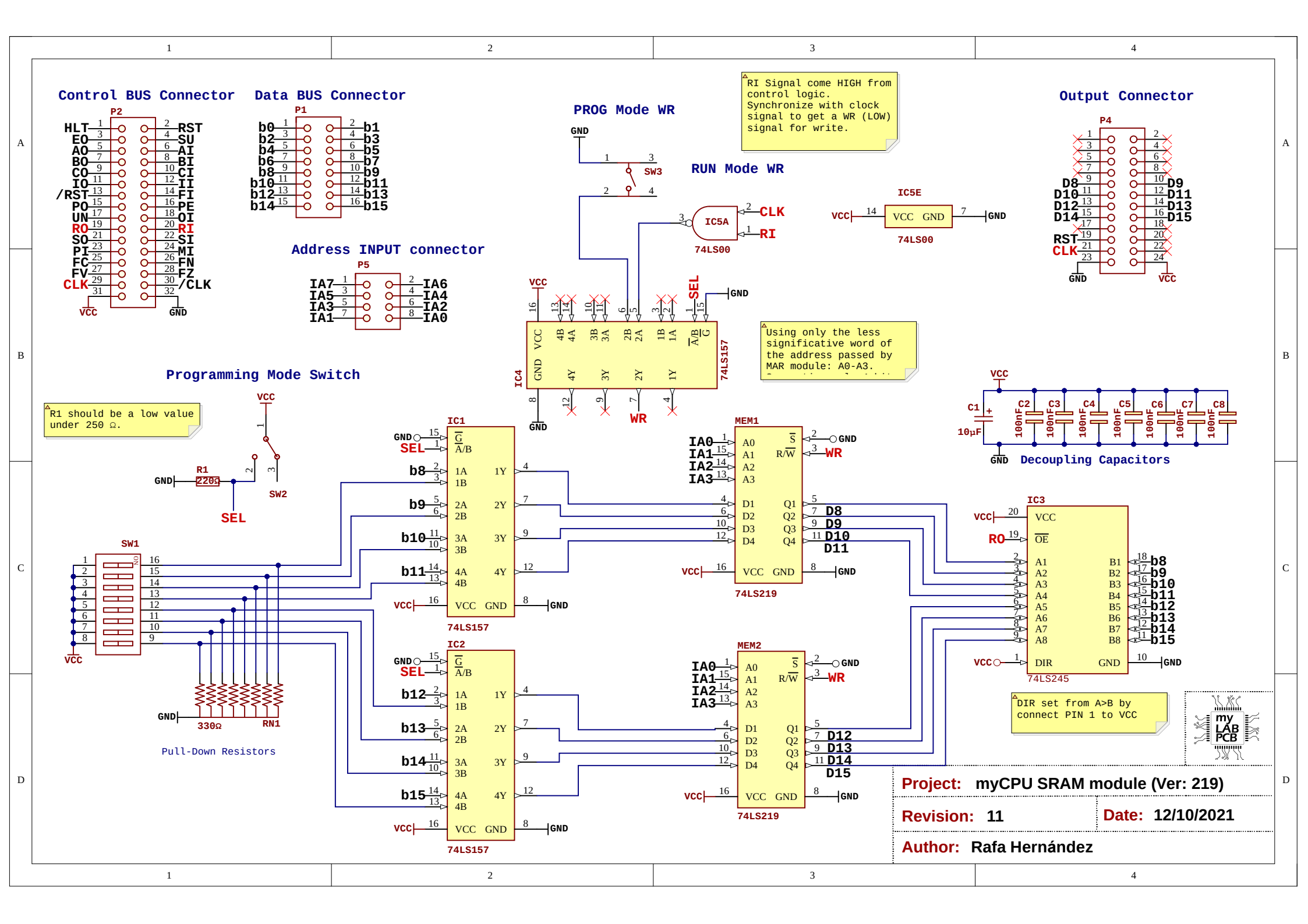
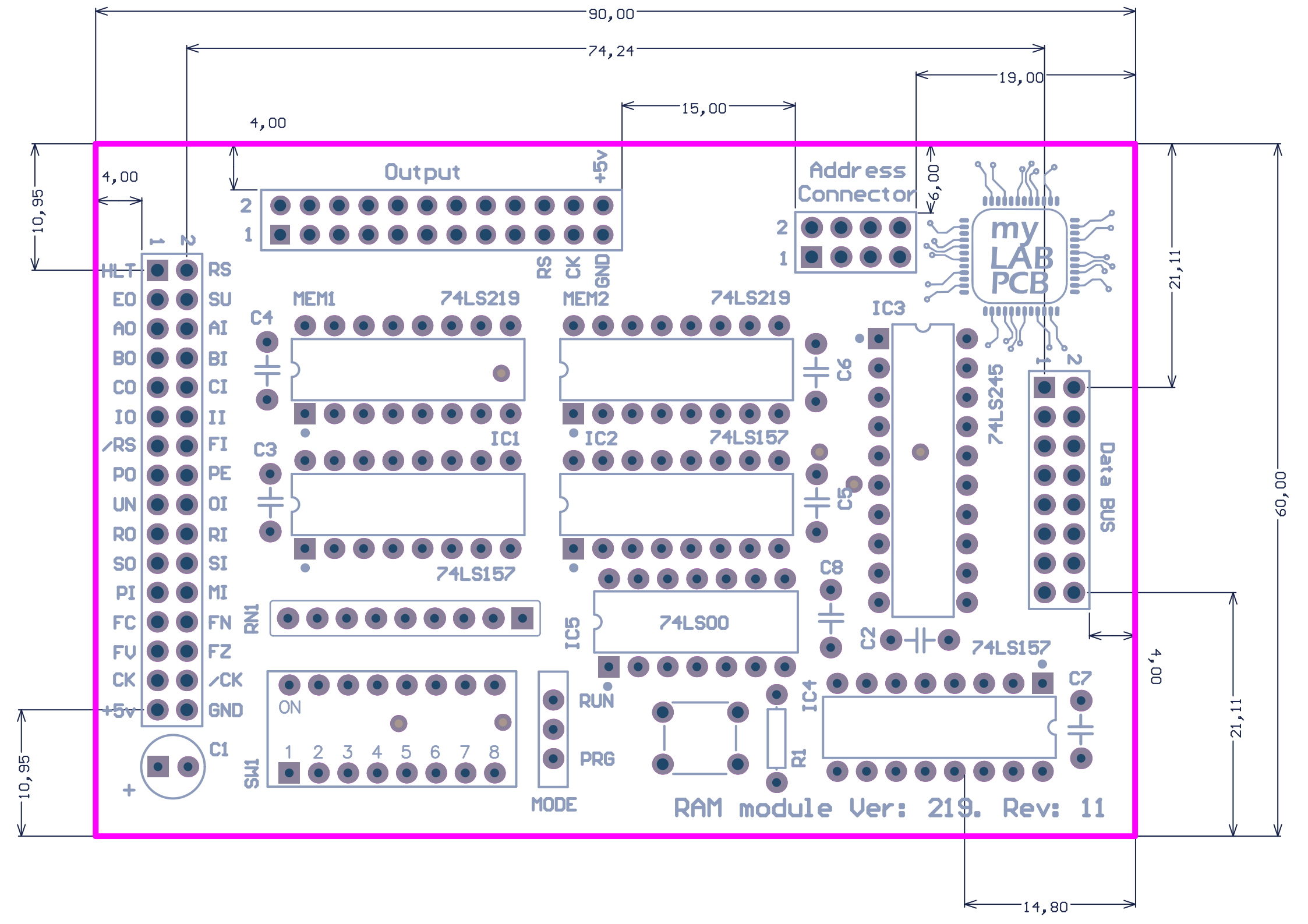
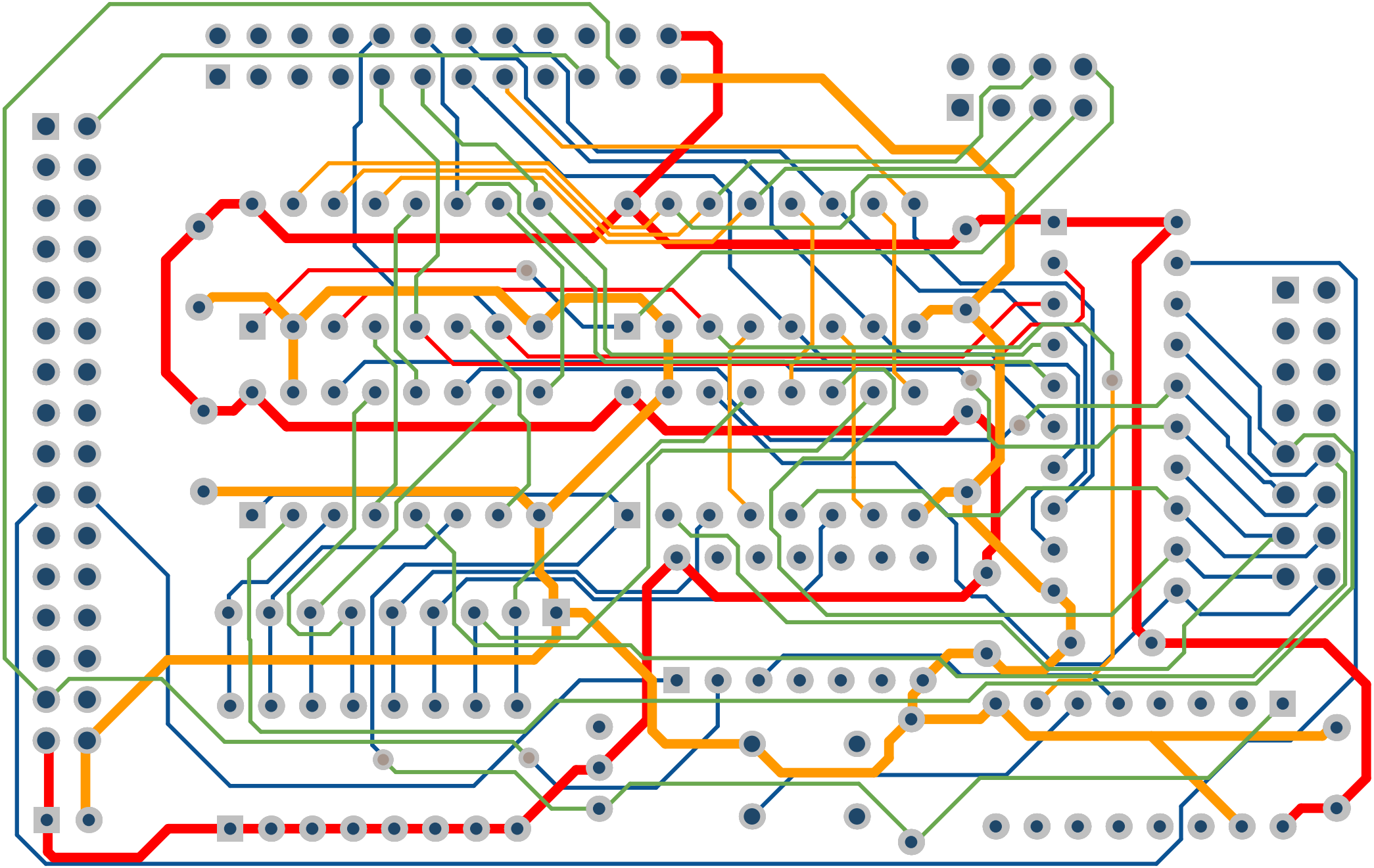

Address
Connector
my
LAB
PCB
5v
RS
CK
GND
MEM1
74LS219
MEM2
74LS219
IC3
74LS245
Data BUS
IC1
IC2
74LS157
74LS157
74LS157
RN1
IC5
IC4
R1
C1
C3
C4
C5
C6
C7
C8
C9
SW1
ON
1 2 3 4 5 6 7 8
RUN
PRG
MODE
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
RAM module Ver: 219. Rev: 11


Control BUS Connector
P2
HLT 1 2 RST
EO 3 4 SU
AO 5 6 AI
BO 7 8 BI
CO 9 10 CI
IO 11 12 II
/RST 13 14 FI
PO 15 16 PE
UN 17 18 OI
RO 19 20 RI
SO 21 22 SI
PI 23 24 MI
FC 25 26 FN
FV 27 28 FZ
CLK 29 30 /CLK
31 32
VCC GND
Data BUS Connector
P1
b0 1 2 b1
b2 3 4 b3
b4 5 6 b5
b6 7 8 b7
b8 9 10 b9
b10 11 12 b11
b12 13 14 b13
b14 15 16 b15
Address INPUT connector
P5
IA7 1 2 IA6
IA5 3 4 IA4
IA3 5 6 IA2
IA1 7 8 IA0
PROG Mode WR
GND
SW3
RUN Mode WR
IC5A
74LS00
CLK
RI
RI Signal come HIGH from control logic. Synchronize with clock signal to get a WR (LOW) signal for write.
IC5E
VCC GND
74LS00
Output Connector
P4
D8 D9
D10 D11
D12 D13
D14 D15
RST
CLK
GND VCC
Using only the less significative word of the address passed by MAR module: A0-A3.
IC4
74LS157
SEL
WR
Programming Mode Switch
R1 should be a low value under 250 Ω.
R1
220Ω
SW2
SEL
SW1
VCC
GND
330Ω
RN1
Pull-Down Resistors
IC1
74LS157
IC2
74LS157
MEM1
74LS219
MEM2
74LS219
IC3
74LS245
DIR set from A>B by connect PIN 1 to VCC
C1
10µF
C2 C3 C4 C5 C6 C7 C8
100nF
Decoupling Capacitors
my LAB PCB
Project: myCPU SRAM module (Ver: 219)
Revision: 11
Date: 12/10/2021
Author: Rafa Hernández


90,00
74,24
19,00
15,00
4,00
4,00
10,95
Output
+5v
2
1
RS
CK
GND
Address
Connector
6,00
my
LAB
PCB
21,11
60,00
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
MEM1
74LS219
MEM2
74LS219
C4
C3
IC1
74LS157
IC2
74LS157
C6
C5
IC3
74LS245
Data BUS
C8
C2
74LS157
RN1
IC5
74LS00
IC4
C7
ON
1 2 3 4 5 6 7 8
SW1
RUN
PRG
MODE
R1
RAM module Ver: 219. Rev: 11
14,80



Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C2, C3, C4, C5, C6, C7, C	Ceramic or tantalum capacitor	100nF	7
IC1, IC2, IC4	4-Bits 2-Line to 1 Line data selector	74LS157	3
IC3	Non inverting bus transceiver	74LS245	1
IC5	Quad 2-input NAND gates	74LS00	1
MEM1, MEM2	SRAM 16x8 bits, not inverted outputs	74LS219	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P4	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p	1
P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	1
R1	Resistor axial	220Ω	1
RN1	Resistor array 8 elements,9 pins	330Ω	1
SW1	DIP switch 8 positions	8 pos	1
SW2	Mini slide switch 2 pos, 3 pins		1
SW3	Tactile button 6 mm	6mm	1

Assembly List

Desig.	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C2	Ceramic or tantalum capacitor	100nF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
C6	Ceramic or tantalum capacitor	100nF
C7	Ceramic or tantalum capacitor	100nF
C8	Ceramic or tantalum capacitor	100nF
IC1	4-Bits 2-Line to 1 Line data selector	74LS157
IC2	4-Bits 2-Line to 1 Line data selector	74LS157
IC3	Non inverting bus transceiver	74LS245
IC4	4-Bits 2-Line to 1 Line data selector	74LS157
IC5	Quad 2-input NAND gates	74LS00
MEM1	SRAM 16x8 bits, not inverted outputs	74LS219
MEM2	SRAM 16x8 bits, not inverted outputs	74LS219
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P4	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
R1	Resistor axial	220Ω
RN1	Resistor array 8 elements,9 pins	330Ω
SW1	DIP switch 8 positions	8 pos
SW2	Mini slide switch 2 pos, 3 pins	
SW3	Tactile button 6 mm	6mm