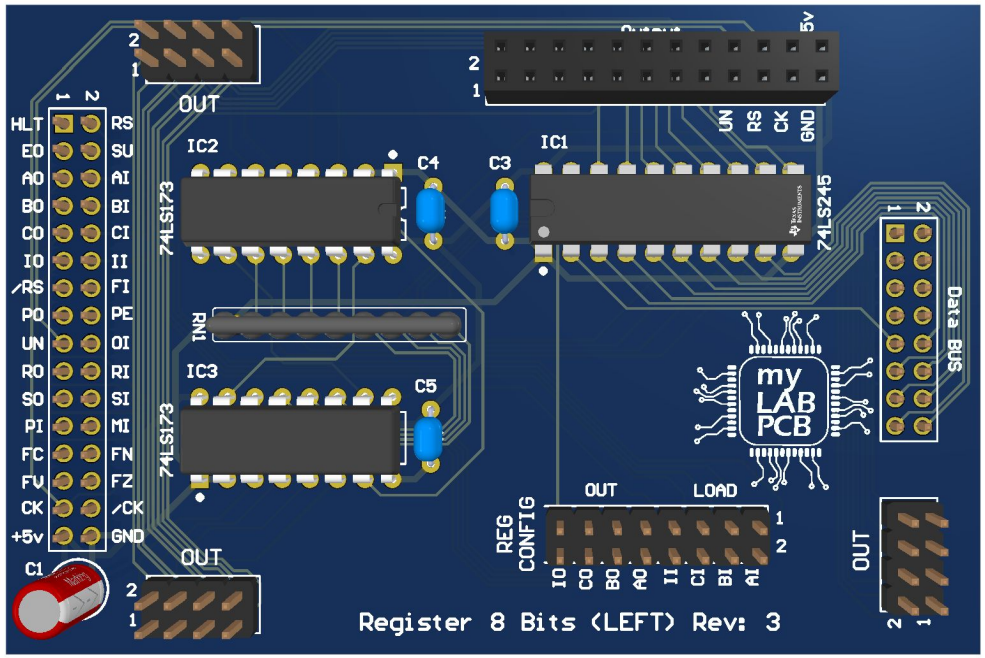
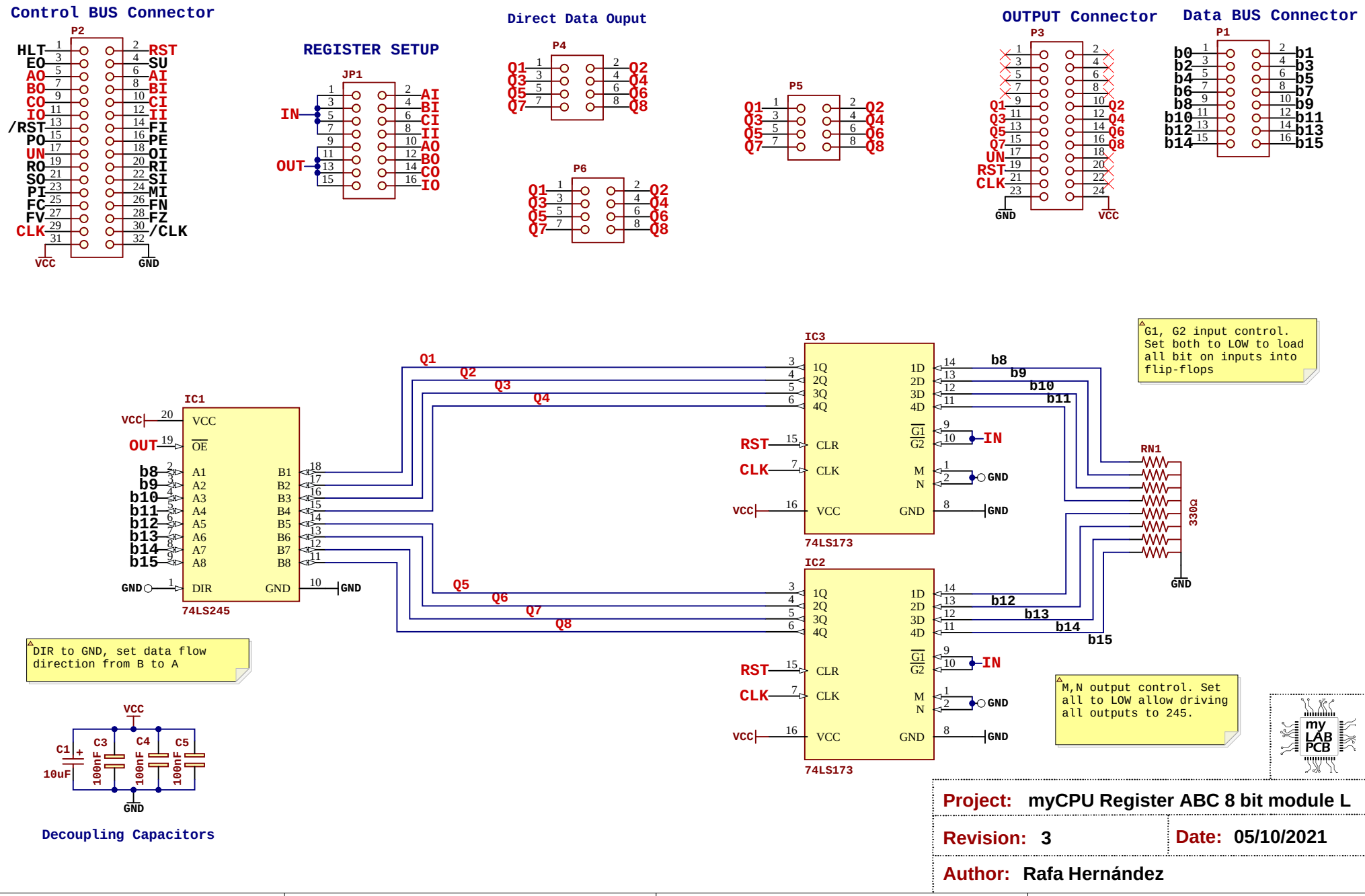
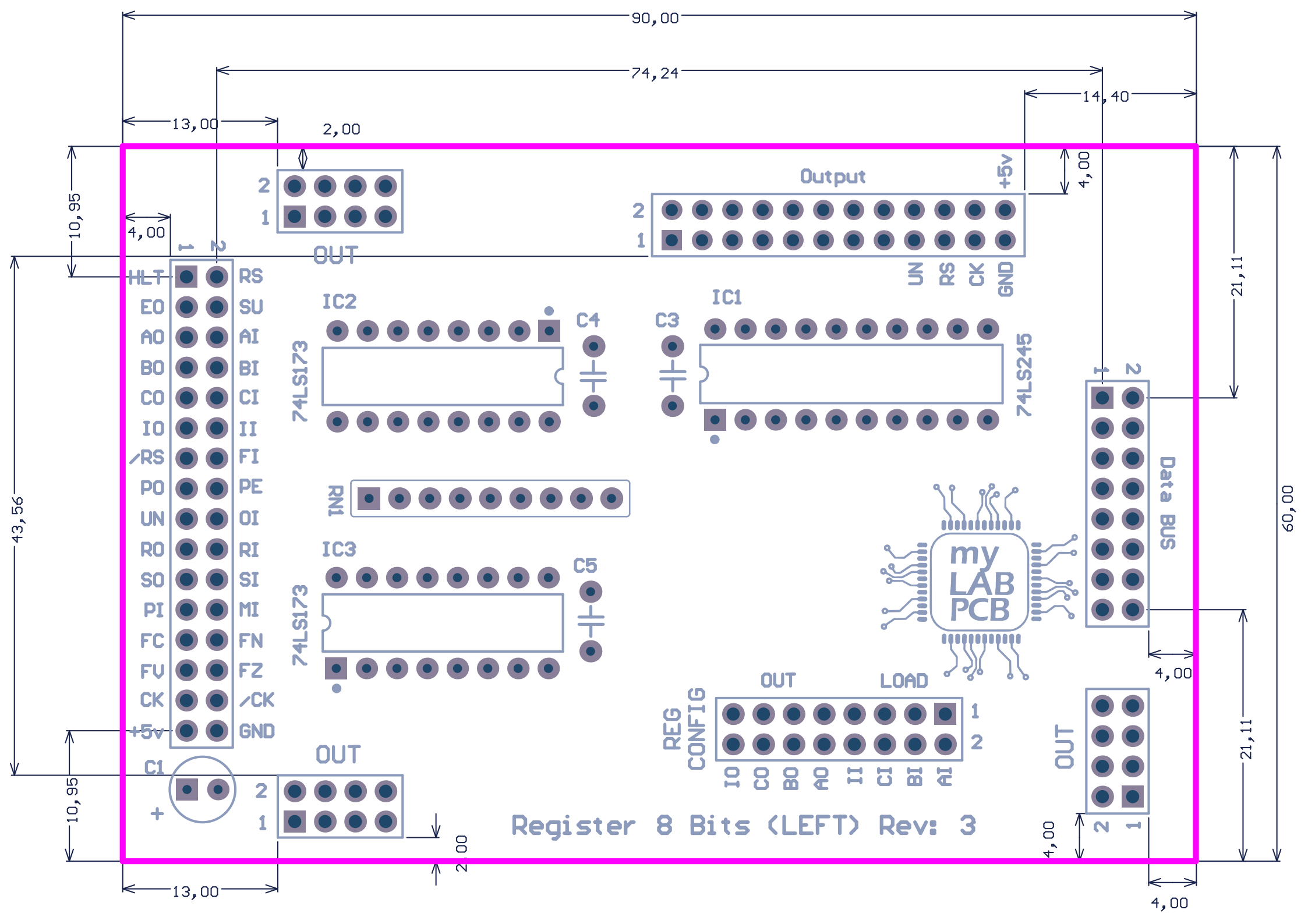
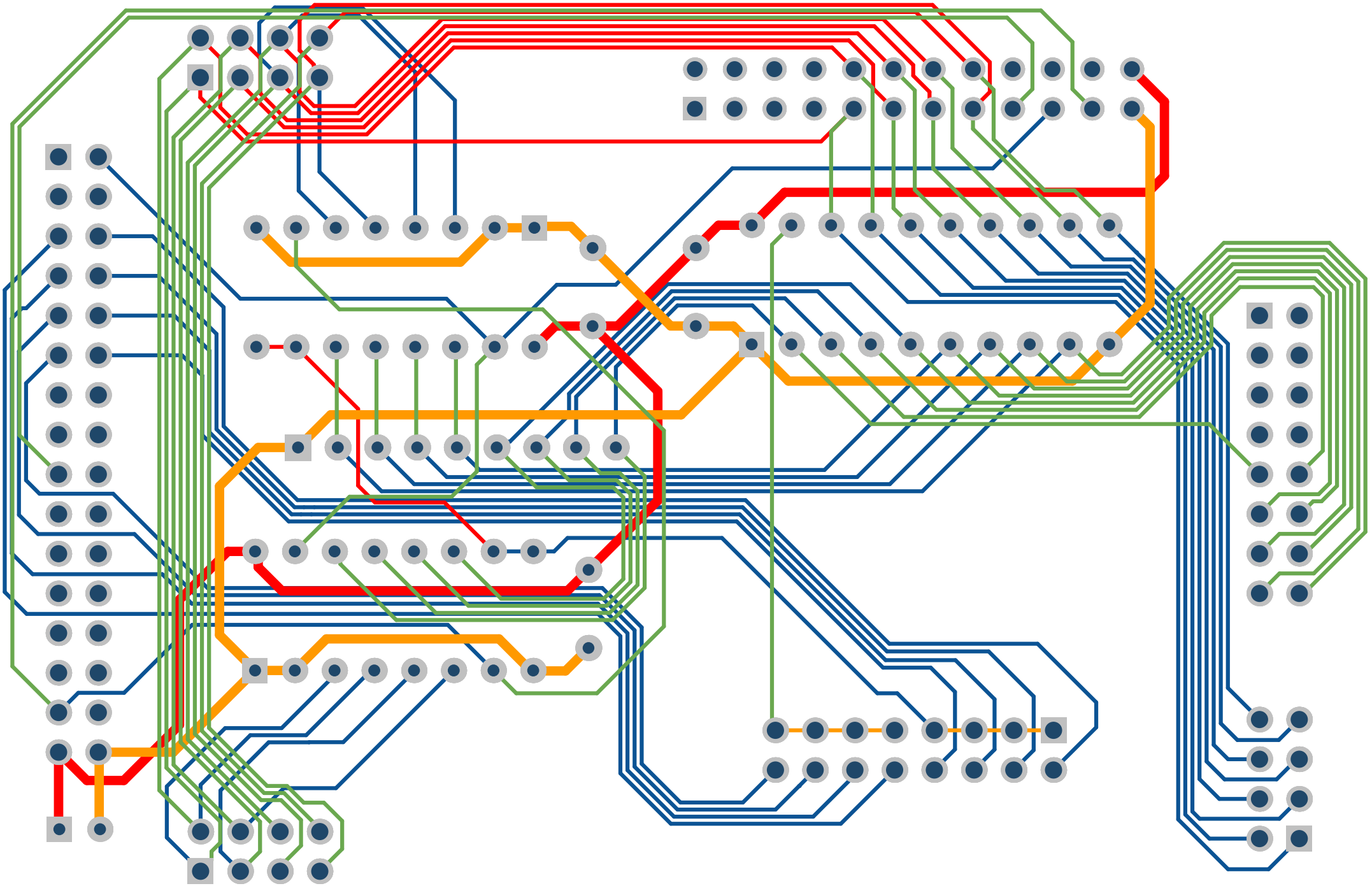

OUT
IC2
74LS173
C4
C3
IC1
74LS245
5v
UN
RS
CK
GND
Data BUS
RN1
IC3
74LS173
C5
my
LAB
PCB
OUT
LOAD
REG
CONFIG
IO
CO
BO
AO
II
CI
BI
AI
OUT
C1
OUT
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Register 8 Bits (LEFT) Rev: 3


Control BUS Connector
P2
HLT 1 2 RST
EO 3 4 SU
AO 5 6 AI
BO 7 8 BI
CO 9 10 CI
IO 11 12 II
/RST 13 14 FI
PO 15 16 PE
UN 17 18 OI
RO 19 20 RI
SO 21 22 SI
PI 23 24 MI
FC 25 26 FN
FV 27 28 FZ
CLK 29 30 /CLK
31 32
VCC
GND
REGISTER SETUP
JP1
IN
OUT
1 2 AI
3 4 BI
5 6 CI
7 8 II
9 10 AO
11 12 BO
13 14 CO
15 16 IO
Direct Data Ouput
P4
Q1 1 2 Q2
Q3 3 4 Q4
Q5 5 6 Q6
Q7 7 8 Q8
P5
Q1 1 2 Q2
Q3 3 4 Q4
Q5 5 6 Q6
Q7 7 8 Q8
P6
Q1 1 2 Q2
Q3 3 4 Q4
Q5 5 6 Q6
Q7 7 8 Q8
OUTPUT Connector
P3
Q1 1 2 Q2
Q3 3 4 Q4
Q5 5 6 Q6
Q7 7 8 Q8
UN 9 10
RST 11 12
CLK 13 14
15 16
17 18
19 20
21 22
23 24
GND
VCC
Data BUS Connector
P1
b0 1 2 b1
b2 3 4 b3
b4 5 6 b5
b6 7 8 b7
b8 9 10 b9
b10 11 12 b11
b12 13 14 b13
b14 15 16 b15
IC1
74LS245
VCC 20 VCC
OUT 19 OE
b8 2 A1 B1 18 Q1
b9 3 A2 B2 17 Q2
b10 4 A3 B3 16 Q3
b11 5 A4 B4 15 Q4
b12 6 A5 B5 14
b13 7 A6 B6 13
b14 8 A7 B7 12
b15 9 A8 B8 11
GND 1 DIR GND 10 GND
IC3
74LS173
1Q 1D 14 b8
2Q 2D 13 b9
3Q 3D 12 b10
4Q 4D 11 b11
G1 9
G2 10 IN
RST 15 CLR
CLK 7 CLK
M 1 GND
N 2 GND
VCC 16 VCC GND 8 GND
IC2
74LS173
1Q 1D 14 b12
2Q 2D 13 b13
3Q 3D 12 b14
4Q 4D 11 b15
G1 9
G2 10 IN
RST 15 CLR
CLK 7 CLK
M 1 GND
N 2 GND
VCC 16 VCC GND 8 GND
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
RN1
330Ω
GND
G1, G2 input control. Set both to LOW to load all bit on inputs into flip-flops
DIR to GND, set data flow direction from B to A
M,N output control. Set all to LOW allow driving all outputs to 245.
VCC
C1 10uF
C3 100nF
C4 100nF
C5 100nF
GND
Decoupling Capacitors
my LAB PCB
Project: myCPU Register ABC 8 bit module L
Revision: 3
Date: 05/10/2021
Author: Rafa Hernández


90,00
74,24
14,40
13,00
2,00
10,95
4,00
43,56
21,11
60,00
OUT
Output
+5v
UN
RS
CK
GND
IC1
IC2
IC3
74LS173
74LS245
C1
C3
C4
C5
RN1
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FU
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Data BUS
LOAD
REG CONFIG
IO
CO
BO
AO
II
CI
BI
AI
my LAB PCB
Register 8 Bits (LEFT) Rev: 3



Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10uF	1
C3, C4, C5	Ceramic or tantalum capacitor	100nF	3
IC1	Non inverting bus transceiver	74LS245	1
IC2, IC3	4-bit D-Type Register with 3 state outputs	74LS173	2
JP1, P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	2
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p	1
P4, P5, P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	3
RN1	Resistor array 8 elements,9 pins	330Ω	1

Assembly List

Desig.	Description	Value
C1	Electrolytic capacitor 16v/50v	10uF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC2	4-bit D-Type Register with 3 state outputs	74LS173
IC3	4-bit D-Type Register with 3 state outputs	74LS173
JP1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P4	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
RN1	Resistor array 8 elements,9 pins	330Ω