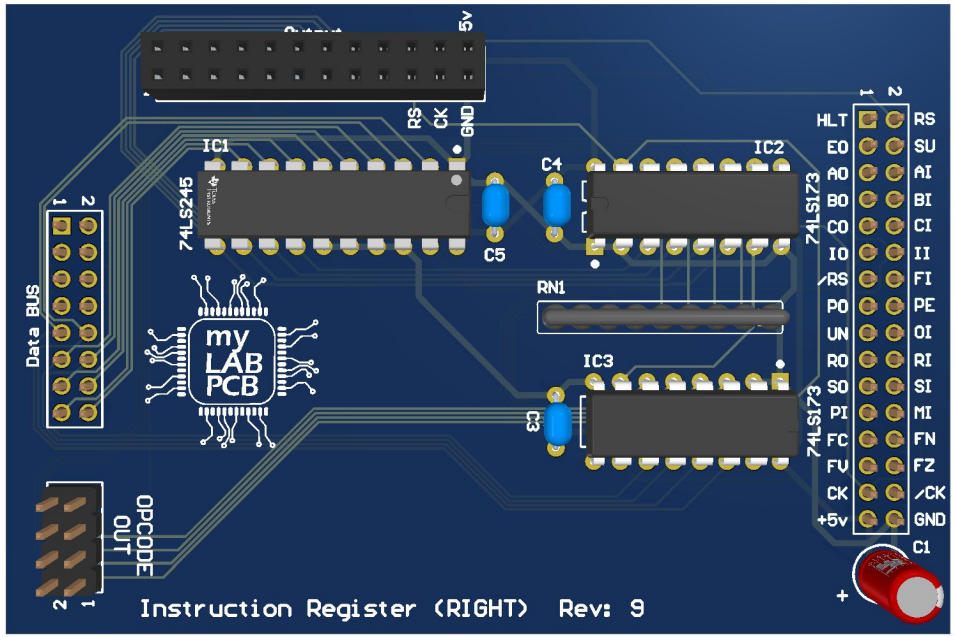
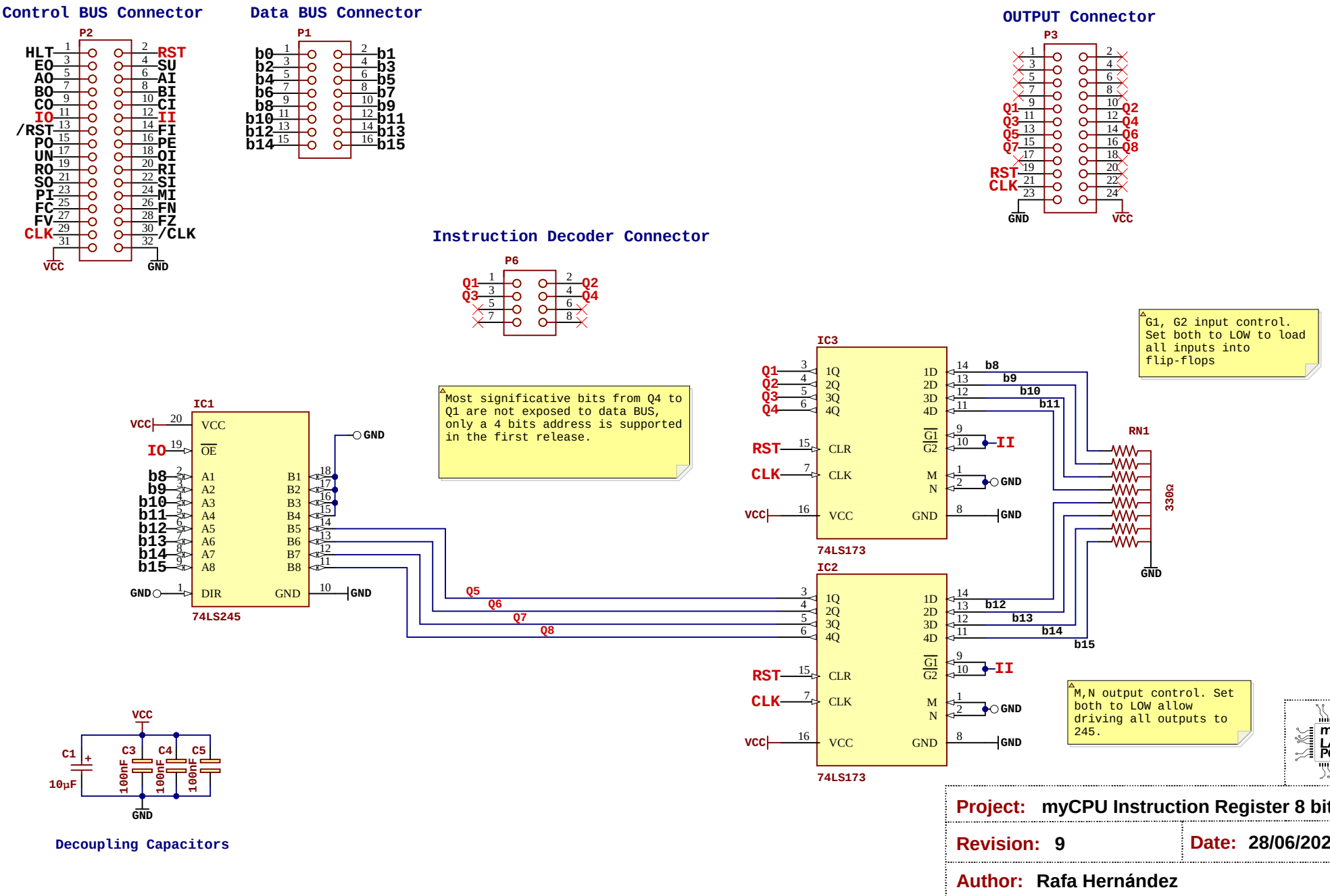
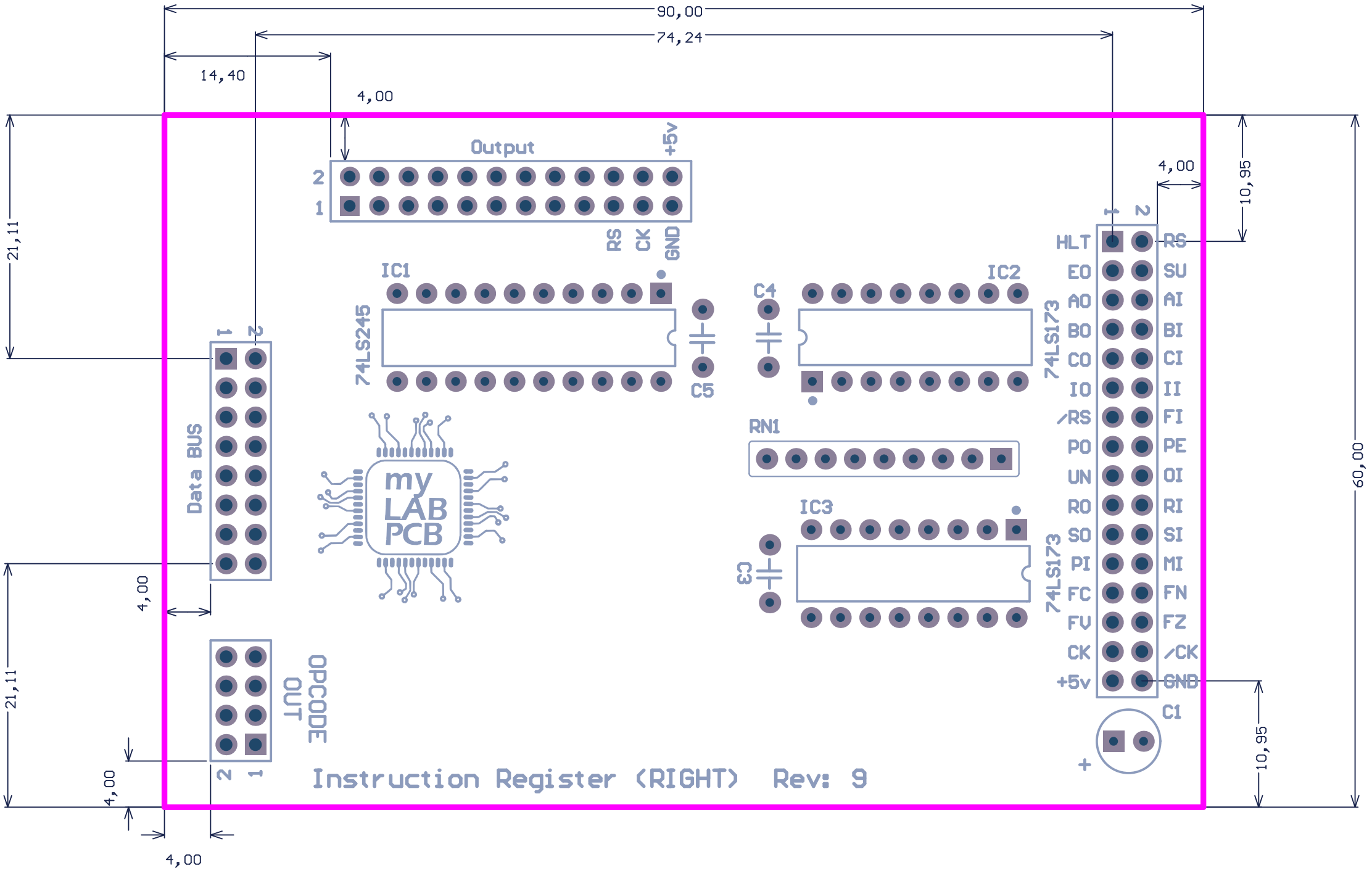
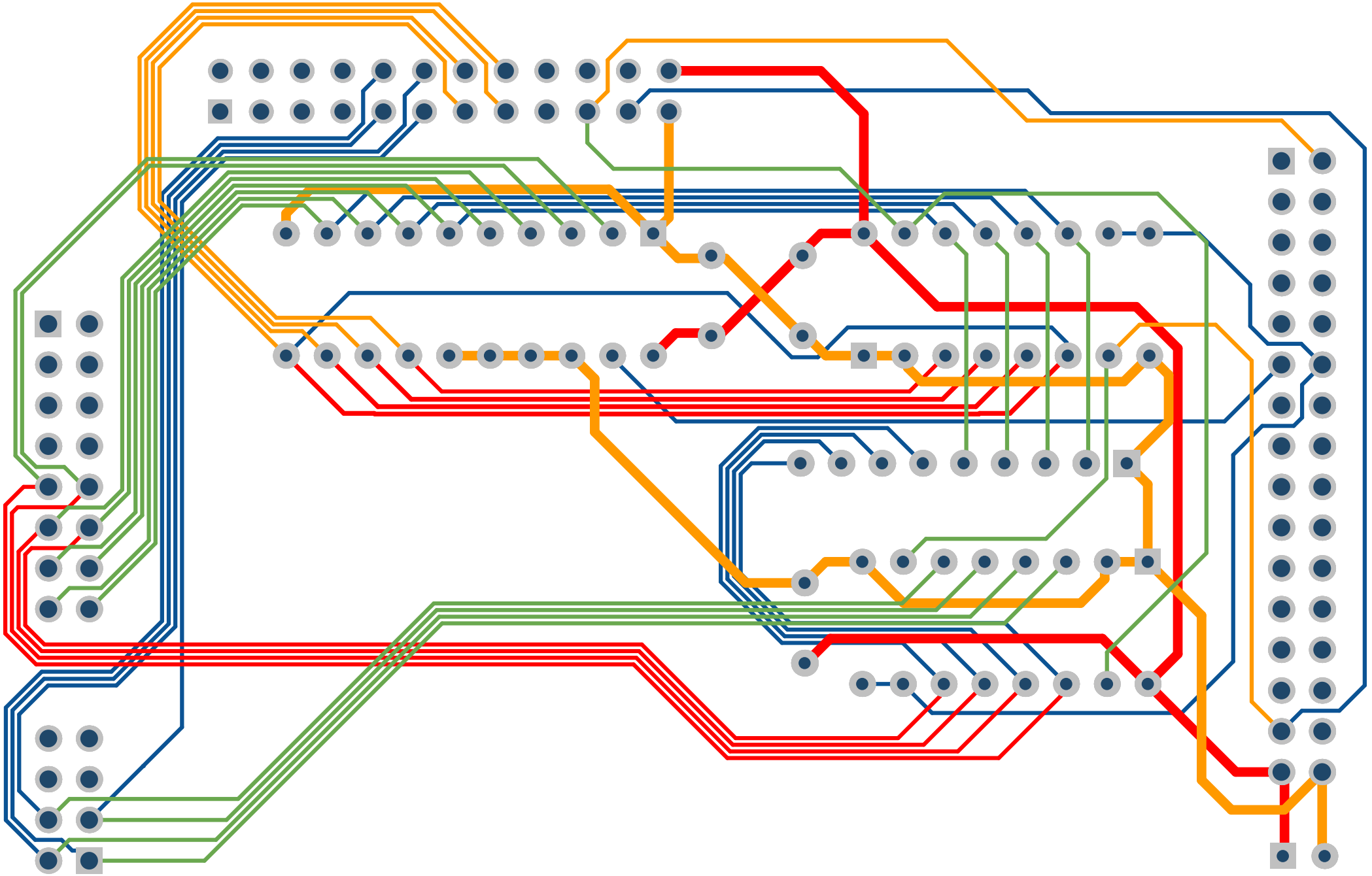

5v
RS
CK
GND
IC1
74LS245
C5
C4
IC2
74LS173
RN1
IC3
C3
74LS173
Data BUS
OPCODE OUT
my LAB PCB
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
Instruction Register (RIGHT) Rev: 9


Control BUS Connector
P2
HLT 1 2 RST
EO 3 4 SU
AO 5 6 AI
BO 7 8 BI
CO 9 10 CI
IO 11 12 II
/RST 13 14 FI
PO 15 16 PE
UN 17 18 OI
RO 19 20 RI
SO 21 22 SI
PI 23 24 MI
FC 25 26 FN
FV 27 28 FZ
CLK 29 30 /CLK
31 32
VCC
GND
Data BUS Connector
P1
b0 1 2 b1
b2 3 4 b3
b4 5 6 b5
b6 7 8 b7
b8 9 10 b9
b10 11 12 b11
b12 13 14 b13
b14 15 16 b15
OUTPUT Connector
P3
1 2
3 4
5 6
7 8
Q1 9 10 Q2
Q3 11 12 Q4
Q5 13 14 Q6
Q7 15 16 Q8
RST 17 18
CLK 19 20
21 22
GND 23 24 VCC
Instruction Decoder Connector
P6
Q1 1 2 Q2
Q3 3 4 Q4
5 6
7 8
Most significative bits from Q4 to Q1 are not exposed to data BUS, only a 4 bits address is supported in the first release.
G1, G2 input control. Set both to LOW to load all inputs into flip-flops
IC1
VCC 20 VCC
IO 19 OE
b8 2 A1 B1 18
b9 3 A2 B2 17
b10 4 A3 B3 16
b11 5 A4 B4 15
b12 6 A5 B5 14
b13 7 A6 B6 13
b14 8 A7 B7 12
b15 9 A8 B8 11
GND 1 DIR GND 10 GND
GND
74LS245
IC3
Q1 3 1Q 1D 14 b8
Q2 4 2Q 2D 13 b9
Q3 5 3Q 3D 12 b10
Q4 6 4Q 4D 11 b11
RST 15 CLR
CLK 7 CLK
VCC 16 VCC
G1 9
G2 10 II
M 1
N 2 GND
GND 8 GND
74LS173
IC2
Q5 3 1Q 1D 14 b12
Q6 4 2Q 2D 13 b13
Q7 5 3Q 3D 12 b14
Q8 6 4Q 4D 11 b15
RST 15 CLR
CLK 7 CLK
VCC 16 VCC
G1 9
G2 10 II
M 1
N 2 GND
GND 8 GND
74LS173
RN1
330Ω
GND
M,N output control. Set both to LOW allow driving all outputs to 245.
VCC
C1 10µF
C3 100nF
C4 100nF
C5 100nF
GND
Decoupling Capacitors
my LAB PCB
Project: myCPU Instruction Register 8 bit R
Revision: 9
Date: 28/06/2022
Author: Rafa Hernández


90,00
74,24
14,40
4,00
21,11
Output
+5v
2
1
RS
CK
GND
IC1
74LS245
C5
C4
IC2
74LS173
RN1
IC3
C3
Data BUS
OPCODE OUT
my LAB PCB
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FZ
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
C1
10,95
60,00
Instruction Register (RIGHT) Rev: 9



Bill of Materials

Designator	Description	Value	Q
C1	Electrolytic capacitor 16v/50v	10µF	1
C3, C4, C5	Ceramic or tantalum capacitor	100nF	3
IC1	Non inverting bus transceiver	74LS245	1
IC2, IC3	4-bit D-Type Register with 3 state outputs	74LS173	2
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p	1
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p	1
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p	1
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p	1
RN1	Resistor array 8 elements,9 pins	330Ω	1

Assembly List

Desig.	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C3	Ceramic or tantalum capacitor	100nF
C4	Ceramic or tantalum capacitor	100nF
C5	Ceramic or tantalum capacitor	100nF
IC1	Non inverting bus transceiver	74LS245
IC2	4-bit D-Type Register with 3 state outputs	74LS173
IC3	4-bit D-Type Register with 3 state outputs	74LS173
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 16p	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 32p	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical, 24p	24p
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical, 8p	8p
RN1	Resistor array 8 elements,9 pins	330Ω