Myles Joshua P. Querimit

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EDUCATION

Purdue University — **Indianapolis, Indiana**
Bachelor of Science, Computer Engineering — *Expected Graduation, May 2028*

EXPERIENCE

Summer Training and Awareness for Semiconductors — **West Lafayette, Indiana**
Design Intern — *May 2025 – Present*

- Collaborated with a team to produce the high-level hardware architecture for multiple FPGA projects, defining module interfaces, data-flow pipelines, and resource budgets to meet stringent area and timing constraints.
- Wrote synthesizable SystemVerilog RTL for a vending machine, drum machine, and pure-hardware Tetris autoplayer—structuring code for modularity, reuse, and ease of verification.
- Developed comprehensive SystemVerilog testbenches and leveraged GTKWave to achieve 100% functional coverage across all RTL assertions, ensuring no post-synthesis functional failures.
- Drove the RTL-to-GDSII hardening flow on the Caravel chip harness using OpenLane, preparing the design for physical tape-out.

Transportation and Autonomous Systems Institute — **Indianapolis, Indiana**
Undergraduate Research Assistant — *January 2025 – March 2025*

- Develop C-based software for autonomous vehicles in Connected Vehicle-to-Everything (CV-V2X) systems.
- Work directly with sensors and radios, including software-defined radio (SDR) technology, to enhance vehicular communication.
- Utilize Wireshark to analyze network traffic, examining packet exchanges between sensors and radios to assess communication performance, data integrity, and protocol efficiency.

Purdue ACM SIGBots — **West Lafayette, Indiana**
Team Member — *August 2024 – Present*

- Collaborated on an engineering focused technical wikipedia with 20-40,000 average monthly pageviews with over 150 articles explaining the purposes of various aspects of robotics.
- Contributed in the design for custom 3-D printed components for prototyping mechanisms to be used in the competition robot.

ECE Ambassador — **Indianapolis, Indiana**
Student Ambassador — *September 2024 – Present*

- Represent Purdue University at recruitment events, promoting the School of ECE to prospective students.
- Developed leadership, communication, and presentation skills through interactions with industry partners and alumni.

PROJECTS

FPGA AI Accelerator — **West Lafayette, Indiana**
Independent Project — *March 2025 – June 2025*

- Implemented a 4×4 systolic-array AI accelerator in SystemVerilog on a Lattice iCE40 FPGA (25 MHz clock), structuring data-flow pipelines for maximum parallelism.
- Synthesized and optimized the design with Yosys, fitting the accelerator within tight resource constraints of the iCE40 fabric.
- Benchmarked against a single-core AMD Ryzen 7 8840HS (via Python emulation), achieving a 3.04× latency reduction and an 18.78× throughput increase on the FPGA.

RISC-V CPU Core Design and Implementation — **West Lafayette, Indiana**
Independent Project — *March 2025*

- Designed a fully functional RISC-V CPU core in TL-Verilog, implementing instruction fetch, decode, execute, and memory access stages.
- Developed support for arithmetic, logic, load/store, and branch instructions while ensuring efficient pipeline execution.

ACTIVITIES AND LEADERSHIP

EPICS - Engineering Projects in Community Service — **Indianapolis, Indiana**
Project Lead — *September 2024 – March 2025*

- Leading a cross-disciplinary team to design and construct a custom greenhouse for a local community partner.

SKILLS

Programming Languages: C, C++, Python, Matlab, Verilog
Tools: Autodesk, Microsoft 365, Notion, Git, KiCad, ModelSim