Myles Joshua P. Querimit

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EDUCATION

Purdue University — **Indianapolis, Indiana**
Bachelor of Science, Computer Engineering — *Expected Graduation, May 2028*

EXPERIENCE

Summer Training and Awareness for Semiconductors — **West Lafayette, Indiana**
Design Intern — *May 2025 – Present*

- Collaborated with a team to produce the high-level hardware architecture for multiple FPGA projects, defining module interfaces, data-flow pipelines, and resource budgets to meet stringent area and timing constraints.
- Developed comprehensive SystemVerilog testbenches and leveraged GTKWave to achieve 100% functional coverage across all RTL assertions, ensuring no post-synthesis functional failures.
- Drove the RTL-to-GDSII hardening flow on the Caravel chip harness using OpenLane, preparing the design for physical tape-out.

Transportation and Autonomous Systems Institute — **Indianapolis, Indiana**
Undergraduate Research Assistant — *January 2025 – March 2025*

- Develop C-based software for autonomous vehicles in Connected Vehicle-to-Everything (CV-V2X) systems.
- Work directly with sensors and radios, including software-defined radio (SDR) technology, to enhance vehicular communication.
- Utilize Wireshark to analyze network traffic, examining packet exchanges between sensors and radios to assess communication performance, data integrity, and protocol efficiency.

PROJECTS

High-Performance GEMM (C++ · OpenMP · AVX2) — **Chicago I**
Independent Project — *August 2025*

- Built FP32 GEMM from naïve → blocked → packed; correctness verified (Frobenius relerr <= 1e-6).
- Achieved ~236 GFLOP/s @ N=4096 on Ryzen 7 8840; ~80x over 1-thread naïve @ N=2048; 2.8x packing vs blocked.
- Implemented BLIS-style 64-B aligned panel packing, cache-sized tiling, thread affinity (PLACES=cores, PROC_BIND=close); reproducible CLI benches (CSV + plots).

Tapeout-Approved Tetris w/ AI Autoplayer (SystemVerilog, FPGA/ASIC) — **West Lafayette, Indiana**
Architecture Lead — *June 2025 – August 2025*

- Final GDSII signed off and queued for fabrication; synthesis, STA, and P&R completed; timing met on target constraints.
- Implemented AI autoplayer on FPGA fabric with N-ply lookahead; tuned heuristics (lines, holes, height, bumpiness).
- Complete game engine in SystemVerilog: spawn/rotate, collision, line clear, scoring, soft-drop, lock delay. Docs include die/layout snapshots.

FPGA AI Accelerator (SystemVerilog, Lattice iCE40) — **West Lafayette, Indiana**
Independent Project — *March 2025 – April 2025*

- Implemented a 4×4 systolic-array AI accelerator in SystemVerilog on a Lattice iCE40 FPGA (25 MHz clock), structuring data-flow pipelines for maximum parallelism.
- Benchmarked against a single-core AMD Ryzen 7 8840HS (via Python emulation), achieving a 3.04× latency reduction and an 18.78× throughput increase on the FPGA.

ACTIVITIES AND LEADERSHIP

ECE Ambassador — **Indianapolis, Indiana**
Student Ambassador — *September 2024 – Present*

- Represented Purdue ECE at recruitment events; strengthened communication with industry partners and alumni.

Purdue ACM SIGBots — **West Lafayette, Indiana**
Team Member — *August 2024 – Present*

- Contributed to an engineering wiki (150+ articles, 20–40k monthly pageviews); designed 3D-printed robot components.

EPICS - Engineering Projects in Community Service — **Indianapolis, Indiana**
Project Lead — *September 2024 – March 2025*

- Leading a cross-disciplinary team to design and construct a custom greenhouse for a local community partner.

SKILLS

Programming Languages: C, C++, Python, Matlab, Verilog
Tools: Autodesk, Microsoft 365, Notion, Git, KiCad, ModelSim