Data Sheet | October 1999 | File Number 4072.3

50A, 60V, 0.022 Ohm, Logic Level N-Channel Power MOSFETs

These N-Channel enhancement mode power MOSFETs are manufactured using the latest manufacturing process technology. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49164.

Ordering Information

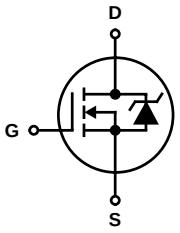
PART NUMBER	PACKAGE	BRAND
RFG50N06LE	TO-247	FG50N06L
RFP50N06LE	TO-220AB	FP50N06L
RF1S50N06LESM	TO-263AB	F50N06LE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. RF1S50N06LESM9A.

Features

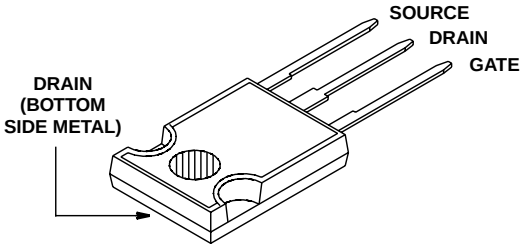
- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

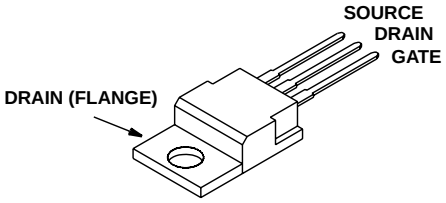


Packaging

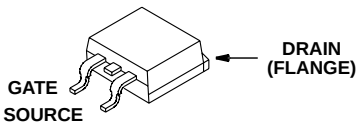
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG50N06LE, RFP50N06LE, RF1S50N06LESM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	50	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	142	W
Derate Above 25^oC		0.95	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V, Figure 13		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA, Figure 12		1	-	3	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 50V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	10	μA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 50A, V_{GS} = 5V, Figure 11		-	-	0.022	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 50A, R_L = 0.6Ω, V_{GS} = 5V, R_{GS} = 2.5Ω Figures 10, 18, 19		-	-	230	ns
Turn-On Delay Time	$t_{d(ON)}$			-	20	-	ns
Rise Time	t_r			-	170	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	48	-	ns
Fall Time	t_f			-	90	-	ns
Turn-Off Time	t_{OFF}			-	-	165	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 50A, R_L = 0.96Ω Figures 21, 21	-	96	120	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	57	70	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	2.2	2.7	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz Figure 14		-	2100	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	230	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.05	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220AB and TO-263AB		-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 45A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 45A, dI_{SD}/dt = 100A/μs	-	-	125	ns

NOTES:

2. Pulse test: pulse width ≤ 80μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

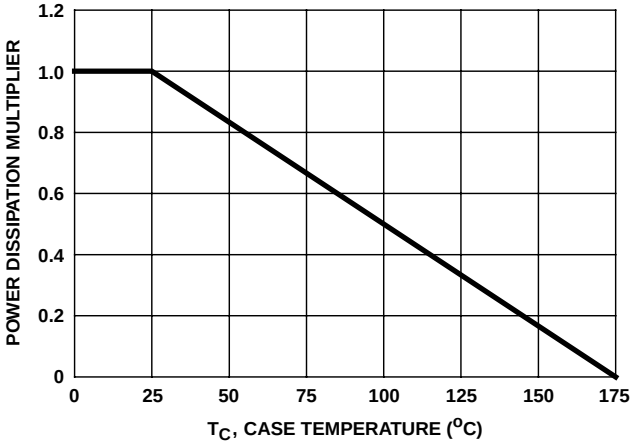


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

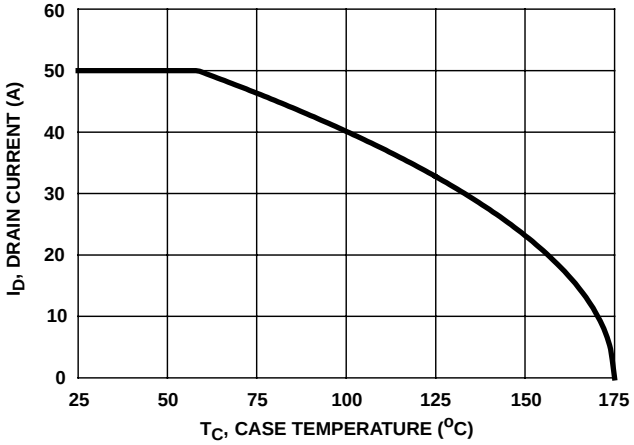


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

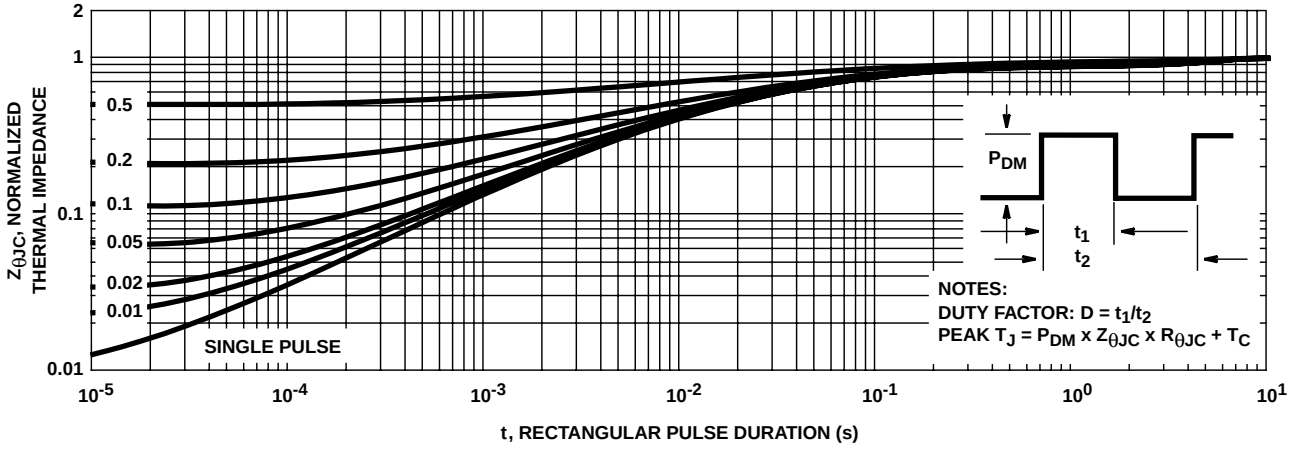


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

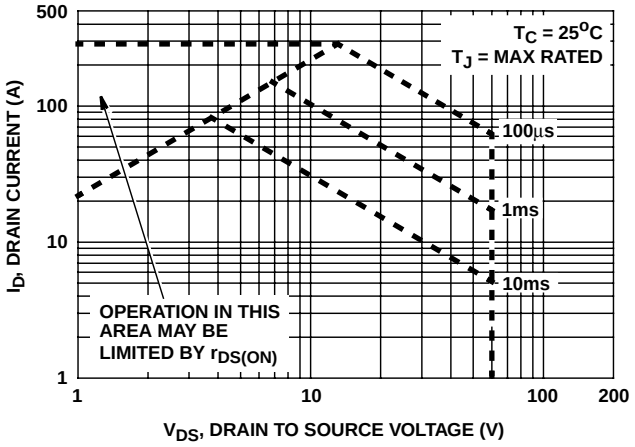


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

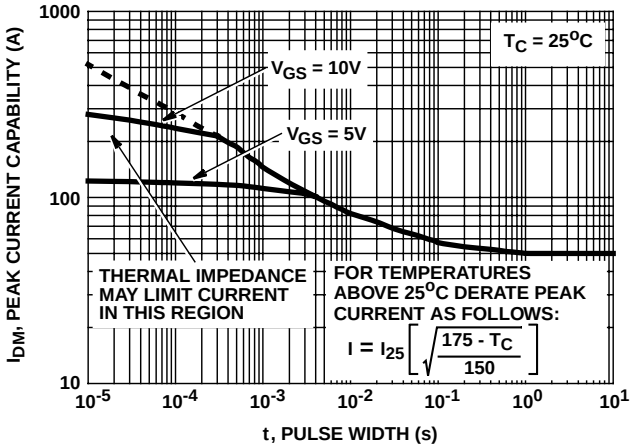
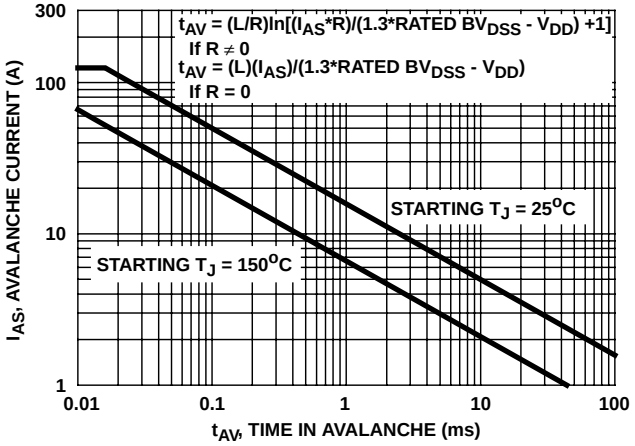


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

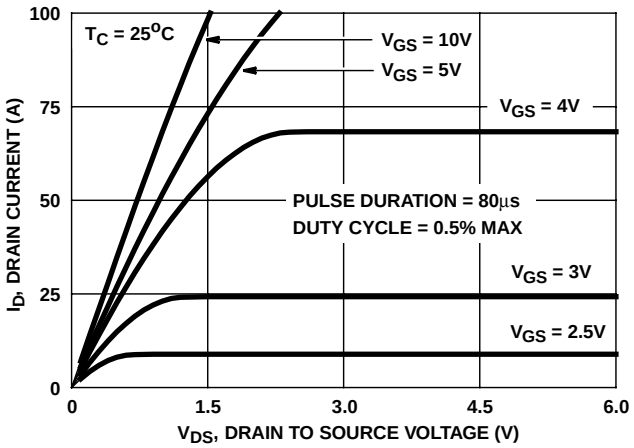


FIGURE 7. SATURATION CHARACTERISTICS

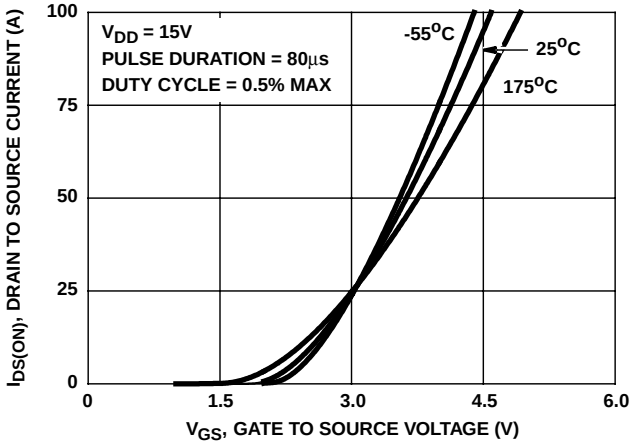


FIGURE 8. TRANSFER CHARACTERISTICS

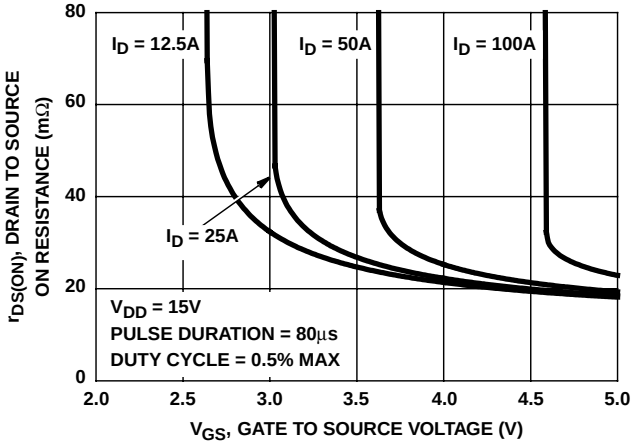


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

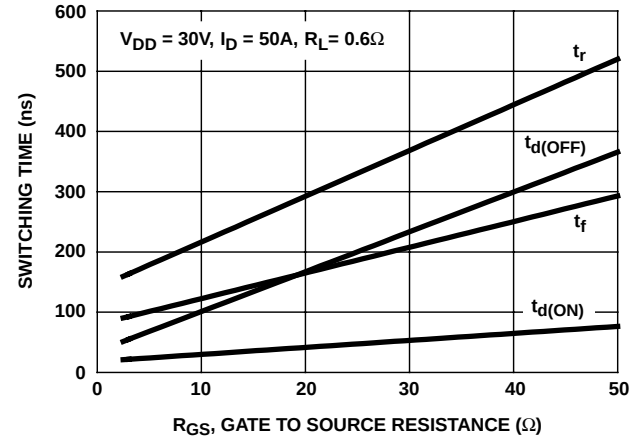


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

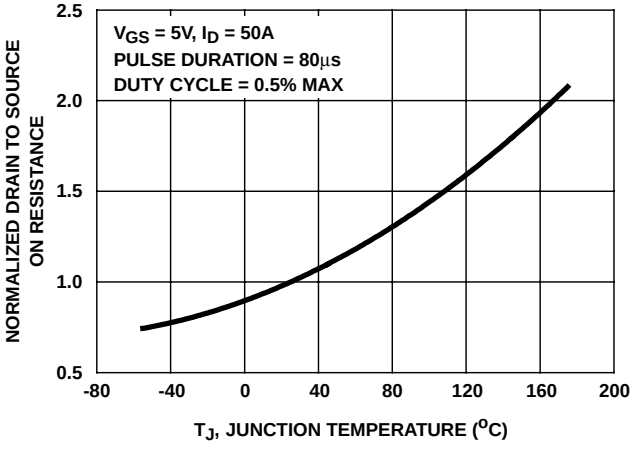


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

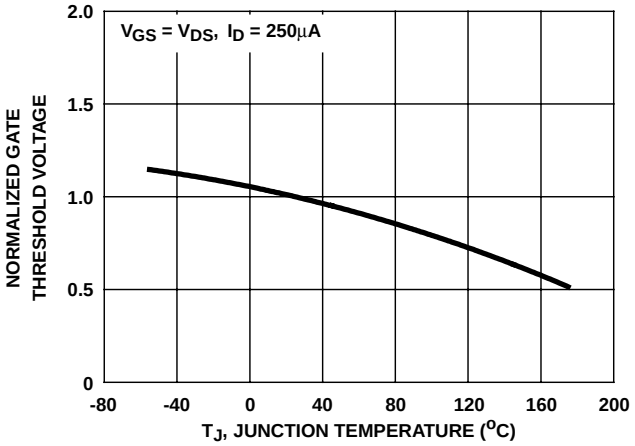


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

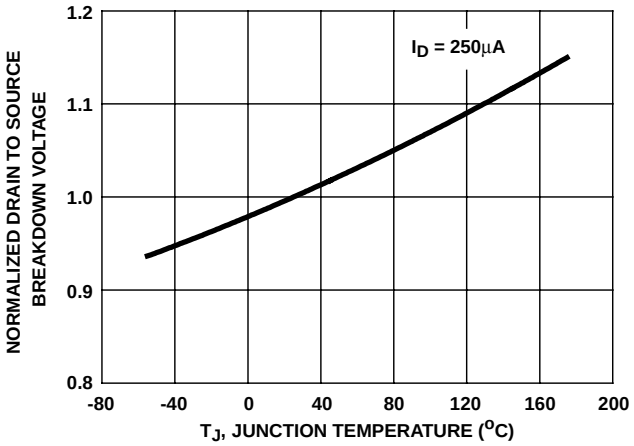


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

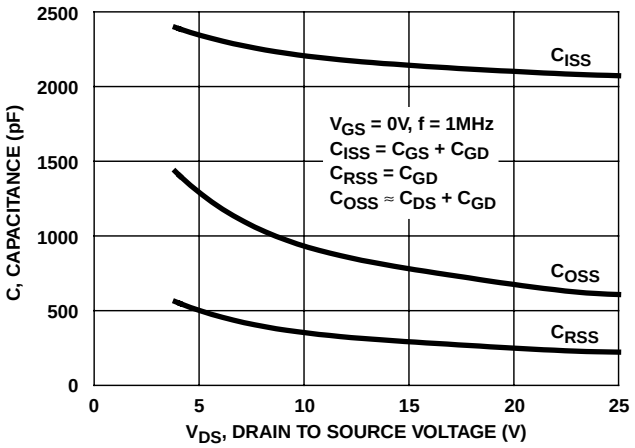
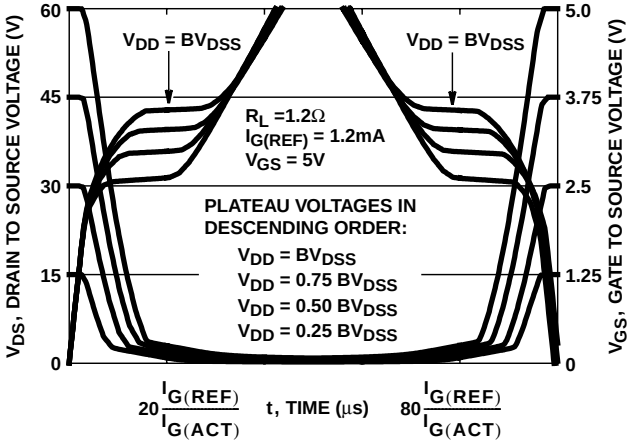


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

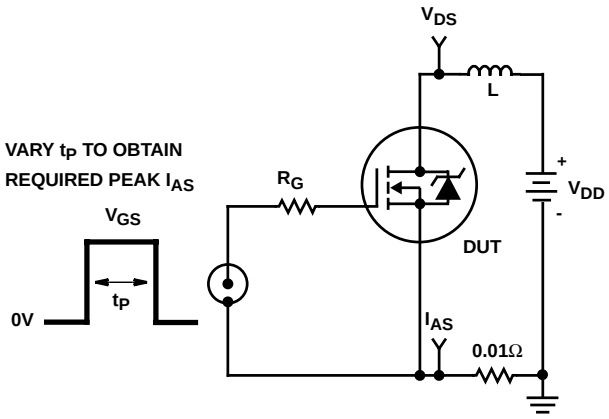


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

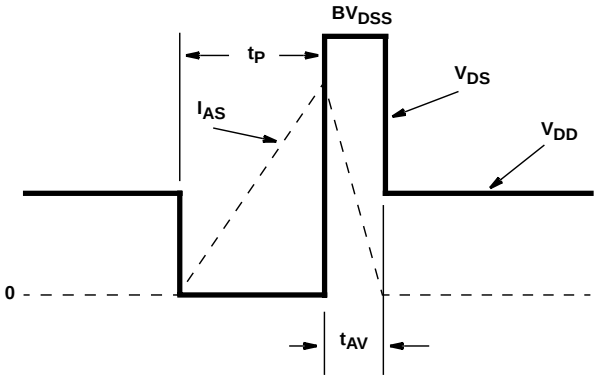


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

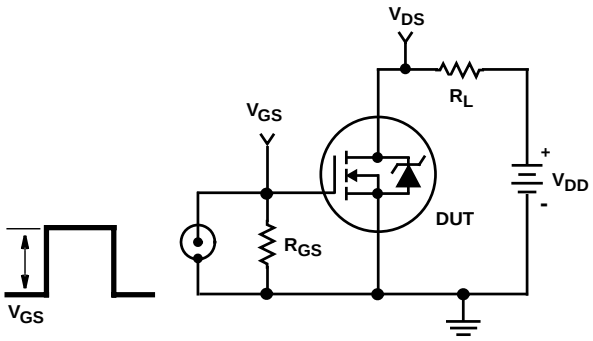


FIGURE 18. SWITCHING TIME TEST CIRCUIT

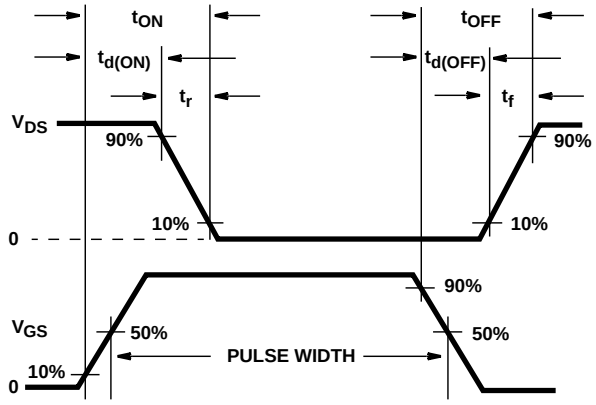


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

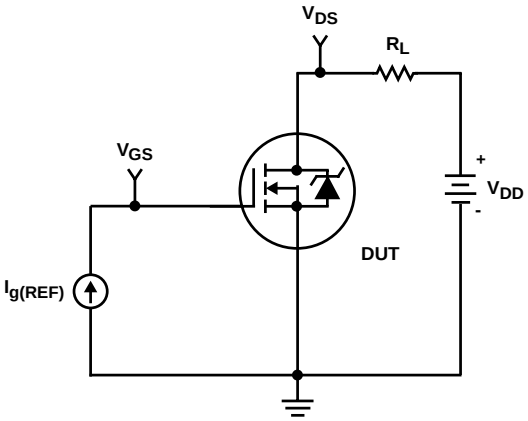


FIGURE 20. GATE CHARGE TEST CIRCUIT

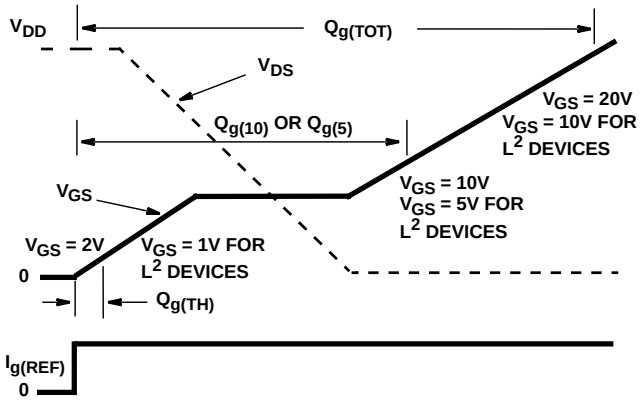
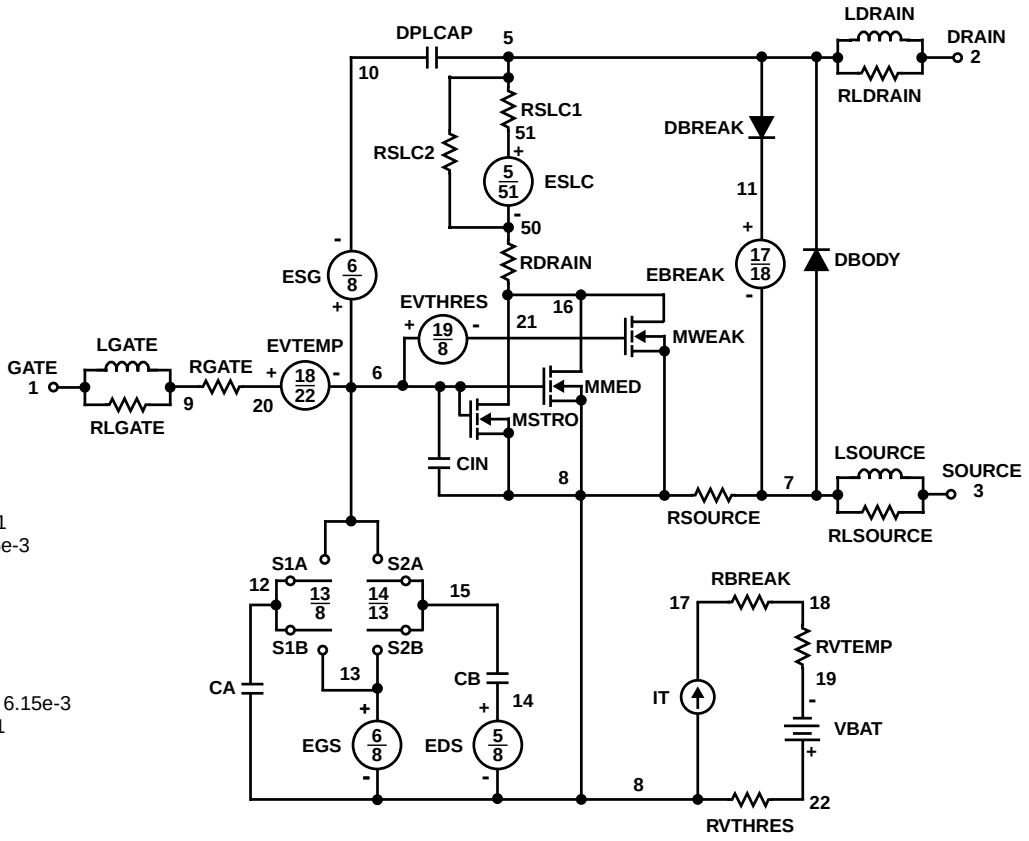


FIGURE 21. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

```
SUBCKT 50N06LE 2 1 3 ;       rev 8/11/95

CA  12  8 3.73e-9
CB  15  14 3.73e-9
CIN  6  8 2.08e-9


DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD


EBREAK 11 7 17  18 66.5
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1


IT  8  17  1

LDRAIN 2 5 4.0e-9
LGATE 1 9 6.0e-9
LSOURCE  3 7 3.0e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 3.75e-3
RGATE  9  20 1.0
RLDRAIN 2 5 40
RLGATE 1 9 60
RLSOURCE 3 7 30
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 6.15e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*200),4))}

.MODEL DBODYMOD D (IS = 1.70e-12  RS = 3.20e-3  TRS1 = 1.75e-3  TRS2 = 1.75e-6  CJO = 2.55e-9  IKF = 13 XTI = 5.2 TT = 7.00e-8 M = 0.47)
.MODEL DBREAKMOD D (RS = 1.70e-1  IKF = 0.1 TRS1 = 2.00e-3  TRS2 = 8.00e-7)
.MODEL DPLCAPMOD D (CJO = 2.00e-9  IS = 1e-30   VJ = 1.1 M = 0.83 N = 10)
.MODEL MMEDMOD NMOS (VTO = 2.00 KP = 5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.0)
.MODEL MSTROMOD NMOS (VTO = 2.42 KP = 128 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.60 KP = 0.01 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 10.0 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.13e-3  TC2 = 0)
.MODEL RDRAINMOD RES (TC1 = 1.20e-2  TC2 = 6.00e-5)
.MODEL RSLCMOD RES (TC1 = 2.00e-3 TC2 = 1.00e-6)
.MODEL RSOURCEMOD RES (TC1 = 2.00e-3 TC2 =-1.00e-5)
.MODEL RVTHRESMOD RES (TC1 = -2.50e-3 TC2 = -8.50e-6)
.MODEL RVTEMPMOD RES (TC1 = -2.00e-3  TC2 = 5.00e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -5.3  VOFF= -2.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.5  VOFF= -5.3)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.4  VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0.5  VOFF= -1.4)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

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