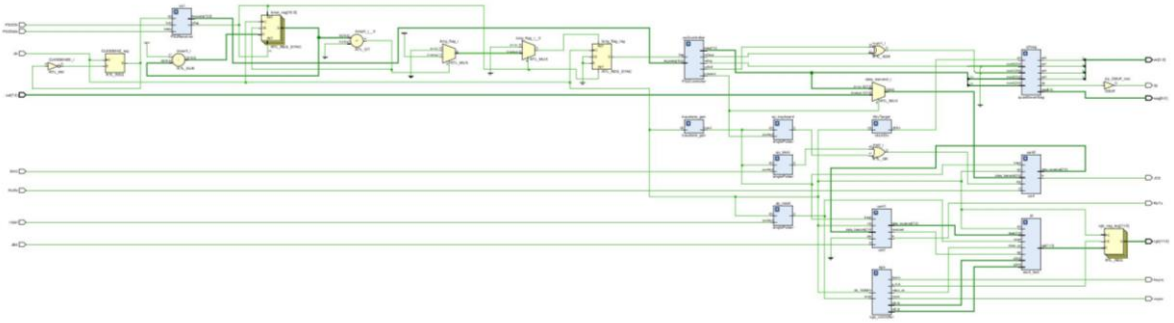

Design Schematic

Module Name	Description
ascii_rom	Mapping pixel color for any characters.
ascii_test	Tests ASCII text rendering with support languages display
baudrate_gen	Generate 9600 Buad rate signal for UART communication.
clockDiv	Divides the input clock frequency.
debouncer	Eliminates noise from input signals using a counter-based stabilization mechanism
hexTo7Segment	Converts a hexadecimal digit (0-9, A-F) into a corresponding 7-segment display pattern.
PS2Controller	Mapping keycodes to system characters.
PS2Receiver	Receives and decodes PS/2 keyboard signals. Producing keycodes and validity flag.
quadSevenSeg	Refers to a 4-digit 7-segment display, where each digit is represented by 7 segments that can be controlled to display hexadecimal numbers.
Seven_segment_display	Define the segments for characters based on the Seiko alphabet. Output to 7-segment display (common anode logic).
singlePulser	A component or circuit that generates a single pulse or a short duration signal, typically used for triggering or timing events in digital systems.
top	Top-level module integrating all module.
uart	UART Controller, including both receive data, auto-transmit data and optional transmit data
uart_rx	Receives data via UART, reconstructing 8-bit data from the serial input and providing a received signal
uart_tx	Transmit 8-bit data serially via UART using an enable signal to trigger transmission
vga_controller	Generate VGA synchronization signals and manages pixel coordinates for screen resolution.
vga_sync	Produces VGA synchronization and timing signals for screen resolution

Source Code and Design Schematic: mynamefaro/HW_Syn_Lab