PROGRAMMABLE LOGIC DEVICES

Electronic and Communication Engineering Department

Lec2: FPGA Structure

Dr. Wahhab R. Mousa

wahhab.albazrqa@uokufa.edu.iq

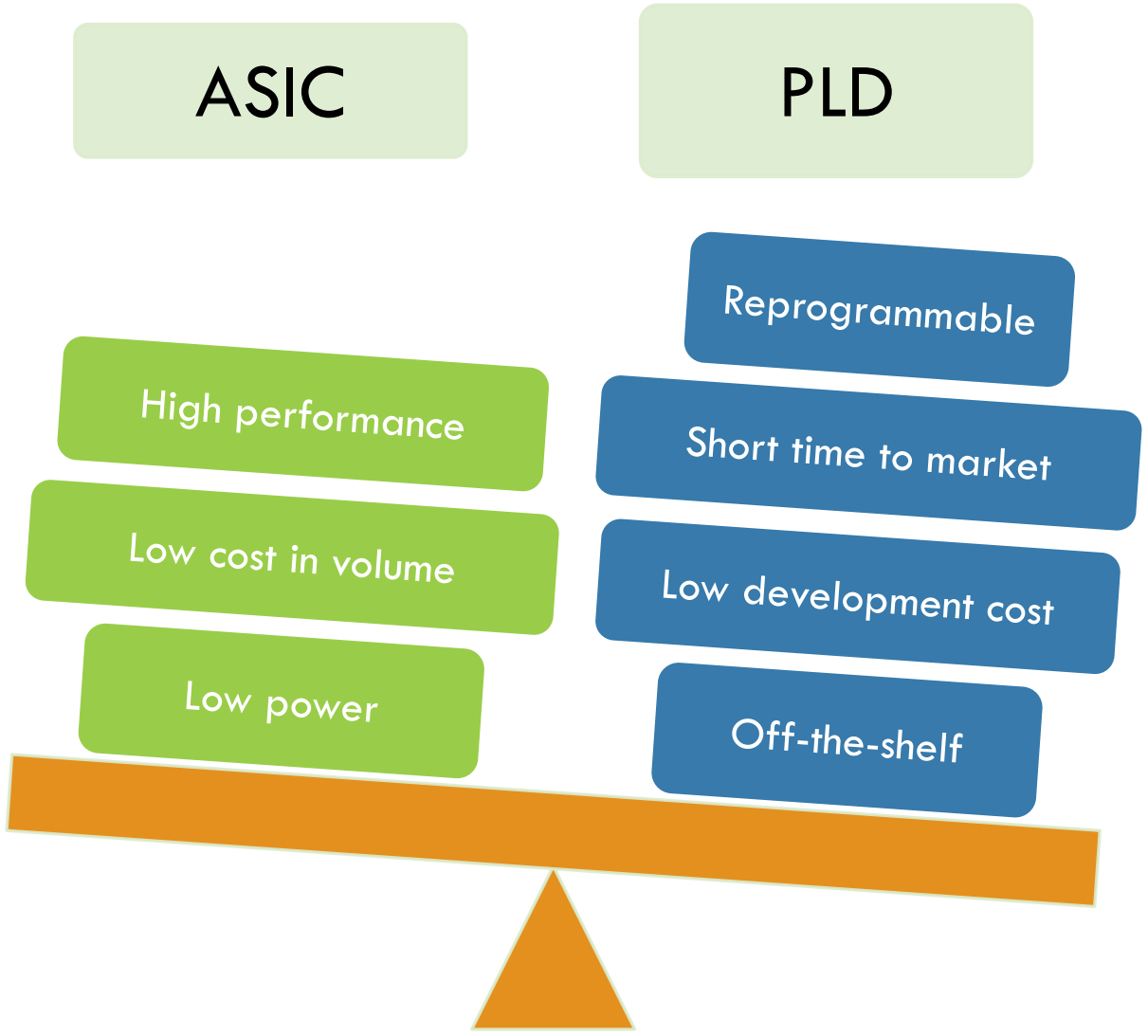
Contents

- Introduction
- FPGA structure
- Altera DE1 SoC board
- Summary

Introduction

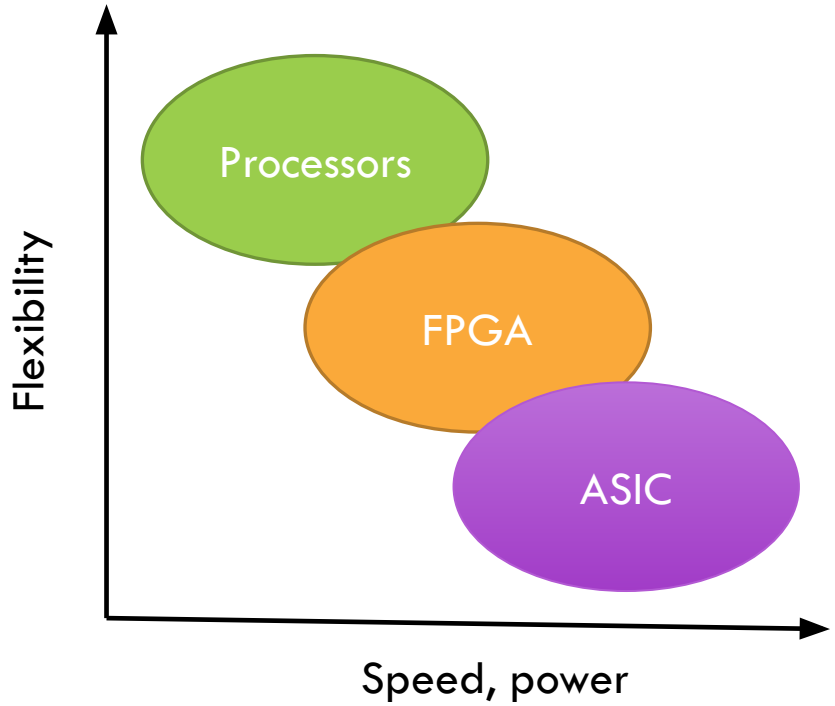
- Programmable Logic Devices (PLDs) is universal logic implementers in the sense that they can be configured (actually programmed) by the user to perform a variety of specific logic functions.

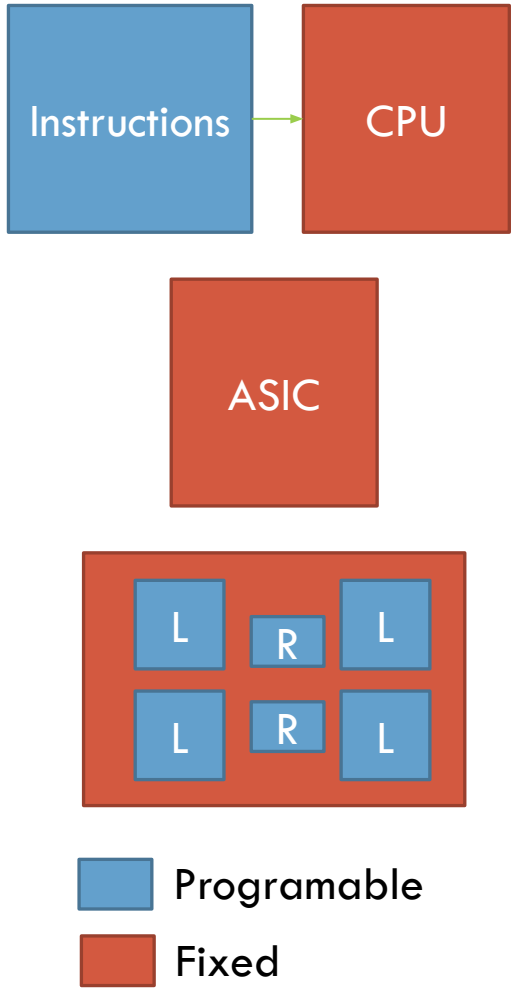
WHY PLDS:


ASIC
PLD
Reprogrammable
High performance
Short time to market
Low cost in volume
Low development cost
Low power
Off-the-shelf

WHY PLDS:

- Processors:
  - Flexibility in the programs
- ASIC (App Specific IC)
  - No flexibility
- FPGA
  - Device re-programpility

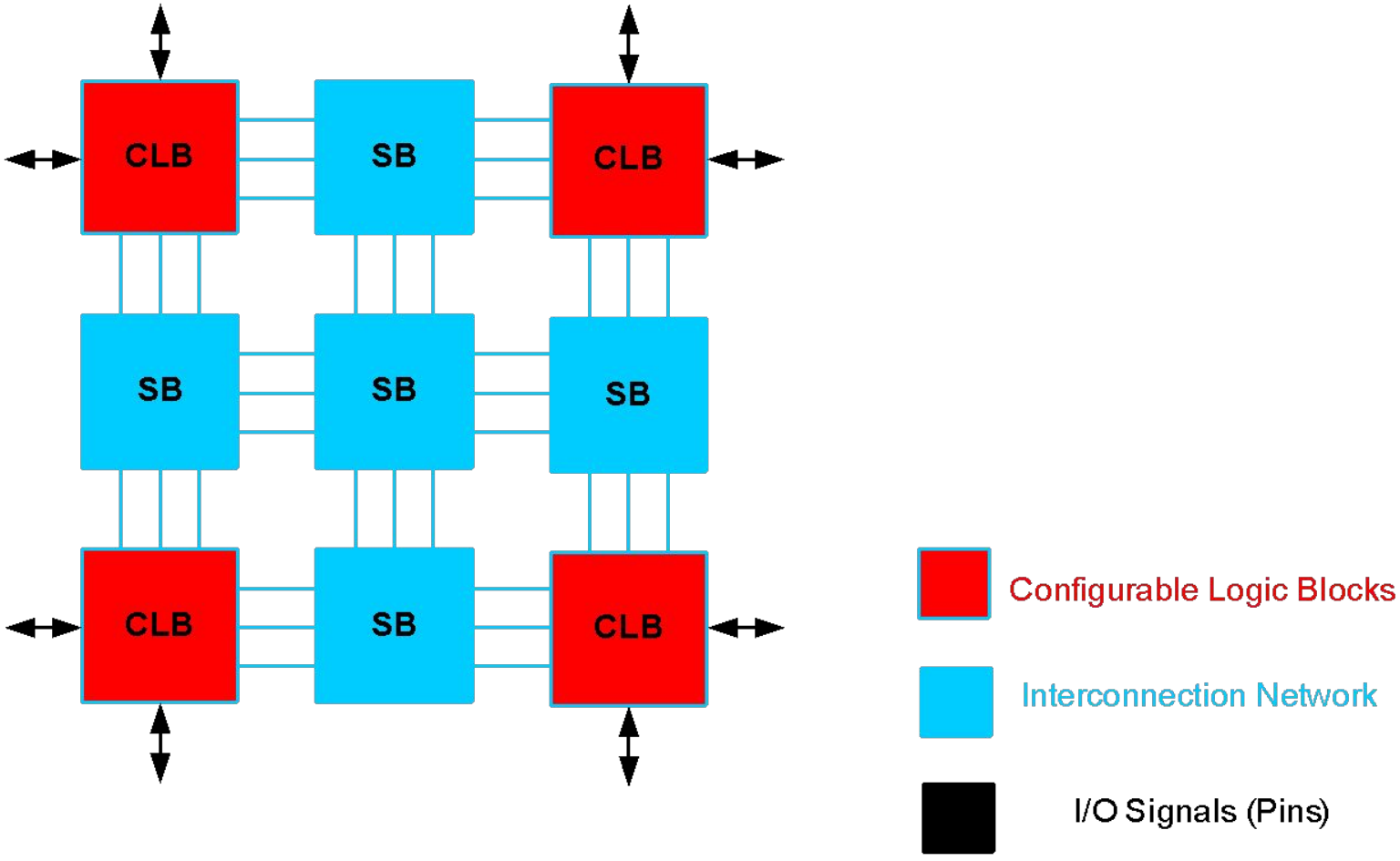




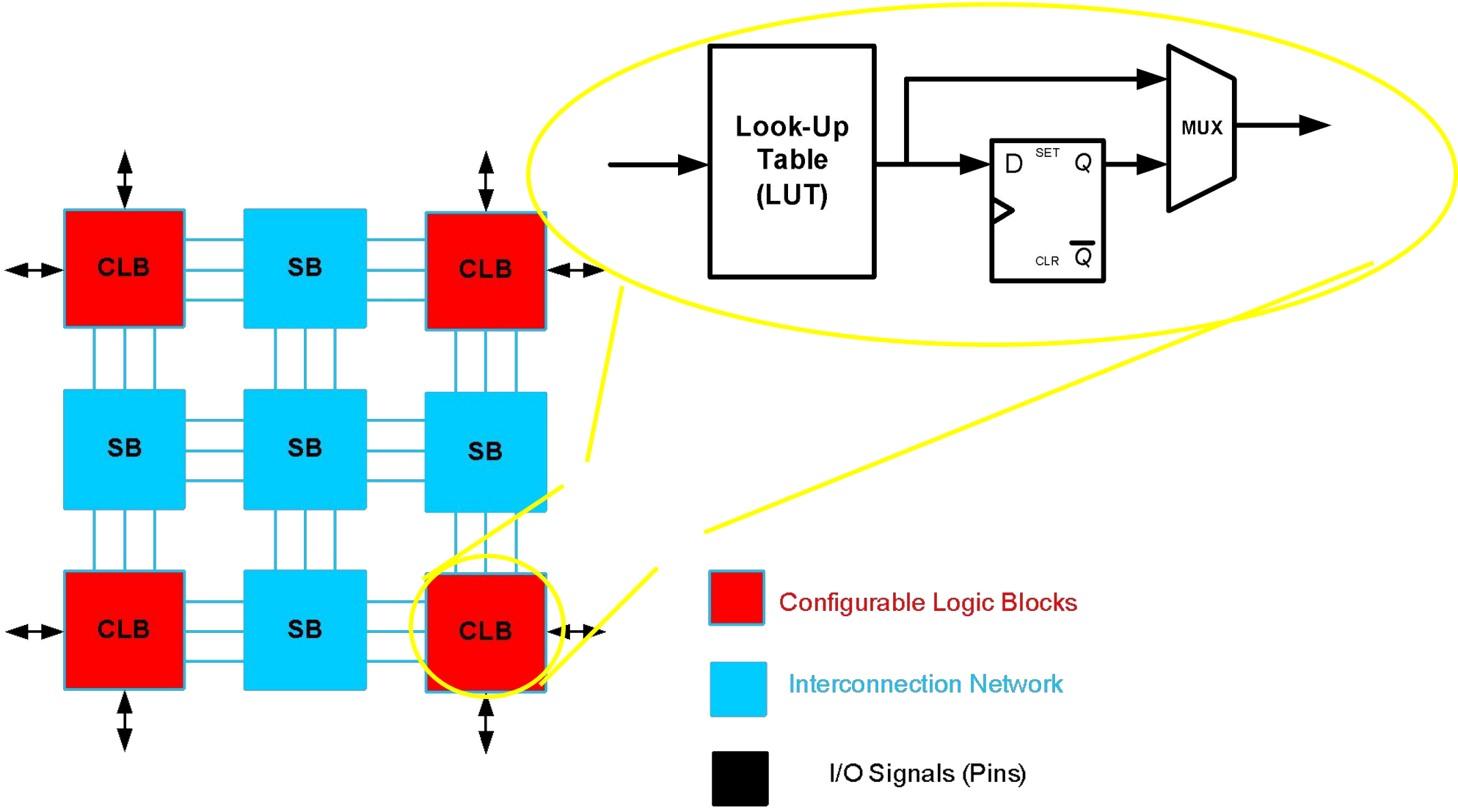
FPGA priceable

- A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be configured by the user to emulate any digital circuit as long as there are enough resources
- An FPGA can be seen as an array of Configurable Logic Blocks (CLBs) connected through programmable interconnect (Switch Boxes)

FPGA STRUCTURE

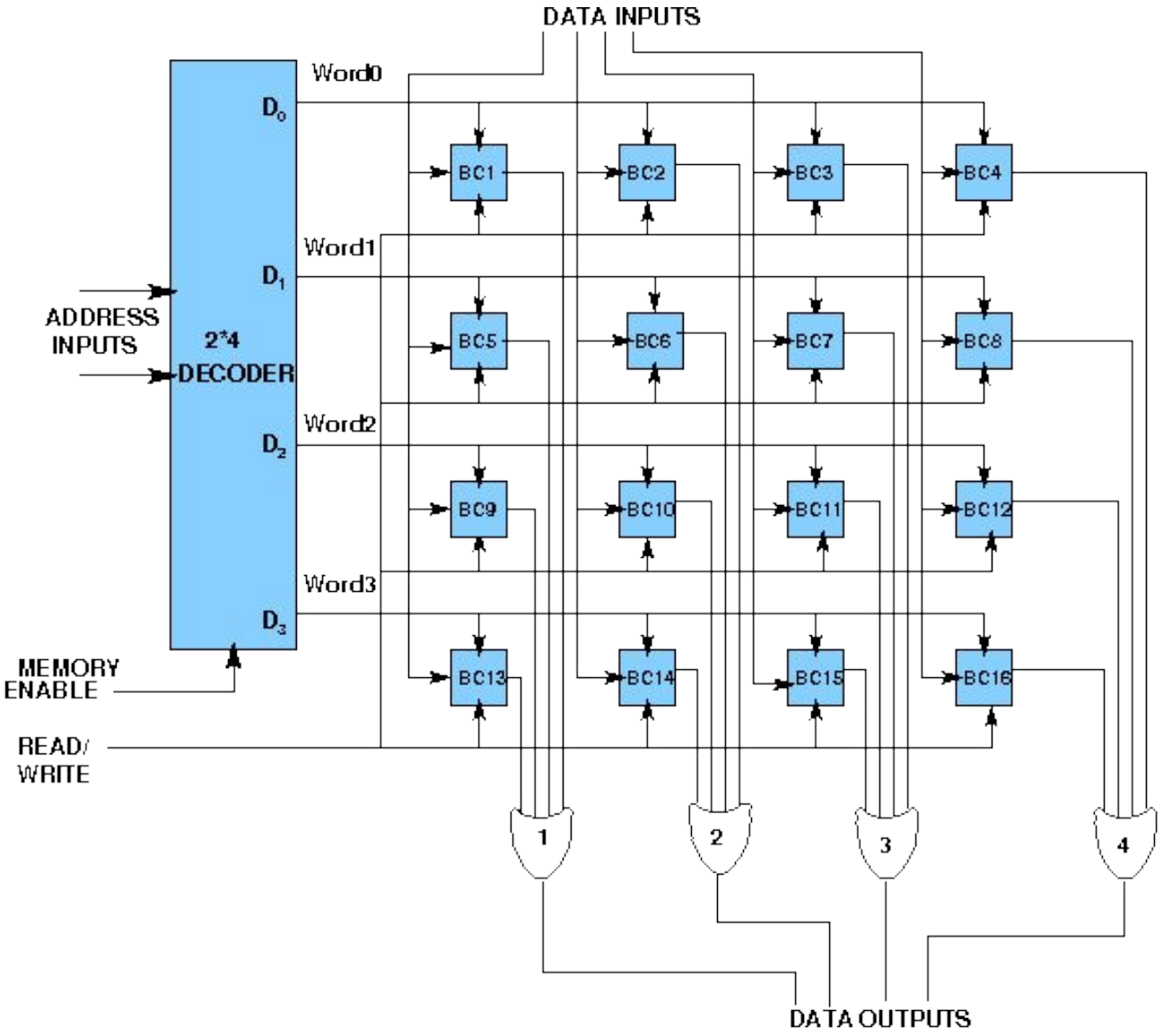


SIMPLIFIED CLB STRUCTURE



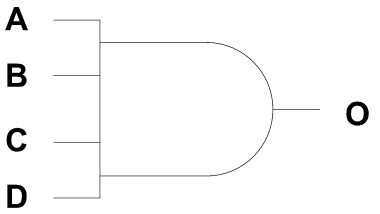
Memory

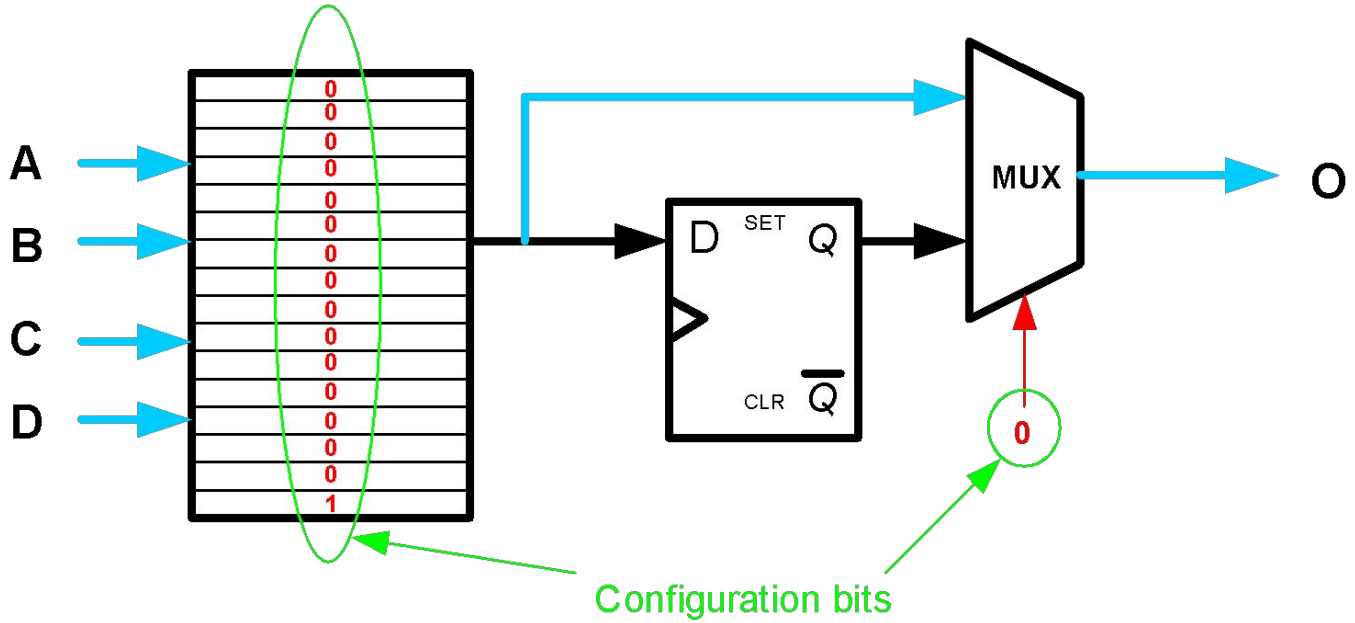
- 4 words x 4 bits memory
  - Address is n for 2^n words
  - Each word is stored in a register (Ex: RAM)



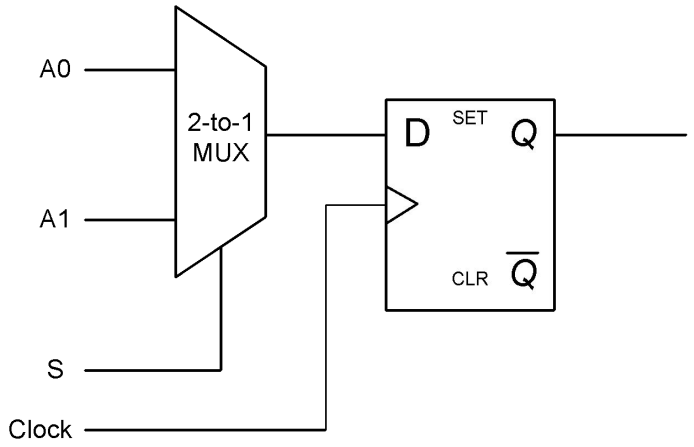
Example: 4-input AND gate

A	B	C	D	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

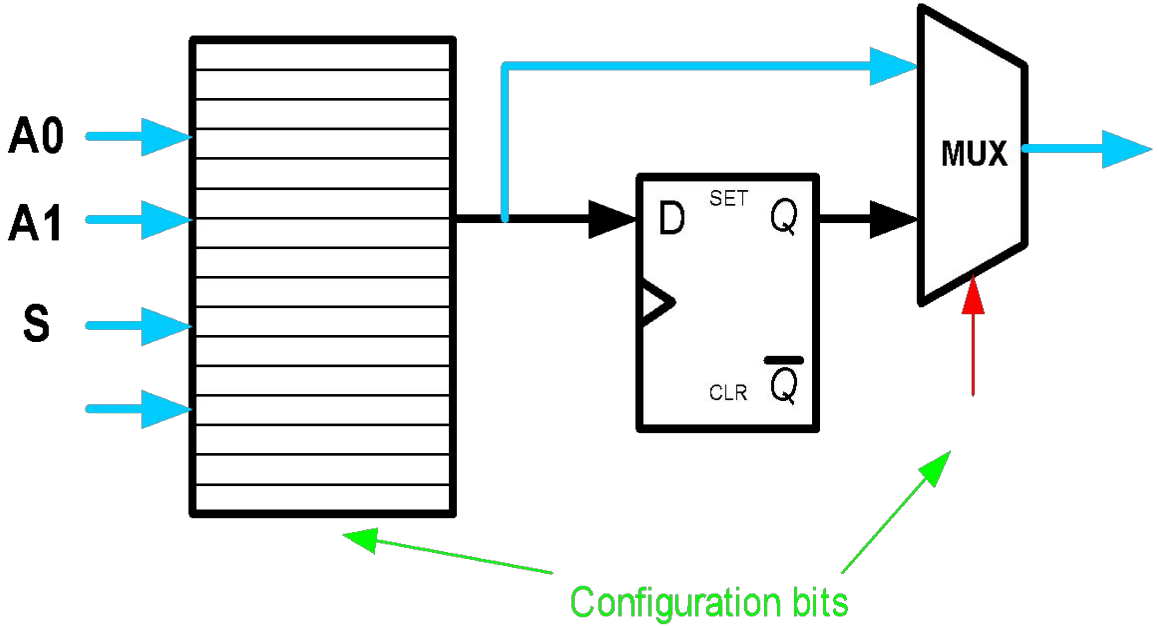




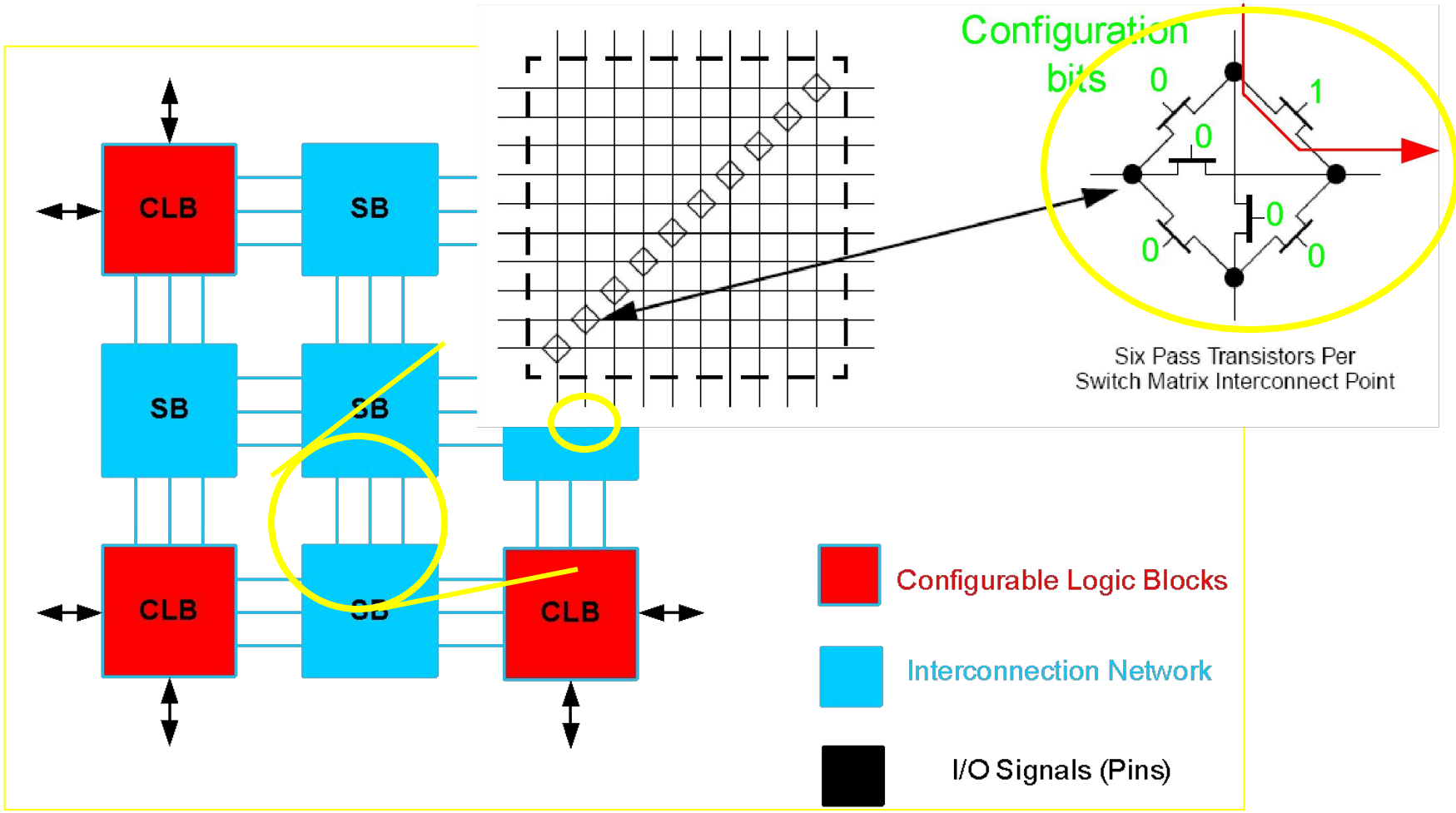
Example 2: Find the configuration bits for the following circuit



S	A1	A0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

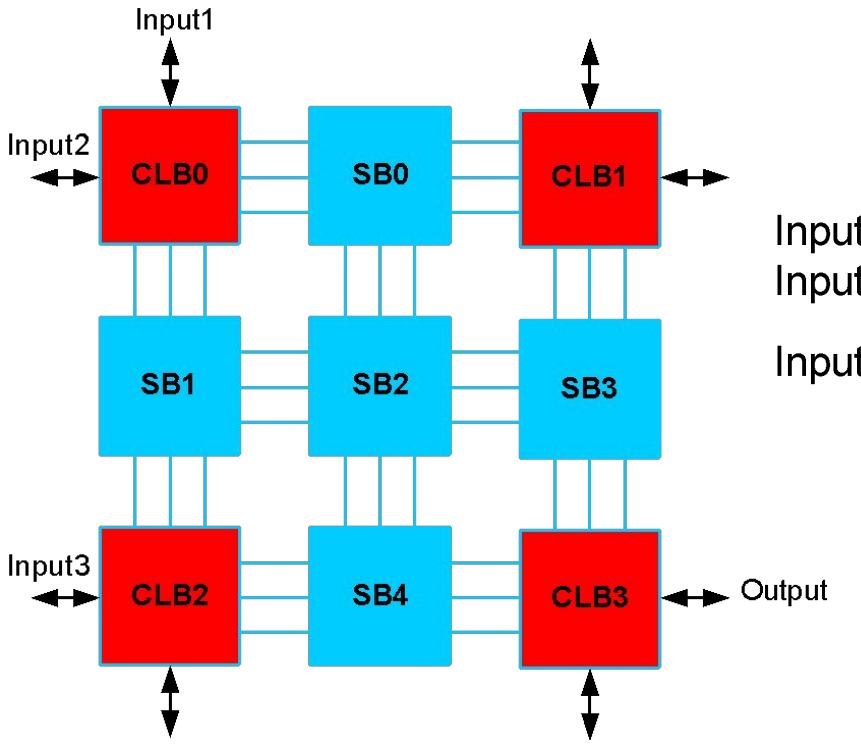


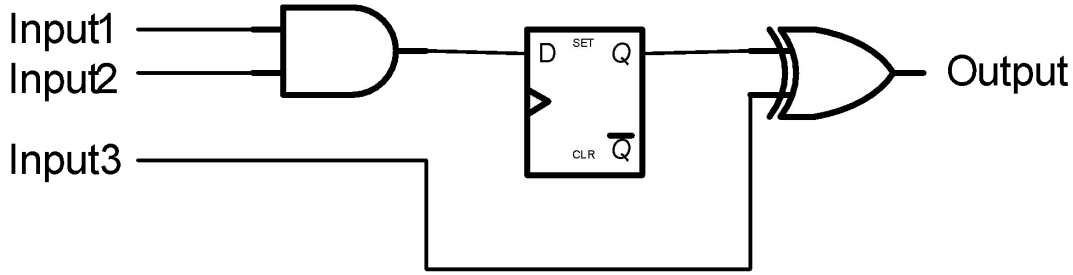
INTERCONNECTION NETWORK



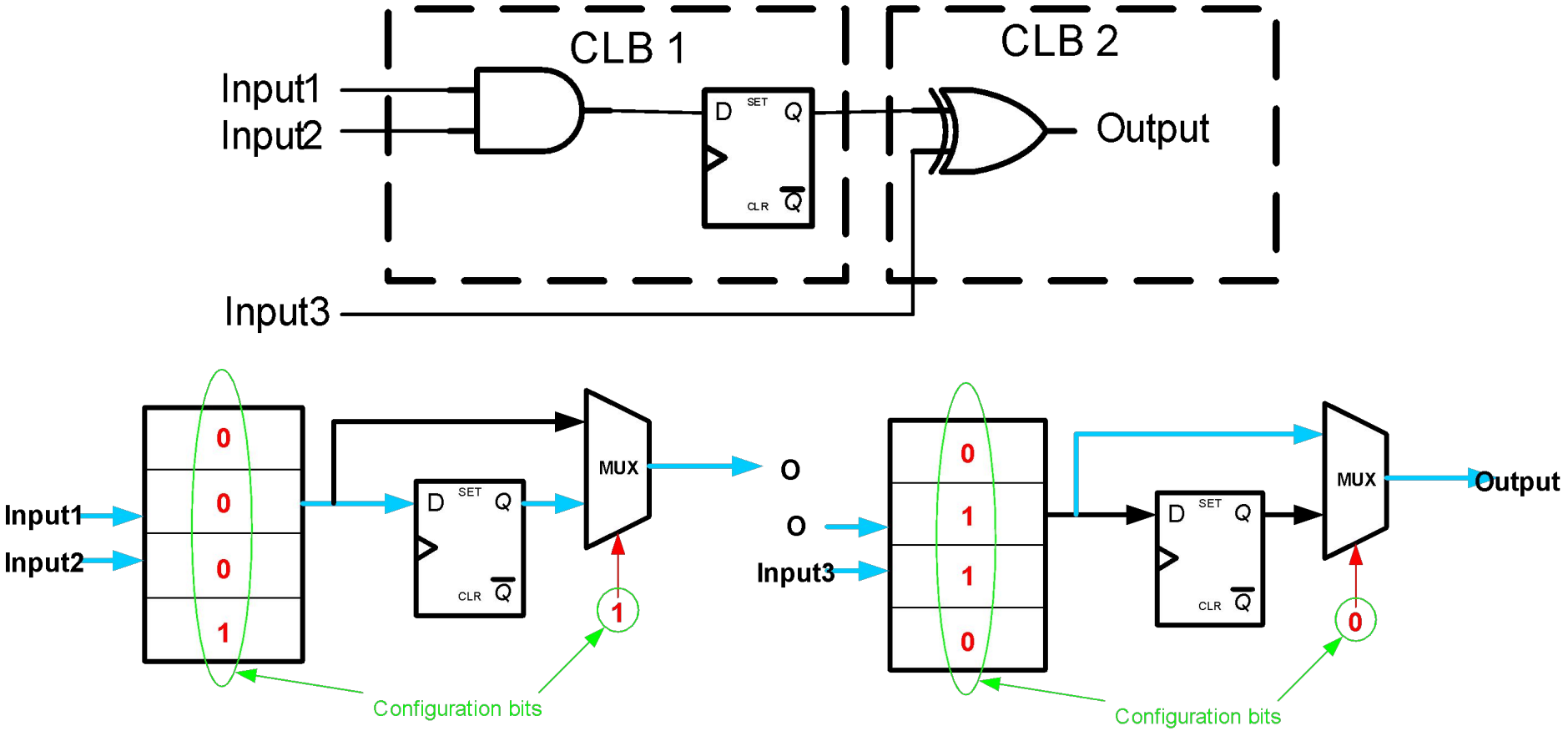
EXAMPLE 3

- Determine the configuration bits for the following circuit implementation in a 2x2 FPGA, with I/O constraints as shown in the following figure. Assume 2-input LUTs in each CLB.

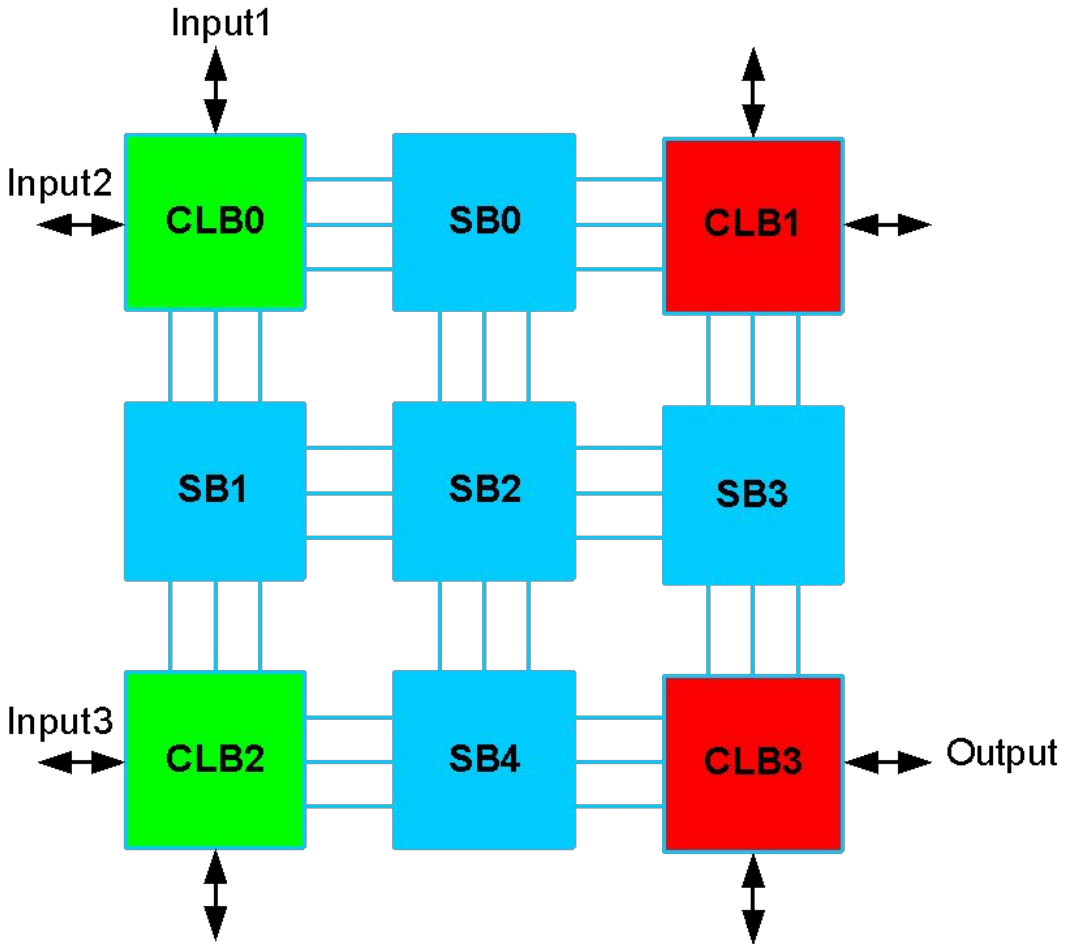




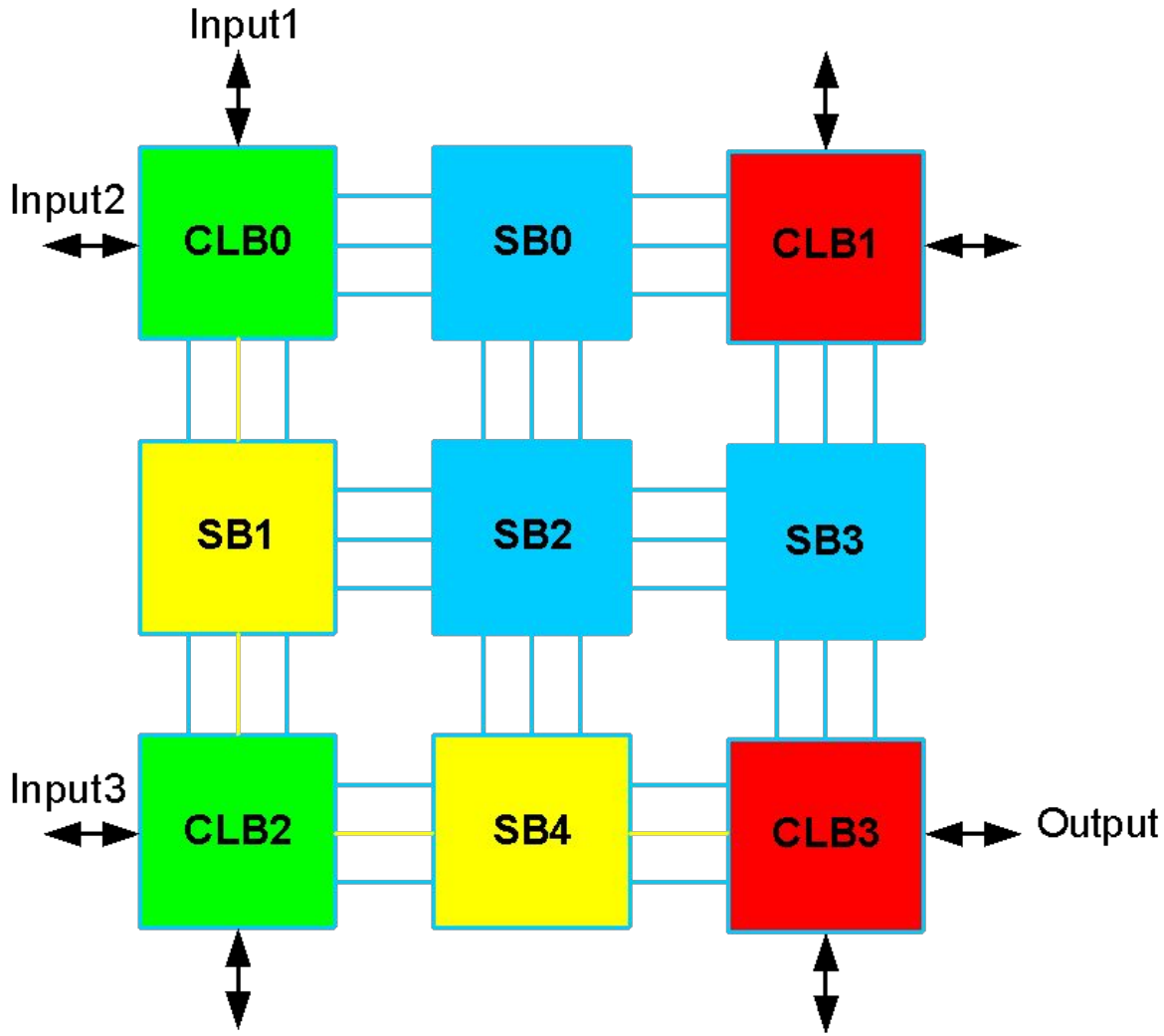
CLBs Required



Placement: Select CLBs

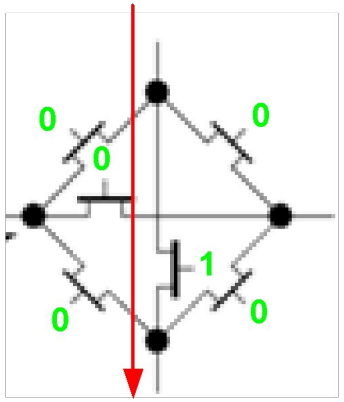


Routing: Select path



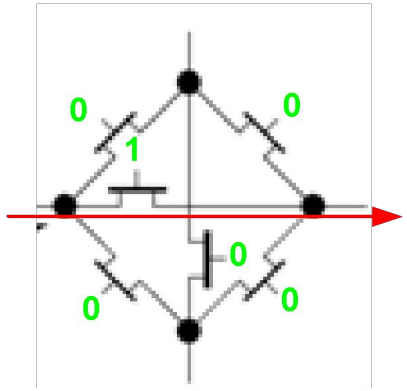
SB1

Configuration bits



SB4

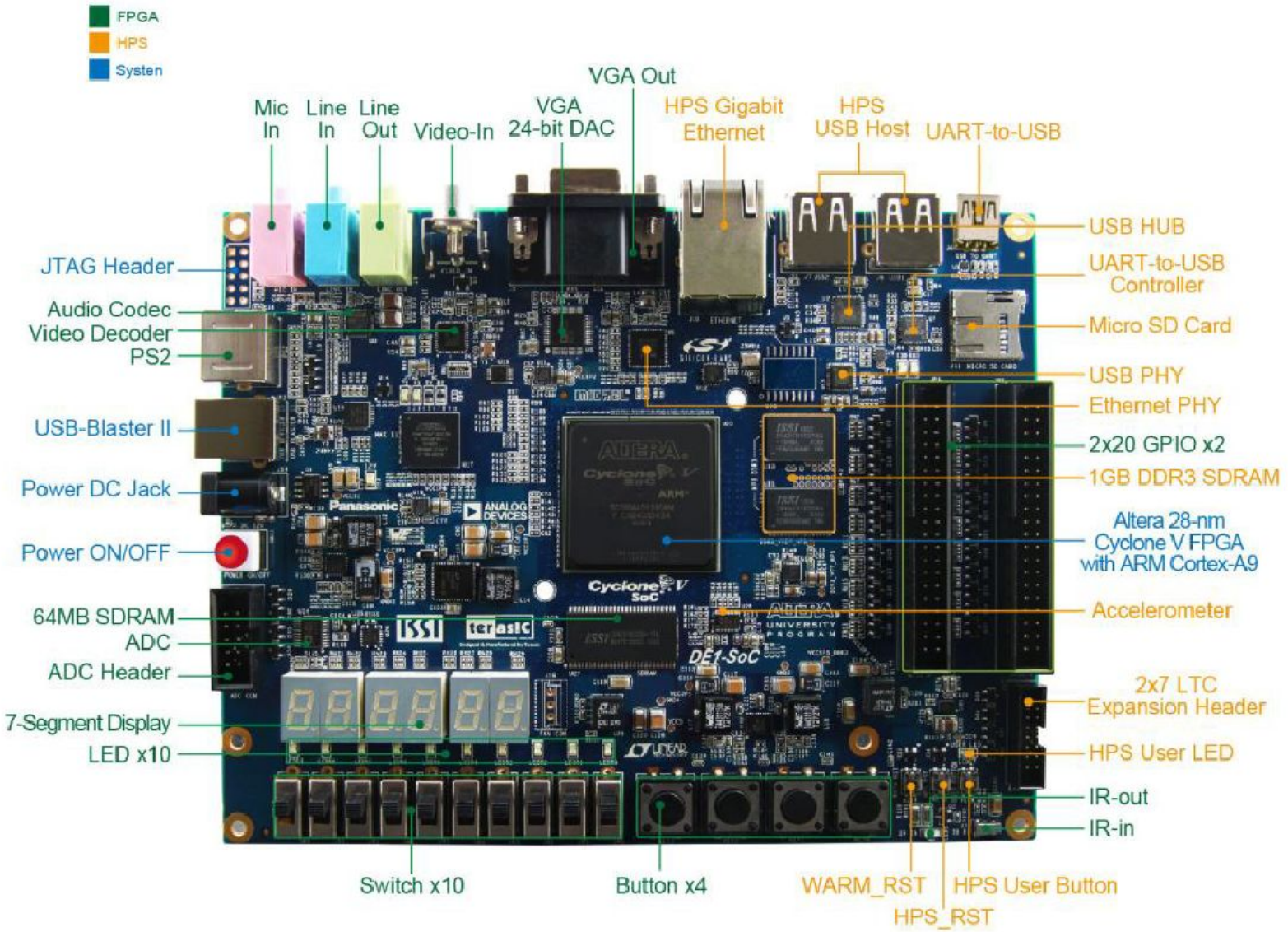
Configuration bits



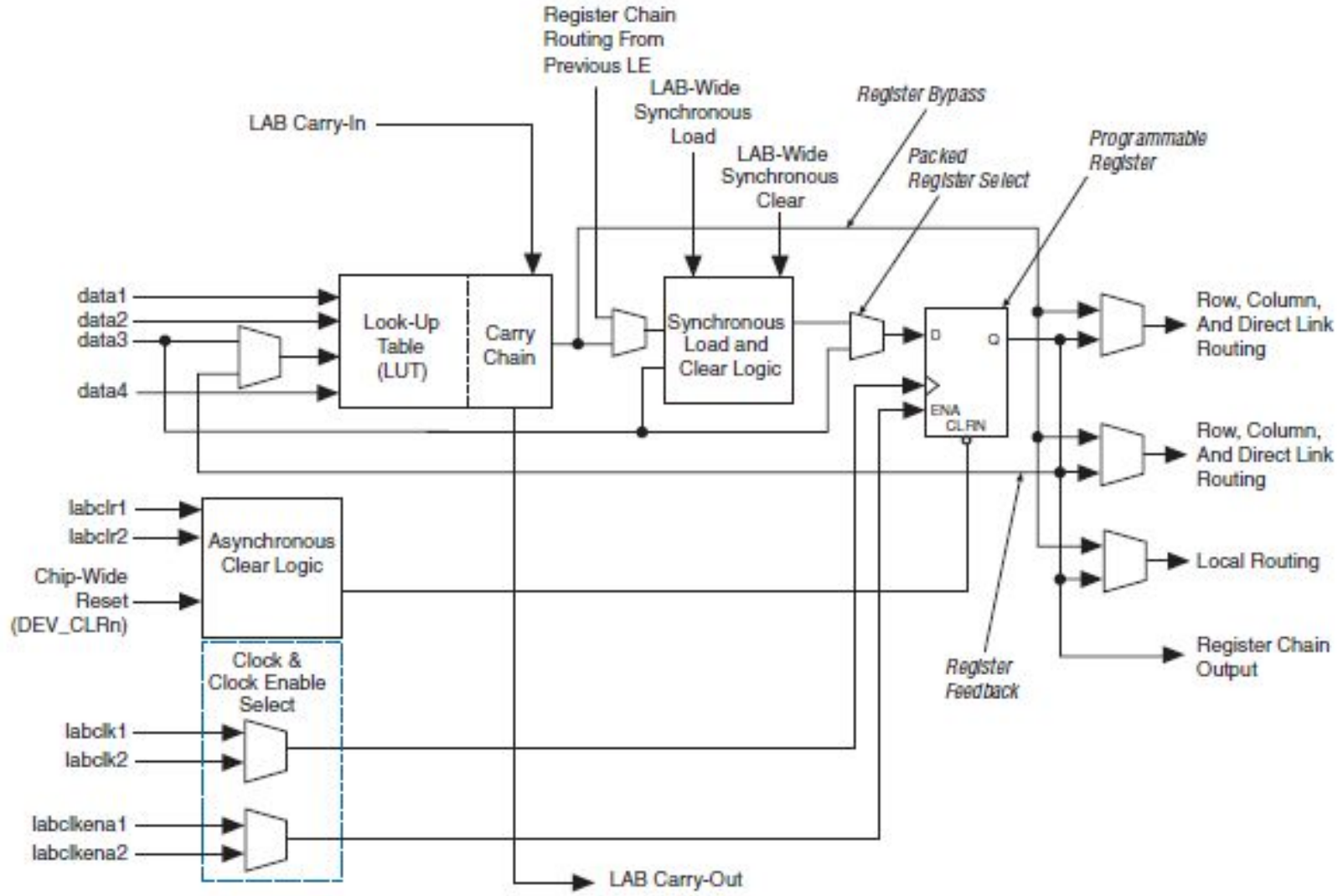
Configuration Bitstream:

- The configuration bitstream must include ALL CLBs and SBs, even unused ones
- CLB0: 00011
- CLB1: XXXXX
- CLB2: 01100
- CLB3: XXXXX
- SB0: 000000
- SB1: 000010
- SB2: 000000
- SB3: 000000
- SB4: 000001

Altera DE1 SOC board



Cyclone Logic element (LE)



3/23/2020

External links

- https://www.youtube.com/watch?v=aPXMkTJxD_s

Specifications

Features	Cyclone V SE SoC	Cyclone V SX SoC	Cyclone V ST SoC
Processor	Dual-core ARM Cortex-A9 MPCore		
Processor Performance	925 MHz		
Logic Density Range	25 – 110K logic element (LE)		85 – 110K LE
Embedded Memory	5,761 kb		
18 x 19 Multipliers	224		
Maximum Transceivers	N/A	9	
Maximum Transceiver Data Rate (Chip to Chip)	N/A	3.125 Gbps	6.144 Gbps
Memory Devices Supported (Hard Memory Controllers)	x1 32 bit, 400 MHz DDR2/DDR3 with ECC – HPS x1 32 bit, 400 MHz, DDR2/DDR3 - FPGA		
Hard Protocol IP	x2 10/100/1000 EMAC – HPS	x2 10/100/1000 EMAC – HPS x2 PCIe Gen1 - SX x2 PCIe Gen2 - ST	

SUMMERY

- FPGA provide the ability to implement logic design with low cost and high speed
- FPGA structure require main blocks are:
  - Configurable logic blocks
  - Interconnect networks
- Designers may need to alter the placement and routing of the selected blocks to improve the design

Thank you
Questions?