DDC and DUC Filters in SDR platforms

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Abstract

Software Defined Radio (SDR) platforms make use of Digital Down Converter (DDC) and Digital Up Converter (DUC), while performing baseband processing. In this paper, various filters being used in DDC as well as DUC sections of two different SDR platforms, USRPB100 and USRPN210 are considered. A simulation study has been made for the filters, Cascade Integrator Comb (CIC), Half Band (HBF) and Root Raised Cosine (RRC), while being used as interpolators and decimators. While comparing these filters, respective computational complexities and magnitude responses have been considered.

Keywords: Software Defined Radio, CIC Filter, RRC Filter, DDC, DUC

1. Introduction

SDR platforms are being widely used in various modes of communication as they are reconfigurable. Digital radio receivers require fast ADC converters to digitize the band limited RF or IF signal generating higher data rates. However, the signal containing information within the digitized RF/ IF signal is usually a fraction of the total RF/ IF bandwidth. The DDC in a digital radio receiver is used to translate the frequency band of interest down the spectrum without violating the Nyquist criterion for the message bandwidth so that sample rate can be reduced and in turn the filter requirements and further processing on the signal of interest become more easily realizable.

The DUC is another important component in digital radio transmitter. The DUC is used to translate a complex digital baseband signal to a real pass band signal. The input complex baseband signal to be up-converted is sampled at a relatively lower sampling rate. The baseband signal is filtered and translated using a higher sampling rate before being modulated onto a direct digitally synthesized (DDS) carrier frequency. The DUC performs pulse shaping of the incoming signal and modulation of an intermediate carrier frequency appropriate for driving a final analog up-converter. The multi stage implementation of these sample rate converters are computationally efficient [1]. The rest of the paper is organized as follows: Section 2 presents various filters used in DDC's and DUC's, sections 3 and 4 explain the implementations DDC and DUC in USRP B100 and USRP N210 respectively. Section 5 compares these filters and the final section provides results and conclusions.

2. Filters used in DDC and DUC

Many USRP platforms are available in the market and each of them makes use of different filters while realizing DDC and DUC. These filters are mainly: Cascaded integrator-comb (CIC) filter, Half Band filter (HBF), Hilbert filter and Root Raises Cosine (RRC) filter. The functionality of these filters and their application in DDC and DUC implementations are presented in the following subsections:

2.1. *Cascaded Integrator –Comb Filter*

The Cascaded integrator-comb (CIC) filters are computationally efficient implementations of various narrowband low-pass filters and are often embedded into the hardware. In order to introduce anti-aliasing filtering before decimation (i.e. reducing sample rate) and anti-imaging filtering for the signals that are to be interpolated (i.e. increasing sample rate), CIC filters are best suited and are widely used. Unlike most FIR filters, it has a decimator or interpolator built into its architecture. The difference equation of the CIC filter is given by the Eq. (1).

$$y(n) = x(n) - x(n - D) + y(n - 1), \quad (1)$$

where D is the delay

The CIC Filters have a linear phase characteristic response. It uses only delay, addition and subtraction operations alone and its realization does not require multiplication operation [2]. The system function for the composite CIC filter is given by the Eq. (2).

$$H(z) = [\sum_{k=0}^{RM-1} z^{-k}]^n, \quad (2)$$

where R = decimation or interpolation ratio, M = number of samples per stage, n = number of stages in filter.

While realizing a CIC filter, its comb section can be placed before the integrator section or/and after it. It is advantageous to place the comb section of CIC filter on that side of the filter which is operating at a lower sampling rate so that the storage requirements are reduced. The placement of the integrator section followed by its comb section results in a decimator and whereas the opposite placement of comb section followed by the integrator results in an interpolator. Fig. 1 illustrates the CIC filter as decimator and interpolator.

The comb section of the decimation filter has a delay length (N), called differential delay of D/R. In a similar manner, for the interpolation filter, introducing an N-sample delay before interpolation by R is equivalent to introducing a D-sample delay after interpolation by R which yields two major benefits:

a) the comb section's new differential delay or delay length is reduced to N = D/R which in turn decreases requirements for data storage

b) the comb section now operates at reduced clock rate.

Both of these yield reduced power consumption [3]. The multi-stage CIC cosine filter can be realized by cascading cosine pre-filters to the CIC filter to improve the stop-band CIC characteristics [4].

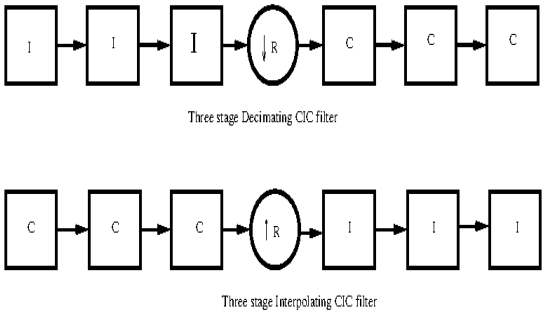

Fig. 1 CIC filter as Interpolator and Decimator [5]

2.2 Half- band filter

Half-band filter is a FIR filter with its transition region centered at one fourth of the sampling rate. Fig. 2 shows the structure of a Half Band filter (HBF). In the frequency response of the filter, the end of the pass-band and the beginning of the stop-band are equally spaced on either side of $f_s/4$.

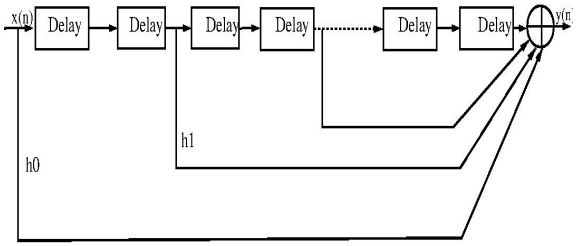

Fig. 2 Structure of a Half Band filter (HBF)[6]

Half-band filter is often used in decimation and interpolation filtering as half of its time domain coefficients are zero. This helps in achieving the performance of an M-tap FIR filter, while consuming the computational complexity of (M+1)/2+1 multiplications per filter output sample. Two HBF's are needed one as a filter and another as a decimator. The first HB filter acts as a filter to improve the attenuation of the low frequency signal as well as reduce the sampling frequency. A practical implementation of the Half Band Filters for decimation and interpolation can be seen in USRP-N210 and USRP-B100 platforms.

2.3 Hilbert filter

Hilbert Transform or precisely Hilbert filter finds its application while realizing the complex band-pass sampling scheme (CBPS). Hilbert transform introduces a 90-degree phase shift to all the sinusoidal components of the input signal. In the discrete-time periodic-

frequency domain, the transfer function of Hilbert transform is specified by the Eq. (3).

$$H(\jmath * \omega) = \begin{cases} -\jmath, & 0 < \omega < \Pi \\ \jmath, & -\Pi < \omega < 0 \end{cases} \qquad (3)$$

The CBPS can be used to overcome the difficulty of spectral signal placement in the frequency domain. In the realization of CBPS, the Hilbert filter is inserted prior to ADC to eliminate the negative frequency components of band-pass RF signals. By eliminating these, a reduction in the number of signal sets to be placed can be achieved and a lower sampling rate is sufficient without violating the Nyquist criterion when compared to Real Band Pass Sampling scheme (RBPS).

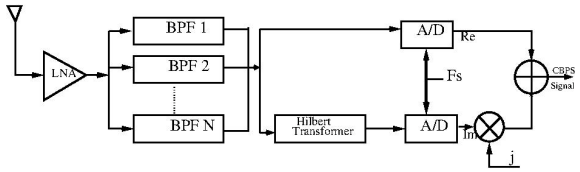

Fig. 3 depicts the usage of Hilbert transform in the CBPS [7]

2.4 Root Raised Cosine (RRC) filter

Root-raised-cosine filter (RRC) is prominently used as a matching filter in the transmitting and receiving sections in a digital communication system to reduce the ISI. The combined response of two such filters is that of the raised-cosine filter. The RRC filter is characterized by β, the roll-off factor and the reciprocal of symbol rate T_S. The impulse response of an RRC filter is given by Eq. (4). In order to shape the signal pulse in DDC and DUC applications, RRC filters are most suitable. In USRP-N210 platform, the RRC filter is used to shape the output signal. These RRC filters can also be used to down-sample or up-sample the incoming signal by a factor of 2.

3. Implementation of DDC/DUC in USRP-B100

3.1 Implementation of DDC

In USRPB100, Spartan-3A DSP1800 FPGA is used to process high speed sample rate incoming signals. In the receive path, two DDC's are implemented with each having 4 stages of CIC filters and two half-band filters. This platform uses the coordinate rotation digital computer (CORDIC) algorithm to implement numerically controlled oscillator (NCO). One DDC is used for the in-phase (I) channel and a second DDC for the quadrature (Q) channel. The conversion of the signal to its I and Q components can be done by making use of the Hilbert filter.

$$H(t) = \begin{cases} 1 - \beta + 4 * \frac{\beta}{\Pi}, & t = 0 \\ \frac{\beta}{\sqrt{2}}[(1 + \frac{2}{\Pi})\sin(\frac{\Pi}{(4\beta)}) & \\ +(1 - \frac{2}{\Pi}) * \cos(\frac{\Pi}{4\beta})], & t = \pm\frac{T_s}{4\beta} \\ \sin(\frac{t\Pi}{T_s(1-\beta)}) + & \\ (\frac{4t\beta}{T_s}) * \frac{(\cos(\frac{(1+\beta)t\Pi}{T_s}))}{(1 - (\frac{4t\beta}{T_s})^2)\frac{t\Pi}{T_s}} & \text{otherwise} \end{cases} \qquad (4)$$

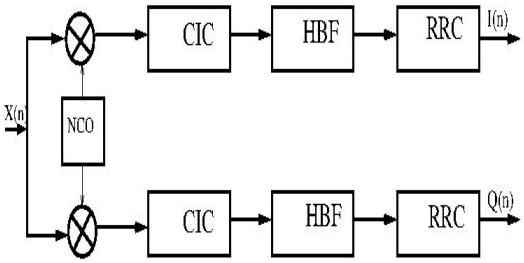

Fig. 4 shows the DDC block diagram with its RRC filter [8]

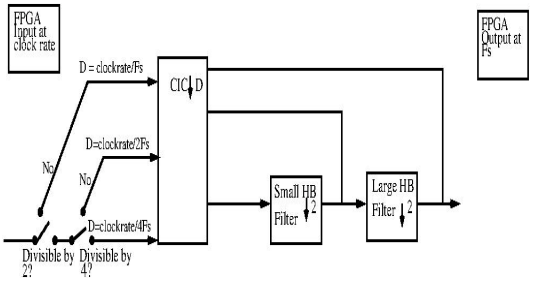

Fig. 5 depicts the signal flow in the DDC in USRPB100 [9]

3.2 Implementation of DUC

The application of DUC is in the transmission path of the signal from the FPGA to the antenna. Therefore, the transmitter path is responsible for interpolating the signal to the required sample rate of 32 MSps for the default 64- MHz clock rate. Two half-band filters are present prior to the CIC if the interpolation rate is a factor of four. If the interpolation rate is a factor of two, then only one half-band filter is used. If the interpolation factor is odd, then no half-band filters are used. Also, there are two transmit paths for a single complex channel just like in the receive data path.

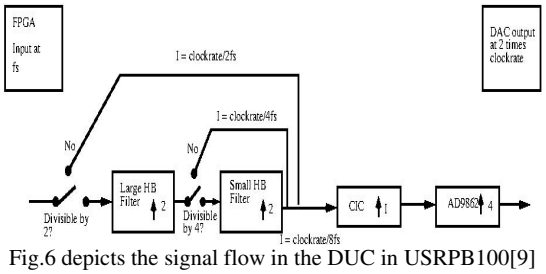

Fig.6 depicts the signal flow in the DUC in USRPB100[9]

4. Implementation of DDC/ DUC in USRPN210

The FPGA used in USRP N210 is Xilinx Spartan 3A DSP and both DDC and DUC takes place in the FPGA only. The FPGA operation frequency for Spartan-DSP FPGA design is 122.88 MHz.

4.1 Implementation of DDC

In the implementation of DDC, there are 3 main blocks namely first half band filter, second half band filter and finally the RRC filter. For the reference design, the input to the DDC is a real signal sampled at 16xFchip = 61.44 MSPS and quantized to 14 bits. The complex baseband output are generated at a sampling rate of 2xFchip = 7.68 MSPS.

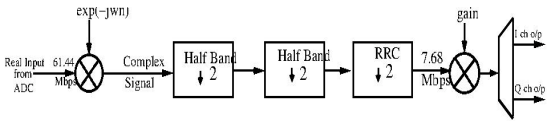

Fig. 7 shows the implementation of DDC in USRPN210[9]

The first decimation filter is designed to reduce the sampling rate by 2. It is realized using the computationally efficient half-band filter structure. The input sample rate of the filter is 61.44 MSPS, and the output sample rate is 30.72 MSPS, 8x the chip rate. The second half band filter further decimates the data by two, from 30.72 MSPS to 15.76 MSPS. The pass band edge is set to 2.34 MHz, the same as that in the first half band filter, determined by the chip rate and the RRC roll-off. The receiver channel filter is an RRC filter matched to the one used in the uplink transmitter. The filter also provides a decimation-by-2 to reduce the sampling rate from 15.36 MSPS to 7.68 MSPS.

4.2 Implementation of DUC

In the transmit section of the USRP, Time Division Multiplexing can be used for streaming the in-phase and quadrature phase components into a single stream before being processed by the interpolation filters.
Xilinx Finite Impulse Response (FIR) Compiler block is used in implementing the four stage interpolators. Multiply-Accumulate (MAC) architecture can be utilized for a FIR compiler block which provides a common interface to generate a parameterizable, area-efficient, and high-performance filter module. Multiple MACs may be used in achieving higher performance filter requirements, such as longer filter coefficients, higher throughput, or support for more channels.

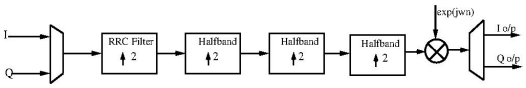

Fig. 8 shows the signal flow in DUC in USRPN210[9]

5. Comparison of different filters

Using MATLAB, we compared the performance of these filters and also with a single stage interpolator or decimator realized from a single FIR filter. Fig. 9 shows the magnitude response of 8-scale interpolator realized from a single FIR filter and a multi-stage three Half Band Filters. Each Half Band Filter provides an interpolation factor of 2 and hence a combination of 3 Half Band filters provides a interpolation factor of 8. Tables 1 and 2 show the computations required for both the interpolation and the decimation systems, respectively.

Table 1 Comparison of Single stage Vs. Multi –stage HBF 8-Interpolation

Parameter	Single stage	Multi-stage HBF
Multipliers	637	99
Adders	636	96
States	720	186
Mults per sample	79.625	15.375
Adds per sample	79.5	14.5

Table 2 Comparison of Single stage Vs. Multi –stage HBF 8-Decimation

Parameter	Single stage	Multi-stage HBF
Multipliers	650	188
Adders	649	185
States	648	194
Mults per sample	81.25	27.25
Adds per sample	81.125	26.375

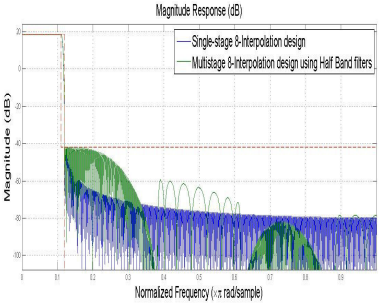

Fig. 9 Magnitude responses for 8-Interpolation using direct filter and 3 stage HBF

Fig. 10 shows a similar analysis for the implementation of 8 scale Decimation using single stage FIR and a multi stage HBF.

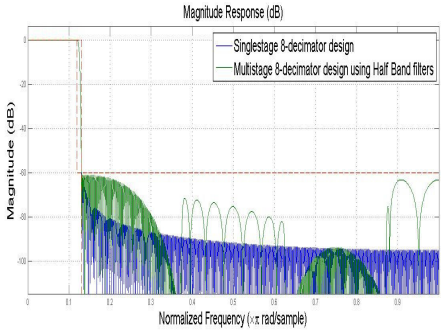

Fig. 10 Magnitude responses for 8-Decimation using direct filter and 3 stage HBF

Fig. 11 shows the interpolation magnitude responses. Fig. 12 shows the decimator magnitude responses. Similar comparison is done with respect to interpolator and decimators realized by RRC filters also. Fig. 13 shows the interpolation magnitude responses and the Fig. 14 shows the decimator magnitude responses. We also tried to compare the magnitude responses of the interpolators and decimators realized by CIC, Half Band Filter and Root Raised Cosine filters. Fig. 15 shows the comparison of Interpolators and the Fig. 16 shows the comparison of decimators.

Tables 3 and 4 present computational requirements comparisons of the three interpolators and the three decimators, respectively.

Table 3 Comparison of CIC, HBF and RRC for 8-Interpolation

Parameter	CIC	HBF	RRC
Multipliers	0	239	784
Adders	12	233	777
States	18	110	98
Mults per sample	0	272	784
Adds per sample	54	262	777

Table 4 Comparison of CIC, HBF and RRC for 8-Decimation

Parameter	CIC	HBF	RRC
Multipliers	0	99	785
Adders	6	96	784
States	9	186	784
Mults per sample	0	15.375	98.125
Adds per sample	3.375	14.5	98

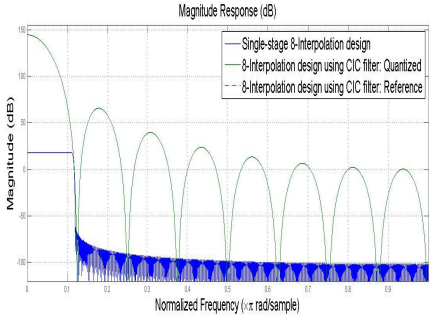

Fig. 11 Magnitude responses for 8-Interpolation using direct filter and 3 stage CIC filter

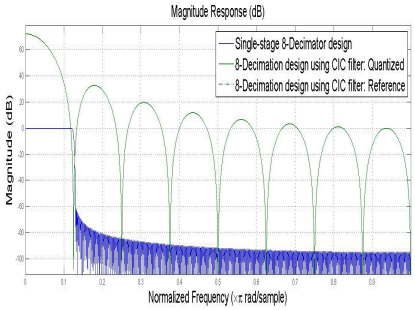

Fig. 12 Magnitude responses for 8-Decimation using direct filter and 3 stage CIC filter

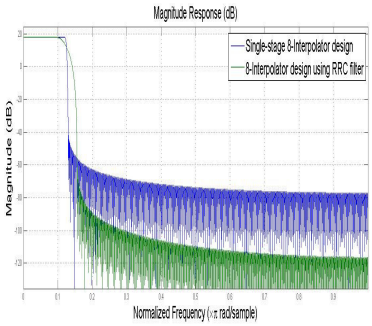

Fig. 13 Magnitude responses for 8-Interpolation using direct filter and 3 stage RRC filter

6. Results and Conclusions

Based on the simulation analysis using MATLAB, the following conclusions can be made while CIC, RRC and Half Band filters are used as interpolators and decimators. The computational requirement for CIC filter is the least and the same for RRC is the highest. The pass band ripple is the least for Root Raised cosine filter, increases for Half Band filter and is the highest for CIC. The implementation of Interpolation and Decimation in multiple stages is more beneficial than using a single filter for realizing the application with

respect to the computational complexity. The multiple stages of implementation results in more ripple in the pass band when compared to its single stage implementation. CIC filters are often used for higher order interpolation and decimation applications. In this work, various filters and their structures, used in DDC/DUC processing in different USRP platforms,

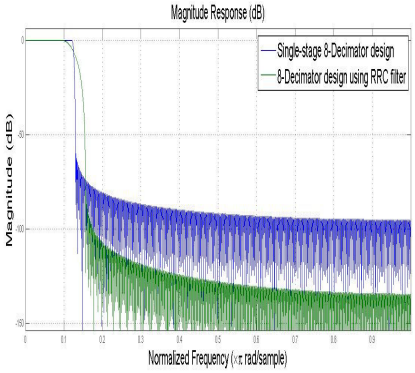

Fig. 14 Magnitude responses for 8-Decimation using direct filter and 3 stage RRC filter

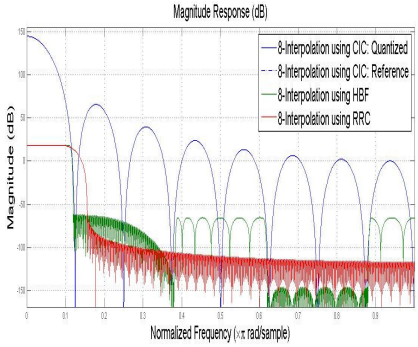

Fig. 15 Magnitude responses for 8-Interpolation using all three filters

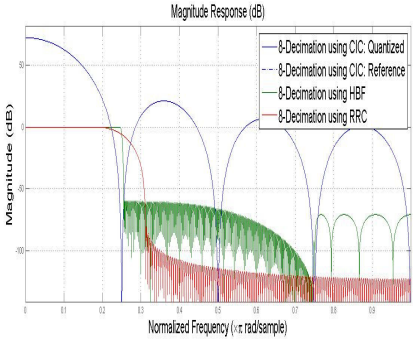

Fig. 16 Magnitude responses for 8-Decimation using all three filters

USRPB100 and USRPN210. The comparison of the magnitude responses and the computational complexities involved when different filters are used as interpolator and decimator is also given. Based on the results, it can be concluded that based on the computational requirements and the allowed pass band ripple factor, the appropriate filter can be chosen during DDC and DUC processing.

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