DDC and DUC Filters in SDR platforms

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***Abstract*—This paper elucidates on the different types of filters used for DDC and DUC conversions. They constitute the most crucial functions in the implementation of SDR.The paper also further discusses filters from the point of view of its usage on different USRP platforms like USRPB100 and USRPN210 along with their respective analysis for interpolation and decimation operations. A comparative study of CIC, RRC and Half band filters on the basis of its computational requirements and magnitude responses is carried out.**

I. INTRODUCTION

Reconfigurable features of SDR platforms makes them widely applicable in different means of wireless communications. In order to digitize the band limited RF or IF signals which generates high data rates, we require fast ADC converters to perform the job. But, generally the information bearing signal present in the RF or IF signal is usually very less when compared to the total bandwidth of the signal. The Digital Down Converter (DDC) is used for translating the frequency band of interest down the spectrum making sure that the Nyquist criterion is not violated for the bandwidth of the information bearing message which results in the reduction of sampling rate. This reduces the overall filter requirements and make the further processing on the signal easily realizable without much computational as well as power requirements. The DUC is another important component in digital radio transmitter. The DUC is used to translate a complex digital baseband signal to a real pass band signal. The input complex baseband signal to be up-converted is sampled at a relatively lower sampling rate. The baseband signal is filtered and translated using a higher sampling rate before being modulated onto a direct digitally synthesized (DDS) carrier frequency. The DUC performs pulse shaping of the incoming signal and modulation of an intermediate carrier frequency appropriate for driving a final analog up-converter. The multi stage implementation of these sample rate converters are computationally efficient [1]. The rest of the paper is organized as follows: Section II presents various filters used in DDCs and DUCs, sections III and IV explain the implementations DDC and DUC in USRP B100 and USRP N210 respectively. Section V compares these filters and the final section provides results and conclusions.

II. FILTERS USED IN DDC AND DUC

Many USRP platforms are available in the market and each of them have their filters used for realizing DDC and DUC. Different types of filters used are Cascaded integrator-comb (CIC) filter, Half Band filters, Hilbert filters and Root Raises Cosine (RRC) filter. The functionality of these filters and their application in the DDC and DUC implementations is discussed in the following sub-sections.

A. CASCADED INTEGRATOR-COMB Filter

The Cascaded integrator-comb (CIC) filters are computationally efficient implementations of various narrowband low-pass filters and are often embedded into the hardware. A CIC filter basically consists of two stages, one having ideal integrator filters and the other stage having comb filters. Both stages have equal number of filters. The frequency response of the CIC filter can be tuned by using the required number of cascaded integrator an comb filter pairs.One of the major benefit of the CIC filter is its symmetric structure which makes the implementation in hardware quite easily realizable. One of the disadvantage is its passband ripple which is quite high and this demands the requirement of compensation filters. The difference equation of the CIC filter is given by equation (1).

$$y(n) = x(n) - x(n - D) + y(n - 1), \tag{1}$$

where D is the delay The response of a CIC filter is linear and its implementation does require only operations like delay, addition and subtraction operations alone and the does not need multiplication operation [2]. The system function for the composite CIC filter is given by equation (2).

$$H(z) = [\sum_{k=0}^{RM-1} z^{-k}]^n, \tag{2}$$

where R = decimation or interpolation ratio, M = number of samples per stage, n = number of stages in filter. The usage of CIC filter as interpolator or decimator depends on the way the integrator and comb sections are placed. The functionality of interpolation can be realized by placing the integrator section followed by comb section where as the reverse will realize in decimation. However,it is beneficial to place the comb section of CIC filter on the side of the filter operating at the lower sample rate because of which the storage requirements are greatly reduced. Fig. 1 illustrates the CIC filter as decimator and interpolator.

The differential delay is the delay length(N) that is present in the comb section and has a value of D/R. In the case of interpolation filter, placing an N sample delay before

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interpolation by R is equivalent of placing a D-sample delay after interpolation. This approach has two major benefits:
a) Reduction in data storage requirements because of the new differential delay of the comb section and the reduction in delay length to N = D/R b) the operation of the comb section at a lower clock rate. Both the above phenomenon yields in reduction of power consumption [3]. In case to improve the stop band characteristics, cascading cosine pre-filters to the CIC filter can be employed [4].

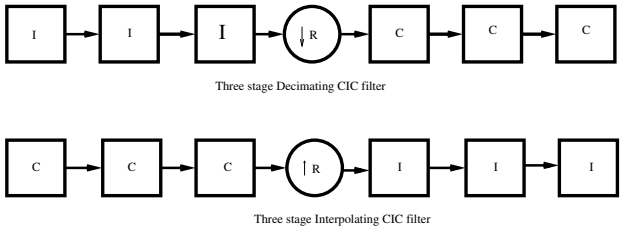

Fig. 1. CIC filter used as decimator and integrator [5]

B. HALF BAND FILTER

Half-band filter (HBF) is a FIR filter where in the transition region of the filter is centered at quarter of the sampling rate. Fig. 2 shows the structure of a Half Band filter (HBF). In the frequency response of the filter, the end of the passband and the beginning of the stop-band are equally spaced on either side of fs/4.

In Interpolation and Decimation applications, Half-band filters are often used with the main reason being that the half of its time domain coefficients are zero which helps in realizing the performance of M-tap filter with the computational complexity of (M+1)/2 + 1 multiplications per filter output sample. Half-band filter is often used in decimation and interpolation filtering as half of its time domain coefficients are zero. This helps in achieving the performance of an M-tap FIR filter, while consuming the computational complexity of (M+1)/2+1 multiplications per filter output sample. Usually we employ two HBFs for interpolation adn decimation in which the first filter acts as filter and the next filter acts as a decimator. The first HB filter helps in improving the attenuation of the lower frequency signal which in turn helps in reducing the sampling rate. A practical implementation of the Half Band Filters for decimation and interpolation can be seen in USRP-N210 and USRP-B100 platforms.

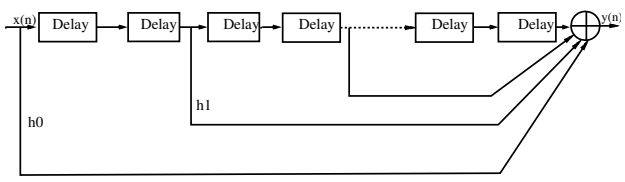

Fig. 2. Structure of a Half Band filter [6]

C. HILBERT FILTERS

Hilbert Transform is a filter which introduces a 90-degree phase shift to the sinusoidal components of the incoming signal and this phenomenon is used in the realization of the Complex Bandpass Sampling Scheme.In the discrete-time periodic-frequency domain, the transfer function of Hilbert transform is specified by equation (3)

$$H(\jmath * \omega) = \begin{cases} -\jmath, & 0 < \omega < \Pi \\ \jmath, & -\Pi < \omega < 0 \end{cases} \tag{3}$$

In time domain Hilbert transform can be expressed as

$$h(n) = \begin{cases} \dfrac{2 * (\sin(\Pi * n))^2}{\Pi * n}, & \text{if } n \neq 0 \\ 0, & \text{otherwise} \end{cases} \tag{4}$$

CBPS when compared to Real Band Pass Sampling scheme (RBPS) can overcome the problem of placing the signal in frequency domain. Because of the introduction of the Hilbert filter before the ADC, the negative frequency components are totally eliminated which gives the benefit of the reduction in the signal components and without the violation of Nyquist criterion, a lower sampling rate can perform the required task on the signal. Fig. 3 depicts the usage of Hilbert transform in the CBPS scheme.

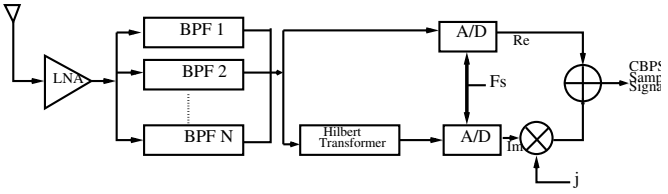

Fig. 3. Complex BandPass Sampling scheme [7]

D. ROOT RAISES COSINE FILTER

The raised cosine filter is used extensively in wireless transmission for pulse shaping the chip stream output in order to overcome problems like Inter Symbol Interference (ISI), before the process of RF modulation. RRC filter makes the spectrum bandwidth limited in order to avoid interferences with neighbour symbols. The RRC filter is characterised by β the roll-off factor and the reciprocal of symbol rate T_s. The

impulse response of an RRC filter is given by equation (5).

$$H(t) = \begin{cases} 1-\beta+4*\frac{\beta}{\Pi}, & t=0 \\ \frac{\beta}{\sqrt{2}}[(1+\frac{2}{\Pi})\sin(\frac{\Pi}{(4\beta)}) & \\ +(1-\frac{2}{\Pi})*\cos(\frac{\Pi}{4\beta})], & t=\pm\frac{T_s}{4\beta} \\ \sin(\frac{t\Pi}{T_s(1-\beta)})+(\frac{4t\beta}{T_s})* & \\ \frac{(\cos(\frac{(1+\beta)t\Pi}{T_s}))}{(1-(\frac{4t\beta}{T_s})^2)\frac{t\Pi}{T_s}} & \text{otherwise} \end{cases} \quad (5)$$

In order to shape the signal pulse in DDC (Digital Down Conversion) and DUC (Digital Up Conversion) applications. Root Raises Cosine filter are most suitable. The interpolation or decimation ratio that can be achieved using RRC is two. In practical applications, RRC filters are used in decimation and interpolation sections of USRPN210 platform.

III. IMPLEMENTATION OF DDC AND DUC IN USRPB100

A. Implementation of DDC

In USRPB100, Spartan-3A DSP1800 FPGA is used to process high speed sample rate incoming signals. Two Digital Down Conversion's are implemented in the receive path. Each route has 4 stages of CIC filters and have two half band filters. Coordinate Rotation Digital Computer(CORDIC) algorithm is used in this platform for the realization of Numerically Controlled Oscillator (NCO). The two DDC's are used for the in-phase and quadrature phase channels of the incoming signals. Hilbert filter is used for the conversion of the signal into In-phase and Quadrature-phase components.

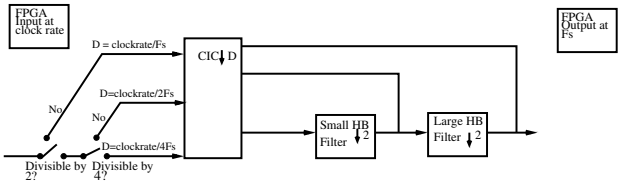

Fig. 4. Implementation of DDC in USRPB100 [8]

Table I gives the computational requirements for different decimation rates. Since CIC filter is used for higher decimation rates , there is no difference in the computations. But the problem of ripple comes with the introduction of CIC.

Fig. 5 shows the magnitude response of the DDC implementation for decimation rates of 16 and 24.

B. Implementation of DUC

DUC is the conversion of the signal in the transmission path from the FPGA to the antenna. In the case of USRPB100, the transmitter path has to interpolate the incoming the signal to

TABLE I
COMPUTATIONAL COMPARISON FOR DDC IN USRPB100

Decimation rate	Adders/sample	Multiplications/sample
4	192	188
8	206	188
16	204	188
24	201	188

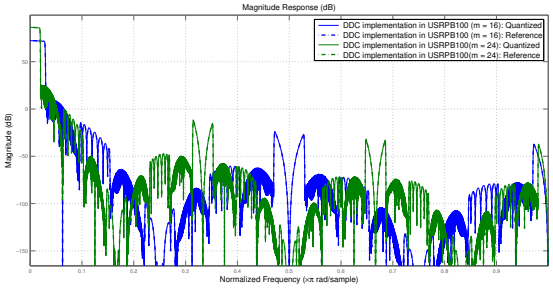

Fig. 5. Magnitude response of DDC implementation in USRPB100

the required 32MSps sampling rate for the default clock rate of 64- Mhz. In the implementation, two half-band filters are present prior to the CIC if the interpolation rate is a factor of four. If the interpolation rate is a factor of two, then only one half-band filter is used. If the interpolation factor is odd, then no half-band filters are used. There are two transmit paths here also just like the receive path for the in-phase and the quadrature phase components. Fig. 7 shows the magnitude

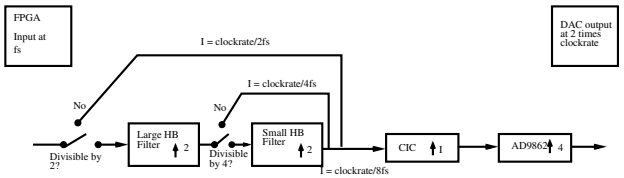

Fig. 6. Implementation of DUC in USRPB100 [8]

response of the DUC implementation for interpolation rates of 16 and 24.

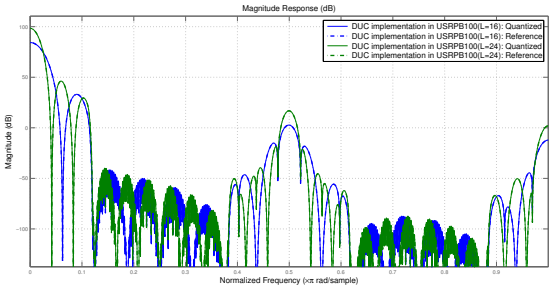

Fig. 7. Magnitude Response of DDC implementation in USRPB210

As shown in Table I, a similar trend is followed.

IV. IMPLEMENTATION OF DDC AND DUC IN USRP N210

Xilinx Spartan 3A DSP is used as FPGA in USRP N210 which performs both the operations of DDC and DUC functions. The FPGA operation frequency for Spartan-DSP FPGA design is 122.88 MHz.

A. Implementation of DDC

In this platform, three stages are employed for decimation with each stage that can perform a decimation factor of 2. In the implementation of DDC, there are 3 main blocks namely first half band filter, second half band filter and finally the RRC filter. For the reference design, the input to the DDC is a real signal sampled at 16xFchip = 61.44 MSPS and quantized to 14 bits. The complex baseband output are generated at a sampling rate of 2xFchip = 7.68 MSPS. Fig. 8 shows the implementation of DDC.

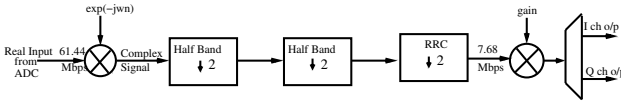

Fig. 8. Implementation of DDC in USRP N210 [8]

The first decimation filter is designed to reduce the sampling rate by 2. It is realized using the computationally efficient half-band filter structure. The input sample rate of the filter is 61.44 MSPS, and the output sample rate is 30.72 MSPS, 8x the chip rate. The second half-band filter further decimates the data by two, from 30.72 MSPS to 15.76 MSPS. The passband edge is set to 2.34 MHz, the same as that in the first halfband filter, determined by the chip rate and the RRC roll-off. The receiver channel filter is an RRC filter matched to the one used in the uplink transmitter. The filter also provides a decimation-by-2 to reduce the sampling rate from 15.36 MSPS to 7.68 MSPS, 2 times the chip rate.

Fig. 9 shows the magnitude response of the DDC system implemented in the USRP platform USRPN210.

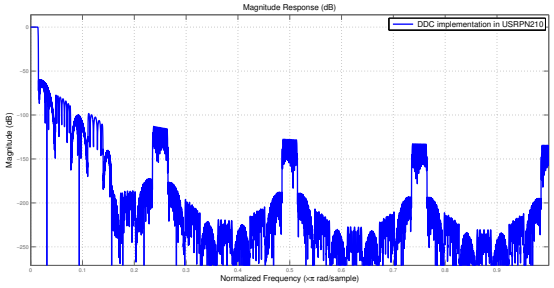

Fig. 9. Magnitude Response of DDC implementation in USRPN210

B. Implementation of DUC

Let us see the transmit section of the USRP in which interpolation function need to be executed. In the transmit section of the USRP, Time Division Multiplexing can be used for streaming the the in-phase and quadrature phase components into a single stream before being processed by the interpolation filters. Fig. 10 shows the signal flow in DUC.

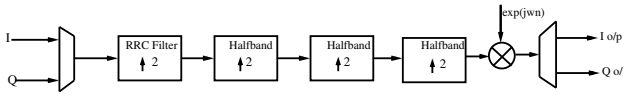

Fig. 10. Implementation of DUC in USRP N210 [8]

Xilinx Finite Impulse Response (FIR) Compiler block is used in implementing the four stage interpolators. Multiply-Accumulate (MAC) architecture can be utilized for a FIR compiler block which provides a common interface to generate a parameterisable, area-efficient, and high-performance filter module. Multiple MAC's may be used in achieving higher performance filter requirements, such as longer filter coefficients, higher throughput, or support for more channels. Fig. 11 shows the magnitude response of the DUC system implemented in the USRP platform USRPN210. Table II gives

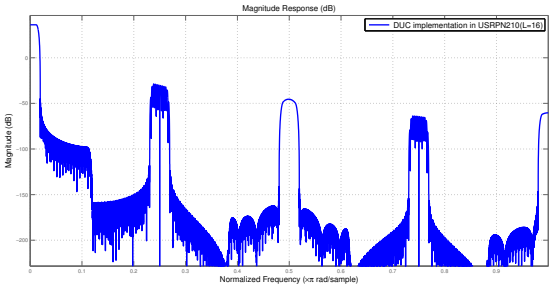

Fig. 11. Magnitude Response of DUC implementation in USRPN210

the computational requirements needed for interpolation and decimation in USRPN210 which shows more computational requirement for Interpolation due to 3 Half band filters present.

TABLE II
COMPUTATIONAL ANALYSIS FOR DDC AND DUC IN USRPN210

Implementation	Adders/sample	Multiplications/sample
Interpolation	2480	2409
Decimation	104.2	103.9

V. COMPARISON AMONG DIFFERENT FITERS

The performance comparison of these filters and also with a single stage interpolator or decimator realized from a single FIR filter is done by using MATLAB. Fig. 12 shows the magnitude response of 8-scale interpolation realized from a single FIR filter and a multi-stage three Half Band Filters. Each Half Band Filter provides an interpolation factor of 2 and hence a combination of 3. Half Band filter provides an interpolation factor of 8. Tables 1 and 2 show the computations required for both the interpolation and the decimation systems, respectively.

TABLE III
COMPARISON OF SINGLE STAGE V/S MULTI-STAGE HBF 8-INTERPOLATION

Parameter	Single-stage	Multi-stage HBF
Multipliers	637	99
Adders	636	96
States	720	186
Mults per Sample	79.625	15.375
Adds per Sample	79.5	14.5

TABLE IV
COMPARISON OF SINGLE STAGE V/S MULTI-STAGE HBF 8-DECIMATION

Parameter	Singlestage	Multistage HBF
Multipliers	650	188
Adders	649	185
States	648	194
Mults per Sample	81.25	27.25
Adds per Sample	81.125	26.375

Fig. 13 shows a similar analysis for the implementation of 8 scale Decimation using single stage FIR and a multi stage HBF.

Fig. 14 shows the interpolation magnitude responses and Fig. 15 shows the decimator magnitude responses using CIC filters. Similar comparison is done with respect to interpolator and decimators realized by RRC filters also. Fig. 15 shows the interpolation magnitude responses and the Fig. 16 shows the decimator magnitude responses. We also tried to compare the magnitude responses of the interpolators and decimators realized by CIC, Half Band Filter and Root Raised Cosine filters. Fig. 16 shows a comparison of Interpolators and the Fig. 17 shows a comparison of decimators.

Tables V and VI present computational requirements comparisons of the three interpolators and the three decimators, respectively.

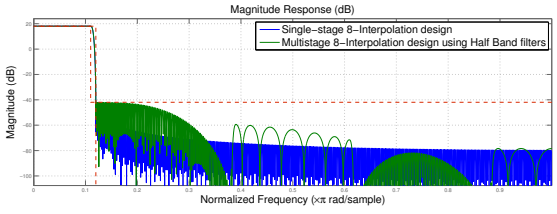

Fig. 12. Magnitude responses for 8-Interpolation using direct filter and 3 stage HBF

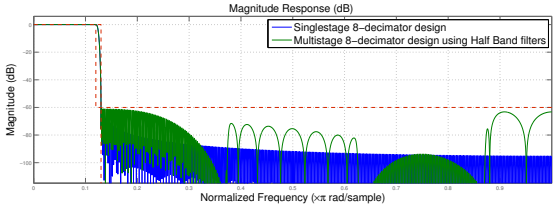

Fig. 13. Magnitude responses for 8-Decimation using direct filter and 3 stage HBF

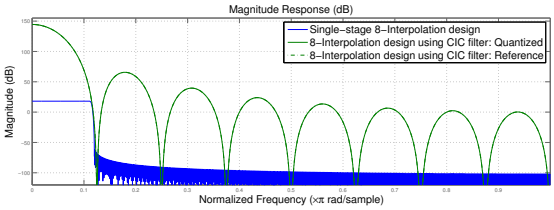

Fig. 14. Magnitude responses for 8-Interpolation using direct filter and a CIC filter

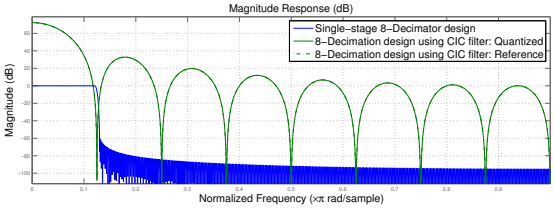

Fig. 15. Magnitude responses for 8-Decimation using direct filter and a CIC filter

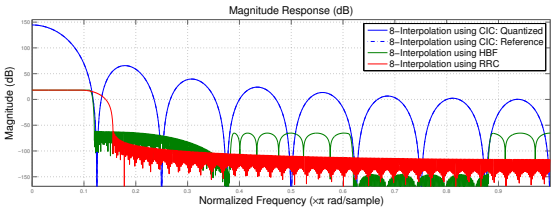

Fig. 16. Magnitude responses of the three filters as interpolators

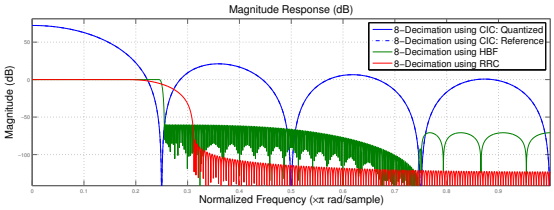

Fig. 17. Magnitude responses of the three filters used as decimators

TABLE V
COMPARISION BETWEEN CIC, HBF AND RCC FOR 8-INTERPOLATION

Parameter	CIC	HBF	RRC
Multipliers	0	239	784
Adders	12	233	777
States	18	110	98
Mults per Sample	0	272	784
Adds per Sample	54	262	777

TABLE VI
COMPARISION BETWEEN CIC, HBF AND RCC FOR 8-DECIMATION

Parameter	CIC	HBF	RRC
Multipliers	0	99	785
Adders	6	96	784
States	9	186	784
Mults per Sample	0	15.375	98.125
Adds per Sample	3.375	14.5	98

VI. RESULTS AND CONCLUSIONS

Based on the simulation analysis using MATLAB, the following conclusions can be made while CIC, RRC and Half

Band filters are used as interpolators and decimators.

From the results obtained using MATLAB, a tabular comparison is presented in Table VII. This comparison is made with respect to the usage of CIC, RRC and Half Band filters for Interpolation and Decimation applications.

TABLE VII
COMPARISON AMONG DIFFERENT FILTERS FOR MULTI-RATE APPLICATIONS

Parameter	CIC	HBF	RRC
Computational Requirement	Least	more	very high
Pass band ripple	Very High	tolerable	very less
Implementation	Higher order	All orders	All orders
Ripple(single-stage)	Very High	more	less
Computations(single-stage)	very less	less	more

CIC filters are mainly employed for higher order interpolation and decimation applications and not for lower order implementations and the CIC filters are used along with other filters when used in application. Various USRP platforms like USRPB100 and USRPN210 are taken into consideration and the process of interpolation and decimation is studied and different filters employed in the process are studied. Based on the results, it can be concluded that based on the computational requirements and the allowed pass band ripple factor, the appropriate filter can be chosen during DDC and DUC processing.

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