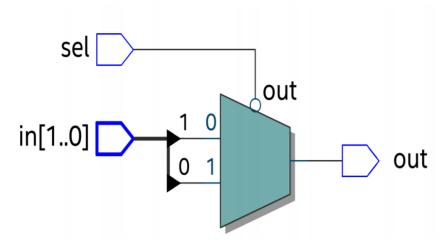
Mux 2to1

o Behavioral



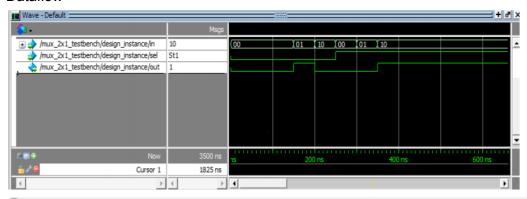
Ana	lysis & Synthesis Resource Usage Summary	
• <	<filter>></filter>	
	Resource	Usage
1	➤ Estimated ALUTs Used	1
1	Combinational ALUTs	1
2	Memory ALUTs	0
3	LUT_REGs	0
2	Dedicated logic registers	0
3		
4	> Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	▽ Combinational ALUTby number of inputs	
1	7 input functions	0
2	6 input functions	0
3	5 input functions	0
4	4 input functions	0
5	<=3 input functions	1
8		
9	> Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	> Total registers	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	out~0
21	Maximum fan-out	1
22	Total fan-out	8
22	Average for out	0.00



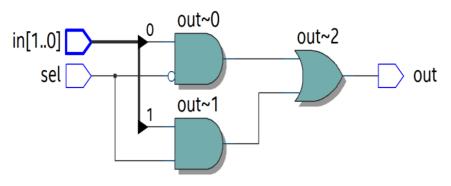
Transcript =

```
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim > vsim work.mux_2x1_testbench
# vsim work.mux 2x1 testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv_std.std
# Loading work.mux_2xl_testbench
# Loading work.mux_2x1
add wave -position insertpoint sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run
# time=0, in=00 sel=0 out=0
 time=150, in=01 sel=0 out=1
  time=200, in=10 sel=0 out=0
  time=250, in=00 sel=1 out=0
  time=300, in=01 sel=1 out=0
  time=350, in=10 sel=1 out=1
```

Dataflow

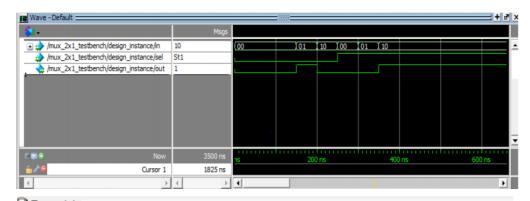


```
🖳 Transcript 🗆
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim > vsim work.mux_2x1_testbench
# vsim work.mux_2xl_testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv_std.std
# Loading work.mux 2x1 testbench
# Loading work.mux_2xl
add wave -position insertpoint sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run
# time=0, in=00 sel=0 out=0
  time=150, in=01 sel=0 out=1
  time=200, in=10 sel=0 out=0
  time=250, in=00 sel=1 out=0
  time=300, in=01 sel=1 out=0
   time=350, in=10 sel=1 out=1
```

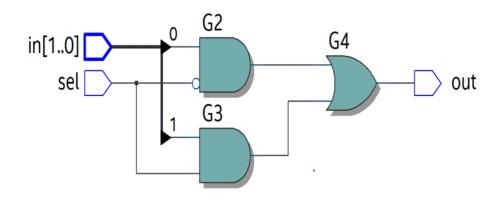


Ana	lysis & Synthesis Resource Usage Summary	
٩.	< <filter>></filter>	
	Resource	Usage
1	✓ Estimated ALUTs Used	1
1	Combinational ALUTs	1
2	Memory ALUTs	0
3	LUT_REGs	0
2	Dedicated logic registers	0
3		
4	> Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	➤ Combinational ALUTby number of inputs	
1	7 input functions	0
2	6 input functions	0
3	5 input functions	0
4	4 input functions	0
5	<=3 input functions	1
8		
9	> Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	▼ Total registers	0
1	Dedicated logic registers	0
2	I/O registers	0
3	LUT_REGs	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan aut nada	at0

Gate-Level Model



```
🖳 Transcript 🗆
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim > vsim work.mux_2x1_testbench
# vsim work.mux 2x1 testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv std.std
# Loading work.mux 2x1 testbench
# Loading work.mux 2x1
add wave -position insertpoint sim:/mux_2xl_testbench/design_instance/*
VSIM 6> run
# time=0, in=00 sel=0 out=0
  time=150, in=01 sel=0 out=1
  time=200, in=10 sel=0 out=0
  time=250, in=00 sel=1 out=0
  time=300, in=01 sel=1 out=0
  time=350, in=10 sel=1 out=1
```



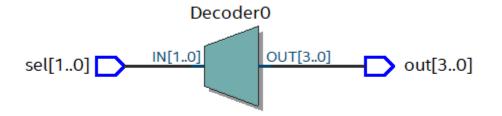
	lysis & Synthesis Resource Usage Summary	
• <	< <filter>></filter>	
	Resource	Usage
1	➤ Estimated ALUTs Used	1
1	Combinational ALUTs	1
2	Memory ALUTs	0
3	LUT_REGs	0
2	Dedicated logic registers	0
3		
4	> Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	♥ Combinational ALUTby number of inputs	
1	7 input functions	0
2	6 input functions	0
3	5 input functions	0
4	4 input functions	0
5	<=3 input functions	1
8		
9	> Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	> Total registers	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	G4~0
21	Maximum fan-out	1
22	Total fan-out	8
22	A	0.00

• 2to4 Decoder

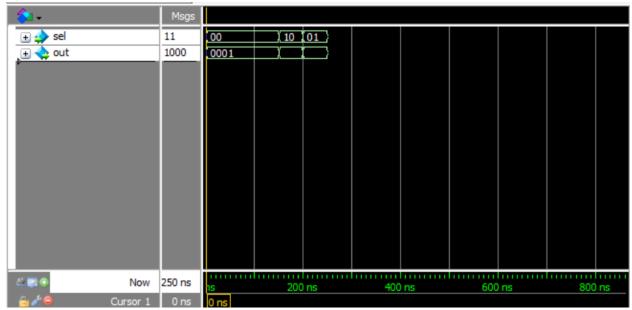
o Behavioral

■ Usage Summary: **observe**

	sis & Synthesis Resource Usage Summary			lysis & Synthesis Resource Usage Summary	
<<	Filter>>			< <filter>></filter>	
	Resource	Usage		Resource	Usage
1 ~	Estimated ALUTs Used	4	2	Dedicated logic registers	0
1	Combinational ALUTs	4	3		
2	Memory ALUTs	0	4	➤ Estimated ALUTs Unavailable	0
3	LUT_REGs	0	1	Due to unpartnered combinational logic	0
2	Dedicated logic registers	0	2	Due to Memory ALUTs	0
3			5	Due to Fichiory A2013	
4 🔻	✓ Estimated ALUTs Unavailable	0	6	Total combinational functions	4
1	Due to unpartnered combinational logic	0	7	➤ Combinational ALUT usage by number of inputs	1
2	Due to Memory ALUTs	0	1	7 input functions	0
5			2	6 input functions	0
6	Total combinational functions	4	3	5 input functions	0
7 ~	Combinational ALUT usage by number of inputs		4	4 input functions	0
1	7 input functions	0	5	<= 3 input functions	4
2	6 input functions	0	8	<- 3 input functions	4
3	5 input functions	0		As Combinational ALUTa burneds	
4	4 input functions	0	9	✓ Combinational ALUTs by mode normal mode	
5	<= 3 input functions	4	1		4
8	·		2	extended LUT mode	0
9 🔻	✓ Combinational ALUTs by mode		3	arithmetic mode	0
1	normal mode	4	4	shared arithmetic mode	0
2	extended LUT mode	0	10		
3	arithmetic mode	0	11	Estimated ALUT/register pairs used	4
4	shared arithmetic mode	0	12		
10			13	▼ Total registers	0
11	Estimated ALUT/register pairs used	4	1	Dedicated logic registers	0
12	/0		2	I/O registers	0
	✓ Total registers	0	3	LUT_REGs	0
1	Dedicated logic registers	0	14		
2	I/O registers	0	15		
3	LUT REGs	0	16	I/O pins	6
14			17		
15			18	DSP block 18-bit elements	0
16	I/O pins	6	19		
17	4 - F	-	20	Maximum fan-out node	sel[0]~inpu
18	DSP block 18-bit elements	0	21	Maximum fan-out	4
19	Doi block to bicelements		22	Total fan-out	18
20	Maximum fan aut nada	colfOleripput	23	Average fan-out	1.13



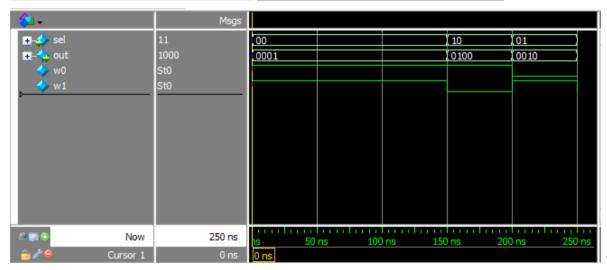
Modelsim:

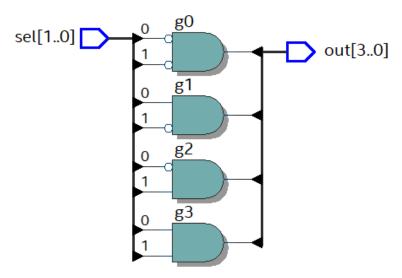


```
ModelSim> vsim work.decoder_2to4_testbench
# vsim work.decoder_2to4_testbench
# Start time: 11:50:12 on Jul 17,2021
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -position insertpoint sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
# time=0, sel=00 out=0001
#
# time=150, sel=10 out=0100
#
# time=200, sel=01 out=0010
#
# time=250, sel=11 out=1000
```

Gate-Level Model

	lysis & Synthesis Resource Usage Summary			llysis & Synthesis Resource Usage Summary	
٩ <	< <filter>></filter>		_	< <filler>></filler>	
	Resource	Usage		Resource	Usage
	▼ Estimated ALUTs Used	4	2	Dedicated logic registers	0
	Combinational ALUTs	4	3		
	Memory ALUTs	0	4	➤ Estimated ALUTs Unavailable	0
	LUT_REGs	0	1	Due to unpartnered combinational logic	0
	Dedicated logic registers	0	2	Due to Memory ALUTs	0
			5		
	▼ Estimated ALUTs Unavailable	0	6	Total combinational functions	4
	Due to unpartnered combinational logic	0	7	▼ Combinational ALUT usage by number of inputs	
	Due to Memory ALUTs	0	1	7 input functions	0
			2	6 input functions	0
	Total combinational functions	4	3	5 input functions	0
	▼ Combinational ALUT usage by number of inputs		4	4 input functions	0
	7 input functions	0	5	<=3 input functions	4
	6 input functions	0	8		
	5 input functions	0	9		
	4 input functions	0	1	normal mode	4
	<= 3 input functions	4	2	extended LUT mode	0
			3	arithmetic mode	0
1			4	shared arithmetic mode	0
	normal mode	4	10		
	extended LUT mode	0	11	Estimated ALUT/register pairs used	4
	arithmetic mode	0	12		
	shared arithmetic mode	0	13	➤ Total registers	0
0			1	Dedicated logic registers	0
1	Estimated ALUT/register pairs used	4	2	I/O registers	0
2			3	LUT_REGs	0
3	▼ Total registers	0	14		
	Dedicated logic registers	0	15		
	I/O registers	0	16	I/O pins	6
	LUT_REGs	0	17		
4			18	DSP block 18-bit elements	0
5			19		
6	I/O pins	6	20	Maximum fan-out node	sel[0]~inpu
7			21	Maximum fan-out	4
8	DSP block 18-bit elements	0	22	Total fan-out	18
9			23	Average fan-out	1.13



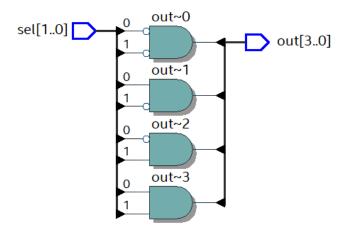


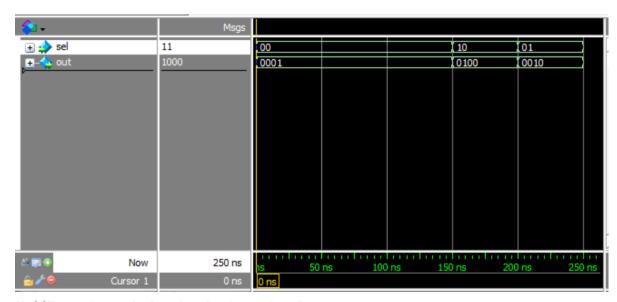
```
ModelSim> vsim work.decoder_2to4_testbench
# vsim work.decoder_2to4_testbench
# Start time: 20:20:52 on Jul 16,2021
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -position insertpoint sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
# time=0, sel=00 out=0001
# time=150, sel=10 out=0100
# time=200, sel=01 out=0100
# time=250, sel=11 out=1000
#
```

VSIM 7>

Dataflow

			Ana	llysis & Synthesis Resource Usage Summary	
Analvs	is & Synthesis Resource Usage Summary		Q -	< <filter>></filter>	
< <f< th=""><th></th><th></th><th></th><th>Resource</th><th>Usage</th></f<>				Resource	Usage
	Resource	Usage	2	Dedicated logic registers	0
1 ~	Estimated ALUTs Used	4	3		
1	Combinational ALUTs	4	4	➤ Estimated ALUTs Unavailable	0
2	Memory ALUTs	0	1	Due to unpartnered combinational logic	0
3	LUT REGs	0	2	Due to Memory ALUTs	0
	Dedicated logic registers	0	5	·	
3	5 5		6	Total combinational functions	4
4 ~	Estimated ALUTs Unavailable	0	7	➤ Combinational ALUT usage by number of inputs	
	Due to unpartnered combinational logic	0	1	7 input functions	0
2	Due to Memory ALUTs	0	2	6 input functions	0
j i			3	5 input functions	0
6	Total combinational functions	4	4	4 input functions	0
· ·	Combinational ALUT usage by number of inputs		5	<=3 input functions	4
	7 input functions	0	8	4-5 input functions	7
	6 input functions	0	9	✓ Combinational ALUTs by mode	
	5 input functions	0	1	normal mode	4
	4 input functions	0	2	extended LUT mode	0
i	<=3 input functions	4	3	extended LOT mode arithmetic mode	0
3					-
· ·	Combinational ALUTs by mode		4	shared arithmetic mode	0
	normal mode	4	10		
	extended LUT mode	0	11	Estimated ALUT/register pairs used	4
	arithmetic mode	0	12		
	shared arithmetic mode	0	13	▼ Total registers	0
0			1	Dedicated logic registers	0
	Estimated ALUT/register pairs used	4	2	I/O registers	0
2			3	LUT_REGs	0
	Total registers	0	14		
	Dedicated logic registers	0	15		
	I/O registers	0	16	I/O pins	6
	LUT_REGs	0	17		
4			18	DSP block 18-bit elements	0
5	1/0 :		19		
	I/O pins	6	20	Maximum fan-out node	sel[0]~inpu
7	DCD blook 10 bit alamanta	0	21	Maximum fan-out	4
	DSP block 18-bit elements	0	22	Total fan-out	18
19	Maximum fan aut nada	colfOleipput	23	Average fan-out	1.13



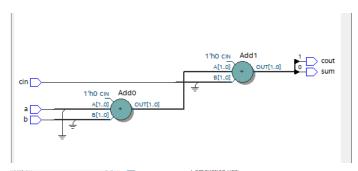


ModelSim> vsim work.decoder_2to4_testbench

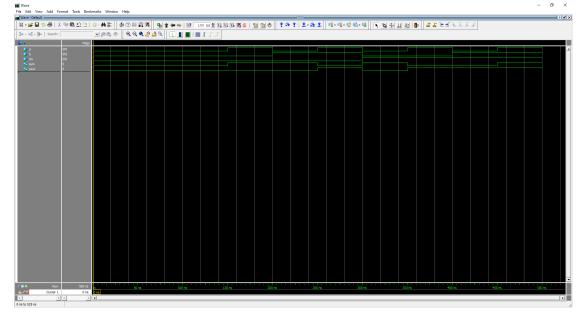
```
# vsim work.decoder_2to4_testbench
# Start time: 12:03:54 on Jul 17,2021
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -position insertpoint sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
# time=0, sel=00 out=0001
#
# time=150, sel=10 out=0100
#
# time=200, sel=01 out=0100
#
# time=250, sel=11 out=1000
```

• Full Adder

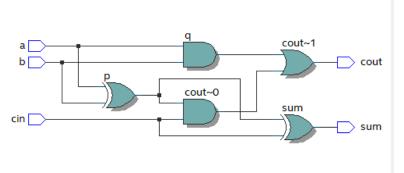
Behavioral

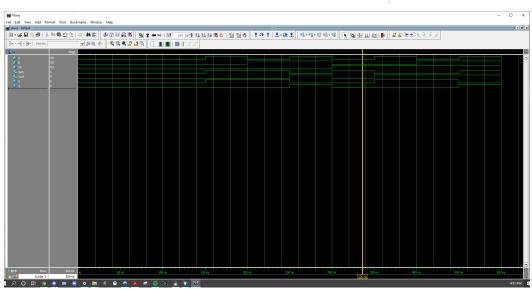


ral.s	v 🖾 🔻	Compilation Kep
Ana	lysis & Synthesis Resource Usage Summary	
•	< <filter>></filter>	
	Resource	Usage
1	▼ Estimated ALUTs Used	2
1	Combinational ALUTs	2
2	Memory ALUTs	0
3	LUT_REGs	0
2	Dedicated logic registers	0
3		
4	▼ Estimated ALUTs Unavailable	0
1	Due to unpartnered combinational logic	0
2	Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	 Combinational ALUT usage by number of inputs 	
1	7 input functions	0
2	6 input functions	0
3	5 input functions	0
4	4 input functions	0
5	<=3 input functions	2
8		
9	▼ Combinational ALUTs by mode	
1	normal mode	2
2	extended LUT mode	0
3	arithmetic mode	0
4	shared arithmetic mode	0



۹.	<hitter>></hitter>	
	Resource	Usage
1	➤ Estimated ALUTs Used	2
1	Combinational ALUTs	2
2	Memory ALUTs	0
3	LUT_REGs	0
2	Dedicated logic registers	0
3		
4	▼ Estimated ALUTs Unavailable	0
1	Due to unpartnered combinational logic	0
2	Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7		
1	7 input functions	0
2	6 input functions	0
3	5 input functions	0
4	4 input functions	0
5	<=3 input functions	2
8		
9		
1	normal mode	2
2	extended LUT mode	0
3	arithmetic mode	0
4	shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	2
12		
13	▼ Total registers	0
1	Dedicated logic registers	0
2	I/O registers	0
3	LUT REGs	0





Gate-Level Model

	Resource	Usage
1	✓ Estimated ALUTs Used	2
1	Combinational ALUTs	2
2	Memory ALUTs	0
3	LUT_REGs	0
2	Dedicated logic registers	0
3		
4	 Estimated ALUTs Unavailable 	0
1	Due to unpartnered combinational logic	0
2	Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	 Combinational ALUT usage by number of inputs 	
1	7 input functions	0
2	6 input functions	0
3	5 input functions	0
4	4 input functions	0
5	<=3 input functions	2
8		
9	▼ Combinational ALUTs by mode	
1	normal mode	2
2	extended LUT mode	0
3	arithmetic mode	0
4	shared arithmetic mode	0

