ECE 111 Lab 1
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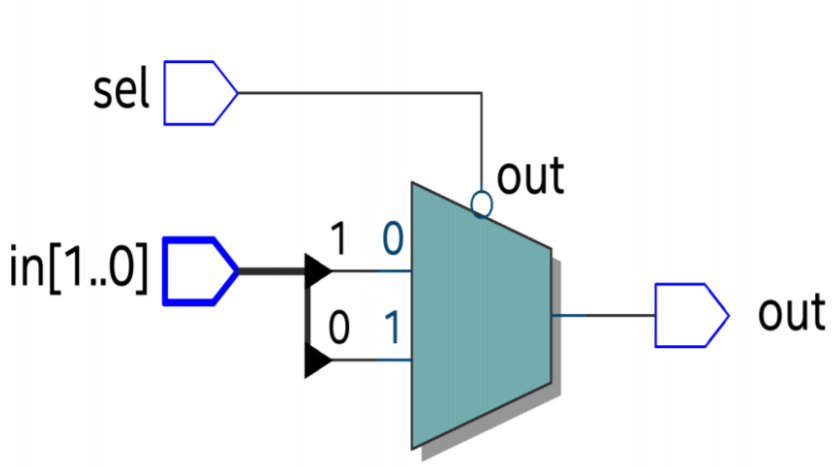
A15078025

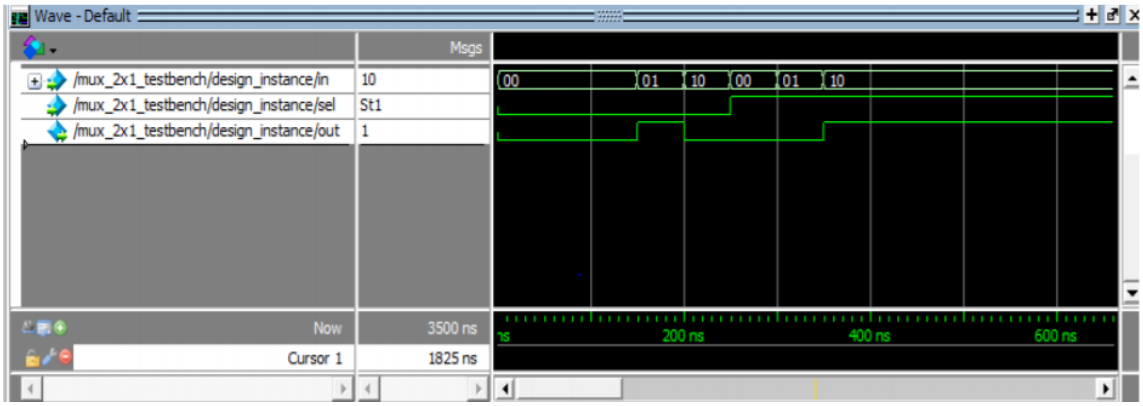
- **Mux 2to1**
  - Behavioral



Analysis & Synthesis Resource Usage Summary

<<Filter>>

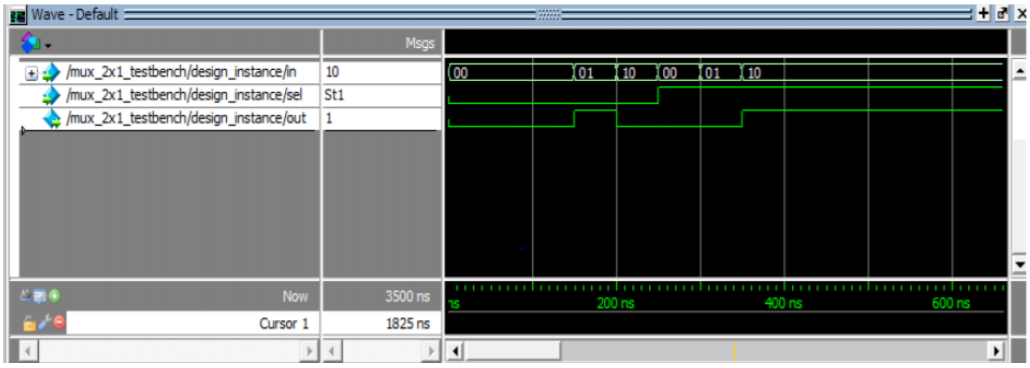
	Resource	Usage
1	Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	Combinational ALUT ...by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	Total registers	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	out~0
21	Maximum fan-out	1
22	Total fan-out	8
23	Average fan-out	0.80



Transcript

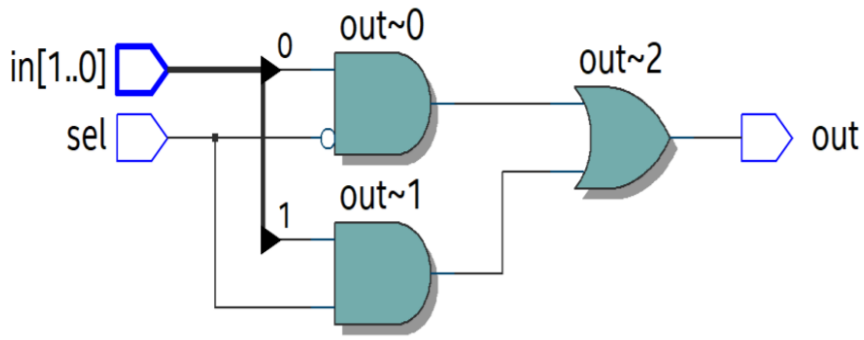
```
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim> vsim work.mux_2x1_testbench
# vsim work.mux_2x1_testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv_std.std
# Loading work.mux_2x1_testbench
# Loading work.mux_2x1
add wave -position insertpoint sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run
#  time=0,  in=00  sel=0  out=0
#
#  time=150,  in=01  sel=0  out=1
#
#  time=200,  in=10  sel=0  out=0
#
#  time=250,  in=00  sel=1  out=0
#
#  time=300,  in=01  sel=1  out=0
#
#  time=350,  in=10  sel=1  out=1
```

- Dataflow



Transcript

```
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim> vsim work.mux_2x1_testbench
# vsim work.mux_2x1_testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv_std.std
# Loading work.mux_2x1_testbench
# Loading work.mux_2x1
add wave -position insertpoint sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run
#  time=0,  in=00  sel=0  out=0
#
#  time=150,  in=01  sel=0  out=1
#
#  time=200,  in=10  sel=0  out=0
#
#  time=250,  in=00  sel=1  out=0
#
#  time=300,  in=01  sel=1  out=0
#
#  time=350,  in=10  sel=1  out=1
```

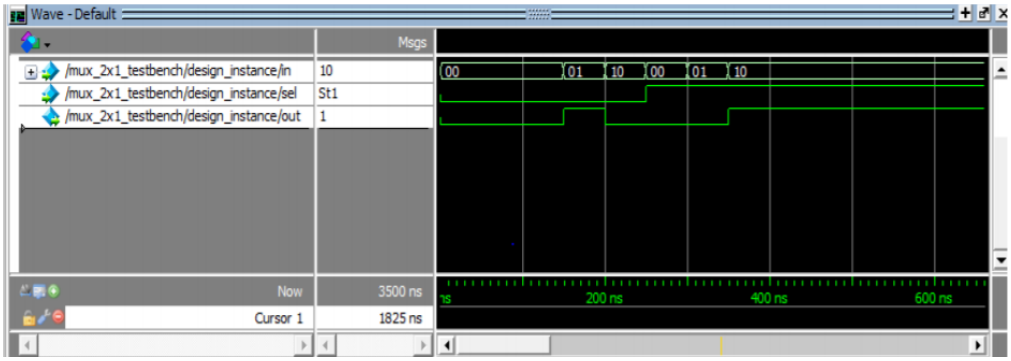


Analysis & Synthesis Resource Usage Summary

<<Filter>>

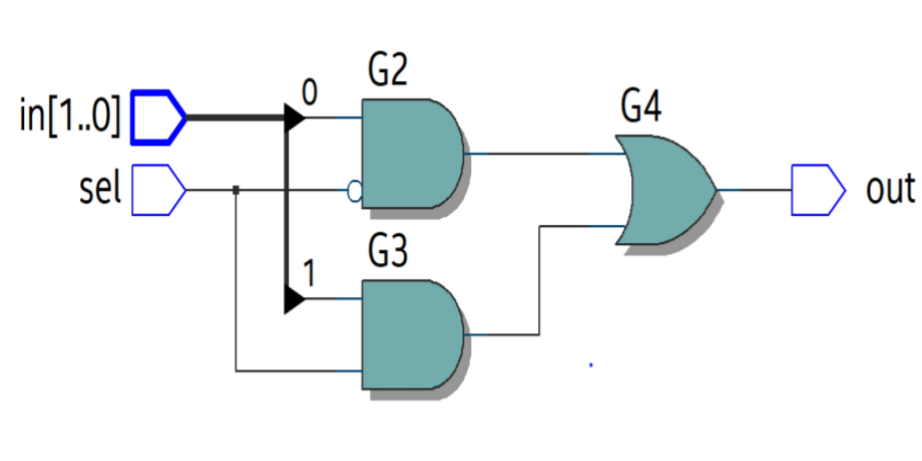
	Resource	Usage
1	Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	Combinational ALUT ...by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	out~0

- Gate-Level Model



Transcript

```
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim> vsim work.mux_2x1_testbench
# vsim work.mux_2x1_testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv_std.std
# Loading work.mux_2x1_testbench
# Loading work.mux_2x1
add wave -position insertpoint sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run
#  time=0,  in=00  sel=0  out=0
#
#  time=150,  in=01  sel=0  out=1
#
#  time=200,  in=10  sel=0  out=0
#
#  time=250,  in=00  sel=1  out=0
#
#  time=300,  in=01  sel=1  out=0
#
#  time=350,  in=10  sel=1  out=1
```



Analysis & Synthesis Resource Usage Summary

<<Filter>>

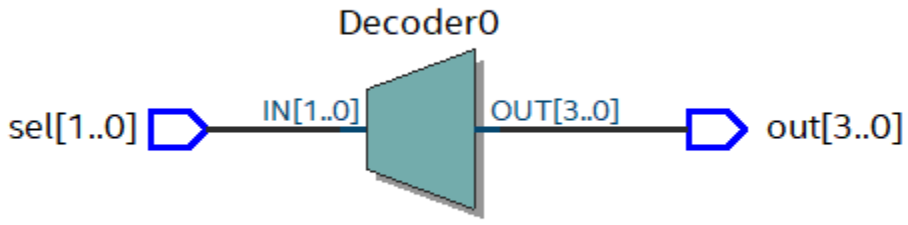
	Resource	Usage
1	Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	Combinational ALUT ...by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	Total registers	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	G4~0
21	Maximum fan-out	1
22	Total fan-out	8

- **2to4 Decoder**
  - Behavioral
    - Usage Summary: **observe**

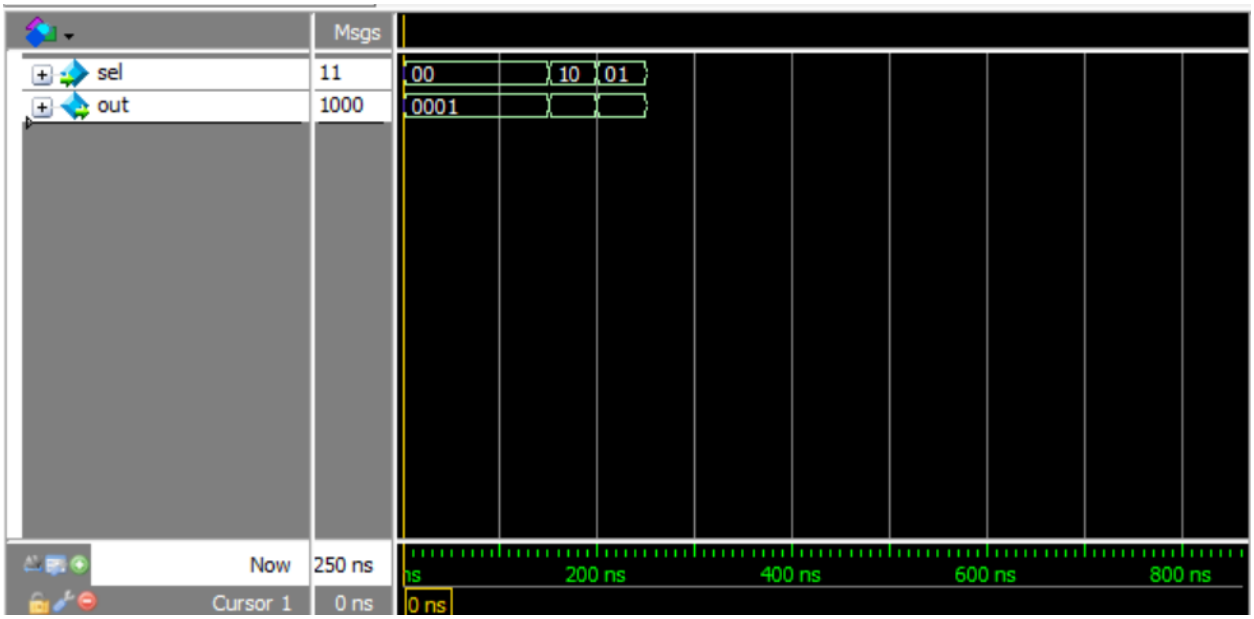
Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimated ALUTs Used	4
1	-- Combinational ALUTs	4
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	sel[0]~input
21	Maximum fan-out	4
22	Total fan-out	18
23	Average fan-out	1.13



Modelsim:




```
ModelSim> vsim work.decoder_2to4_testbench
# vsim work.decoder_2to4_testbench
# Start time: 11:50:12 on Jul 17,2021
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -position insertpoint sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
#  time=0,  sel=00   out=0001
#
#  time=150,  sel=10   out=0100
#
#  time=200,  sel=01   out=0010
#
#  time=250,  sel=11   out=1000
#
```

- Gate-Level Model

Analysis & Synthesis Resource Usage Summary

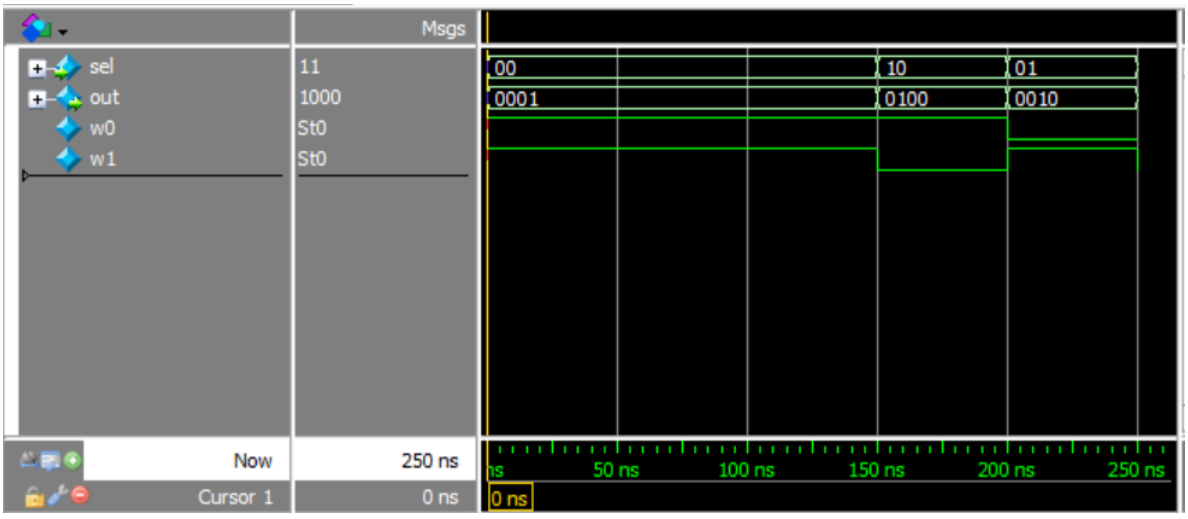
<<Filter>>

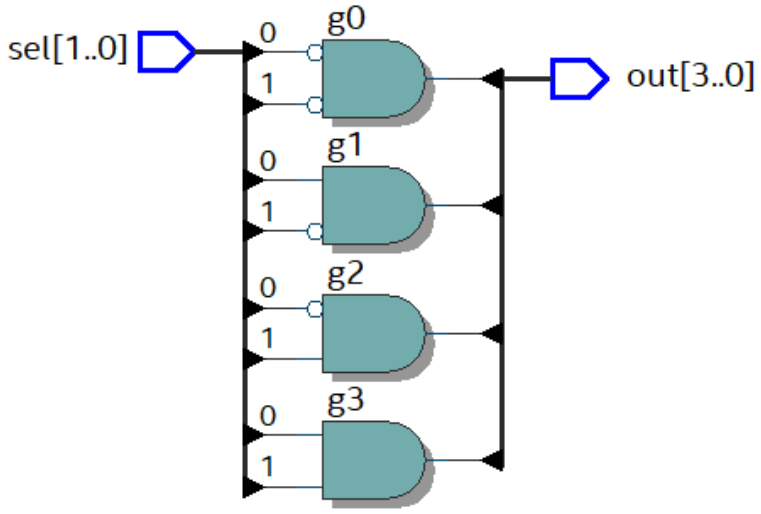
	Resource	Usage
1	Estimated ALUTs Used	4
1	-- Combinational ALUTs	4
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	sel[0]~input
21	Maximum fan-out	4
22	Total fan-out	18
23	Average fan-out	1.13






```
ModelSim> vsim work.decoder_2to4_testbench
# vsim work.decoder_2to4_testbench
# Start time: 20:20:52 on Jul 16,2021
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -position insertpoint sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
#  time=0,   sel=00   out=0001
#
#  time=150,  sel=10   out=0100
#
#  time=200,  sel=01   out=0010
#
#  time=250,  sel=11   out=1000
#

VSIM 7>
```

- Dataflow

Analysis & Synthesis Resource Usage Summary

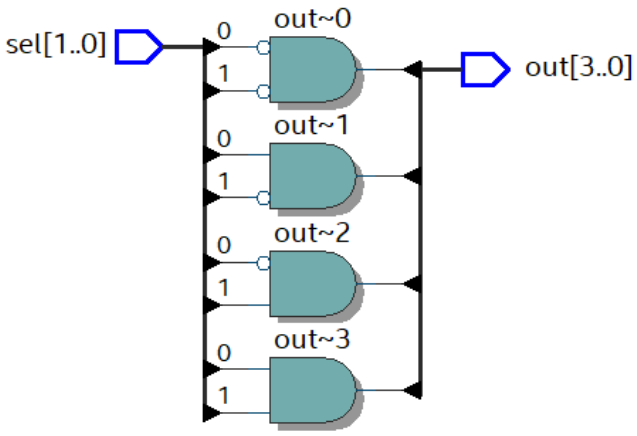
<<Filter>>

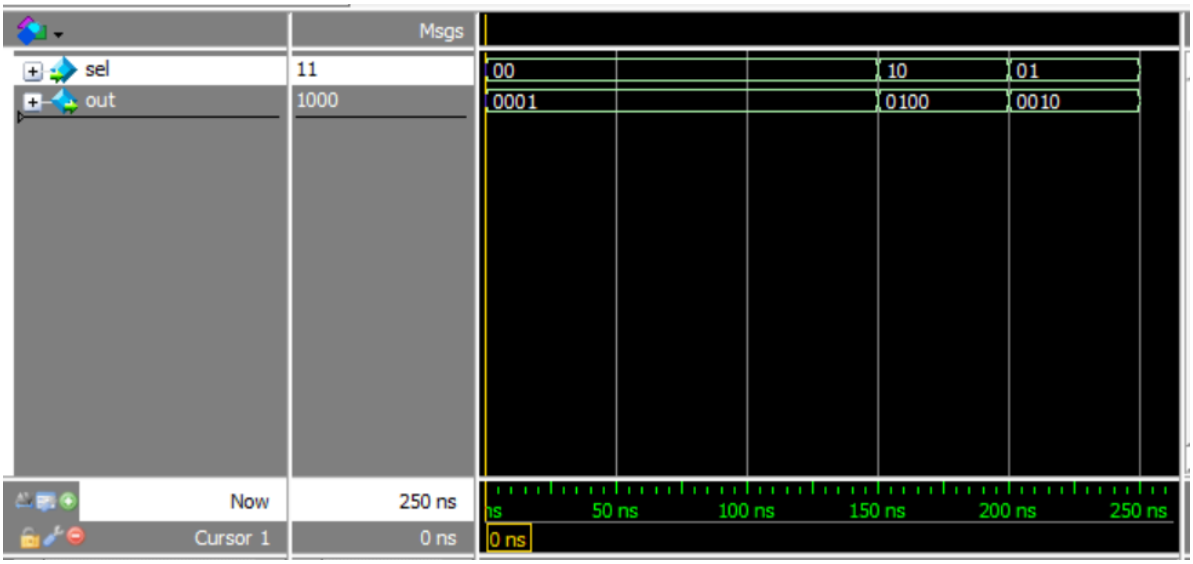
	Resource	Usage
1	Estimated ALUTs Used	4
1	-- Combinational ALUTs	4
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	sel[0]~input
21	Maximum fan-out	4
22	Total fan-out	18
23	Average fan-out	1.13

Analysis & Synthesis Resource Usage Summary

<<Filter>>

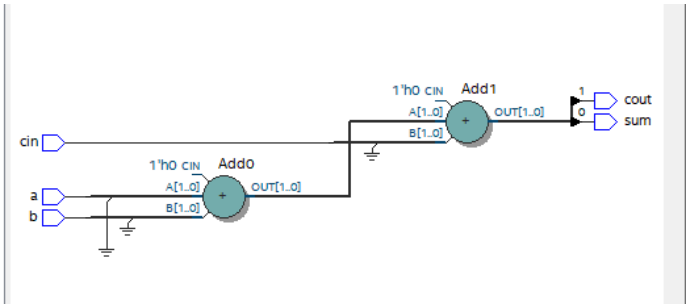
	Resource	Usage
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	sel[0]~input
21	Maximum fan-out	4
22	Total fan-out	18
23	Average fan-out	1.13






```
ModelSim> vsim work.decoder_2to4_testbench
# vsim work.decoder_2to4_testbench
# Start time: 12:03:54 on Jul 17,2021
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -position insertpoint sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
#  time=0,   sel=00   out=0001
#
#  time=150,   sel=10   out=0100
#
#  time=200,   sel=01   out=0010
#
#  time=250,   sel=11   out=1000
#
```

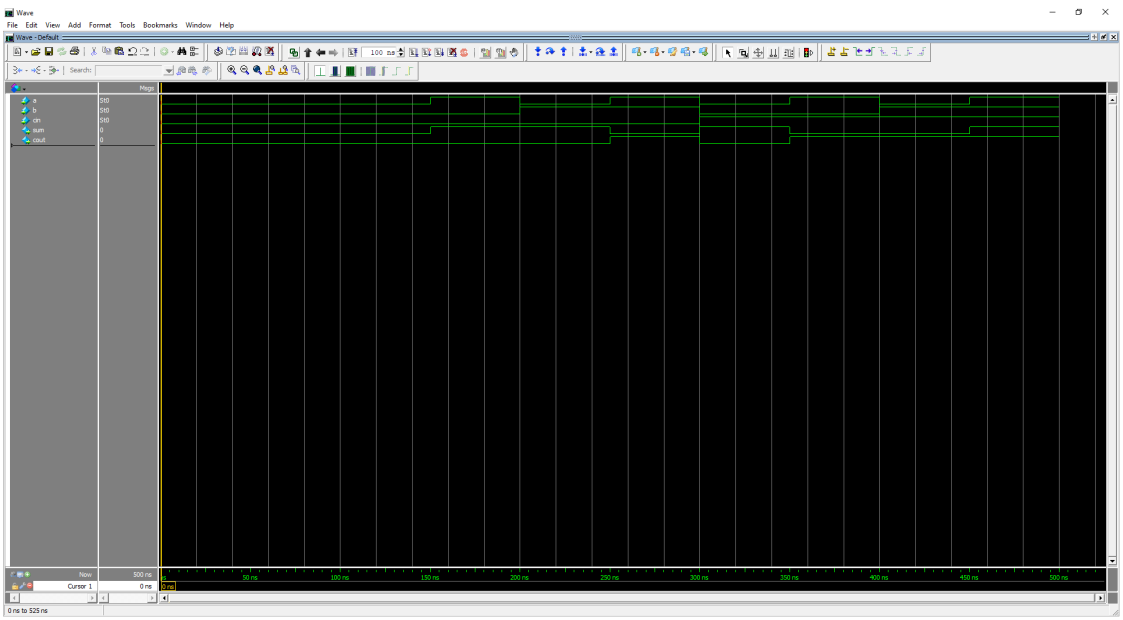
- **Full Adder**
  - Behavioral



Analysis & Synthesis Resource Usage Summary

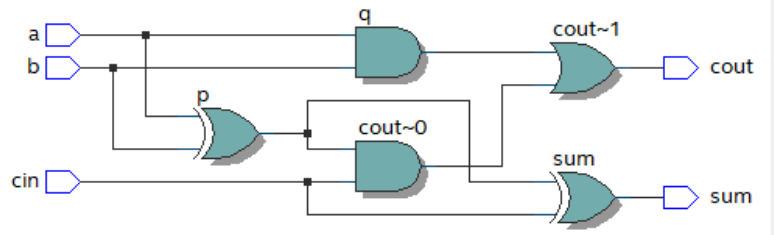
<<Filter>>

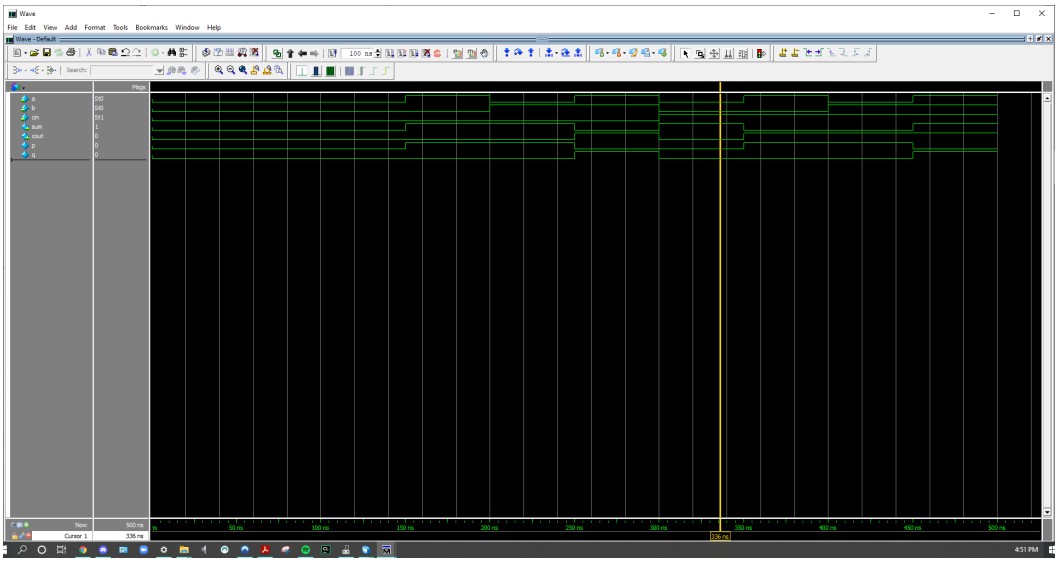
	Resource	Usage
1	Estimated ALUTs Used	2
1	-- Combinational ALUTs	2
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
8		
9	Combinational ALUTs by mode	
1	-- normal mode	2
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0



- Dataflow

	Resource	Usage
1	Estimated ALUTs Used	2
1	-- Combinational ALUTs	2
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
8		
9	Combinational ALUTs by mode	
1	-- normal mode	2
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	2
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0





- Gate-Level Model

<<Filter>>

	Resource	Usage
1	Estimated ALUTs Used	2
1	-- Combinational ALUTs	2
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
8		
9	Combinational ALUTs by mode	
1	-- normal mode	2
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0