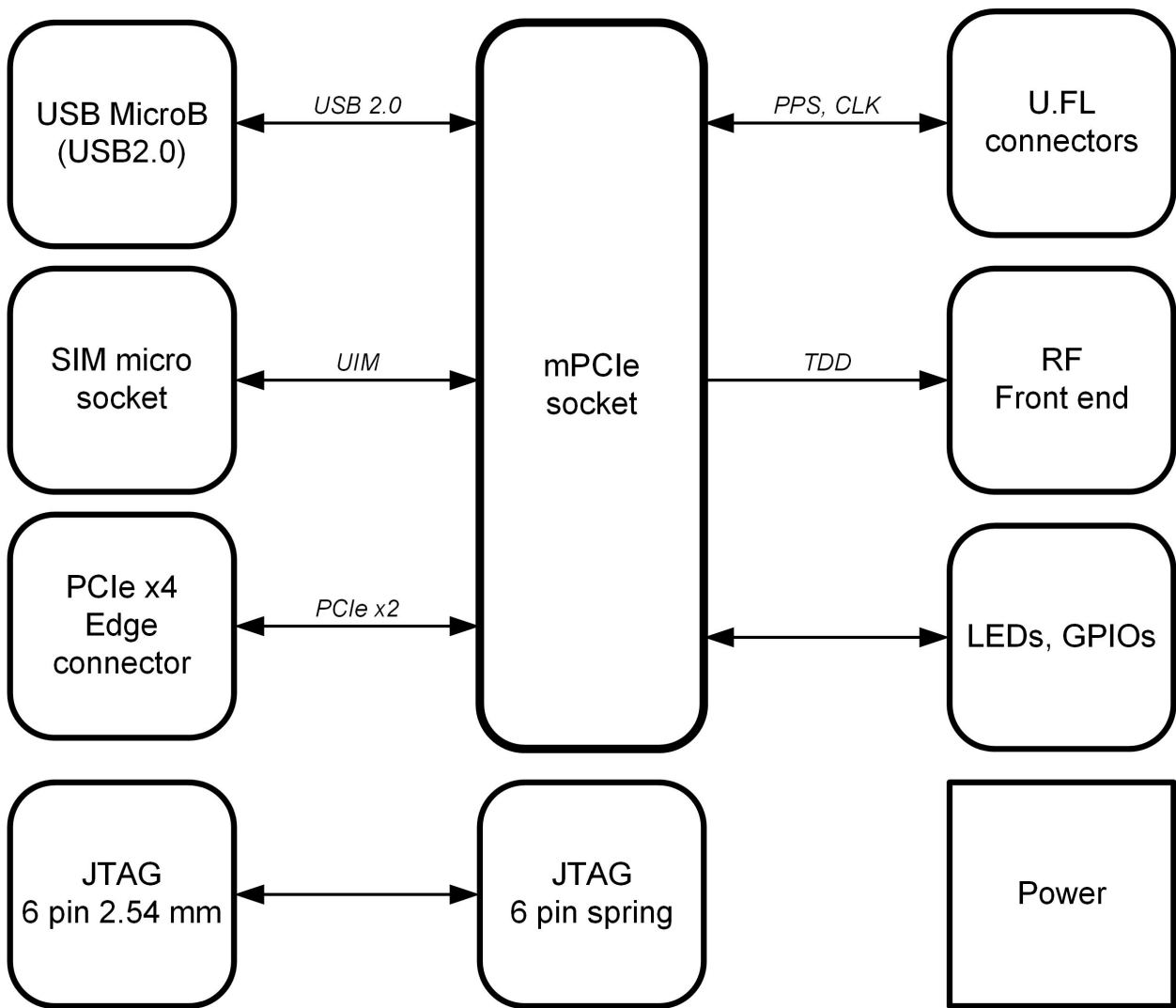


Block diagram



Project name: **LimeFEA-mPCIe\_1v0.PRJPCB**

Title: **Block diagram**

Size: **A4**

Revision: **v1.0**

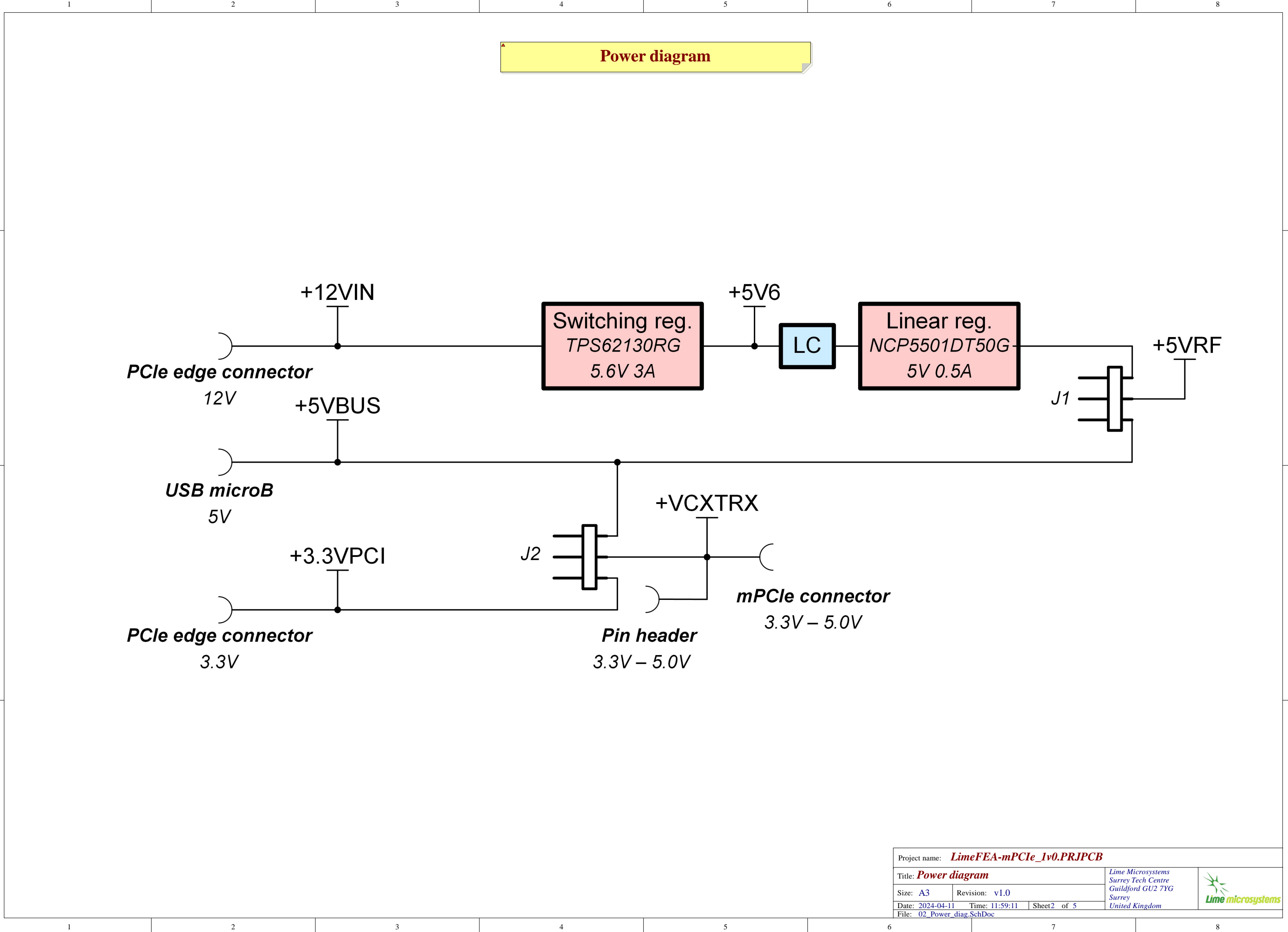
Date: **2024-04-11** Time: **11:59:11**

Sheet **1** of **5**

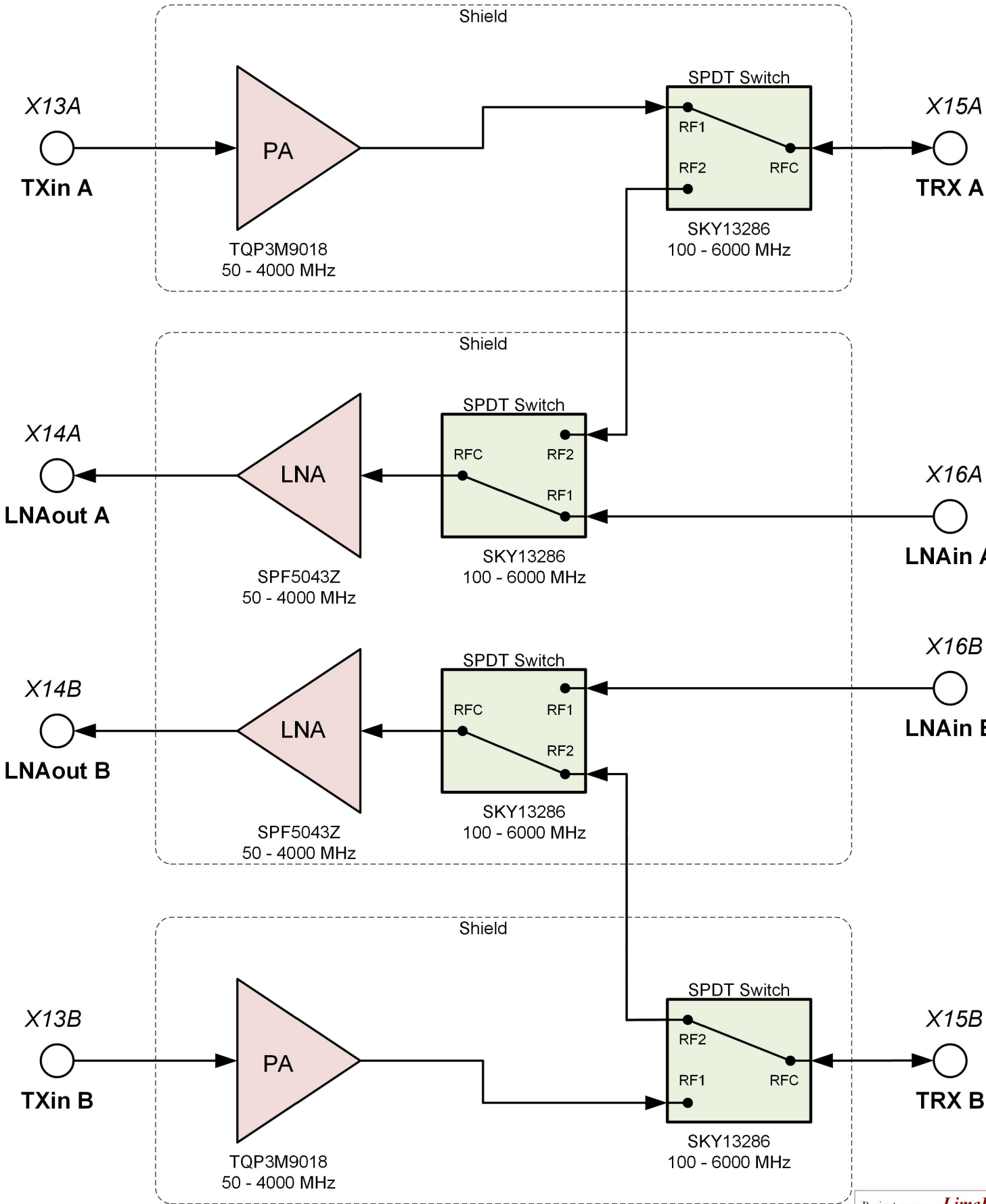
File: **01\_Block\_diag.SchDoc**

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RF front end diagram



\* All RF switches are controlled by the same signal RF\_SW\_TDD

Project name: **LimeFEA-mPCIe\_1v0.PRJPCB**

Title: **RF front end diagram**

Size: **A3**

Revision: **v1.0**

Date: **2024-04-11**

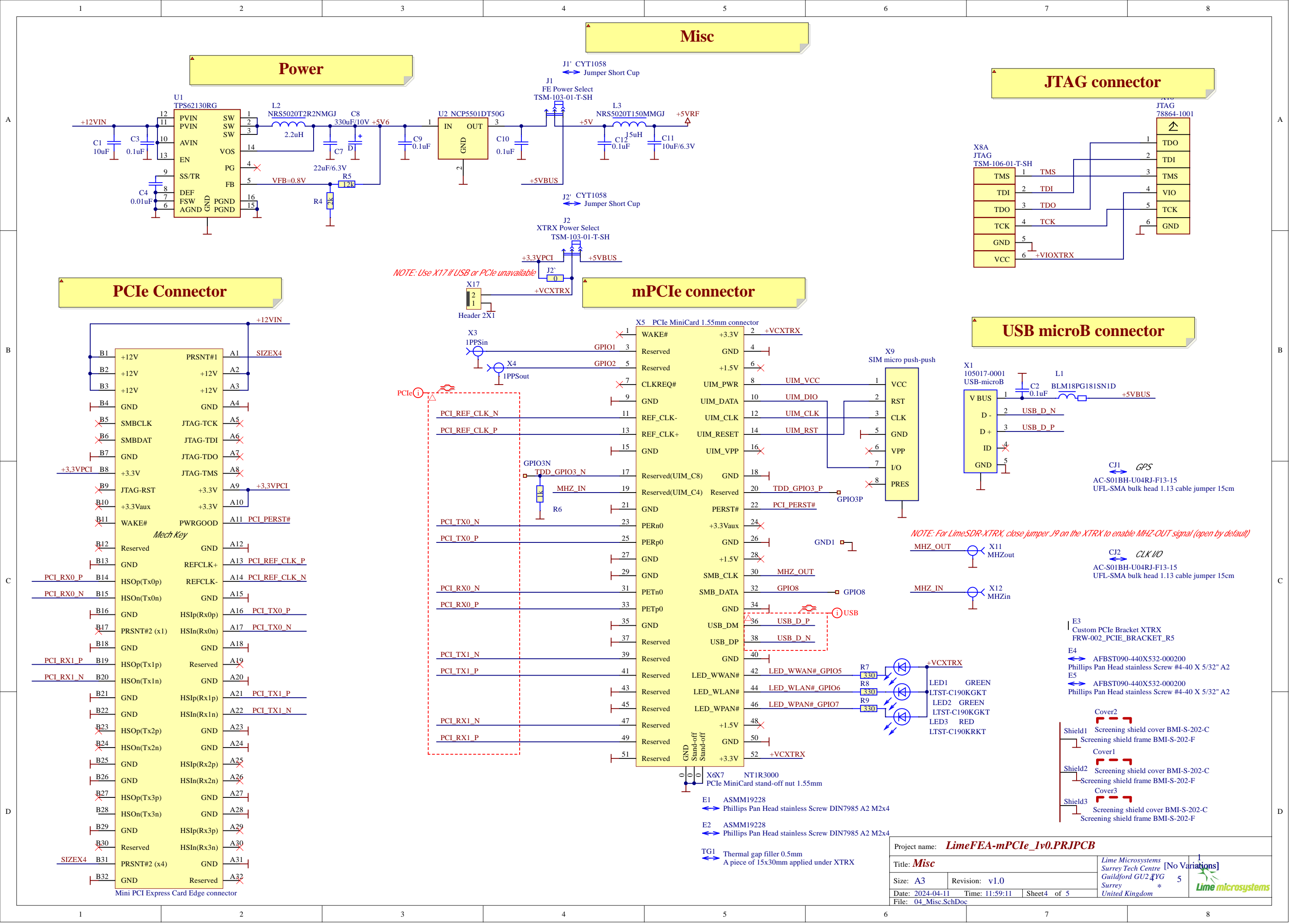
Time: **11:59:11**

Sheet3 of 5

File: **03\_RFFE\_diag.SchDoc**

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**RF front end**

**Channel A**



TDD\_GPIO3\_N

**Channel B**



TDD\_GPIO3\_N

C