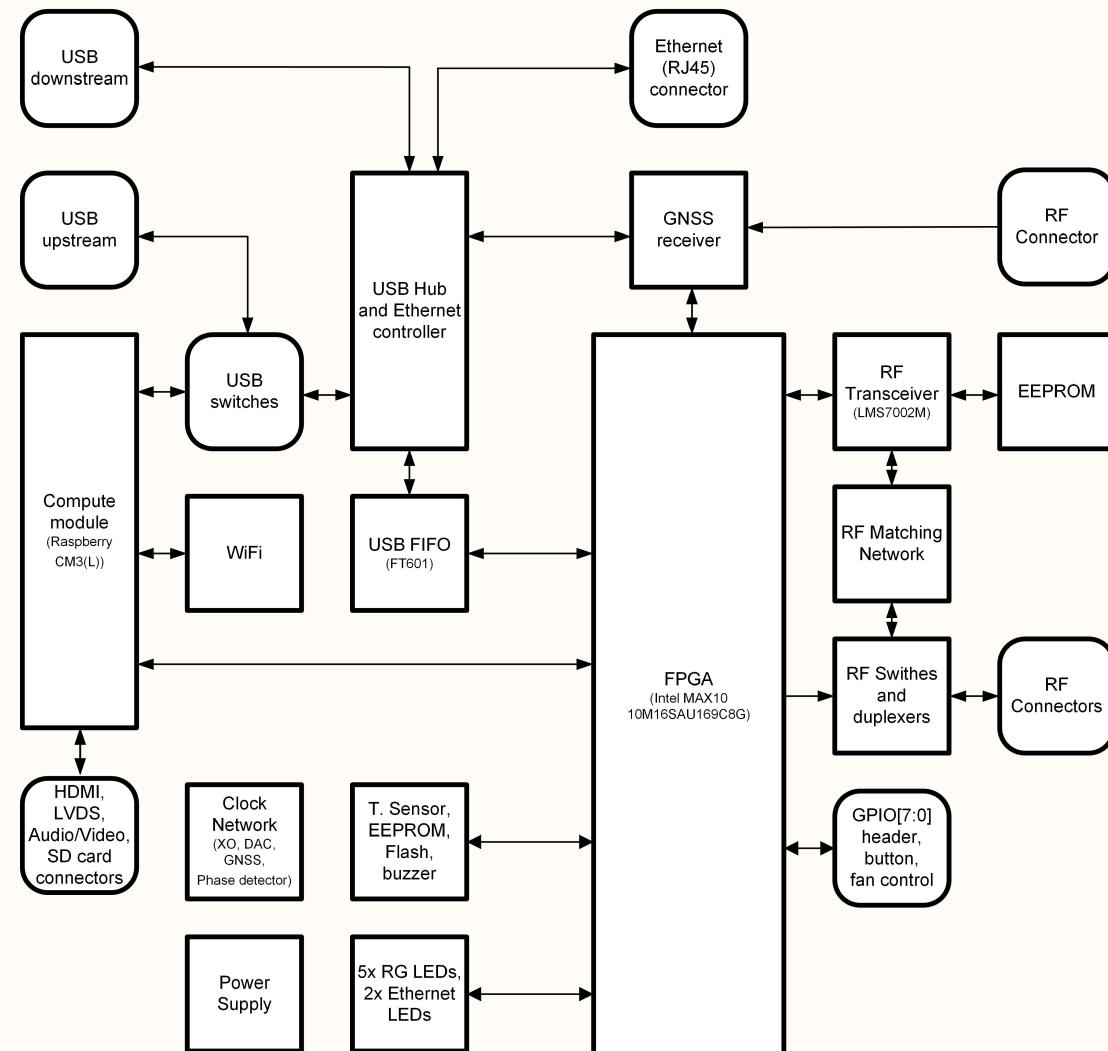


Block diagram



Project name: **LimeNet-Micro_2v1-SDR.PrbPcb**

Title: **Block diagram**

Size: **A4** Revision: **v2.1**

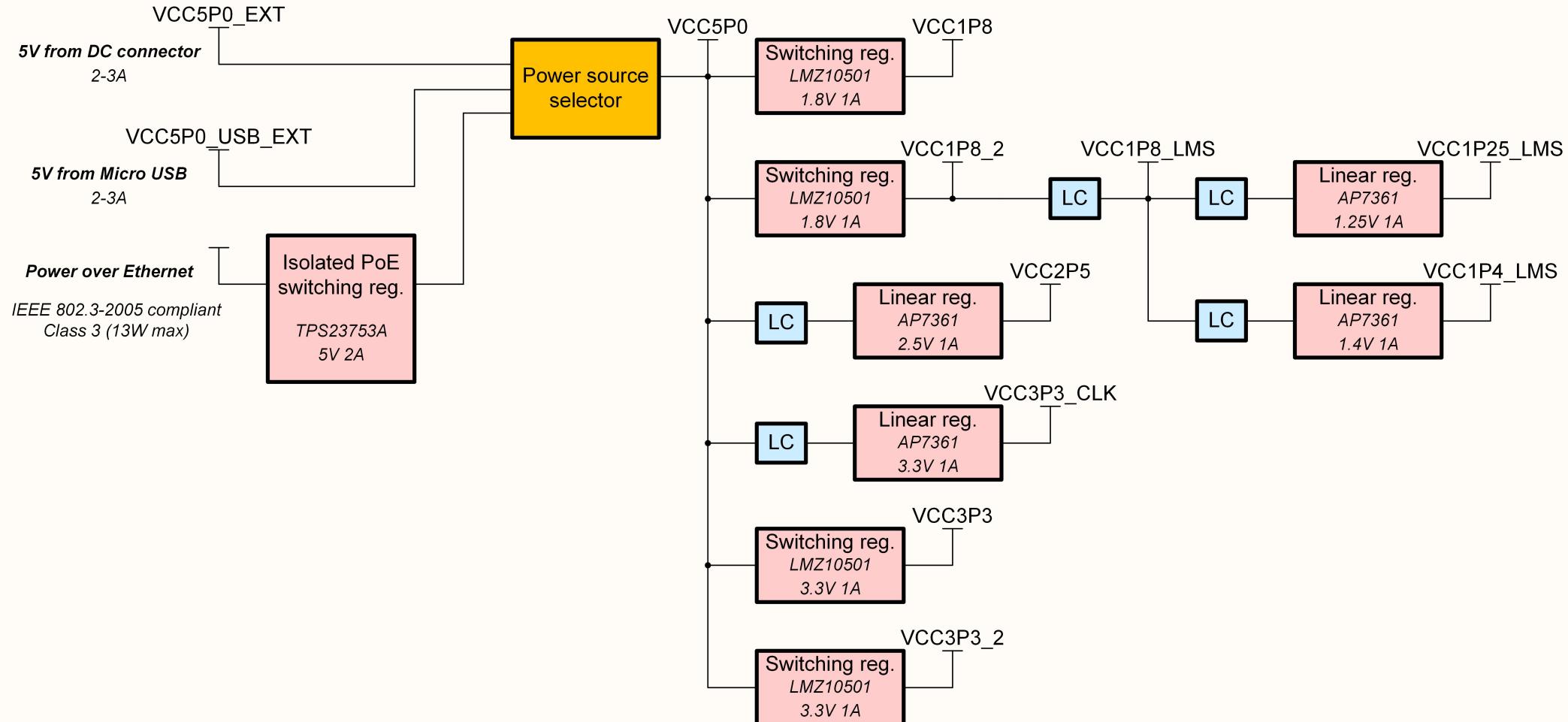
Date: **2019-03-14** Time: **11:43:05** Sheet**1** of **15**

File: **01_BlockDiagram.SchDoc**

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Guildford GU2 7YG
Surrey
United Kingdom



Power diagram



Project name: **LimeNet-Micro_2v1-SDR.PrjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v2.1**

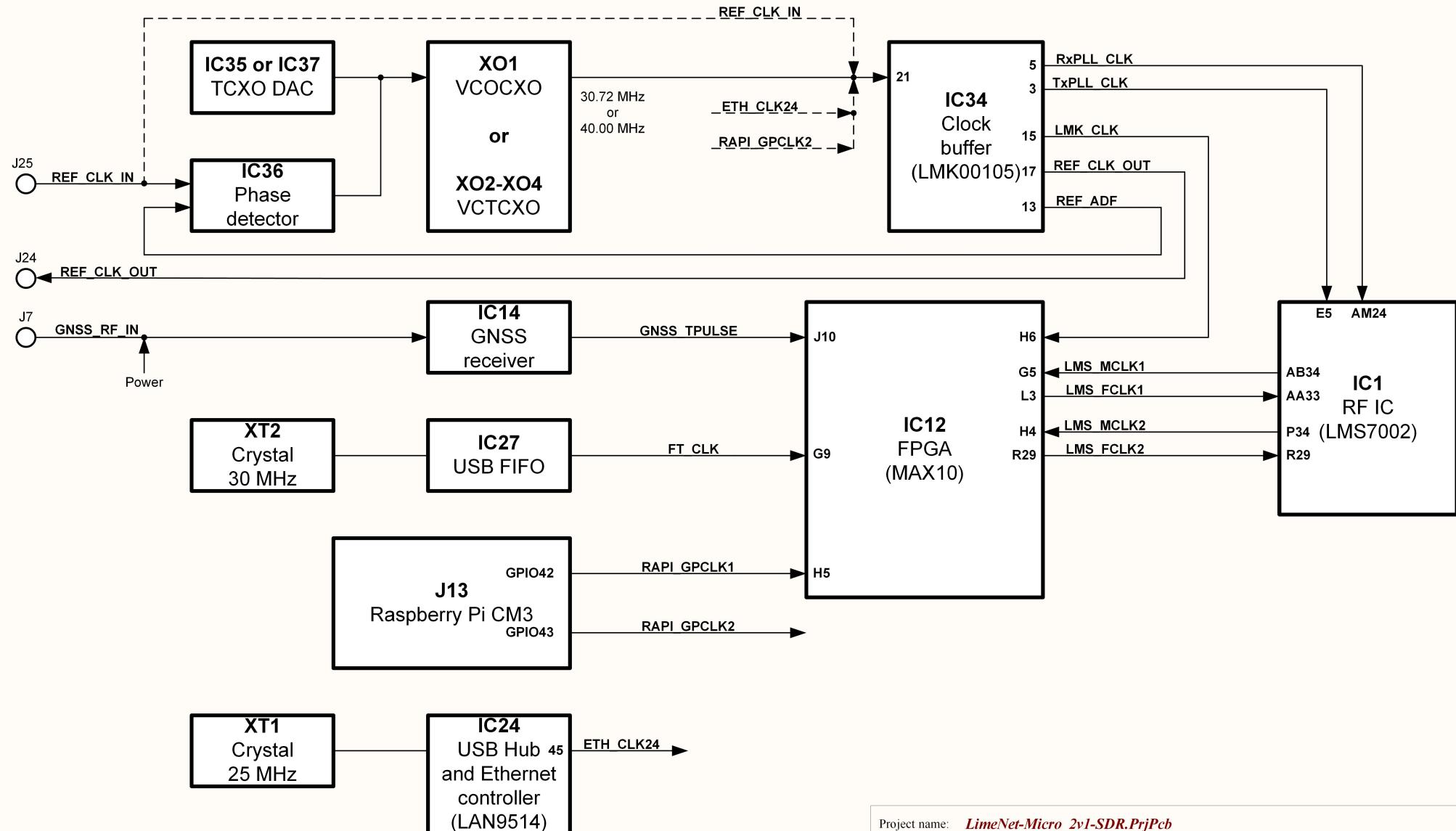
Date: **2019-03-14** Time: **11:43:12** Sheet**2** of **15**

File: **02_PowerDiagram.SchDoc**

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United Kingdom



Clock diagram



Project name: *LimeNet-Micro_2v1-SDR.PrbPcb*

Title: *Clock diagram*

Size: **A4** Revision: **v2.1**

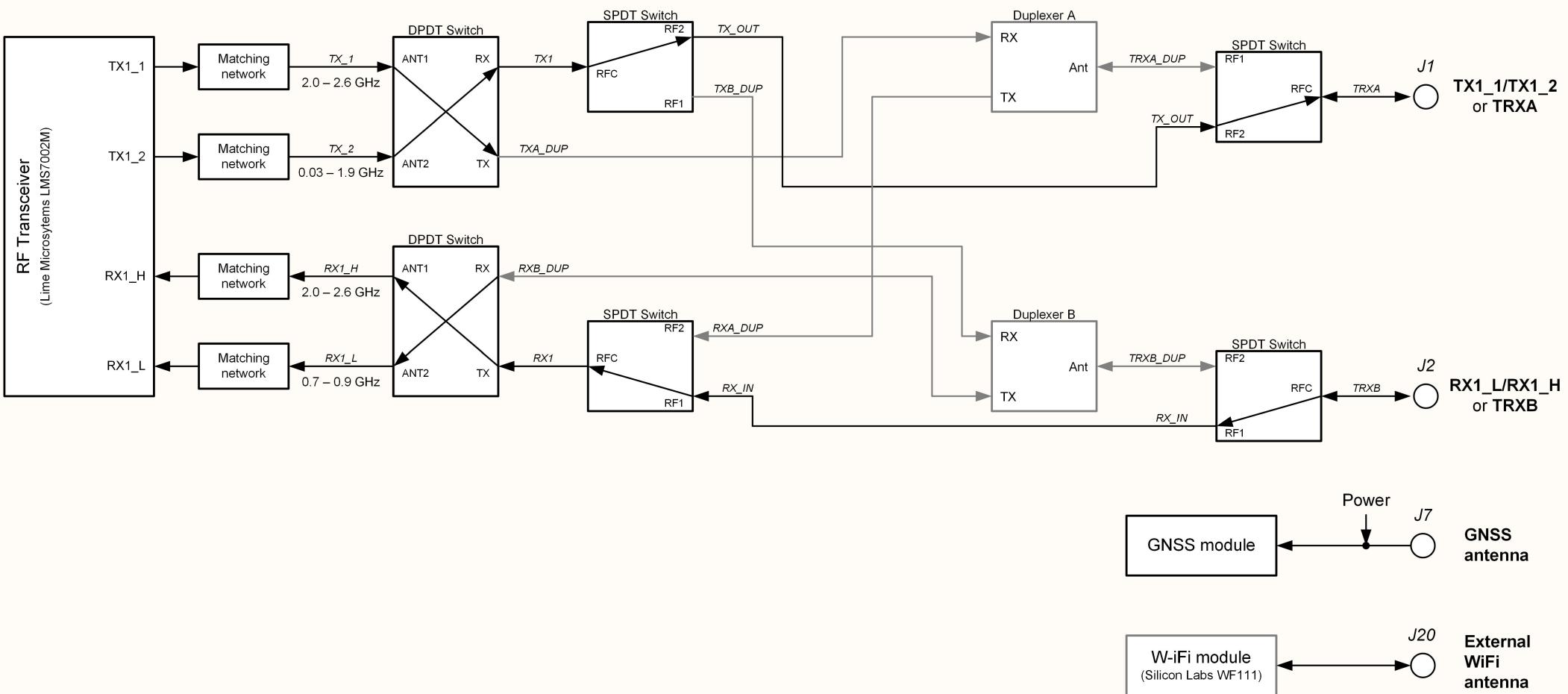
Date: **2019-03-14** Time: **11:43:21** Sheet**3** of **15**

File: **03_ClockDiagram.SchDoc**

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Guildford GU2 7YG
Surrey
United Kingdom



RF diagram



Project name: **LimeNet-Micro_2v1-SDR.PrbPcb**

Title: **RF diagram**

Size: **A4** Revision: **v2.1**

Date: **2019-03-14** Time: **11:43:31** Sheet **4** of **15**

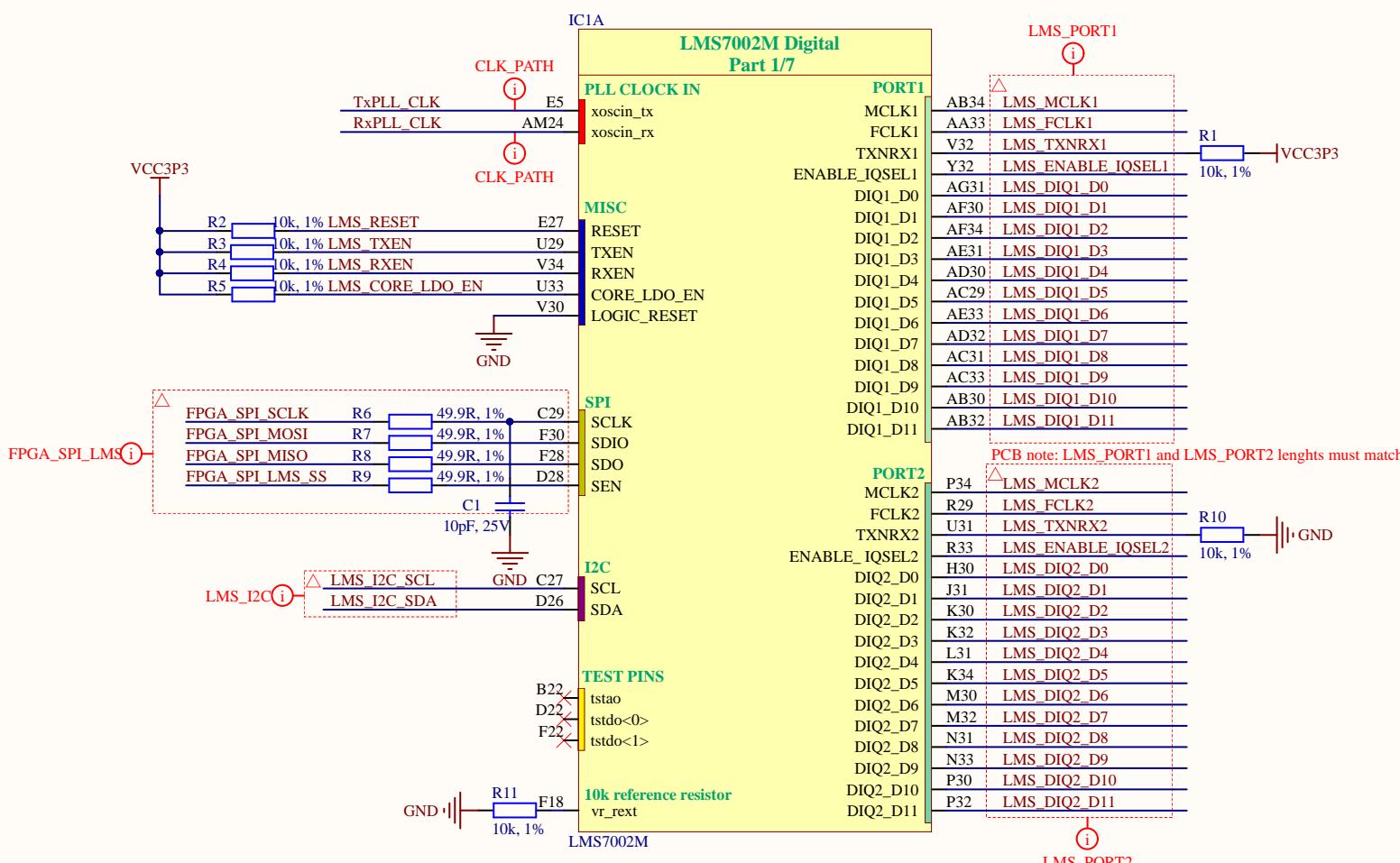
File: **04_RFDiagram.SchDoc**

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United Kingdom

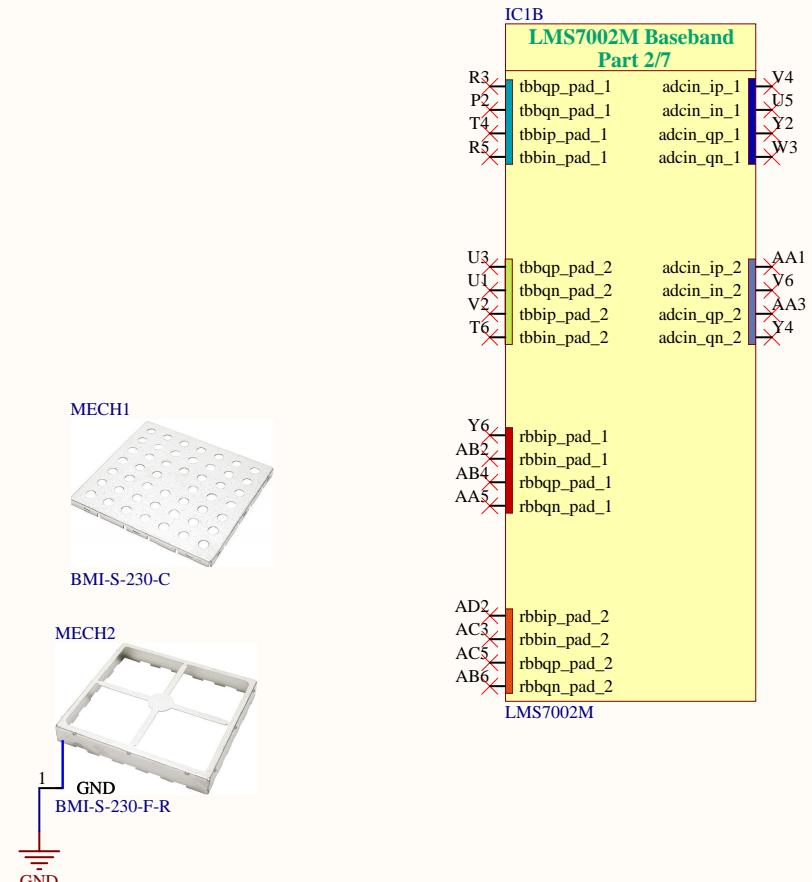


NF elements on sheet: IC2
Number of NF elements on sheet: 1

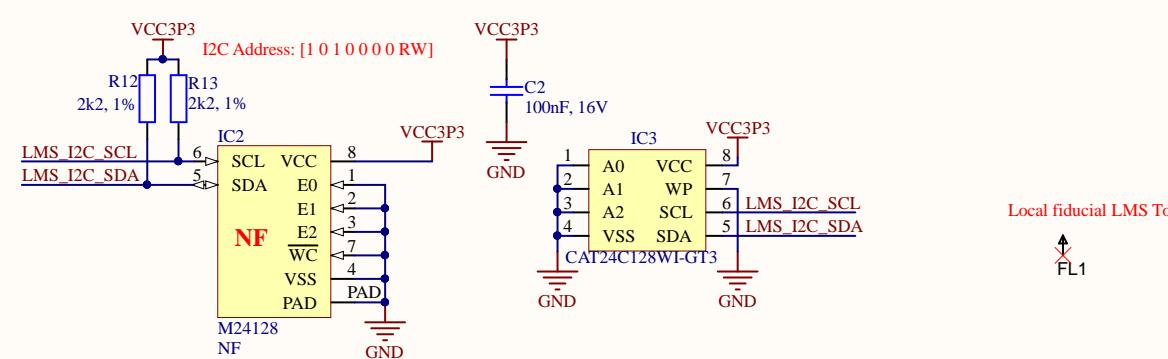
LMS7002M misc



Baseband external IO



LMS EEPROM



Project name: LimeNet-Micro_2v1-SDR.PrdPcb

Title: LMS7002M misc

Size: A3 Revision: v2.1

Date: 2019-03-14 Time: 11:43:39 Sheet 5 of 15

File: 05_LMS7002M_Misc.SchDoc

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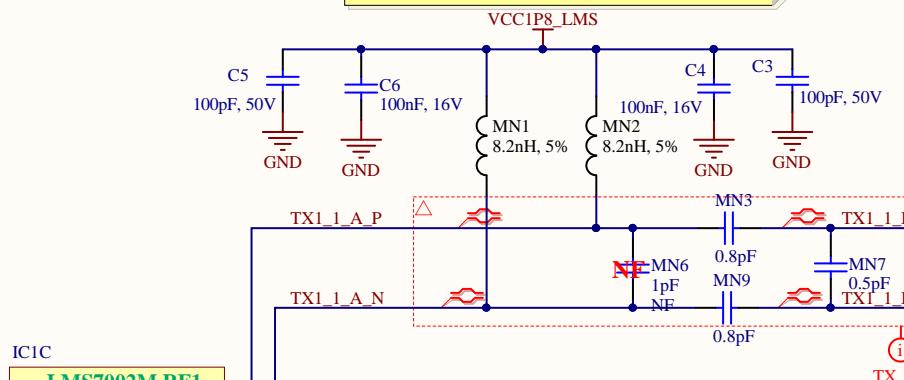


NF elements on sheet: ESD1, ESD2, MN6, MN18, MN22, MN26, C7, C19, C24, C32, MN5, MN8, IC5, C8, MN4, MN16, MN17, IC7, C18, MN12

Number of NF elements on sheet: 20

RF

LMS RF Channel 1



LMS7002M RF1 Part 3/7

TX1_2

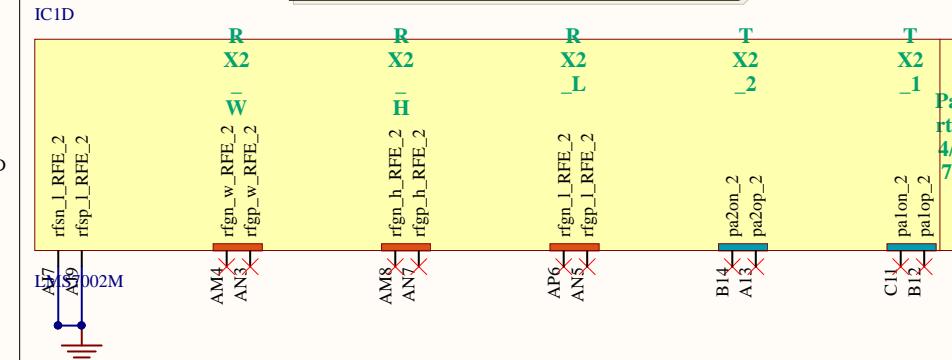
RX1_L

RX1_H

RX1_W

LMS7002M

LMS RF Channel 2



R_X2

W_X2

H_X2

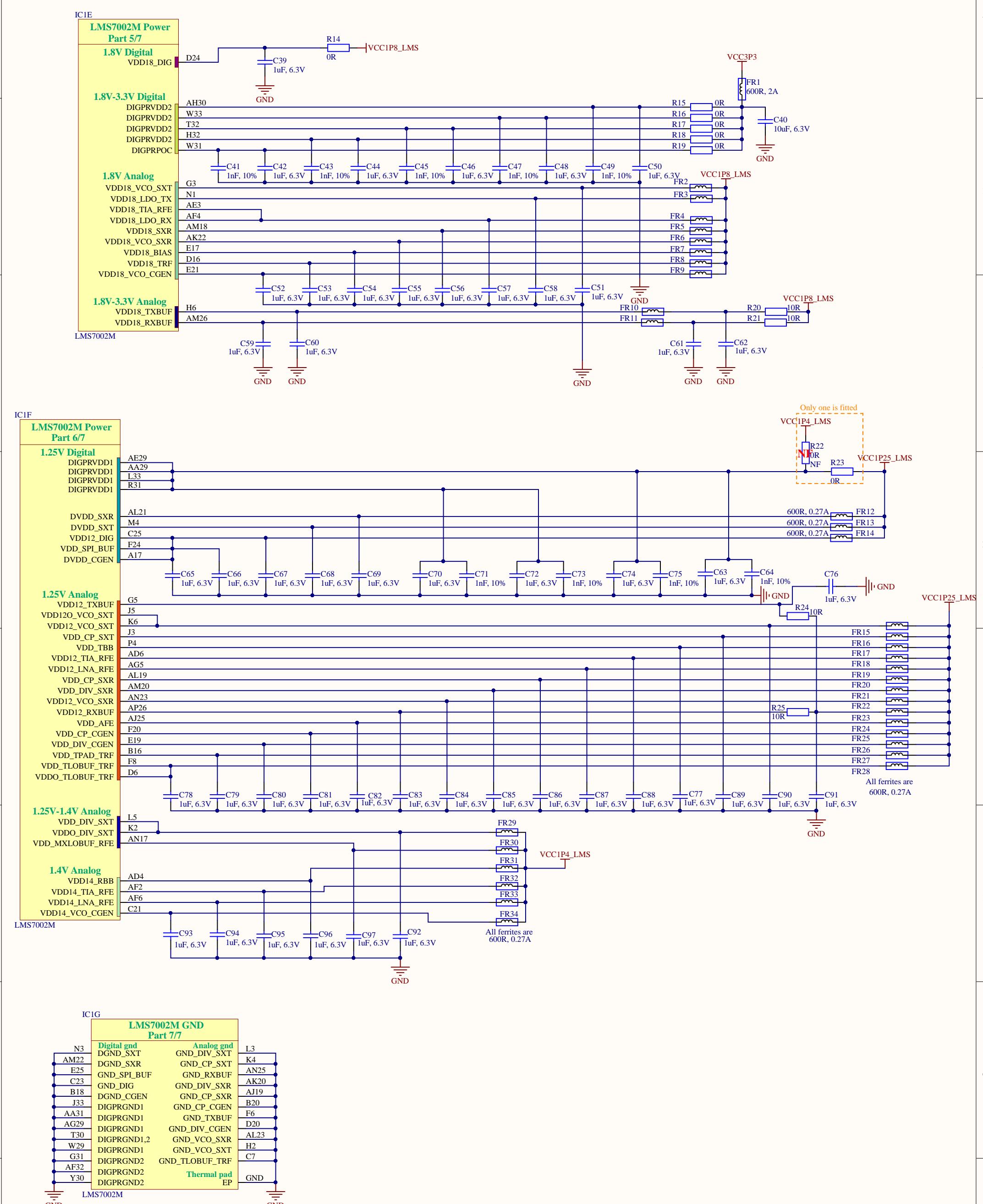
L_X2

T_X2

R_X2

NF elements on sheet: R22
Number of NF elements on sheet: 1

LMS7002M power supply circuit

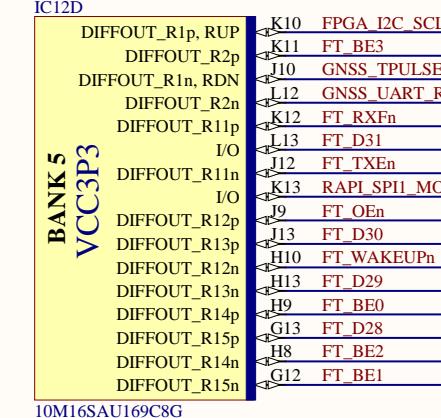
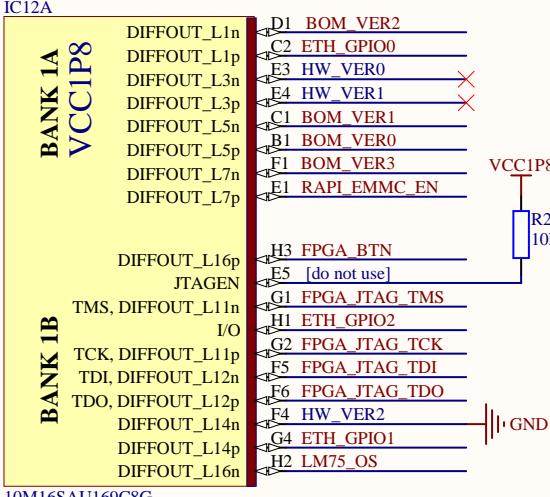


NF elements on sheet: J3, R27, R33, R34

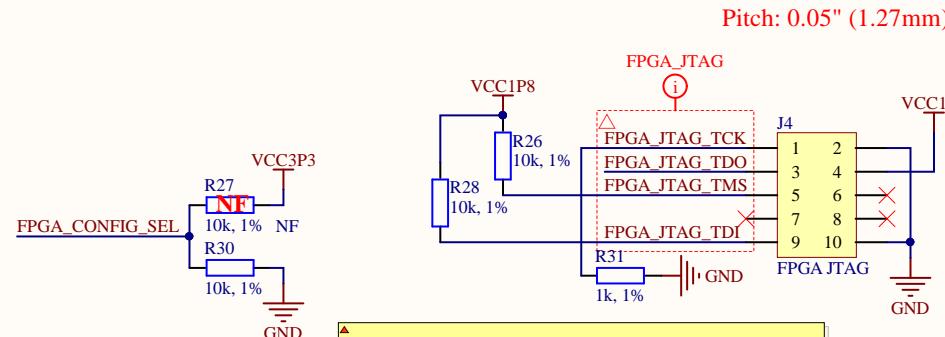
Number of NF elements on sheet: 4

FPGA

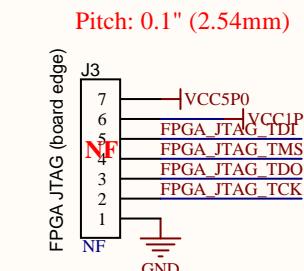
FPGA Banks



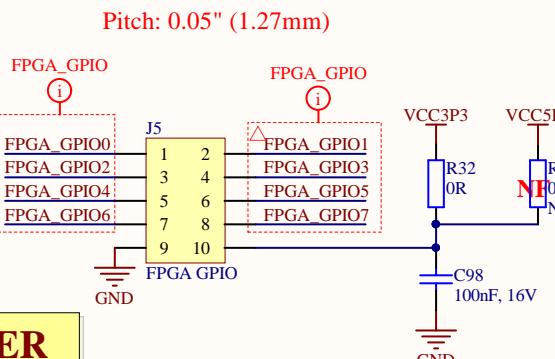
FPGA JTAG



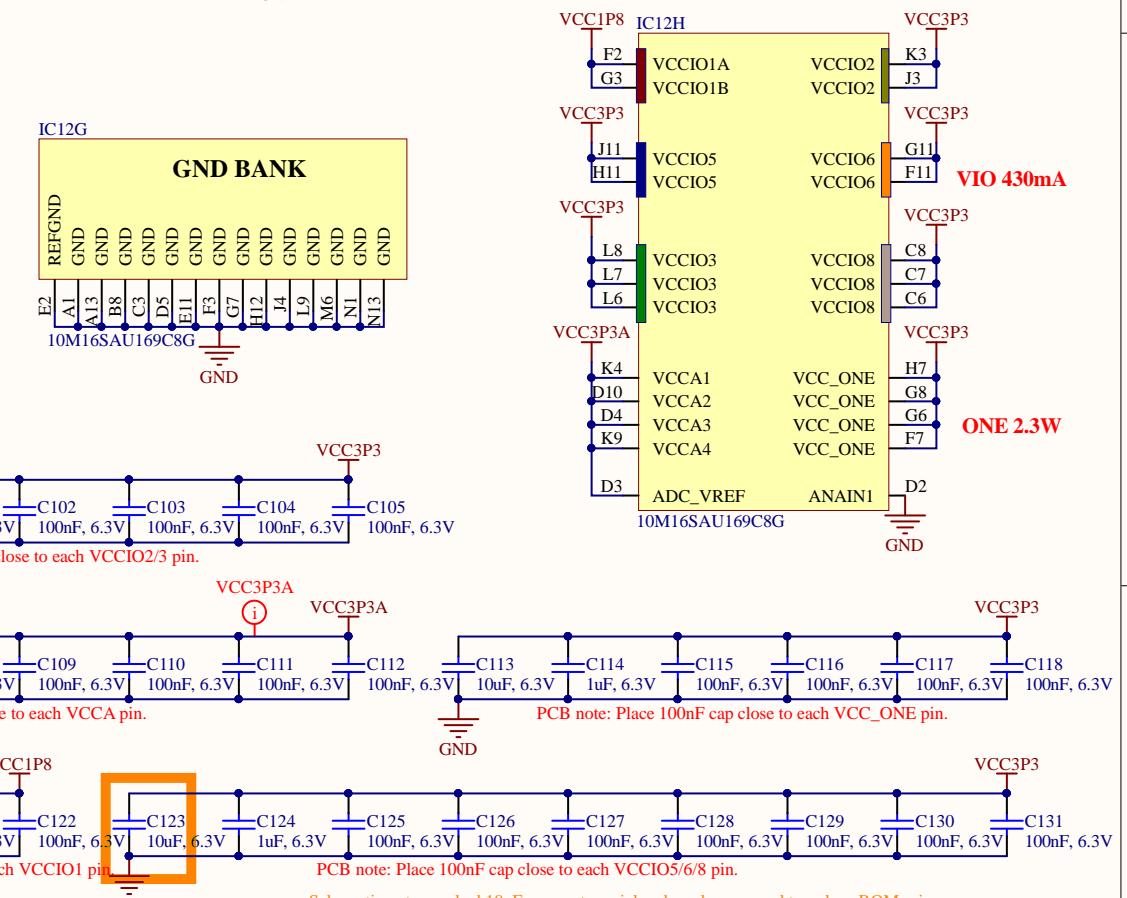
FPGA JTAG (edge)



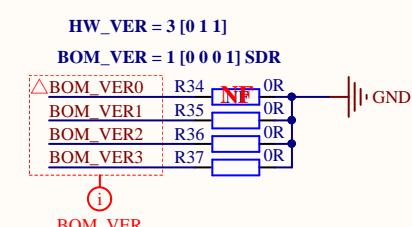
FPGA GPIO



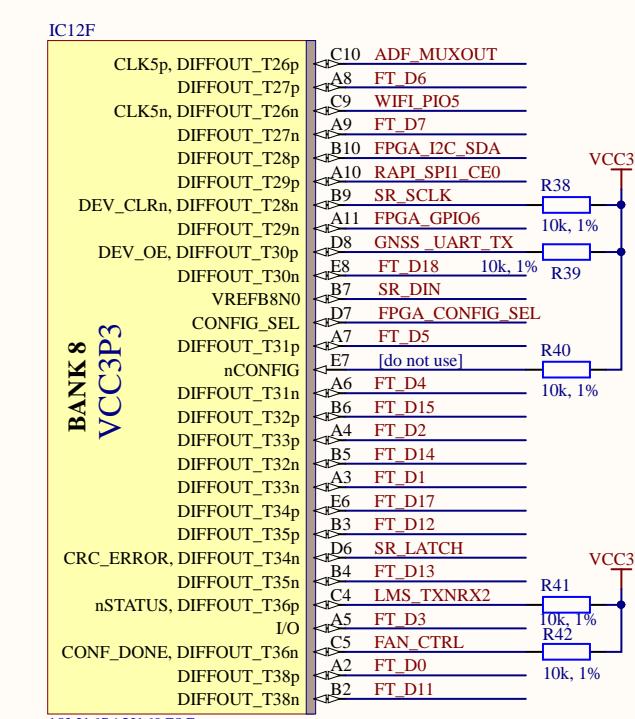
FPGA Power



HW VER & BOM VER



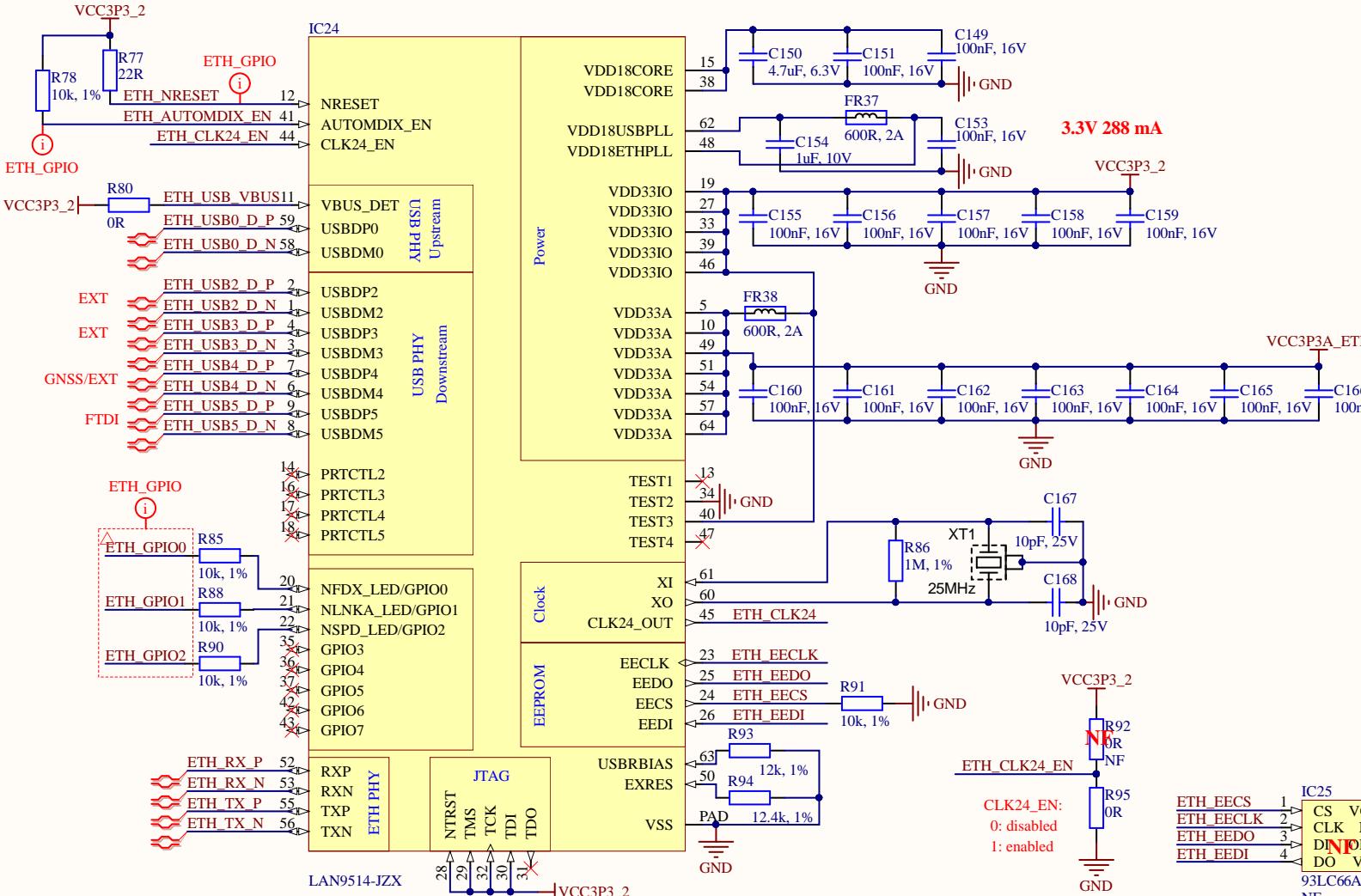
BANK 3	VCC3P3	DIFFOUT_B1n	L5 LMS_DIQ2_D1
		DIFFOUT_B2n	M4 LMS_DIQ2_D4
		DIFFOUT_B1p	L4 LMS_DIQ2_D10
		DIFFOUT_B2p	M5 FPGA_SPI_SCLK
		DIFFOUT_B3n	K5 FPGA_SPI_MOSI
		DIFFOUT_B4n	N4 LMS_DIQ2_D8
		DIFFOUT_B3p	J5 FPGA_SPI_LMS_SS
		DIFFOUT_B4p	N5 FPGA_SPI_MISO
		DIFFOUT_B5n	N6 LMS_TXNRX1
		DIFFOUT_B6n	N7 LMS_ENABLE_IQSEL1
		DIFFOUT_B5p	M7 FPGA_GPIO1
		DIFFOUT_B6p	N8 FPGA_GPIO2
		DIFFOUT_B13n	J6 FPGA_GPIO3
		DIFFOUT_B14n	M8 LMS_DIQ1_D8
		DIFFOUT_B13p	K6 LMS_DIQ1_D10
		DIFFOUT_B14p	M9 LMS_DIQ1_D9
		DIFFOUT_B15n	J7 FPGA_GPIO5
		I/O	N11 LMS_DIQ1_D2
		DIFFOUT_B15	K7 LMS_DIQ1_D11



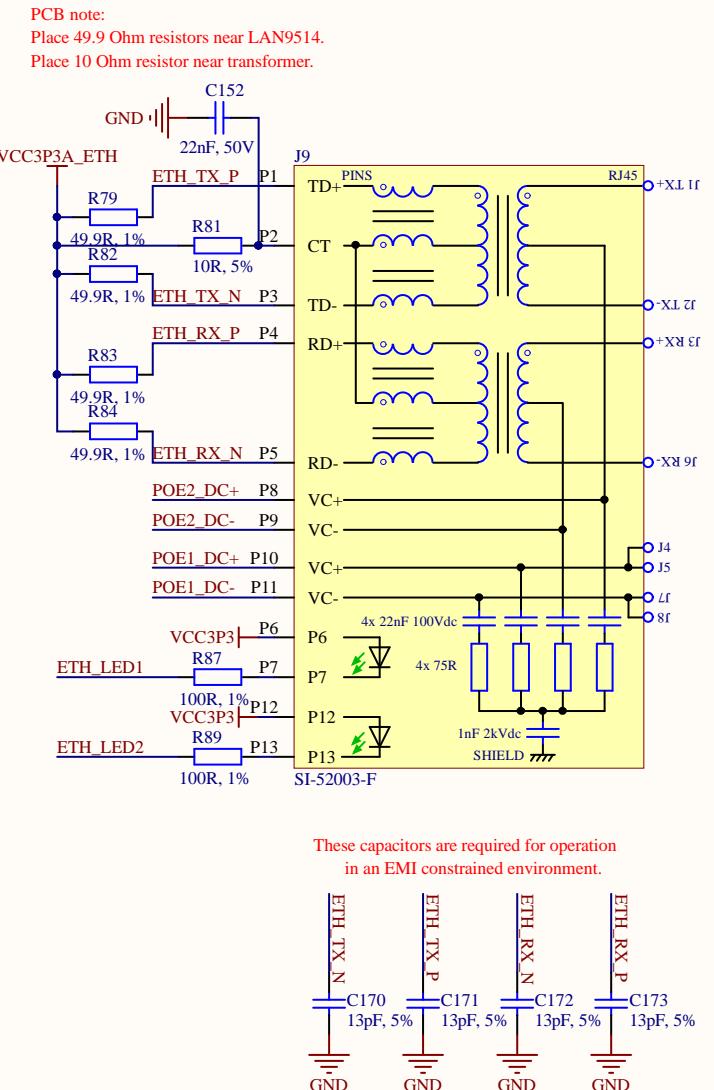
NF elements on sheet: R92, IC25, C169, J11, J12, R96, R97, R98, R101
Number of NF elements on sheet: 9

Misc

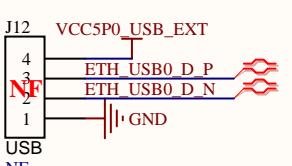
USB hub + Ethernet



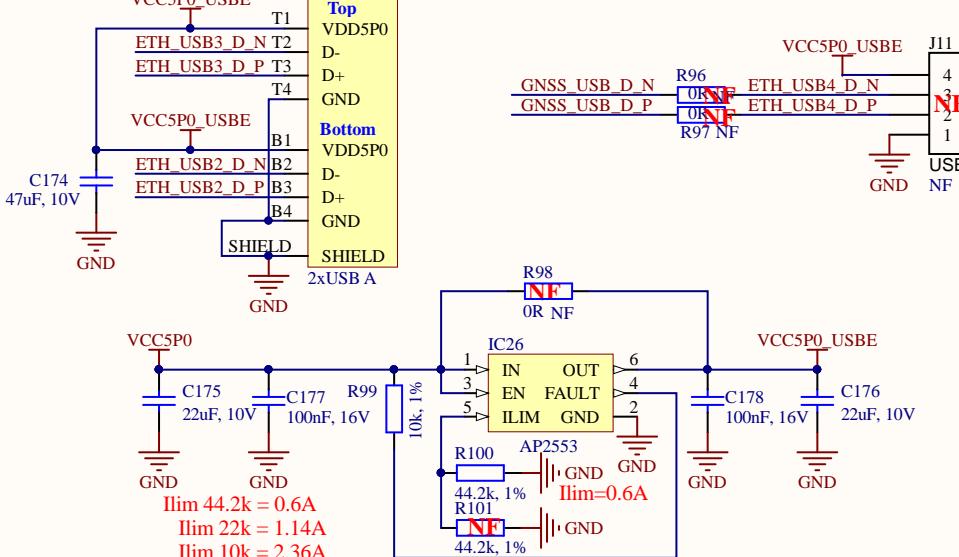
RJ45 connector



USB upstream



USB downstream



Local fiducial Ethernet Top



Project name: LimeNet-Micro_2v1-SDR.PrcPcb

Title: **USB Ethernet**

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United Kingdom

Size: A3 Revision: v2.1

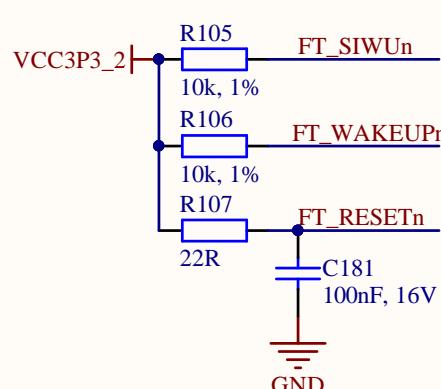
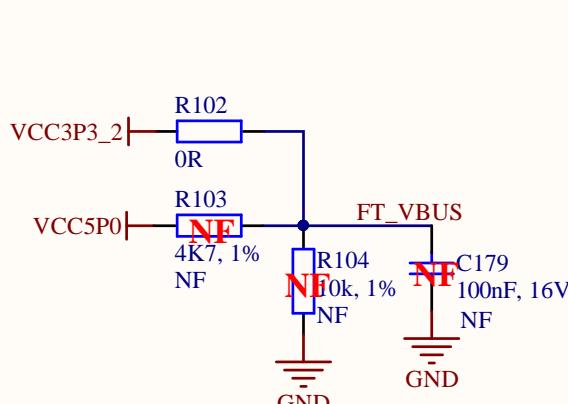
Date: 2019-03-14 Time: 11:43:56 Sheet 10 of 15

File: 10_USB_Ethernet.SchDoc

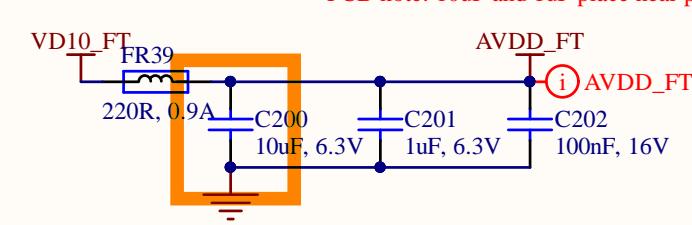
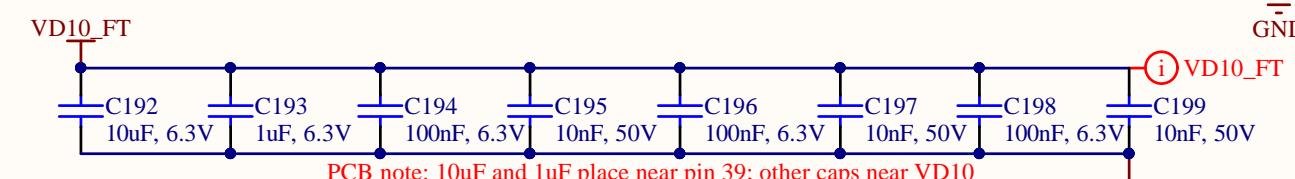
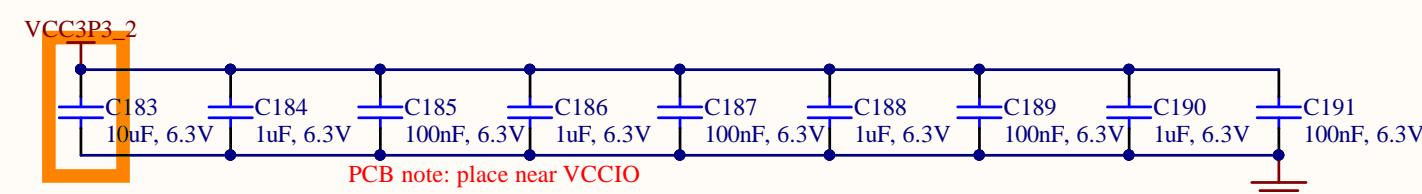
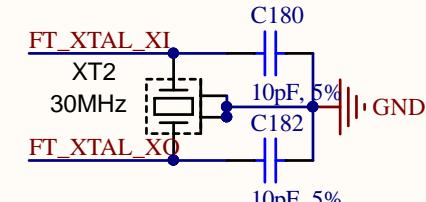
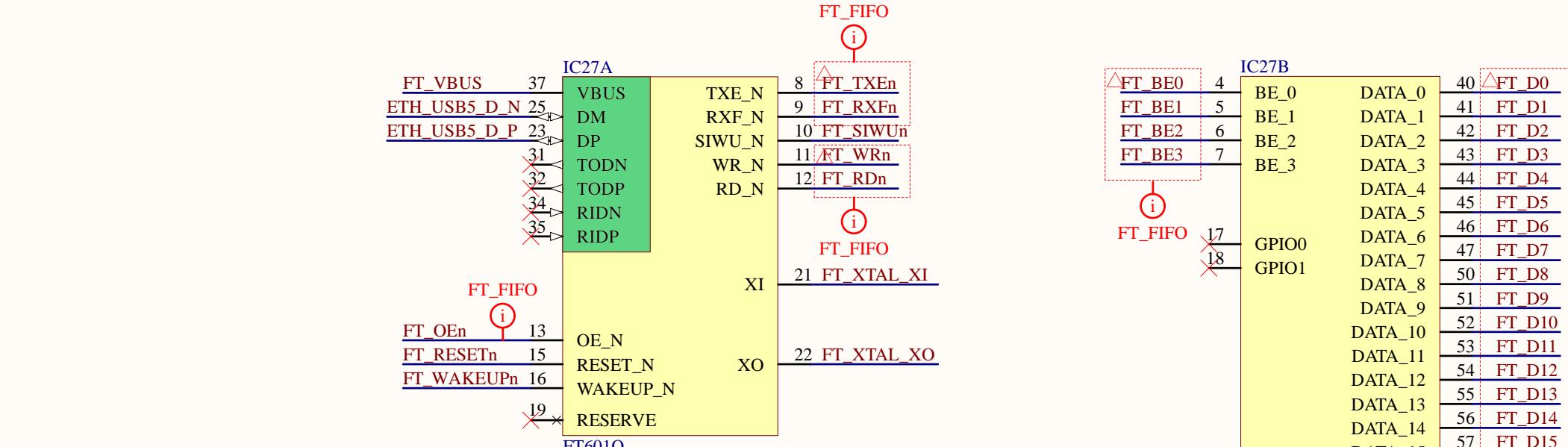
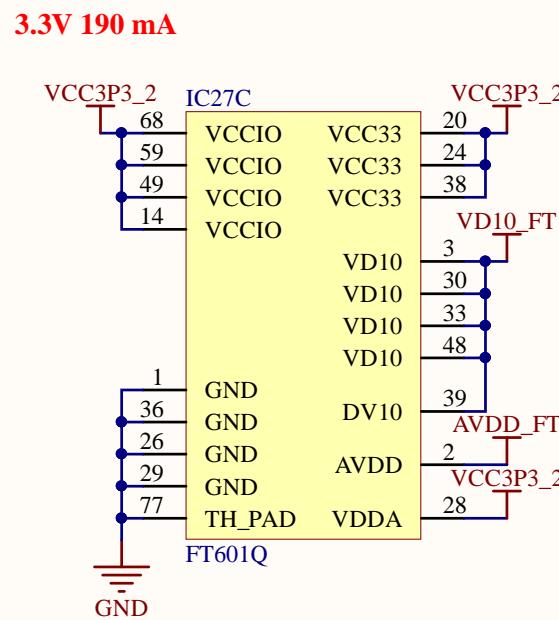
NF elements on sheet: R102, R104, C179

Number of NF elements on sheet: 3

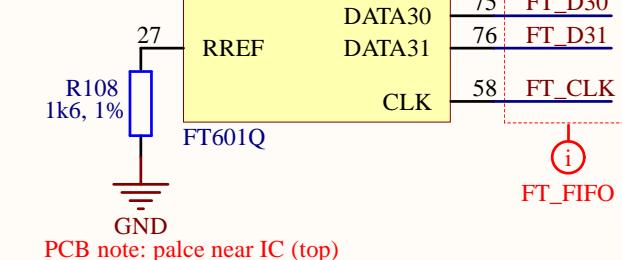
USB FIFO interface



FTDI Power



Schematic note: marked 10uF caps not crucial and can be removed to reduce BOM price



Project name: LimeNet-Micro_2v1-SDR.PrjPcb

Title: **USB FIFO**

Size: A4 Revision: v2.1

Date: 2019-03-14 Time: 11:43:59 Sheet 11 of 15

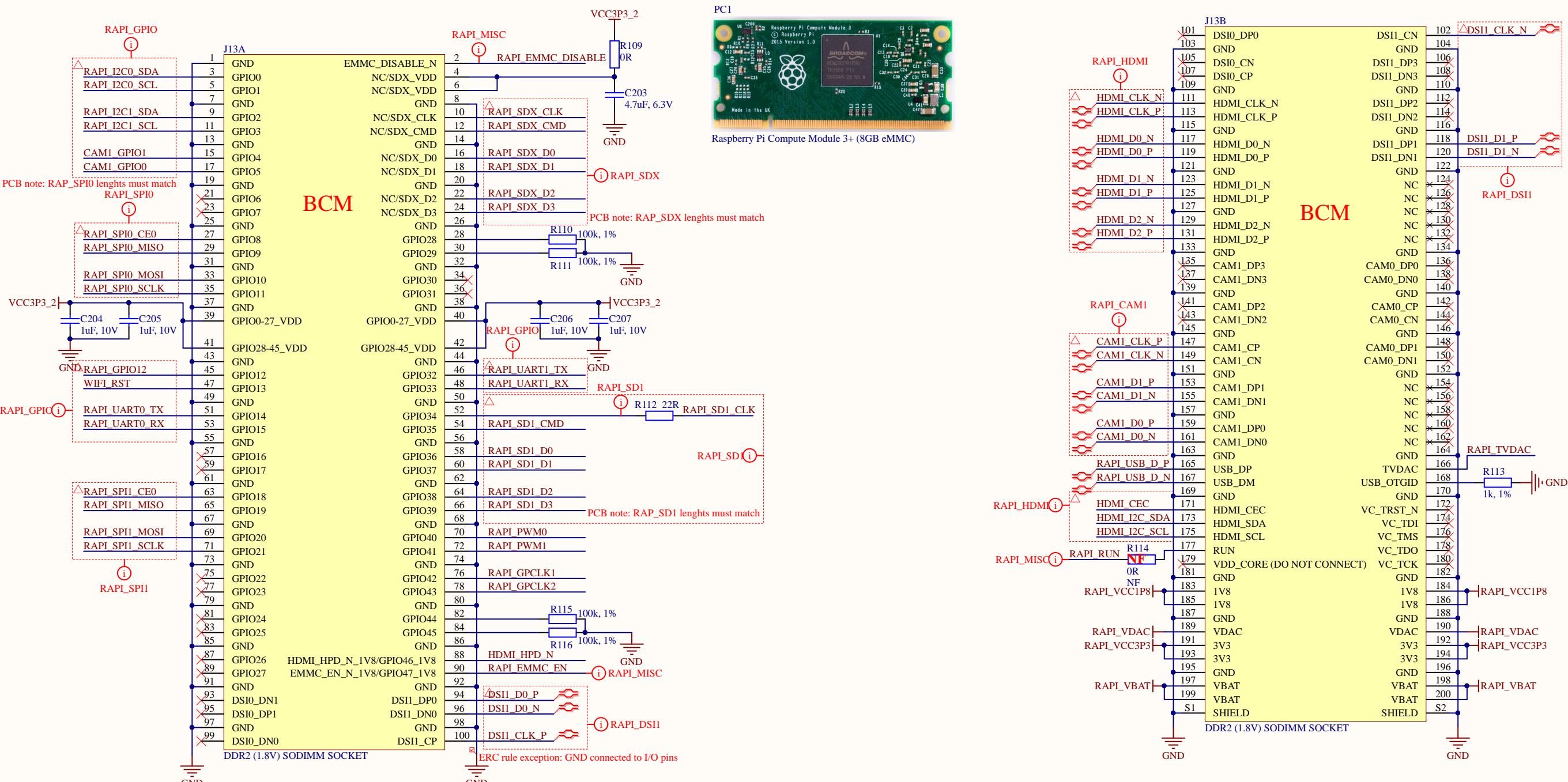
File: 11_USB_FIFO.SchDoc

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United Kingdom

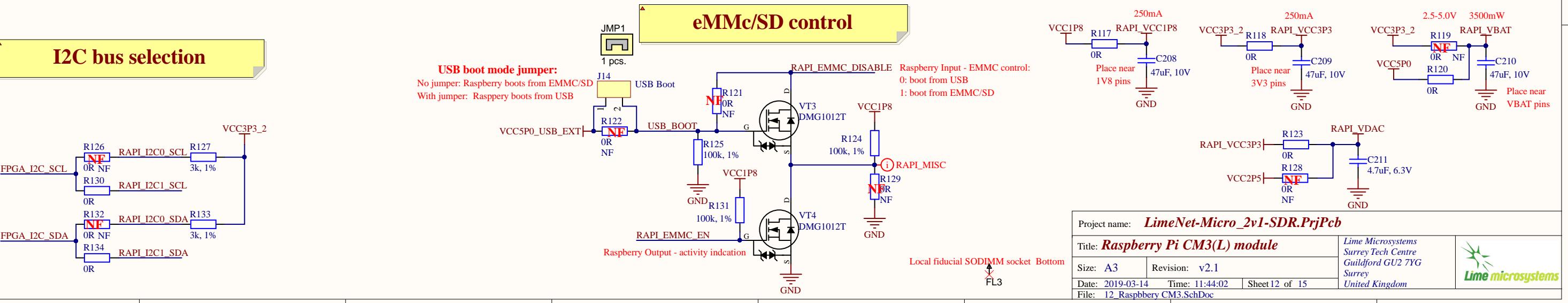


NF elements on sheet: R114, R119, R121, R122, R126, R129, R129, R132
Number of NF elements on sheet: 8

Raspberry Pi CM3(L)

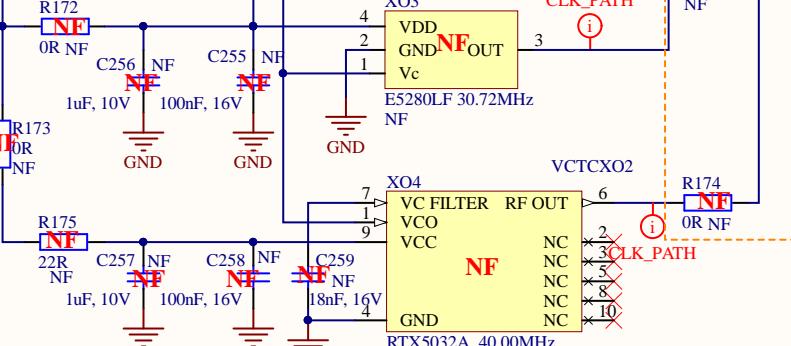
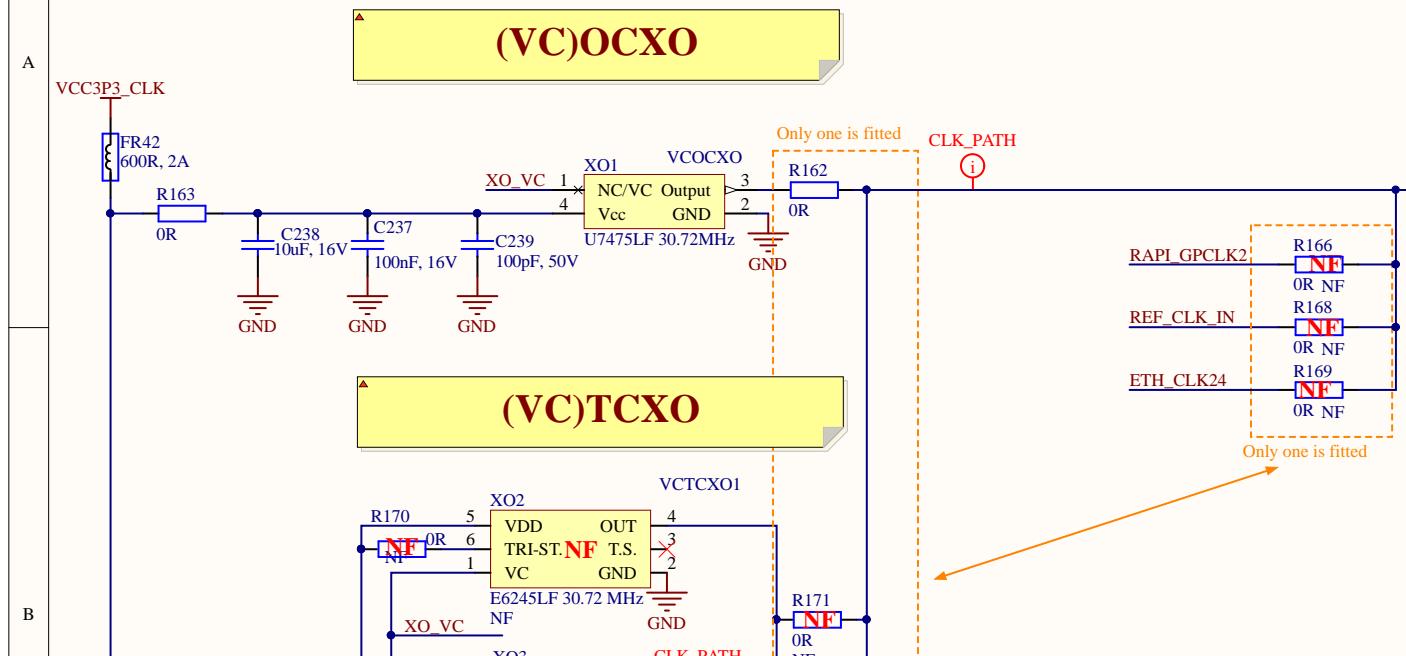


I²C bus selection

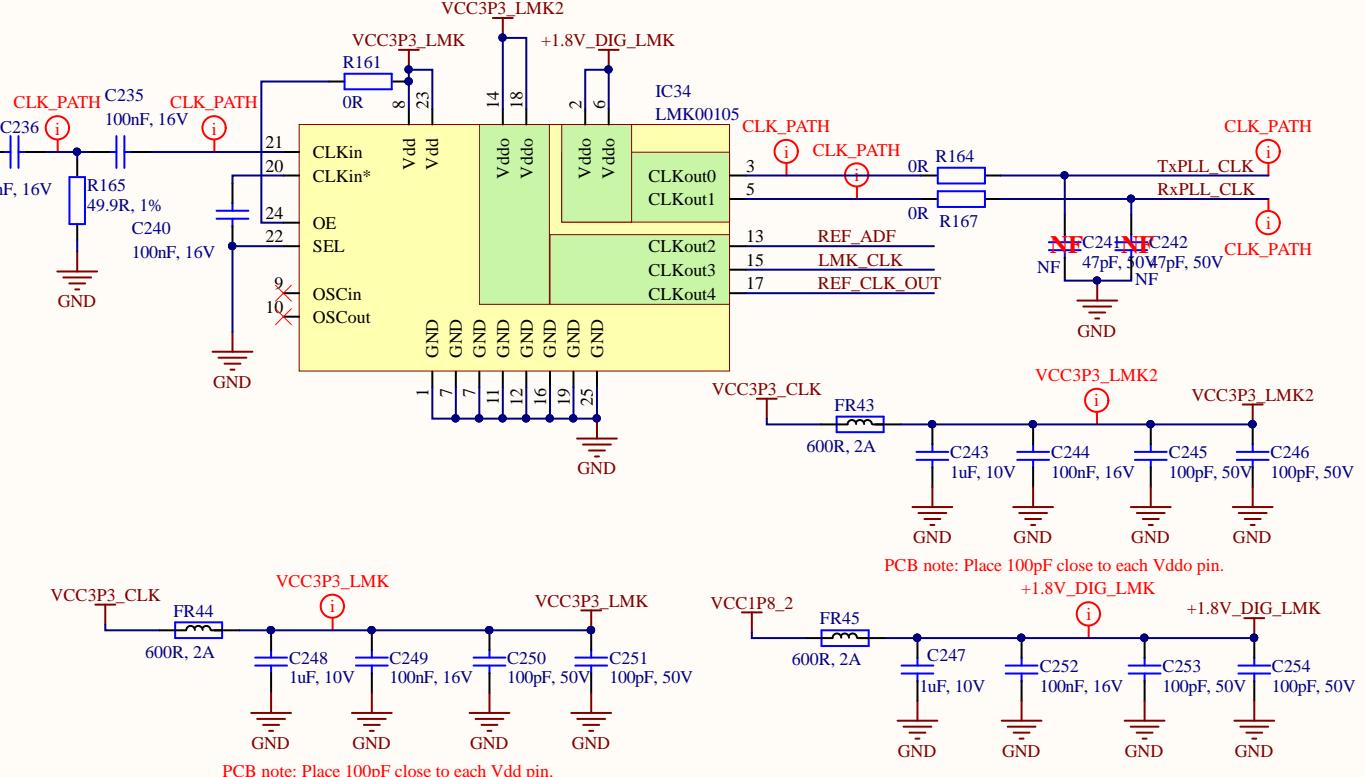
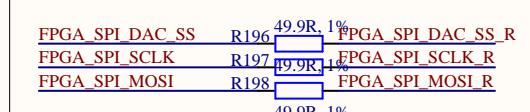
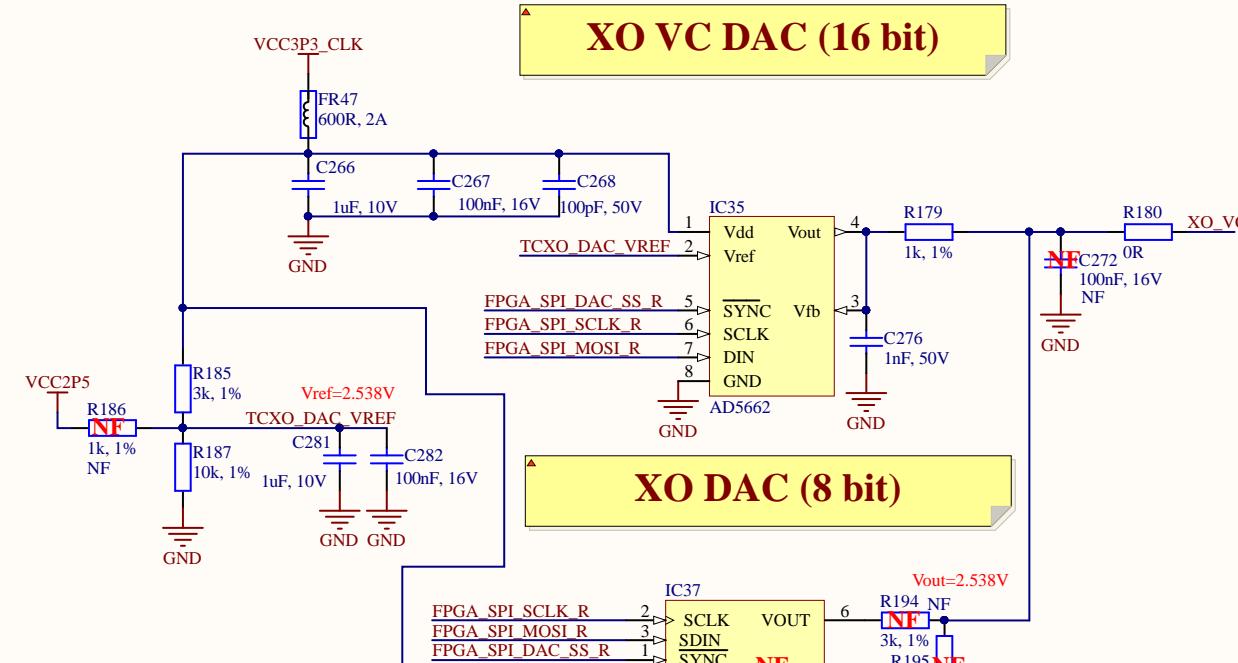


NF elements on sheet: R166, R168, R169, X02, X03, X04, R170, R171, R172, R173, R174, R175, C241, C242, C255, C256, C257, C258, C259, C272, R186, IC37, R194, R195, C286
Number of NF elements on sheet: 25

Clock circuits



XO VC DAC (16 bit)

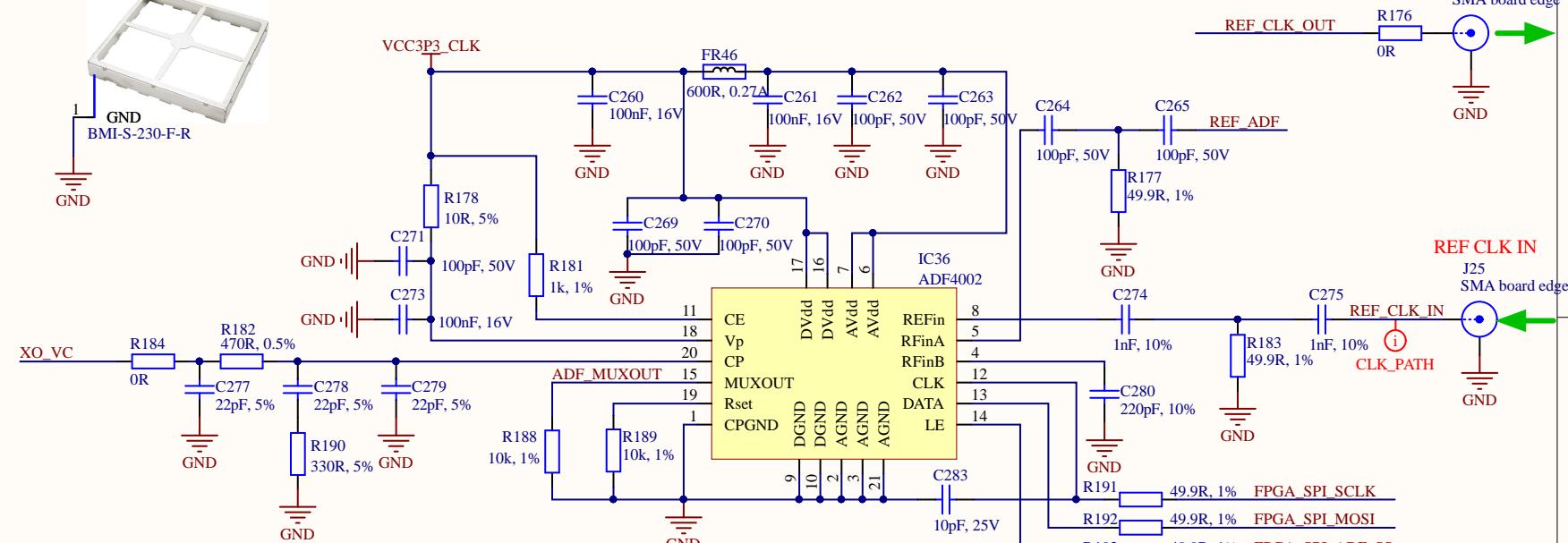


BML-S-230



BMT-S-250-1

Phase detector



Project name: LimeNet-Micro 2v1-SDR PriPc

Title: Clocks		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom	 Lime microsystems
Size: A3	Revision: v2.1		
Date: 2019-03-14	Time: 11:44:09	Sheet 14 of 15	
File: 14_Clocks_SchDoc			

NF elements on sheet: VT10, C307, VD4, FR50, C312, IC41, R219, R223, C313, R235, R239, R240, R241

Number of NF elements on sheet: 13

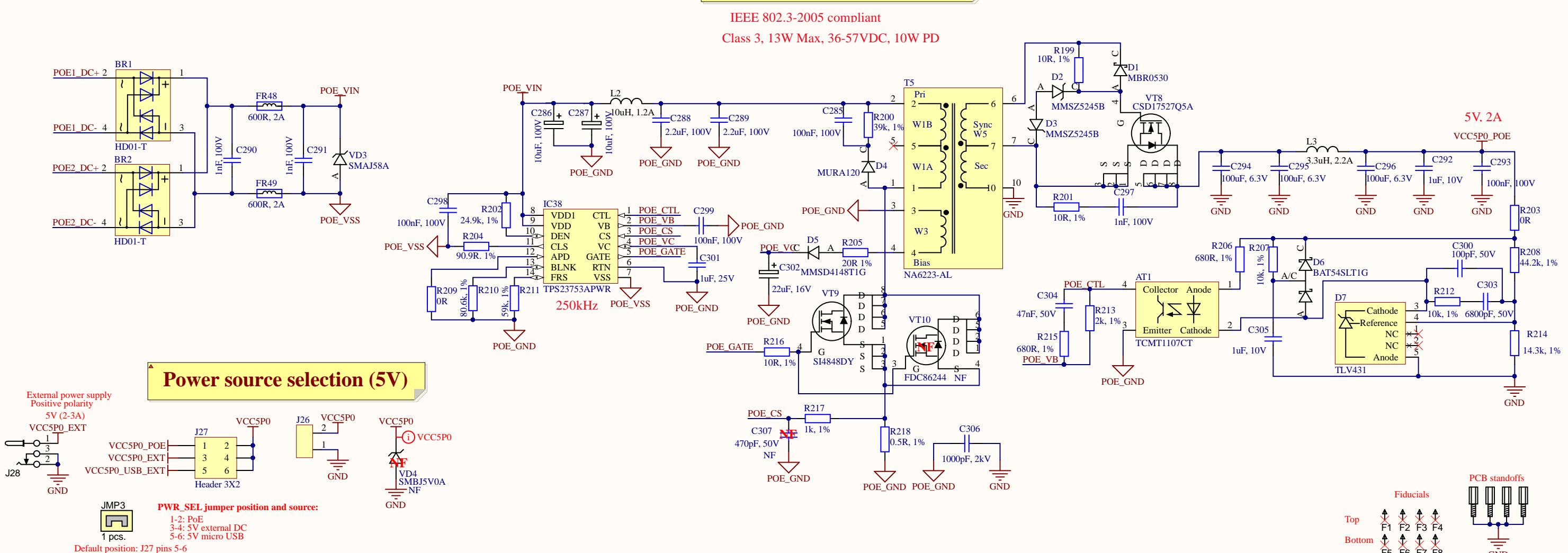
Total number of NF elements on all sheets: 115

Board power circuits

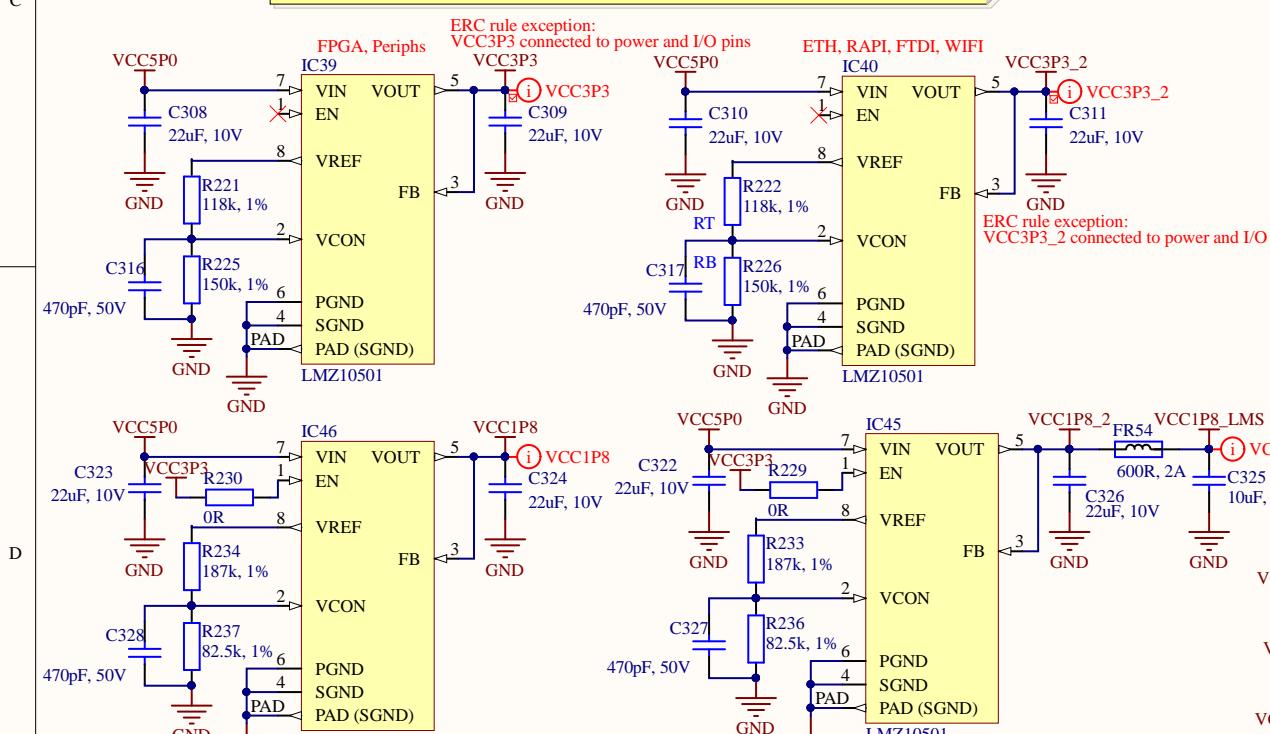
Power over Ethernet

IEEE 802.3-2005 compliant

Class 3, 13W Max, 36-57VDC, 10W PD



Switching regulators



Linear regulators

