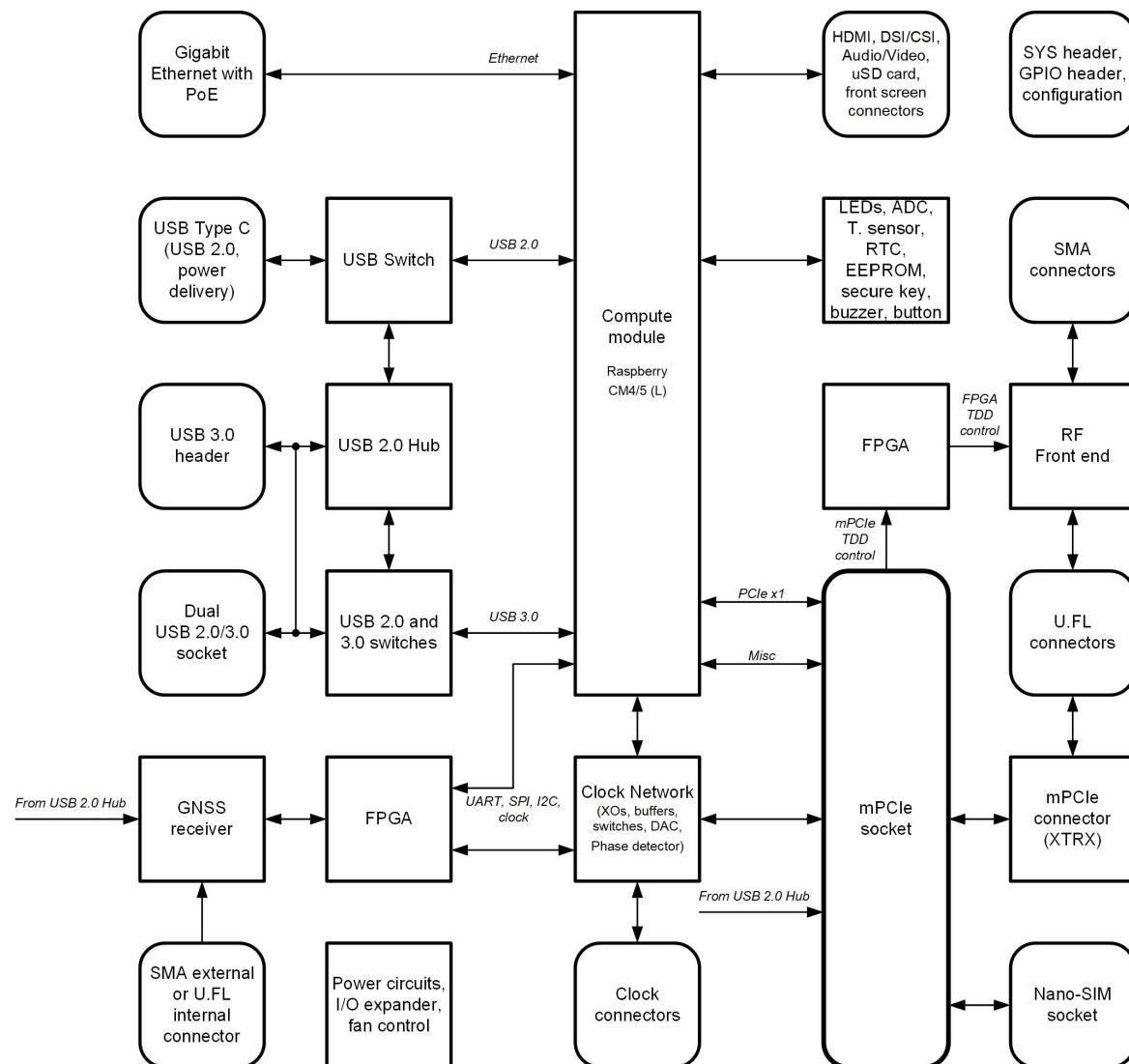


## Block diagram



Project name: **LimePSB-RPCM\_1v4.PrbPcb**

Title: **Block diagram**

Version: 1.4

Variant: Default

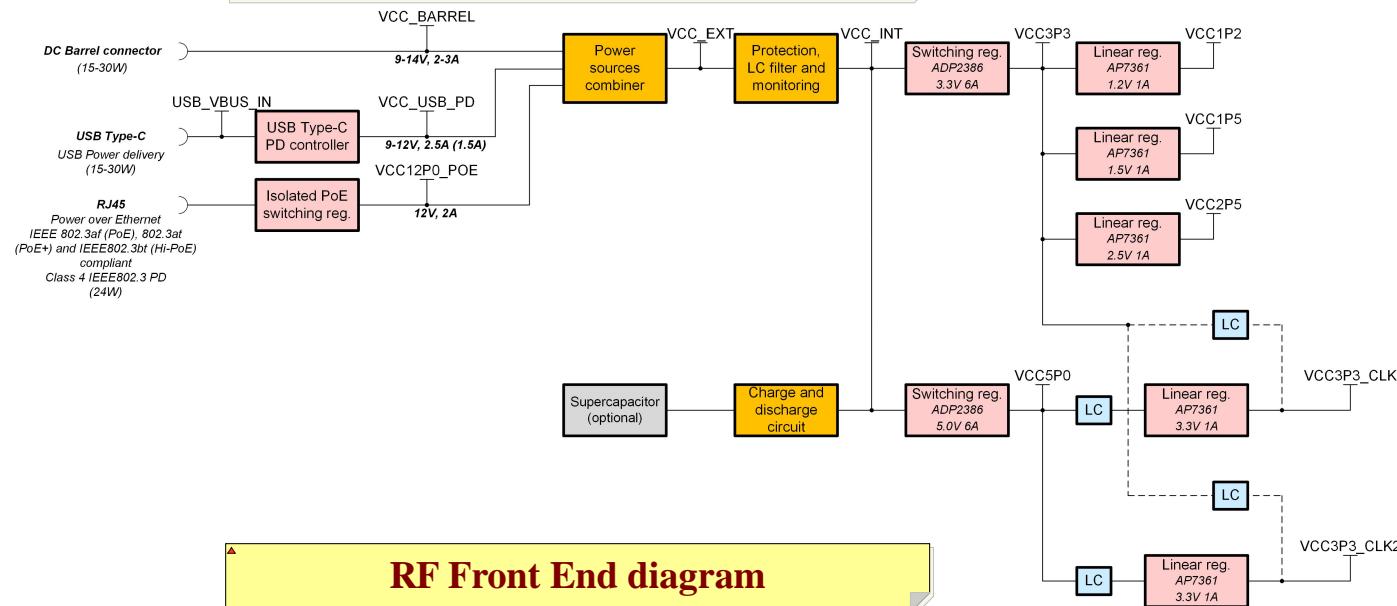
Date: 2025-03-13 Time: 16:22:49 Sheet 1 of 15

File: 01\_Block\_diag.SchDoc

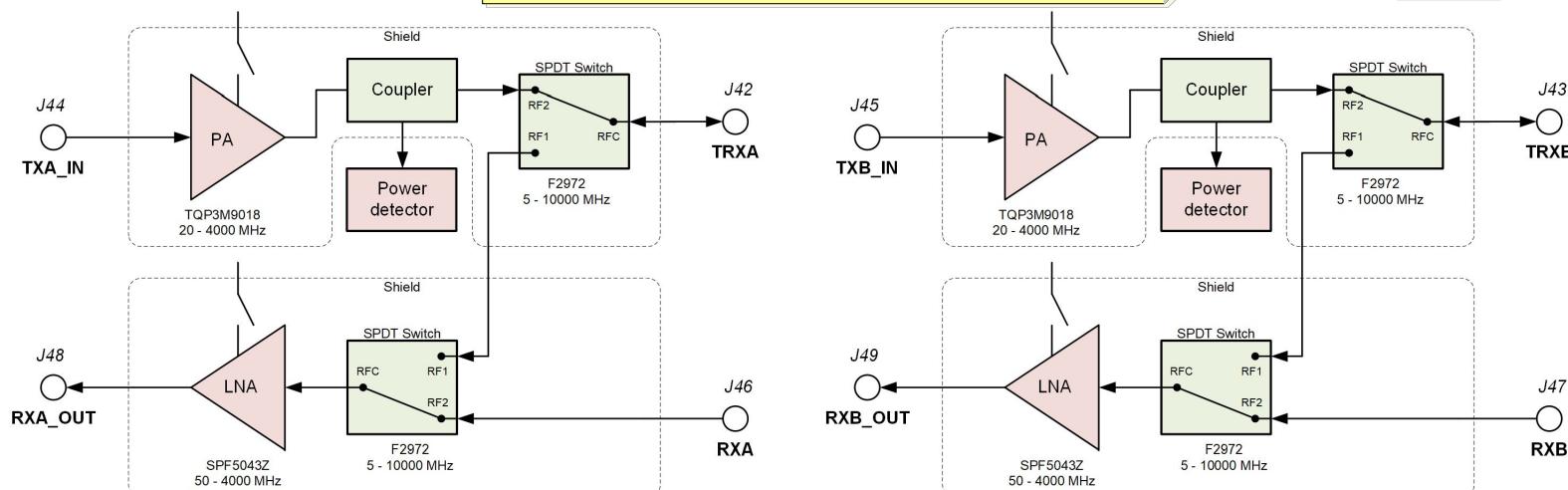
Lime Microsystems  
Surrey Tech Centre  
Guildford GU2 7YG  
Surrey  
United Kingdom



## Power diagram



## RF Front End diagram



\* All RF switches are controlled by the same signal RF\_SW\_TDD

Project name: LimePSB-RPCM\_1v4.PnjPcb

Title: Power + RF Front End diagram

Version: 1.4 Variant: Default

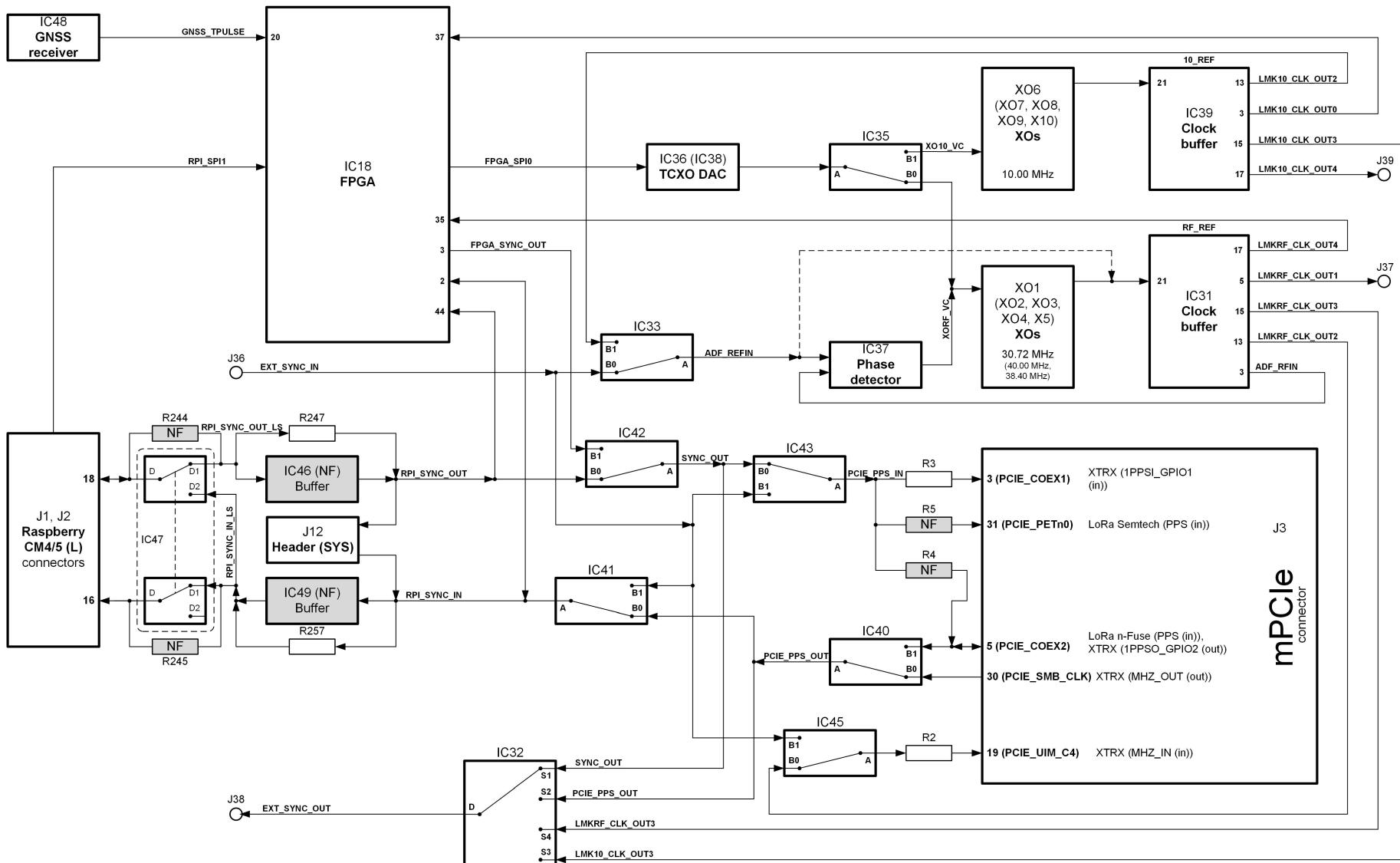
Date: 2025-03-13 Time: 16:22:49 Sheet 2 of 15

File: 02\_Power\_RFFE\_diag.SchDoc Size: A4

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Guildford GU2 7YG  
Surrey  
United Kingdom



## Clock diagram



Project name: **LimePSB-RPCM\_1v4.PrbPcb**

Title: **Clock diagram**

Version: 1.4 Variant: Default

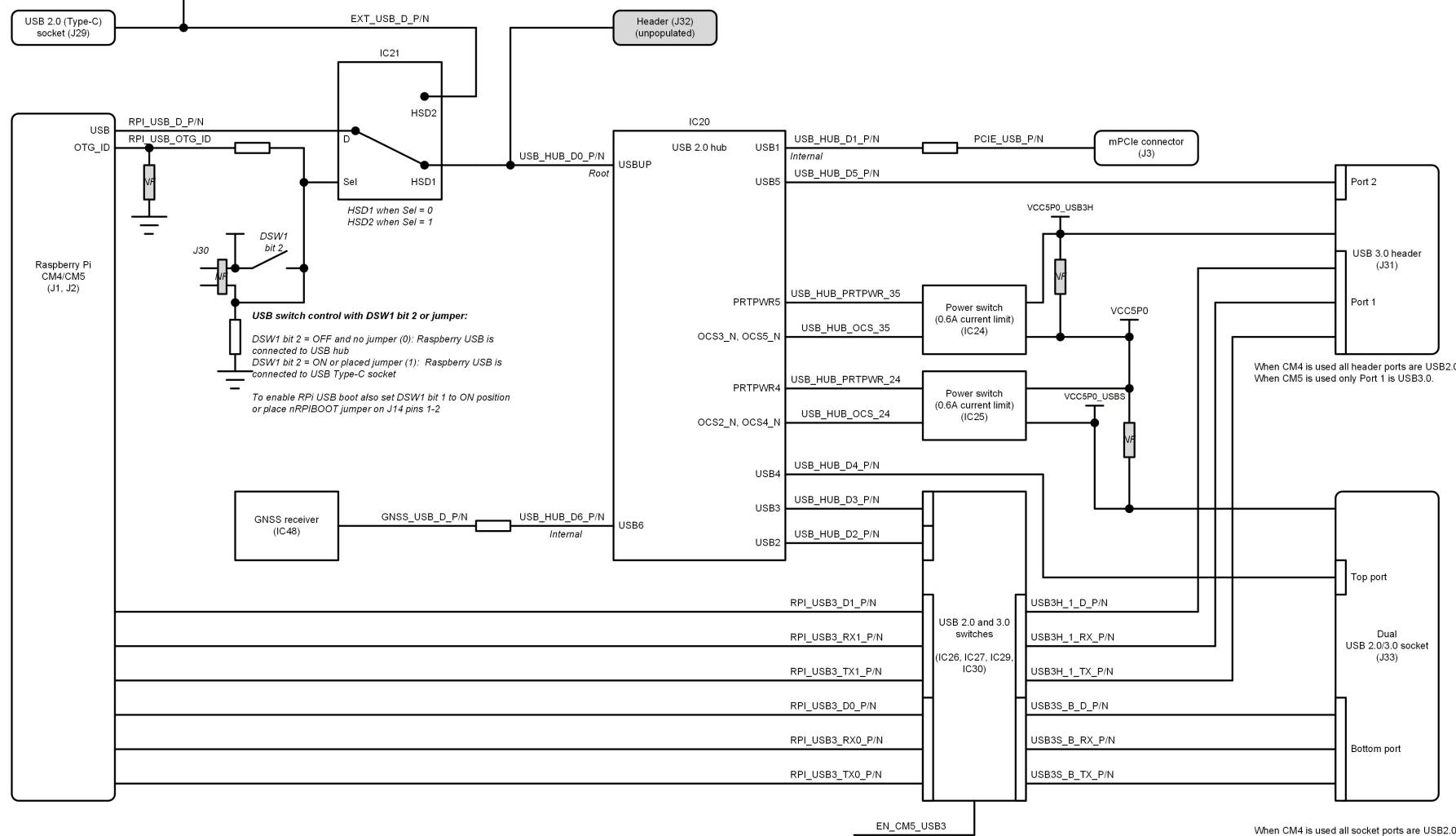
Date: 2025-03-13 Time: 16:22:49 Sheet 3 of 15

File: 03\_Clock\_diag.SchDoc

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United Kingdom



## USB diagram



Project name: **LimePSB-RPCM\_1v4.PpjPcb**

Title: **USB diagram**

Version: 1.4

Variant: Default

Date: 2025-03-13 Time: 16:22:49 Sheet 4 of 15

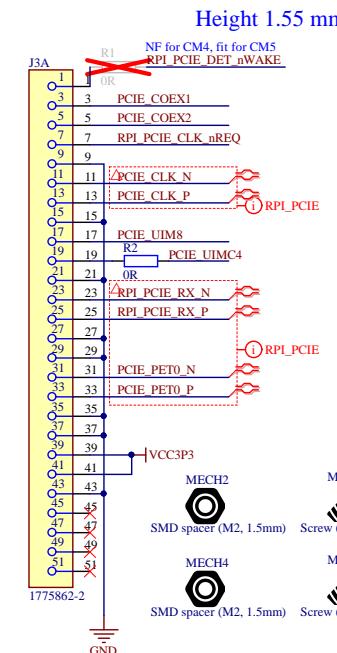
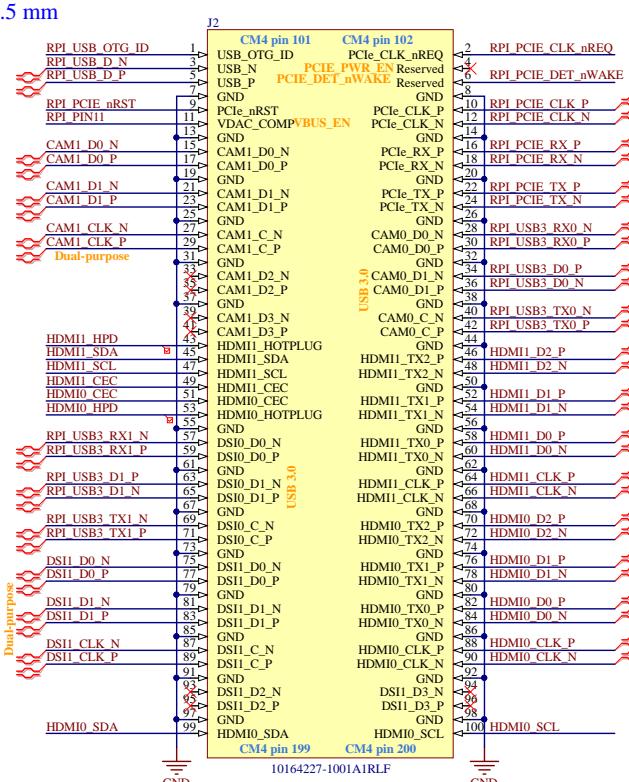
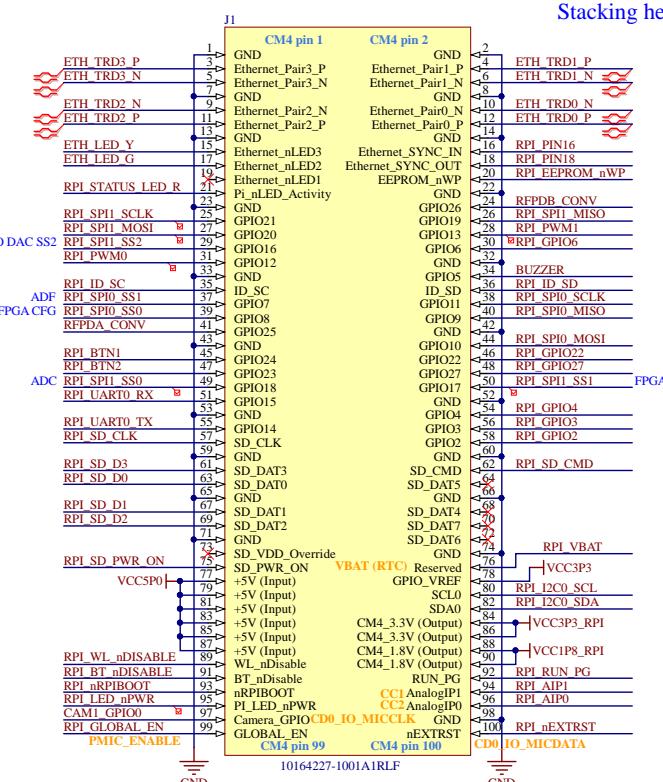
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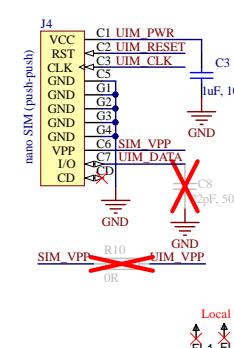
## Raspberry Pi CM4/5(L) and mPCIe

## Board to Board connector for Raspberry Pi CM4/5(L)



- mPCIe is compatible with these non standard mPCIe boards:
  - Fairwaves or LimeSDR XTRX (default)
  - n-Fuse LoRaWANTM Concentrator LRWCXX-MPCIE\*
  - Semtech LoRa Corecell USB version\*
- \* some resistors may need to be soldered/unsoldered to match a specific board.

## **Nano-SIM socket**



Project name: LimePSB-RPCM\_1v4.PriPci

Title: **Raspberry Pi CM4/5(L) and mPCIe**

Version: 1.4 Variant: Default

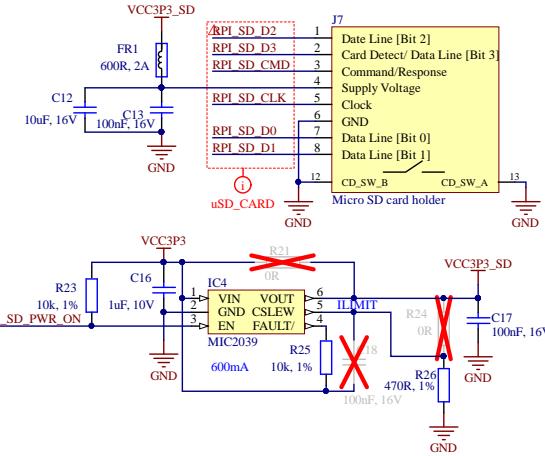
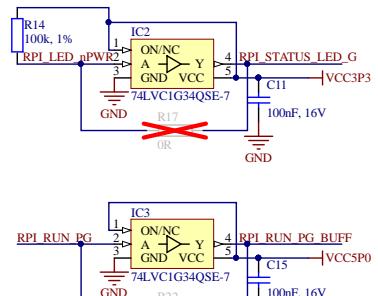
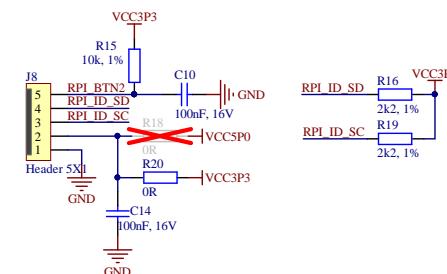
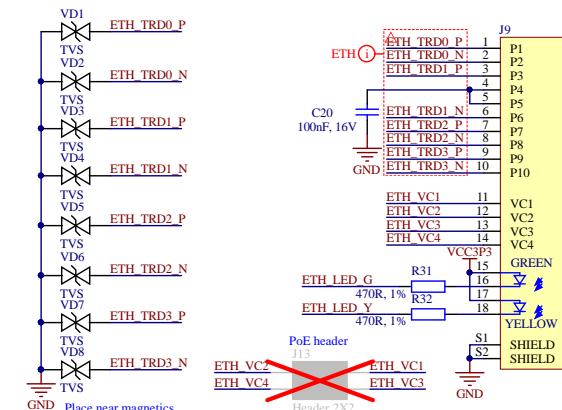
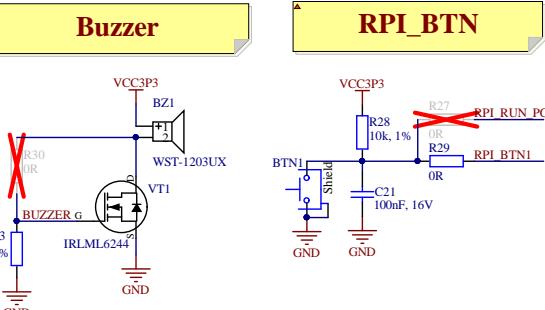
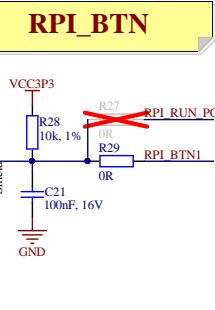
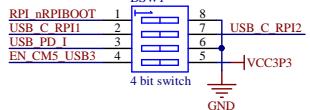
Date: 2025-03-13 Time: 16:22:49 Sheet 5 of 15

Date: 2023-05-15 Time: 16:22:19 Sheets: 01 / 15  
File: 05 RPi mPCIe.SchDoc Size: A3

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United Kingdom

**Misc 1****uSD card socket**

Only for CM4L and CM5L with no on-board Flash (eMMC)

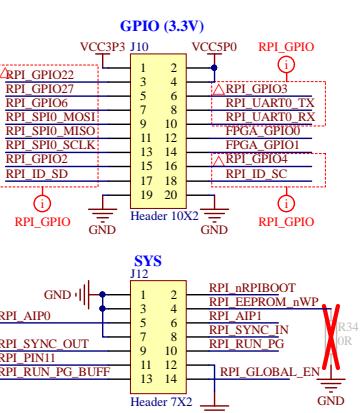
**Buffers, level converters****Front screen I2C + BTN****Gigabit Ethernet (RJ45) connector****Buzzer****RPI\_BTN****DIP switch**

Bit 1: RPi boot source:  
OFF: RPi boots from eMMC/uSD (default).  
ON: Booting from eMMC will be stopped and booting will be transferred to RPi boot which is via USB.

Bit 2: RPi USB 2.0 port mux control:  
OFF: RPi USB is connected to USB hub (default).  
ON: RPi USB is connected to USB C connector.

Bit 3: USB C PD current configuration:  
OFF: I=2.5A (default).  
ON: I=1.5A.

Bit 4: Dual USB socket source:  
OFF: connected to USB 2.0 hub (for CM4).  
ON: connected to CM5 USB3.0 lines (for CM5).

**GPIO ans SYS headers**

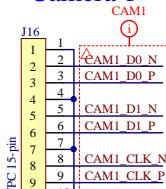
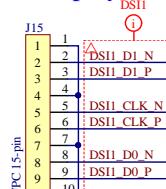
nRPI\_BOOT: During boot if this pin is low booting from eMMC will be stopped and booting will be transferred to rpi boot which is via USB. Place jumper on pins 1-2.

EEPROM\_nWP: can be grounded to prevent writing to the on board EEPROM which stores the bootcode. Place jumper on pins 3-4 or solder R32.

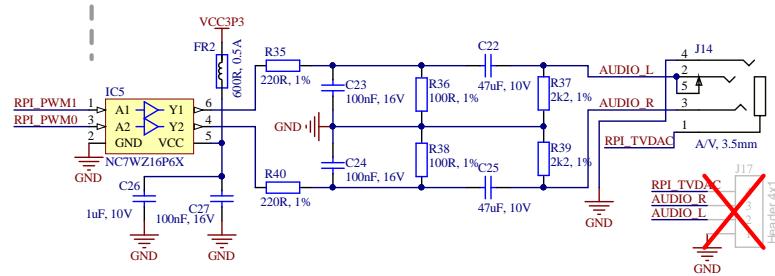
A button between pins 13-14 can be used to wake up compute from power down.

RUN\_PG pin when high signals that the CM4 has started. Driving this pin low resets the module.

A button between pins 10-12 replicates the power button on Raspberry Pi 5. A short press signals that the device should wake up or shut down. A long press forces shutdown.

**LVDS (Camera + Display)****Camera 1****Display 1**

For CM5 CAM1 and DSII signals become dual-purpose and can be used for either a CSI camera or a DS1 display.

**Analog audio + Composite video out**

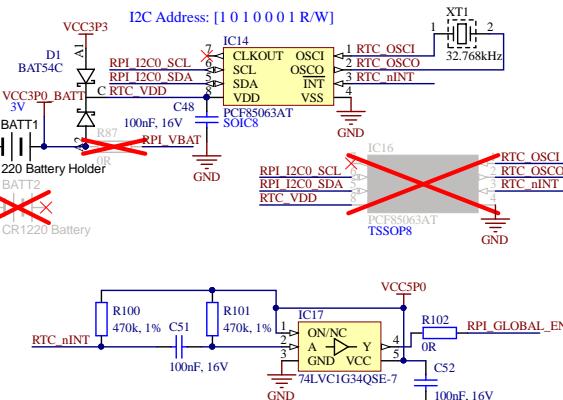
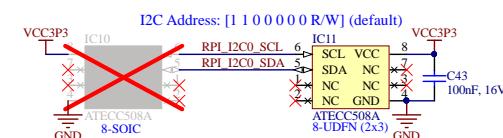
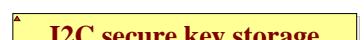
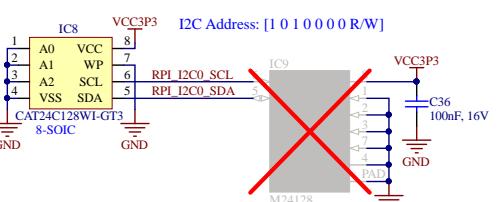
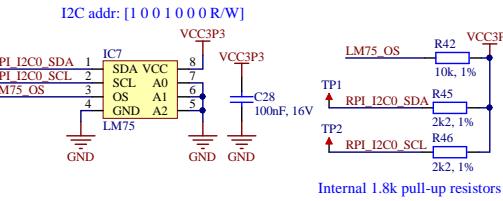
Project name: **LimePSB-RPCM\_Iv4.PrbPcb**

Title: **Misc 1**

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Surve  
United Kingdom

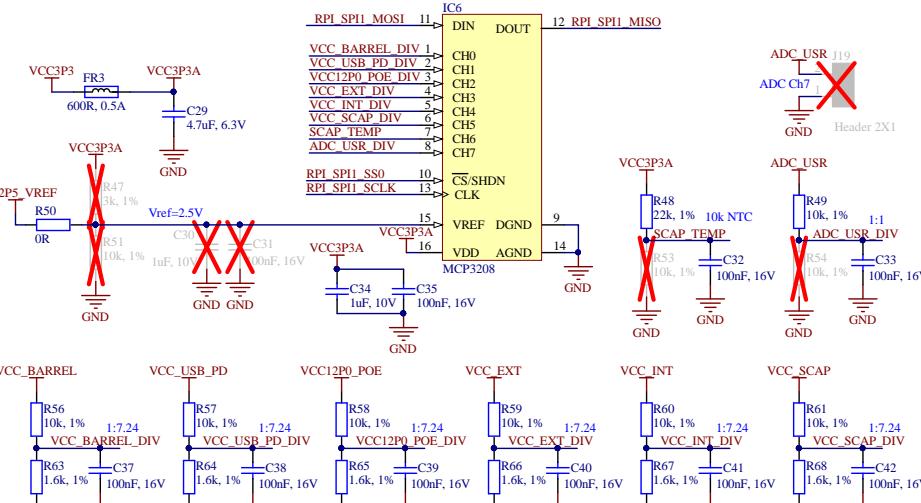


Version: 1.4 Variant: Default  
Date: 2025-03-13 Time: 16:22:50 Sheet 6 of 15  
File: 06\_Misc 1.SchDoc Size: A3

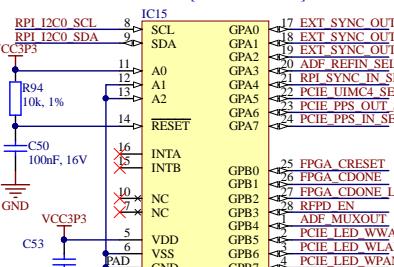
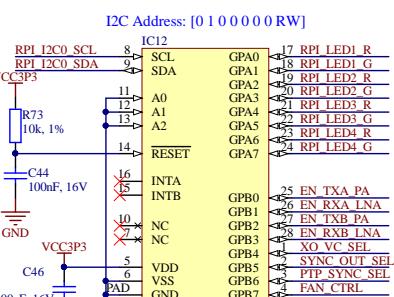


## Misc 2

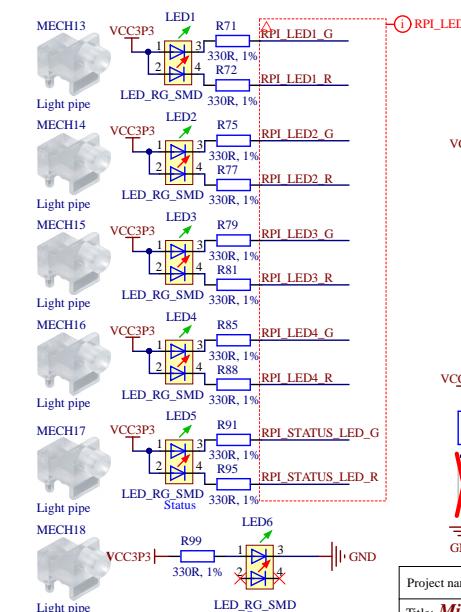
SPI ADC



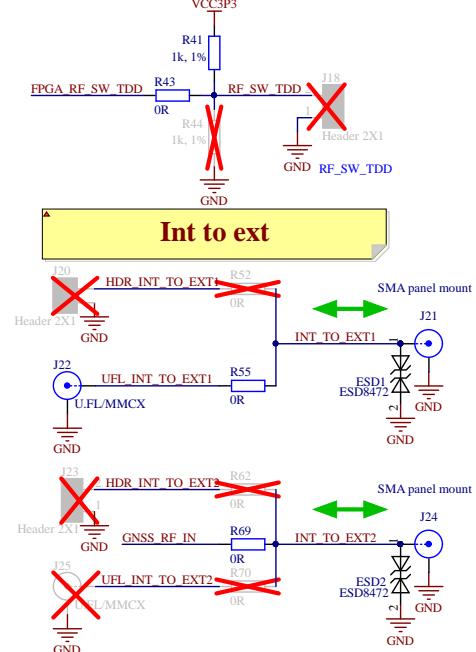
## I2C I/O expanders



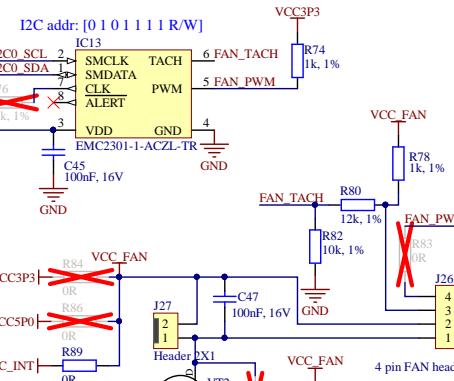
## Raspberry Pi LEDs



RFFE TDD control



FAN control



Project name: **LimePSB-RPCM\_1v4.PrjPcl**

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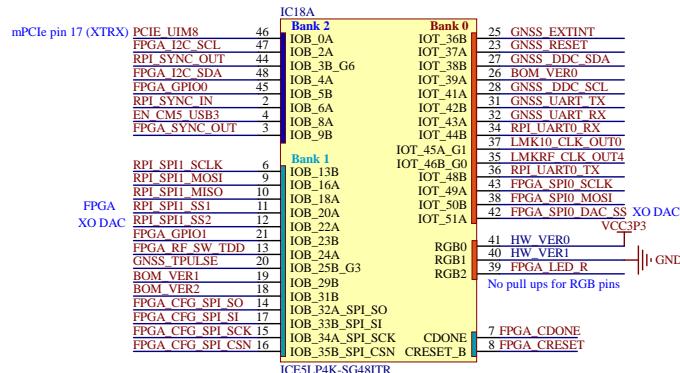
Title: **Misc 2**

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Surrey Tech Centre  
Guildford GU2 7YG  
Surrey  
United Kingdom*

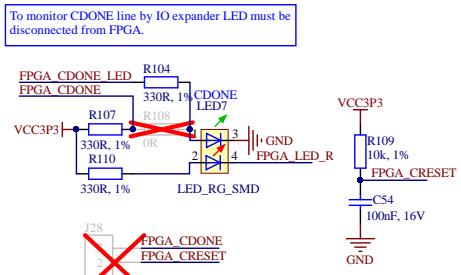


# FPGA

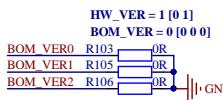
FPGA



FPGA misc



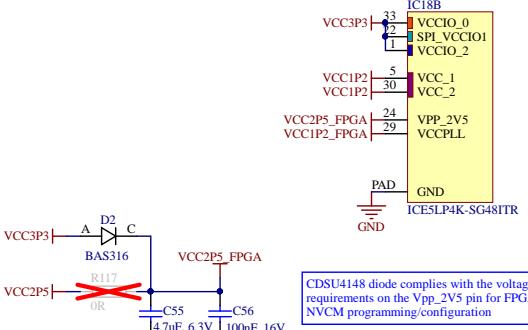
HW\_VER, BOM\_VER



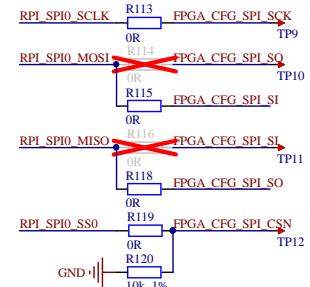
## I<sup>2</sup>C interconnections



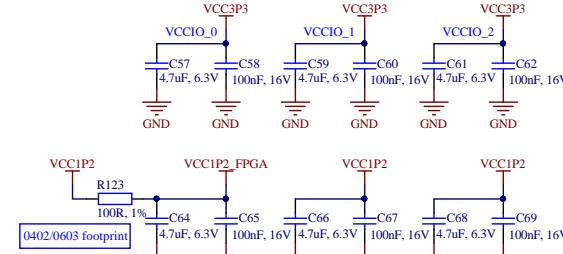
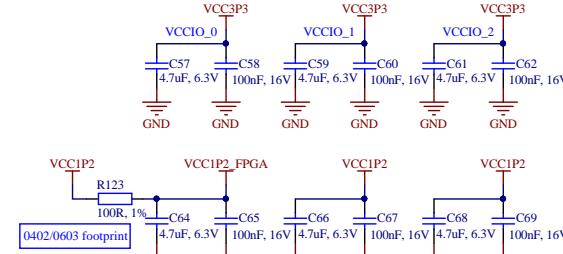
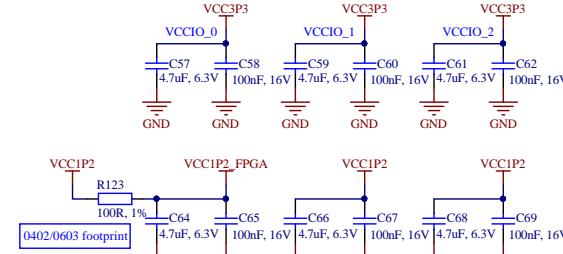
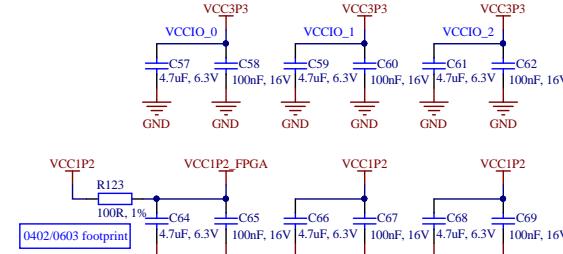
FPGA power



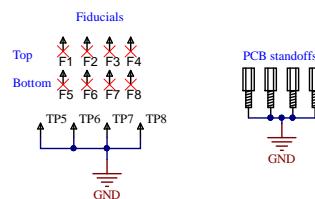
## FPGA configuration modes



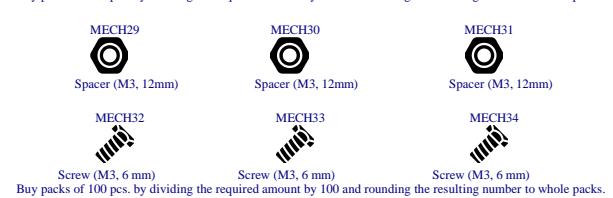
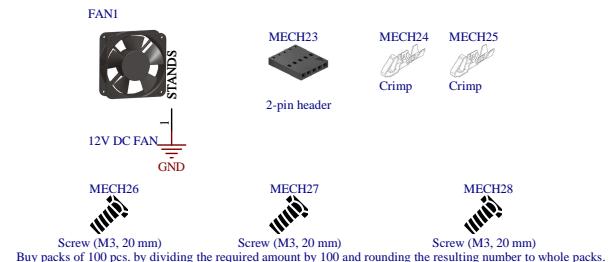
## FPGA configuration Flash



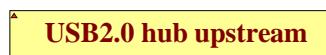
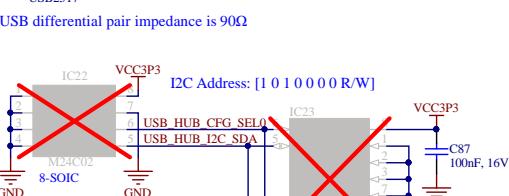
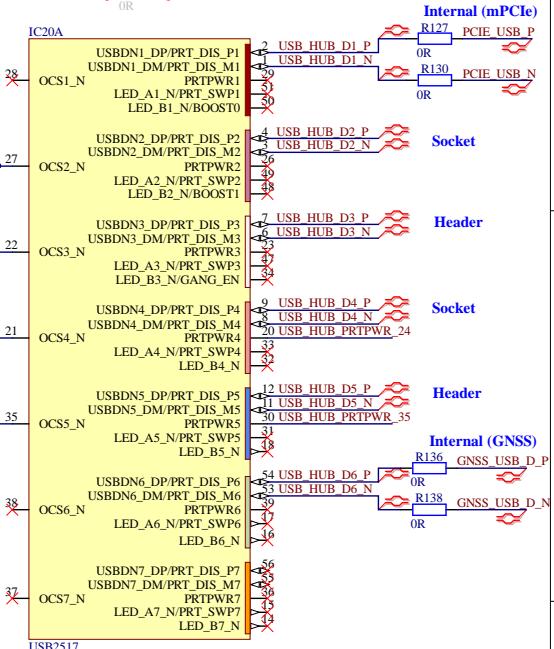
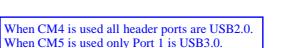
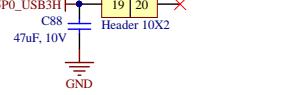
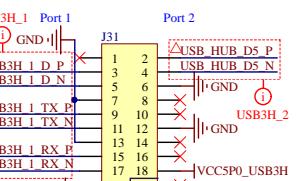
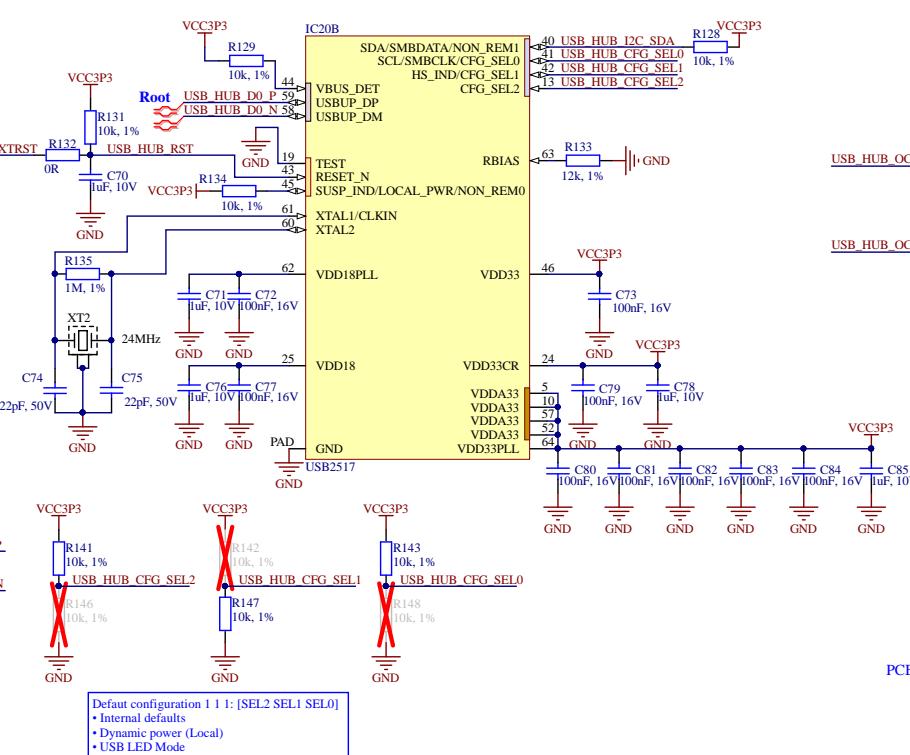
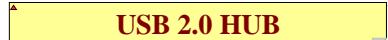
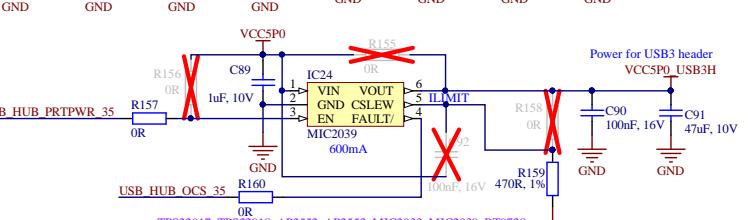
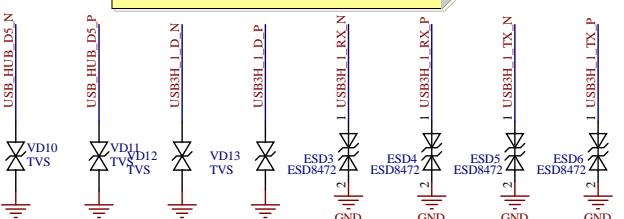
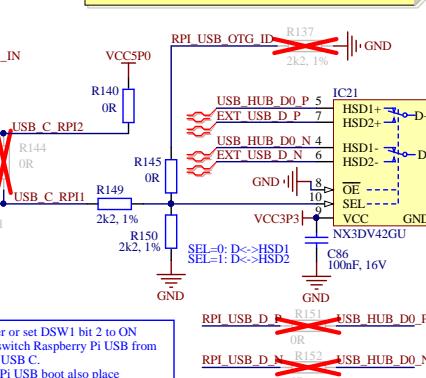
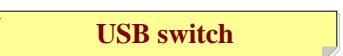
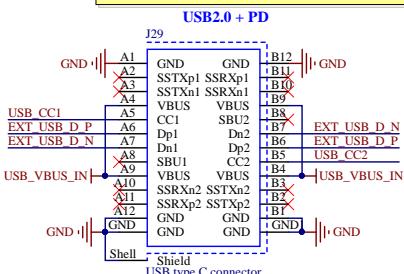
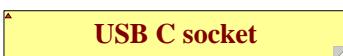
Misc.



Misc for FAN



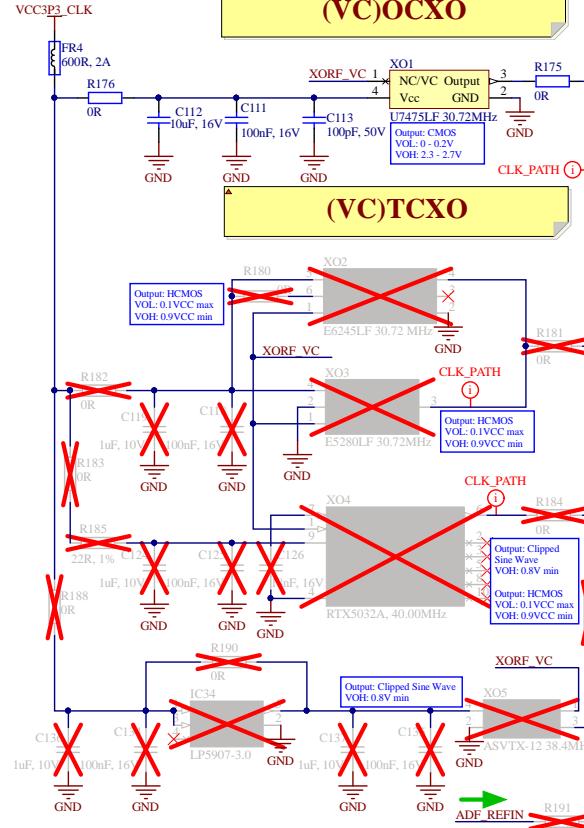
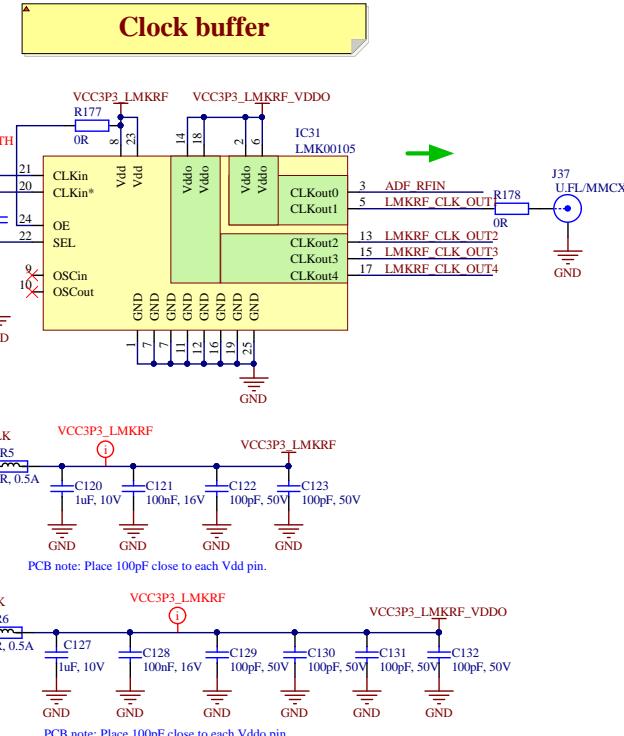
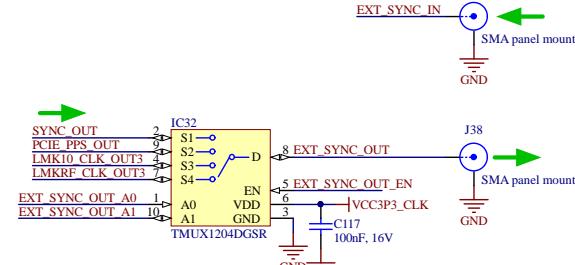
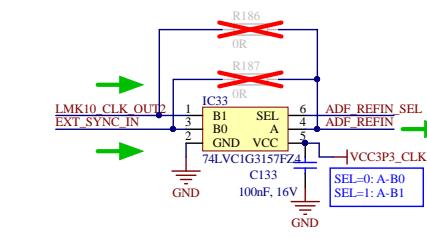
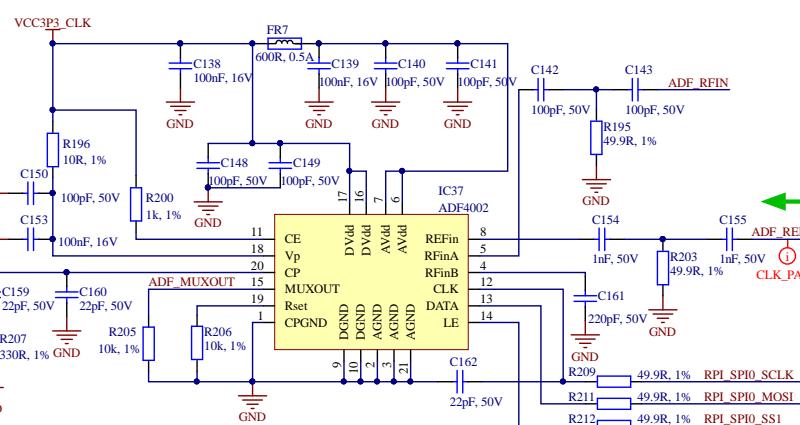
Project name: <b>LimePSB-RPCM_1v4.PrjPcb</b>	
Title: <b>FPGA</b>	Lime Microsystems Survey Tech Centre Guildford GU2 7YG Survey United Kingdom
Version: 1.4	Variant: Default
Date: 2025-03-13	Time: 16:22:50
File: 08_FPGA_SchD.kicad_pcb	Sheet 8 of 15 SHEET A?



GDB

Project name: <b>LimePSB-RPCM_Iv4.PnjPcb</b>	
Title: <b>USB 2.0 hub</b>	
Version: <b>1.4</b>	Variant: <b>Default</b>
Date: <b>2023-03-13</b>	Time: <b>16:22:51</b>
File: <b>00_V3SP_hcb_Schematic</b>	Sheet <b>9</b> of <b>15</b>
	Sign: <b>3/3</b>



**RF\_REF****(VC)OCXO****Clock 1 circuits****Clock buffer****EXT\_SYNC\_IN/OUT****Phase detector REFIN selection****Phase detector**

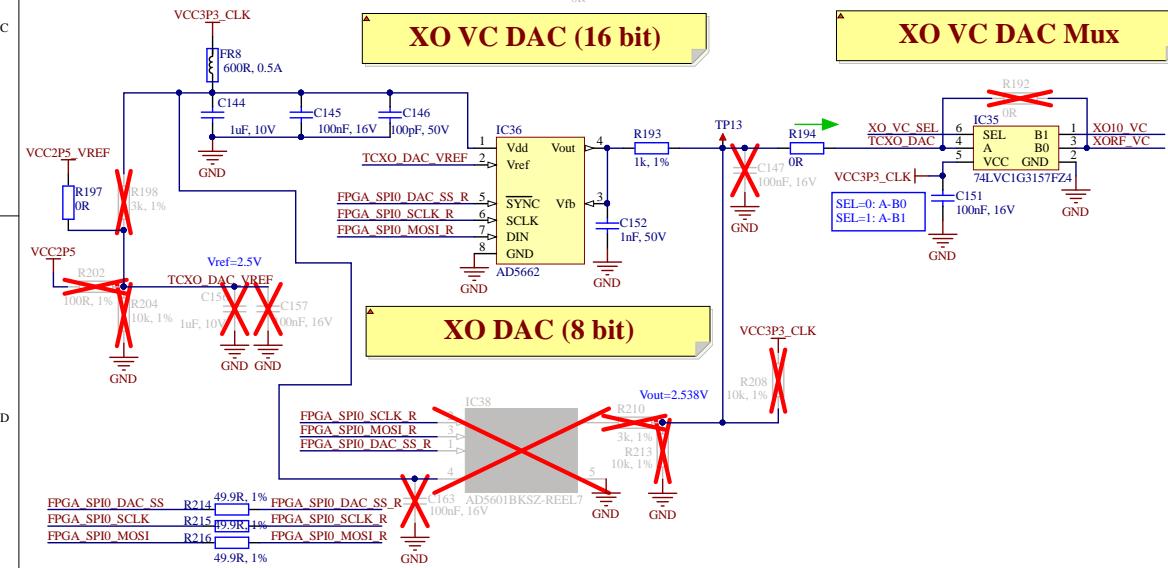
Project name: LimePSB-RPCM\_Jv4.PrjPcb

Title: Clock 1

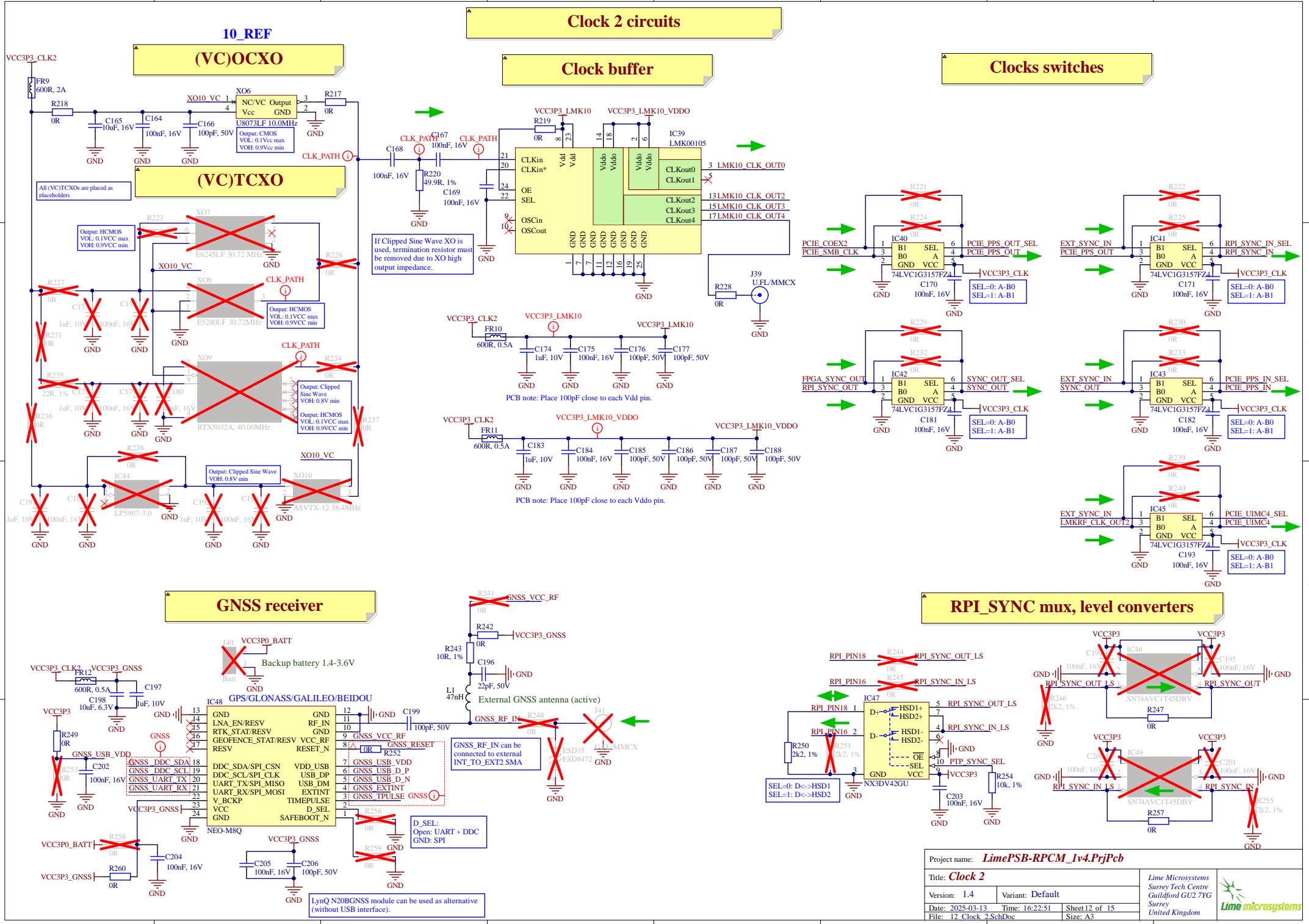
Version: 1.4 Variant: Default

Date: 2025-03-13 Time: 16:22:51 Sheet 11 of 15

File: 11\_Clock\_1.SchDoc

Lime Microsystems  
Survey Tech Centre  
Guildford GU2 7JG  
Survey  
United Kingdom**XO VC DAC (16 bit)****XO VC DAC Mux****XO DAC (8 bit)**

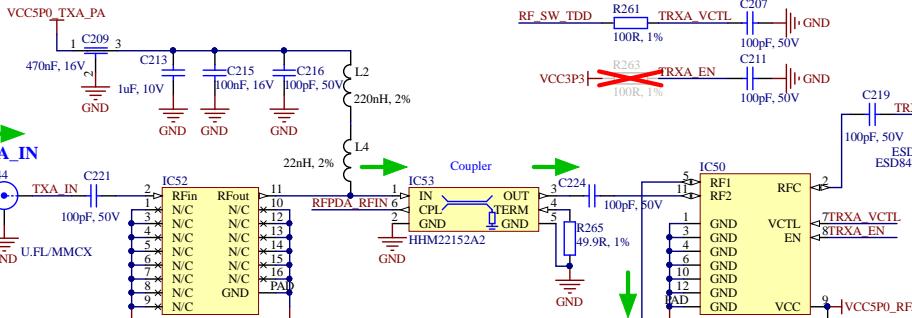
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Title:	Clock 1
Version:	1.4 Variant: Default
Date:	2025-03-13 Time: 16:22:51 Sheet 11 of 15
File:	11_Clock_1.SchDoc
Size:	A3



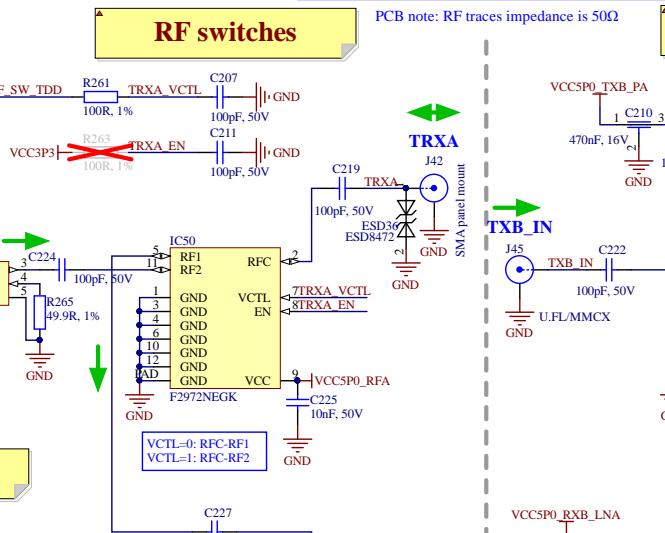
### RF front end

#### Channel A

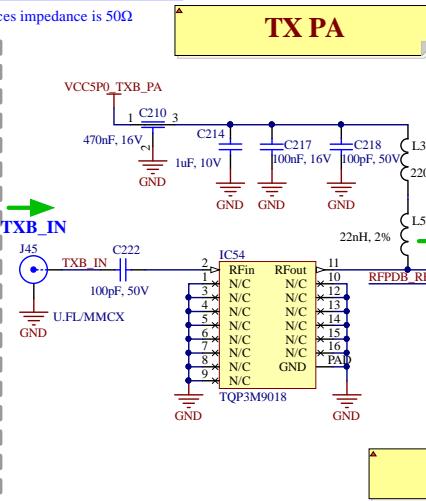
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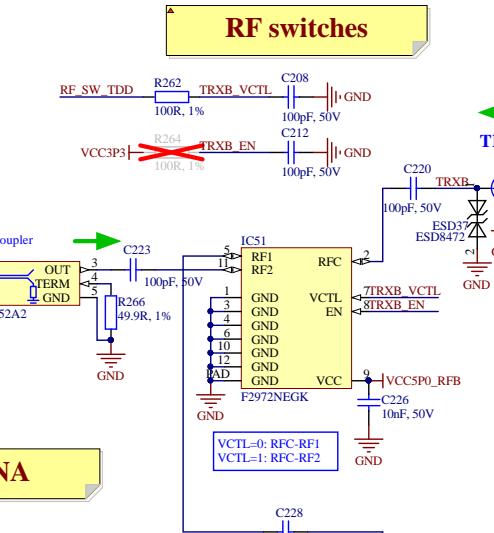
##### RF switches



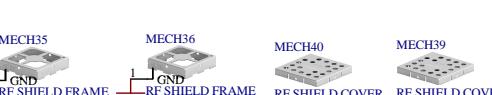
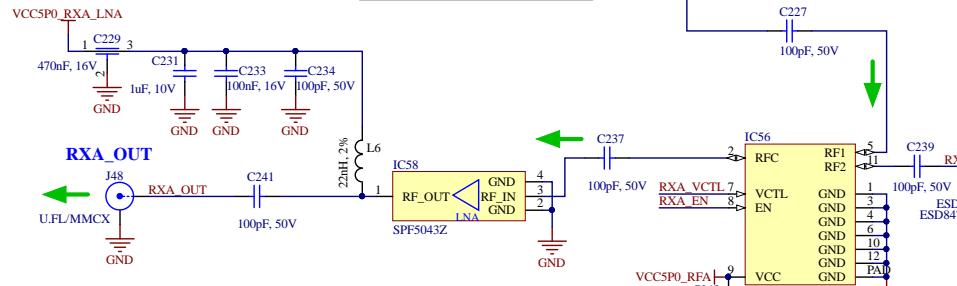
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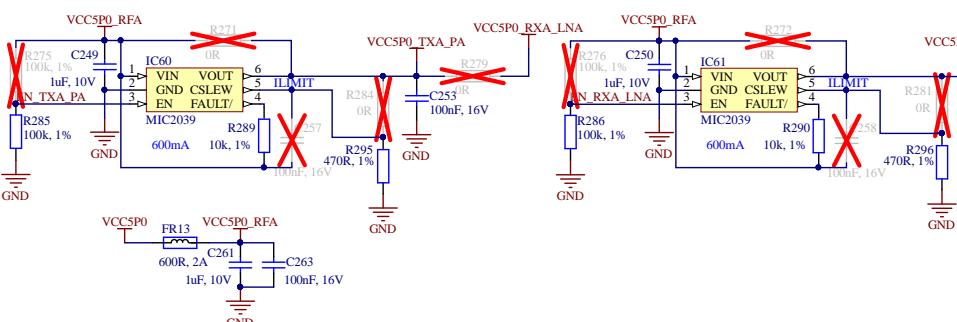
##### RF switches



#### RX LNA



#### Power switches



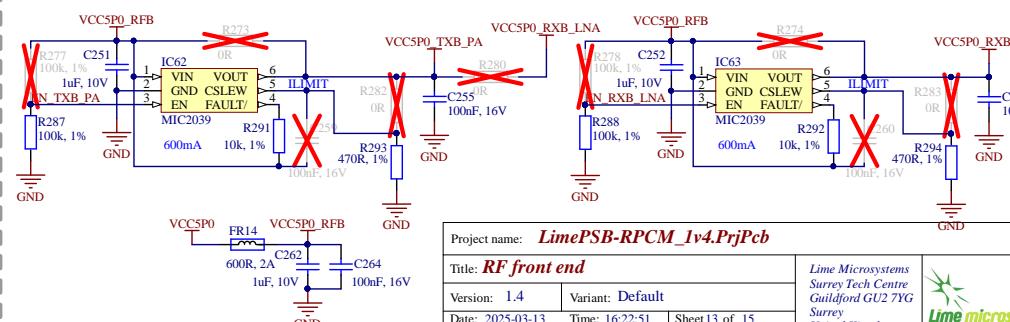
VCCSP0\_RFB → IC62 → LM317 → Power Switch → VCCSP0\_RXB\_LNA

VCCSP0\_RFA → FR13 → VCCSP0\_RFB → Power Switch → VCCSP0\_RXA\_LNA

VCCSP0\_RFB → FR14 → VCCSP0\_RXB\_LNA



#### Power switches



VCCSP0\_RFB → IC62 → LM317 → Power Switch → VCCSP0\_RXA\_LNA

VCCSP0\_RFA → FR13 → VCCSP0\_RFB → Power Switch → VCCSP0\_RXB\_LNA

VCCSP0\_RFB → FR14 → VCCSP0\_RXA\_LNA

Project name: LimePSB-RPCM\_Jv4.PrcPcb

Title: RF front end

Version: 1.4

Variant: Default

Date: 2025-03-13

Time: 16:22:51

Sheet 13 of 15

File: 13\_RFPE.SchDoc

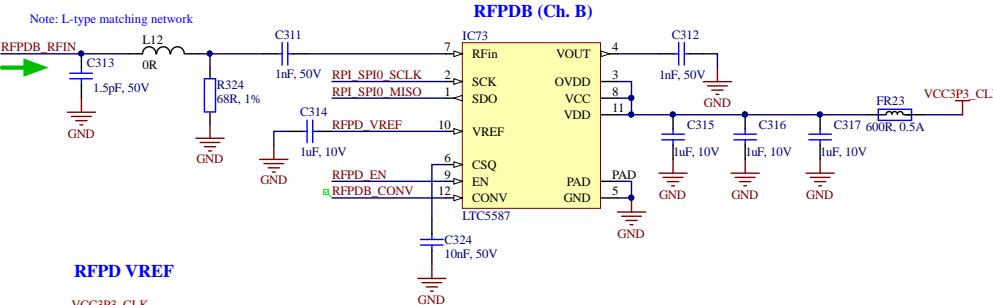
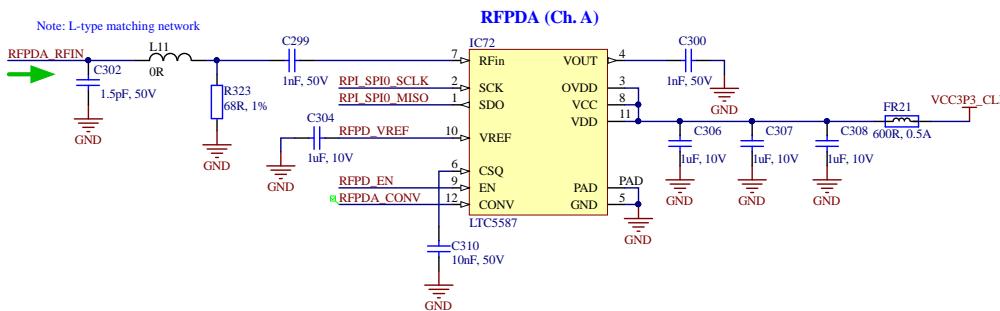
Size: A3

Lime Microsystems  
Survey Tech Centre  
Guildford GU2 7JG  
Survey  
United Kingdom

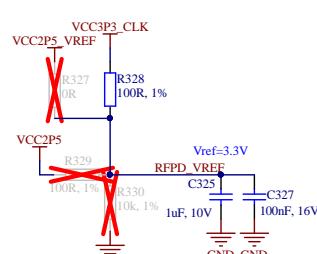


## RF power detectors, PoE and USB PD

### RF power detectors

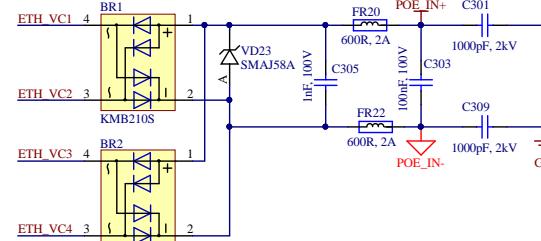


### RFPD\_VREF



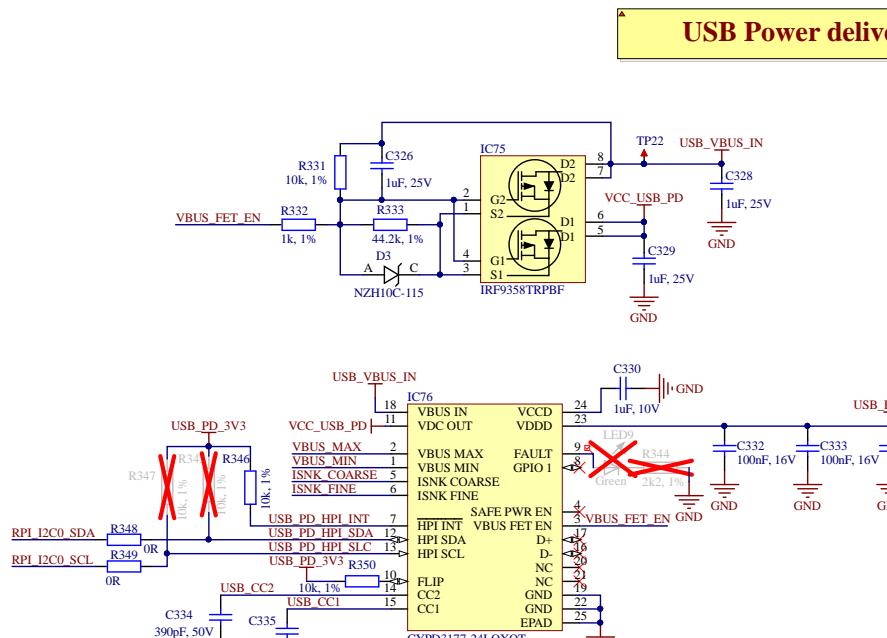
12C Address: [0 0 0 1 0 0 R/W]

### Power over Ethernet

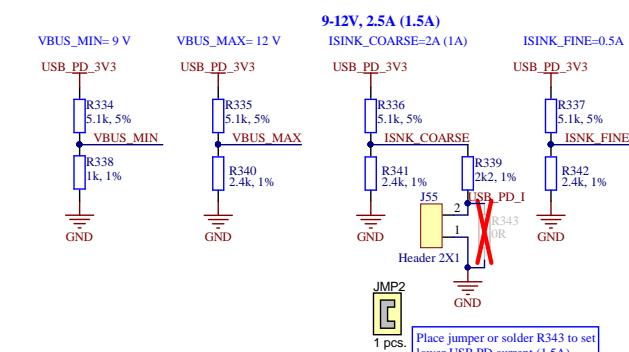


24W continuous output power, 30W peak output power (IEEE802.3at)  
Class 4 IEEE802.3 PD  
IEEE 802.3af (PoE), 802.3at (PoE+) and IEEE802.3bt (Hi-PoE) compliant

### USB Power delivery

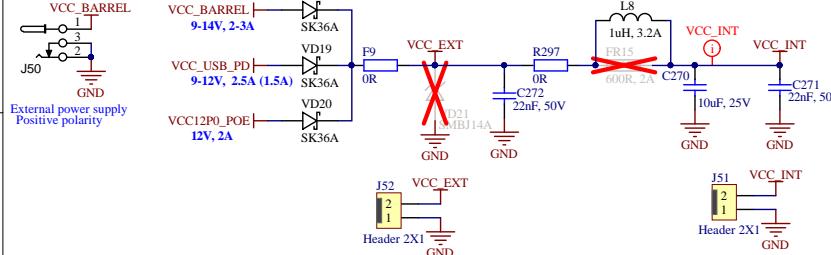


Resistor dividers for selecting VBUS Voltage and Current

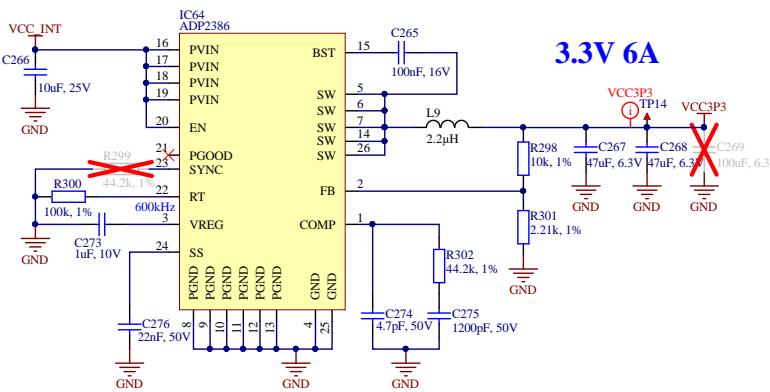


## Board power circuits

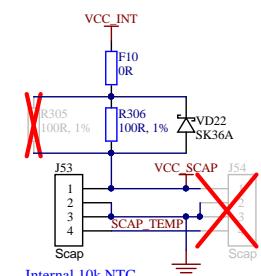
## Power input



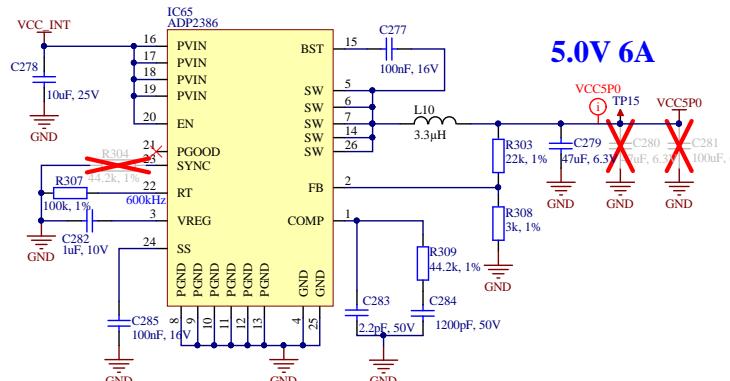
## Switching regulators



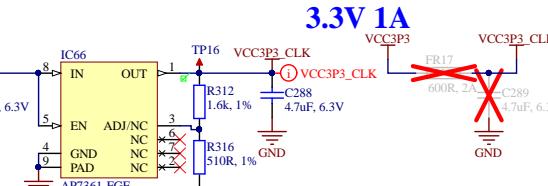
## Supercapacitor



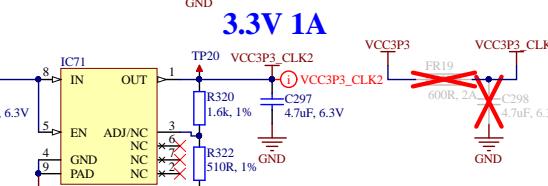
5.0V 6A



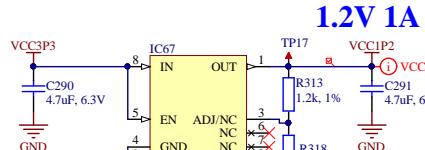
## Linear regulators



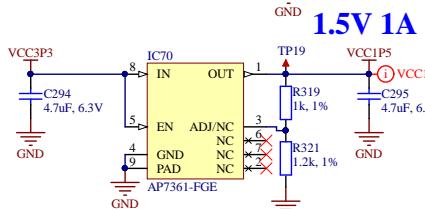
3.3V 1A



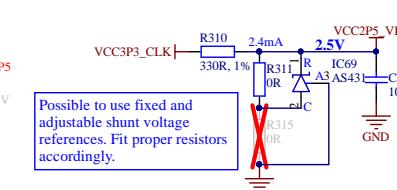
1.2V 1A



5V 1A



## Voltage reference (2.5V)



#### Alternatives for conversion of XODAC and ADPC

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