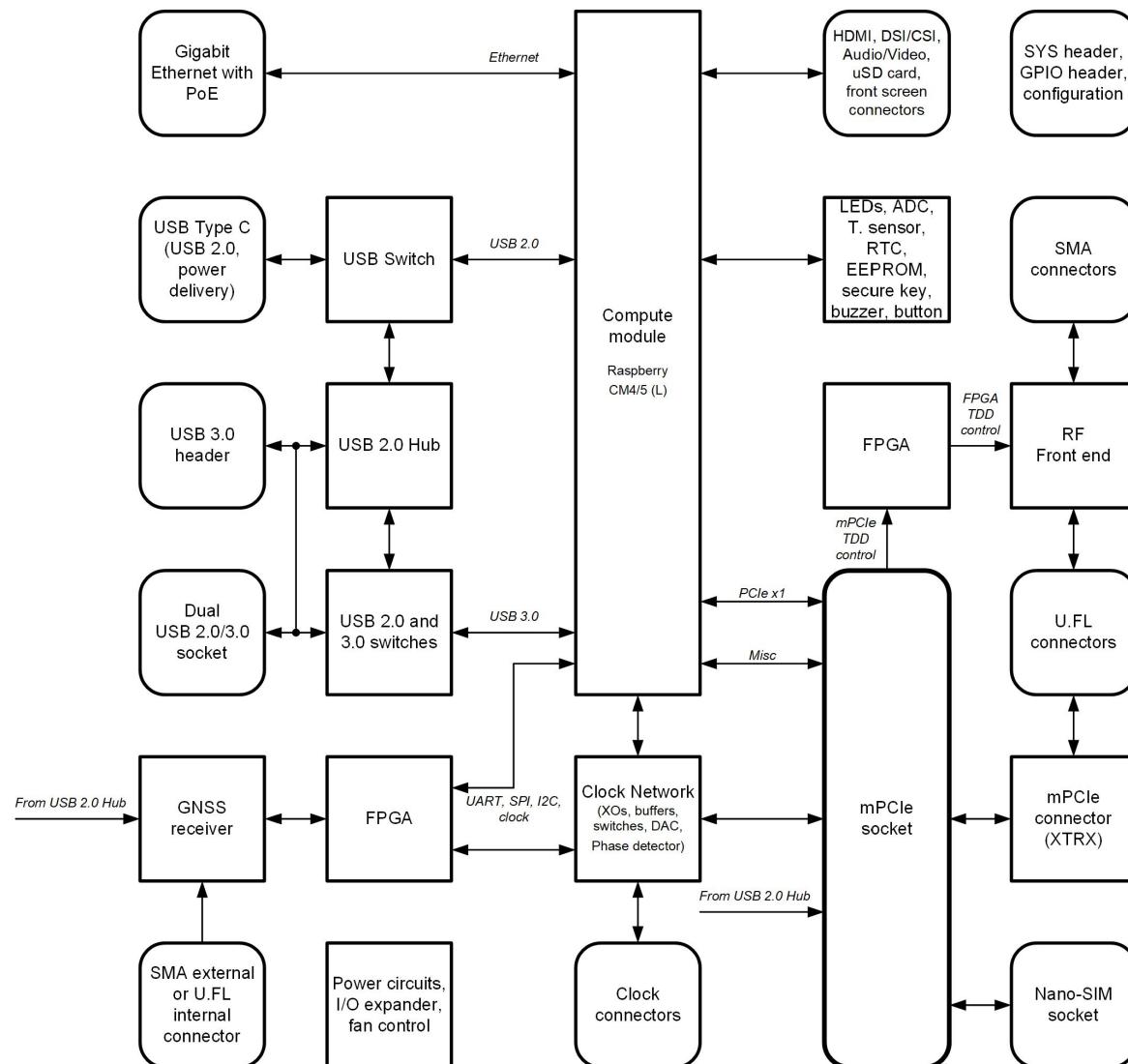


Block diagram



Project name: **LimePSB-RPCM_1v4.PrbPcb**

Title: **Block diagram**

Version: 1.4

Variant: Default

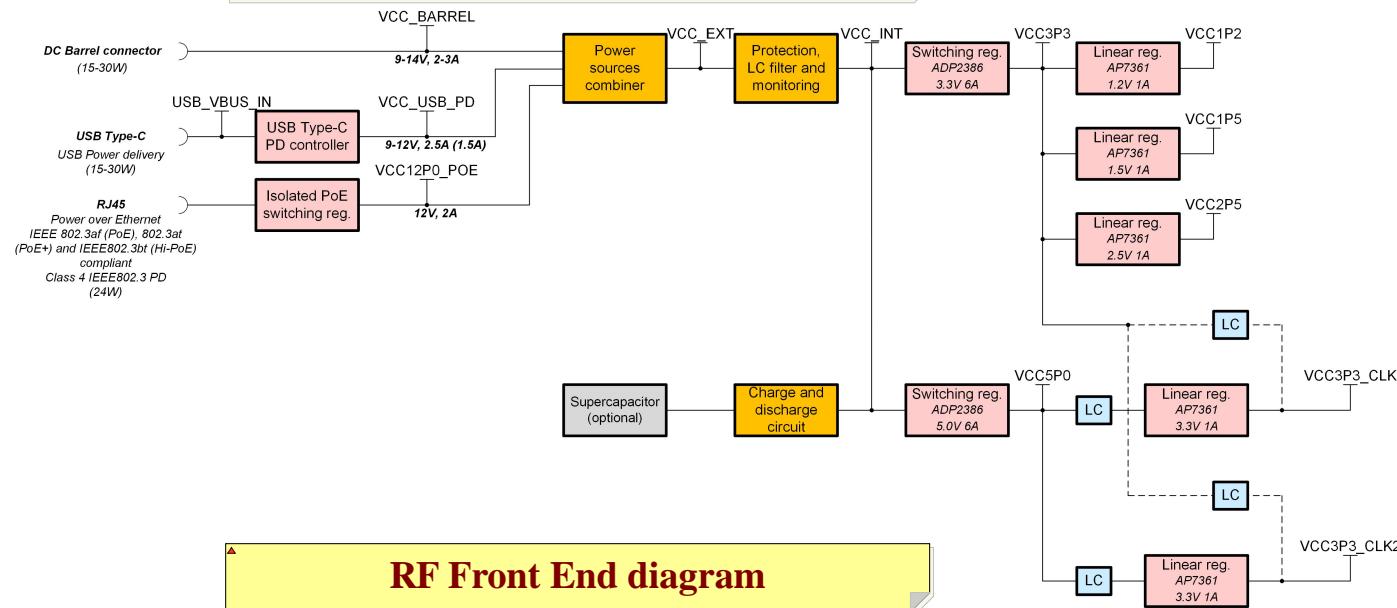
Date: 2025-03-26 Time: 13:43:07 Sheet 1 of 15

File: 01_Block_diag.SchDoc

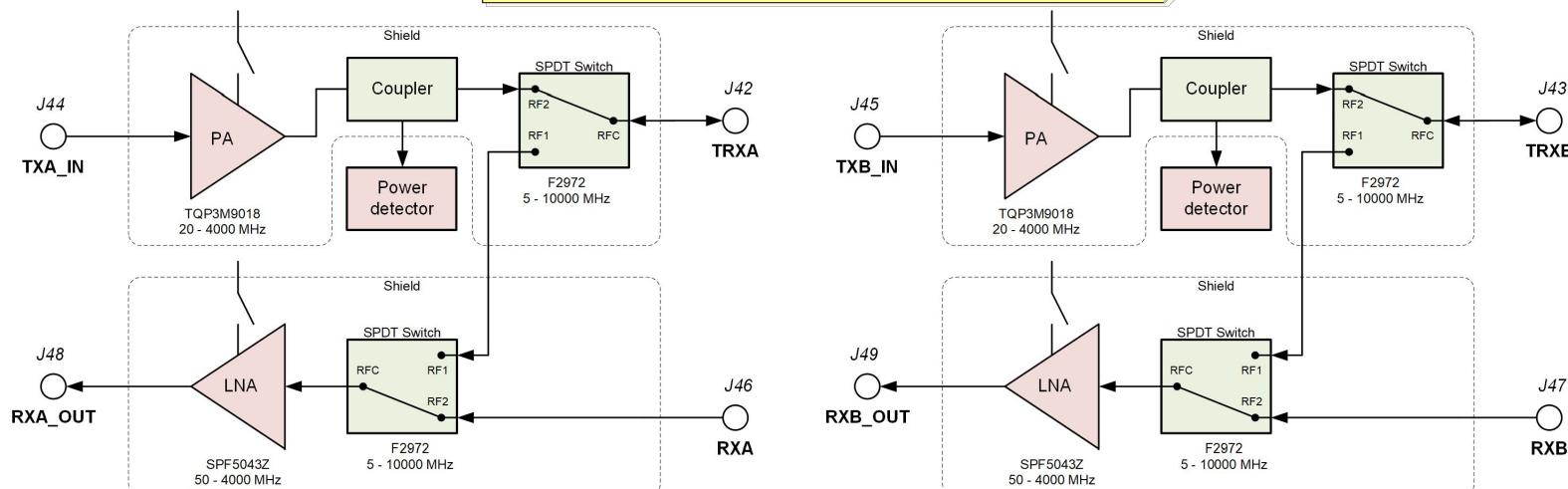
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Surrey
United Kingdom



Power diagram



RF Front End diagram



* All RF switches are controlled by the same signal RF_SW_TDD

Project name: LimePSB-RPCM_1v4.PnjPcb

Title: Power + RF Front End diagram

Version: 1.4 Variant: Default

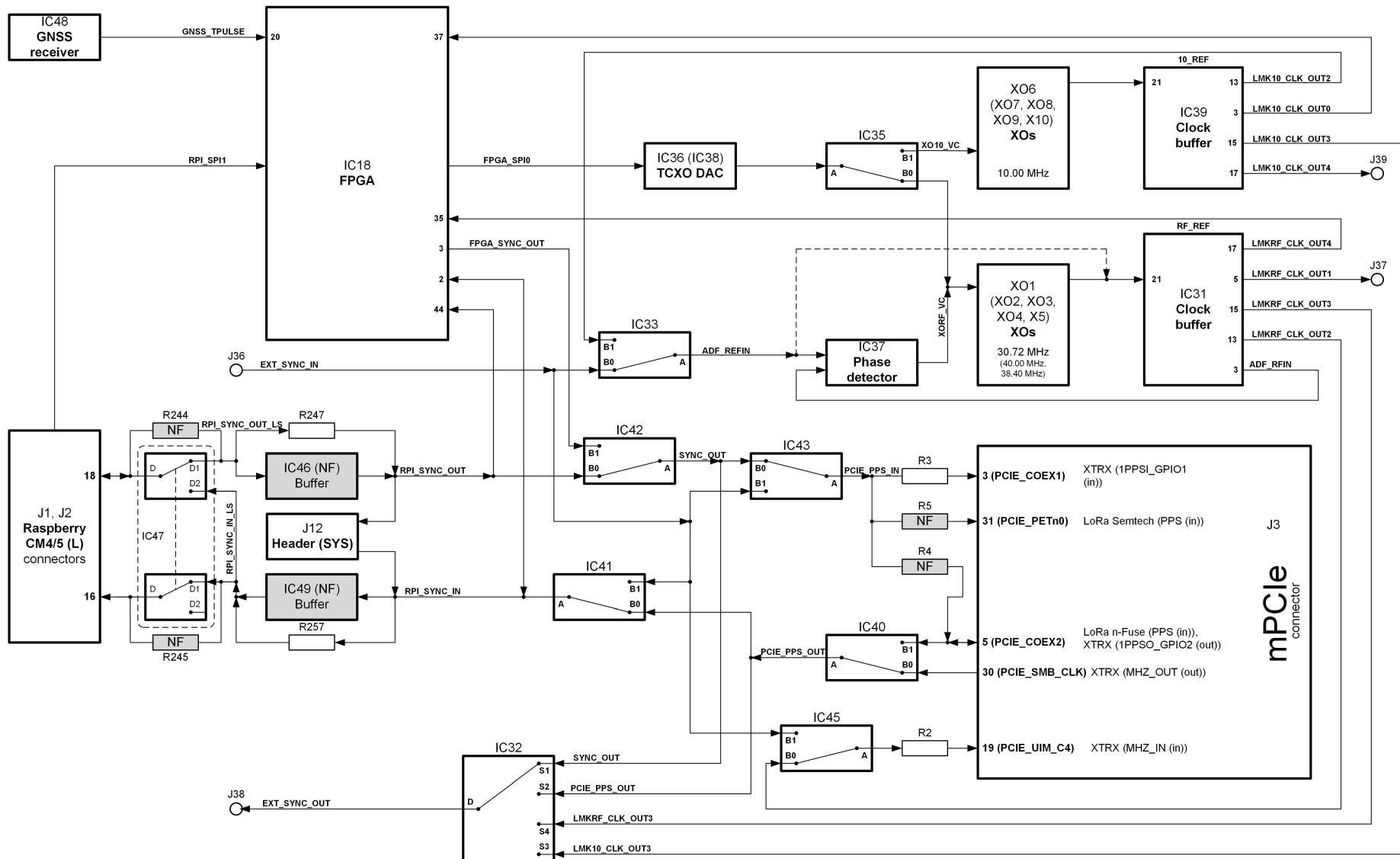
Date: 2025-03-26 Time: 13:43:07 Sheet 2 of 15

File: 02_Power_RFFE_diag.SchDoc Size: A4

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Surrey
United Kingdom



Clock diagram

Project name: **LimePSB-RPCM_1v4.PrbPcb**Title: **Clock diagram**

Version: 1.4 Variant: Default

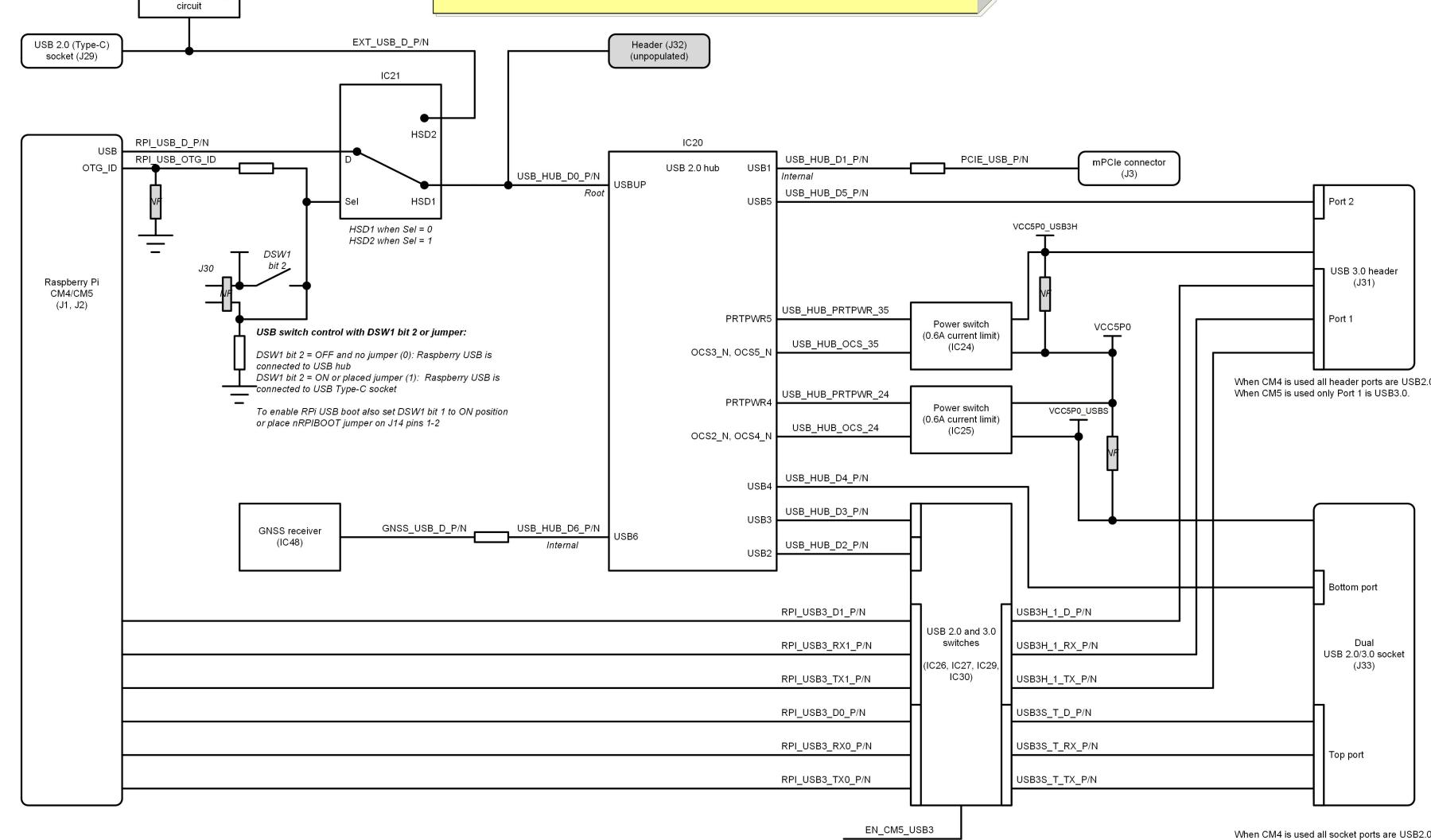
Date: 2025-03-26 Time: 13:43:07 Sheet 3 of 15

File: 03_Clock_diag.SchDoc Size: A4

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Surrey
United Kingdom



USB diagram



Project name: **LimePSB-RPCM_1v4.PpjPcb**

Title: **USB diagram**

Version: 1.4

Variant: Default

Date: 2025-03-26 Time: 13:43:07 Sheet 4 of 15

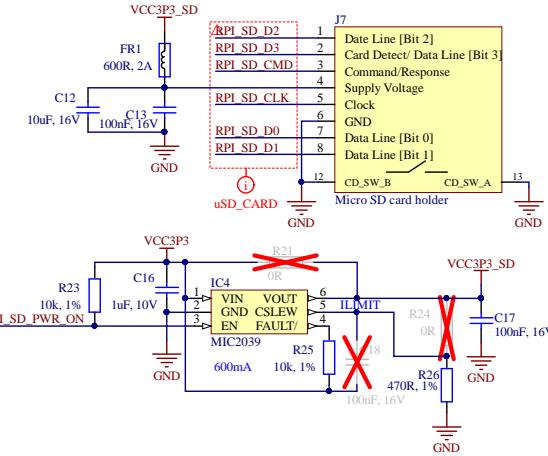
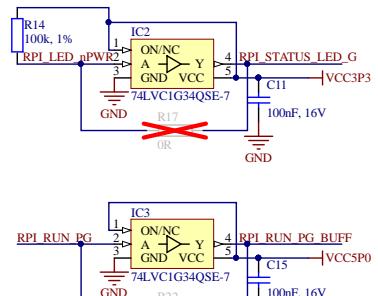
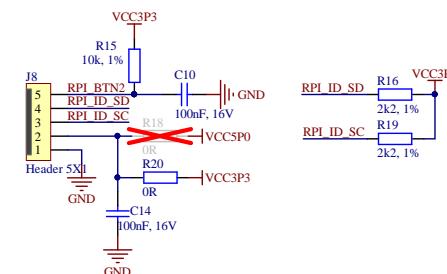
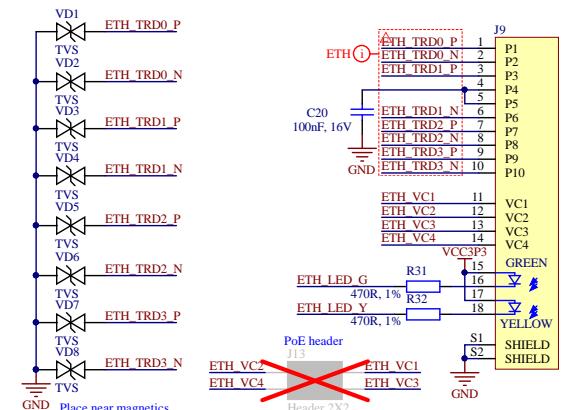
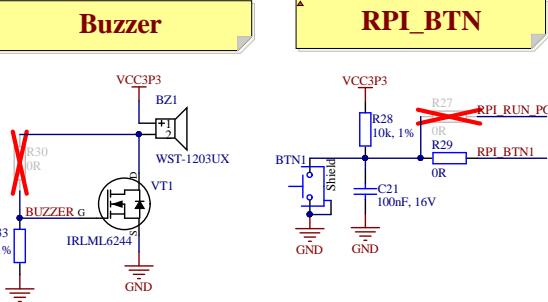
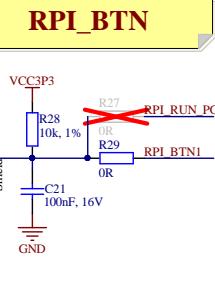
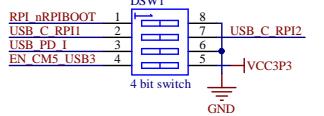
File: 04_USB_diag.SchDoc Size: A4

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Misc 1**uSD card socket**

Only for CM4L and CM5L with no on-board Flash (eMMC)

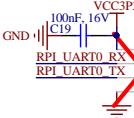
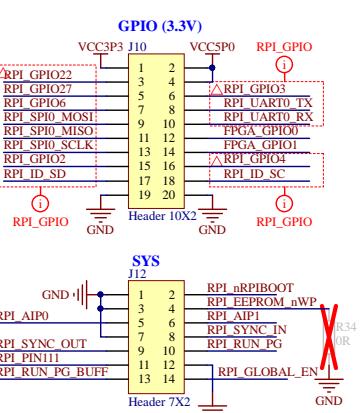
**Buffers, level converters****Front screen I2C + BTN****Gigabit Ethernet (RJ45) connector****Buzzer****RPI_BTN****DIP switch**

Bit 1: RPi boot source:
OFF: RPi boots from eMMC/uSD (default).
ON: Booting from eMMC will be stopped and booting will be transferred to RPi boot which is via USB.

Bit 2: RPi USB 2.0 port mux control:
OFF: RPi USB is connected to USB hub (default).
ON: RPi USB is connected to USB C connector.

Bit 3: USB C/PD current configuration:
OFF: I=2.5A (default).
ON: I=1.5A.

Bit 4: Enable CMS USB3 ports:
OFF: all ports are connected to USB 2.0 hub (for CM4).
ON: USB header Port 1 and USB socket Top port are connected to CM5 USB3.0 lines (for CM5). Also this line controls RPI_PIN111 mux.

GPIO ans SYS headers

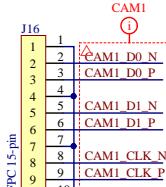
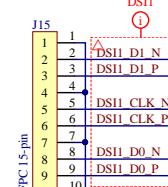
nRPI_BOOT: During boot if this pin is low booting from eMMC will be stopped and booting will be transferred to rpi boot which is via USB. Place jumper on pins 1-2.

EEPROM_nWP: can be grounded to prevent writing to the on board EEPROM which stores the bootcode. Place jumper on pins 3-4 or solder R32.

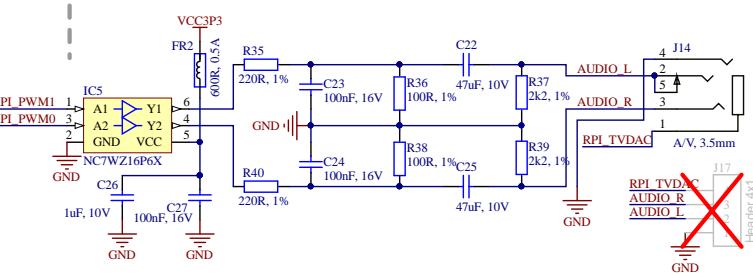
A button between pins 13-14 can be used to wake up compute node from power down.

RUN_PG pin when high signals that the CM4 has started. Driving this pin low resets the module.

A button between pins 10-12 replicates the power button on Raspberry Pi 5. A short press signals that the device should wake up or shut down. A long press forces shutdown.

LVDS (Camera + Display)**Camera 1****Display 1**

For CM5 CAM1 and DSII signals become dual-purpose and can be used for either a CSI camera or a DS1 display.

Analog audio + Composite video out

Project name: **LimePSB-RPCM_Iv4.PrbPcb**

Title: **Misc 1**

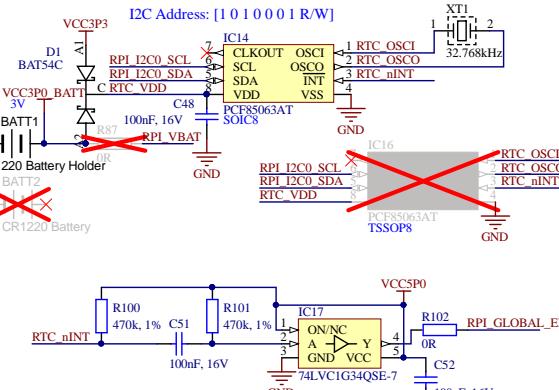
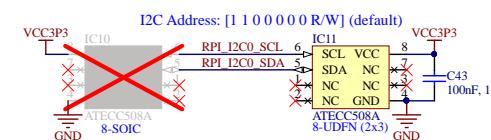
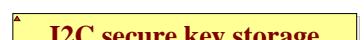
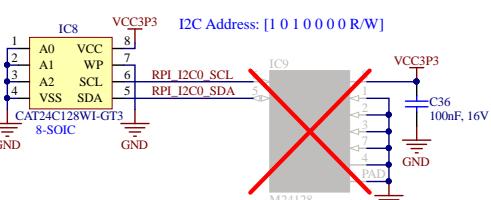
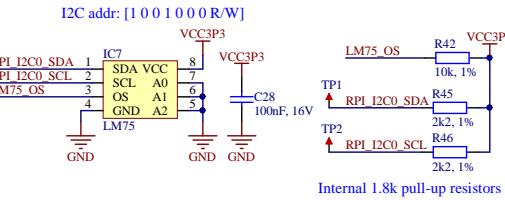
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Guildford GU2 7TG
Surve
United Kingdom



Version: 1.4 Variant: Default

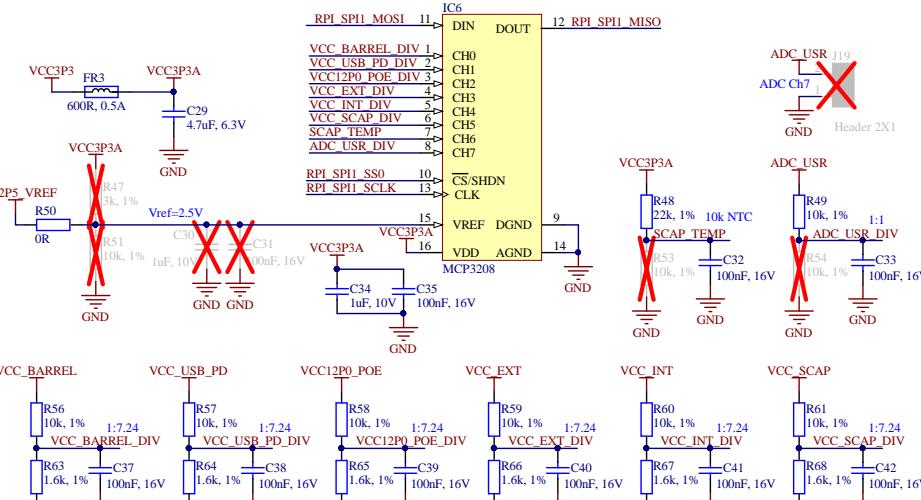
Date: 2025-03-26 Time: 13:43:08 Sheet 6 of 15

File: 06_Misc 1.SchDoc Size: A3

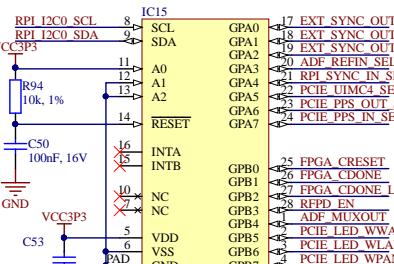
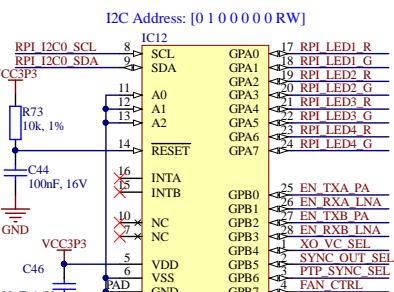


Misc 2

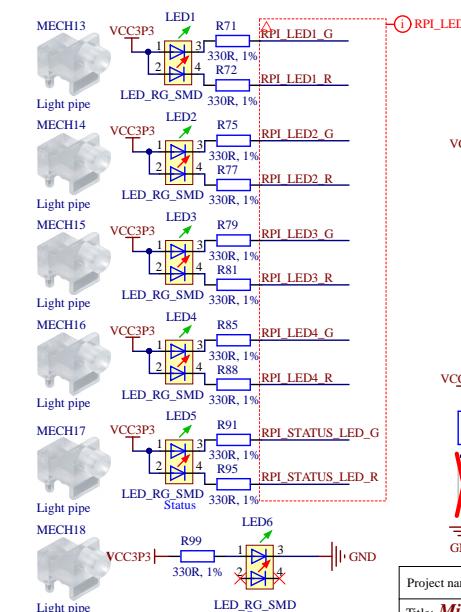
SPI ADC



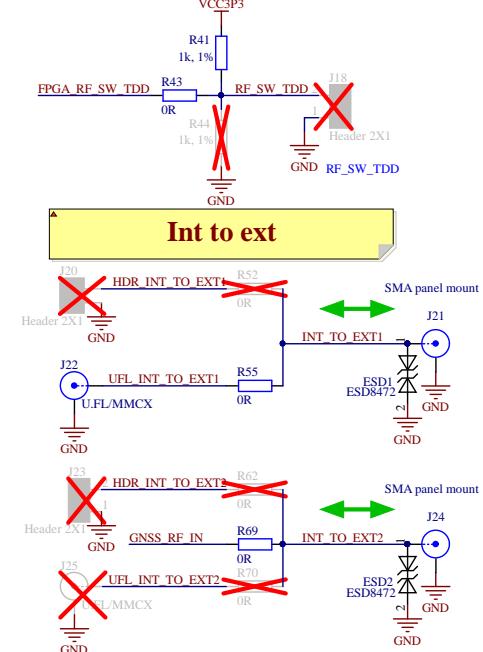
I2C I/O expanders



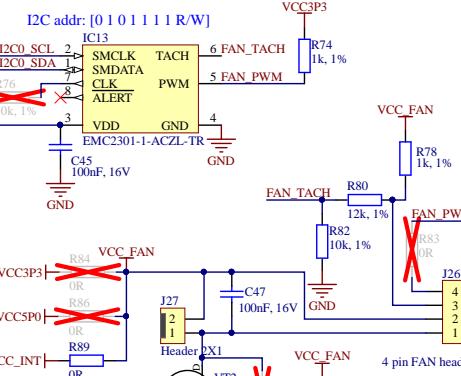
Raspberry Pi LEDs



RFFE TDD control



FAN control



Project name: **LimePSB-RPCM_1v4.PrjPcl**

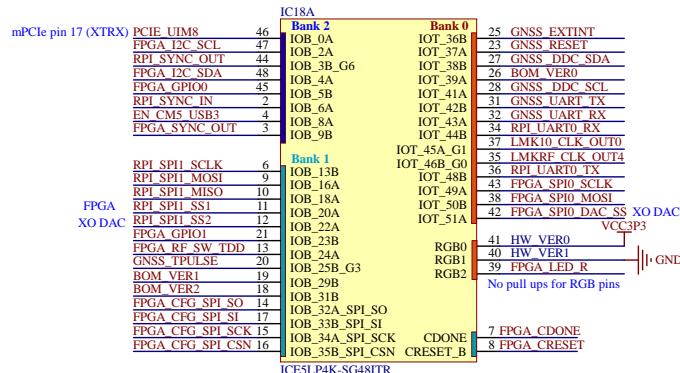
Title: *Misc 2*

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Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom*

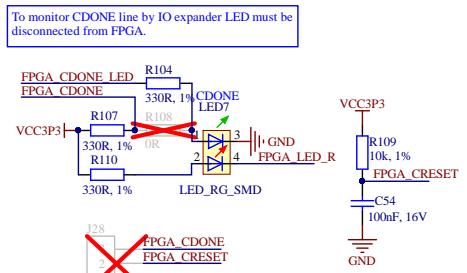


FPGA

FPGA

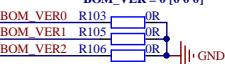


FPGA misc



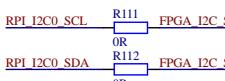
HW_VER, BOM_VER

HW_VER = 1 [0 1]
BOM_VER = 0 [0 0 0]

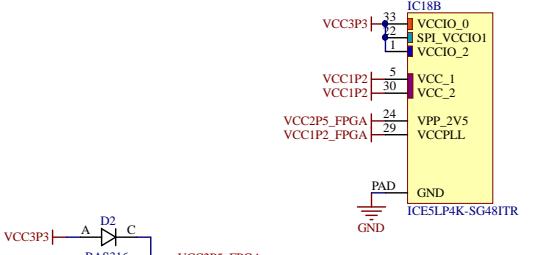


I2C interconnections

Raspberry I2C0 and FPGA I2C interconnections



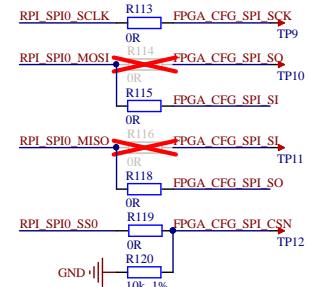
FPGA power



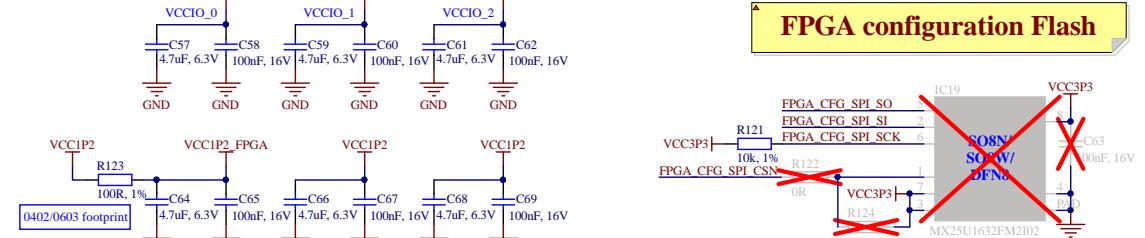
FPGA configuration modes

Slave SPI (default):	R113 fit
	R114 NF
	R115 NF
	R116 NF
	R117 fit
	R118 fit
	R119 fit
	R120 fit
	R122, R124, IC19, C63 fit

Master SPI:	R113 fit
	R114 fit
	R115 NF
	R116 fit
	R117 fit
	R118 fit
	R119 fit
	R120 NF
	R122, R124, IC19, C63 fit

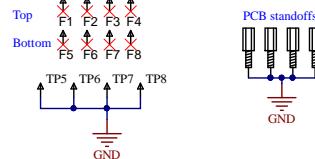


FPGA configuration Flash



Misc

Fiducials



Misc for FAN

FANI



12V DC FAN



2-pin header



Crimp



Crimp



Screw (M3, 20 mm)



Screw (M3, 20 mm)



Screw (M3, 20 mm)



Spacer (M3, 12mm)



Spacer (M3, 12mm)



Spacer (M3, 12mm)



Screw (M3, 6 mm)



Screw (M3, 6 mm)



Screw (M3, 6 mm)

Buy packs of 100 pcs. by dividing the required amount by 100 and rounding the resulting number to whole packs.

Project name: LimePSB-RPCM_Jv4.PrfPcb

Title: **FPGA**

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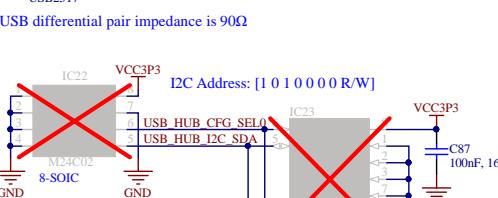
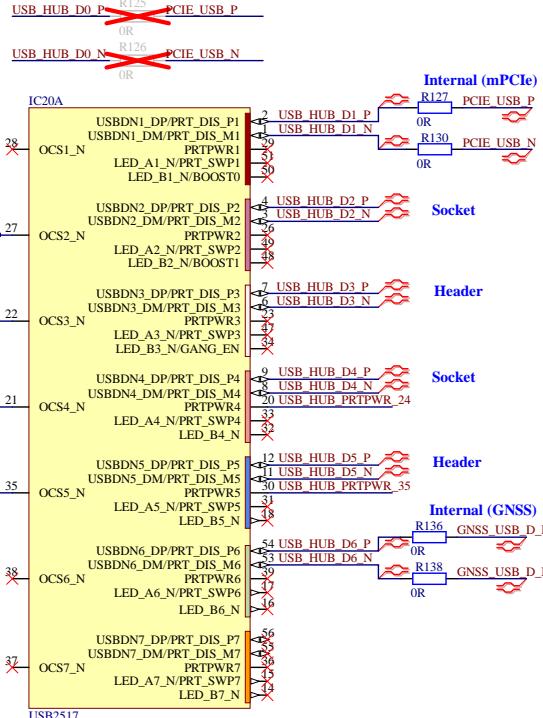
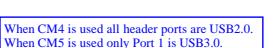
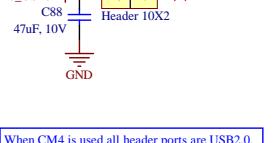
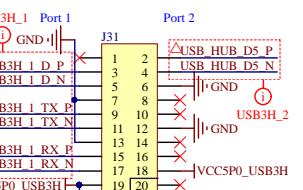
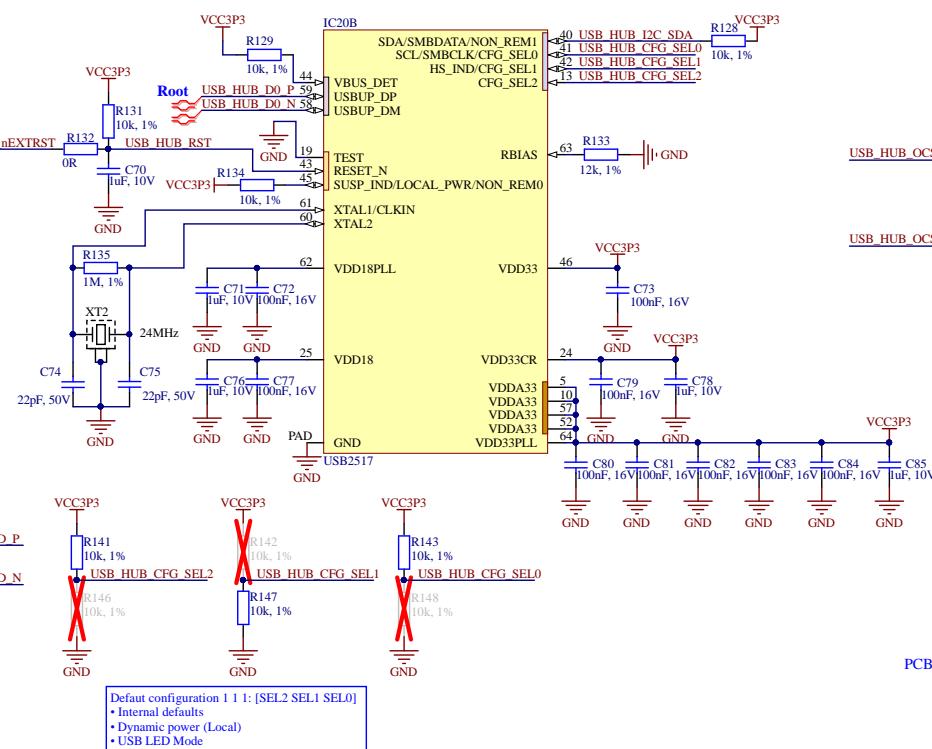
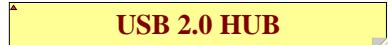
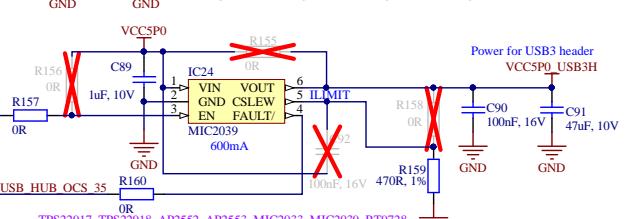
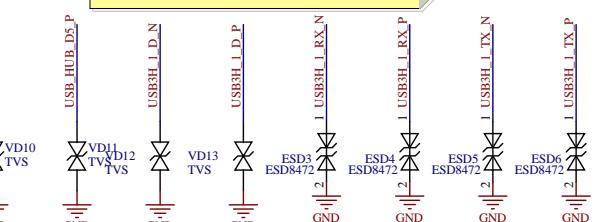
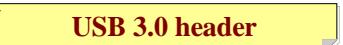
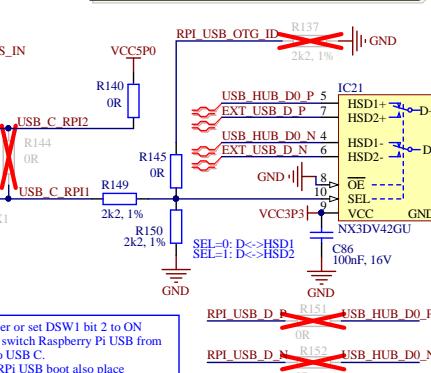
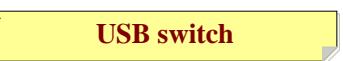
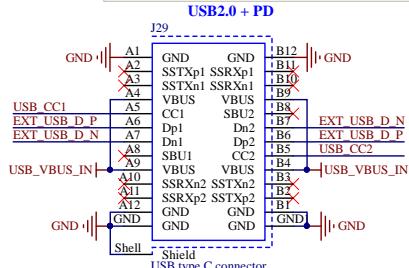
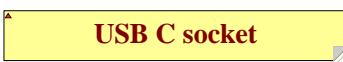
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Survey
United Kingdom



Version: 1.4 Variant: Default

Date: 2025-03-26 Time: 13:43:08 Sheet 8 of 15

File: 08_FPGA.SchDoc Size: A3

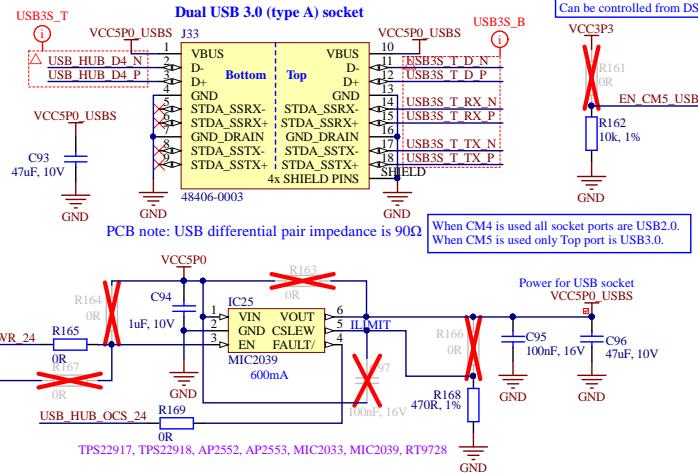


Ergonomics

Project name:	LimePSB-RPCM_Iv4.PrjPcb		
Title:	USB 2.0 hub		
Version:	1.4	Variant:	Default
Date:	2023-03-26	Time:	13:43:09
Sheet	9	of	15
Filesize:	90.15MB	Job ID:	S10000000000000000000000000000000

USB and HDMI sockets

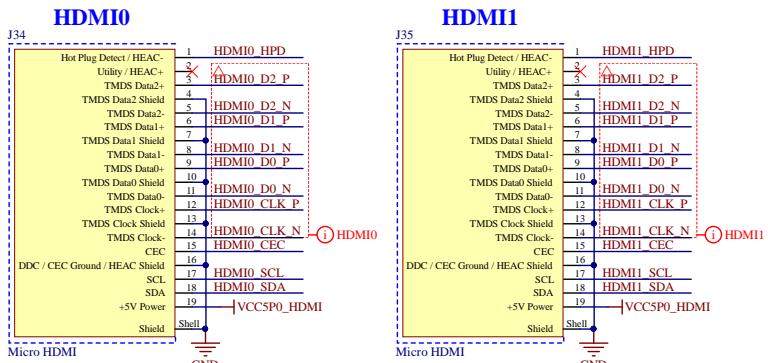
Dual USB 3.0 (type A) socket



EN_CM5_USB3: Enable CM5 USB3 ports:
0: all ports connected to USB 2.0 hub (for CM4)
1: USB header Port 1 and USB socket Top port are
connected to CM5 USB3.0 lines (for CM5).
Also this line controls RPI-PIN111 mux.
Can be controlled from DSW1 Bit 4.

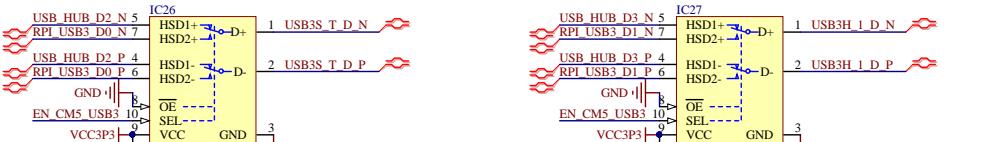
HDMI sockets

Micro (Type D) HDMI sockets

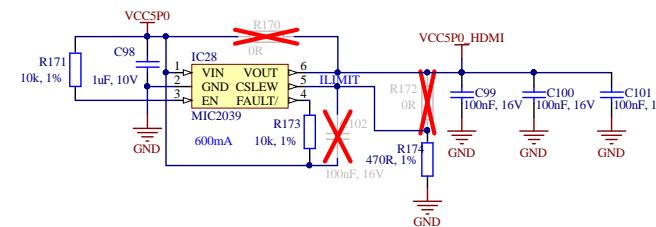


PCB note: make each HDMI group differential traces length equal and impedance of 100Ω

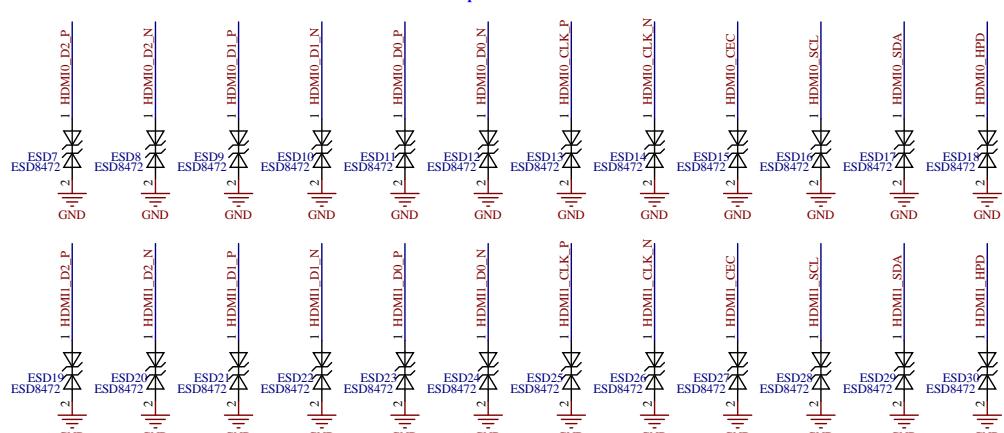
USB 2.0 and 3.0 switches



Power for HDMI sockets



ESD protection for CMS

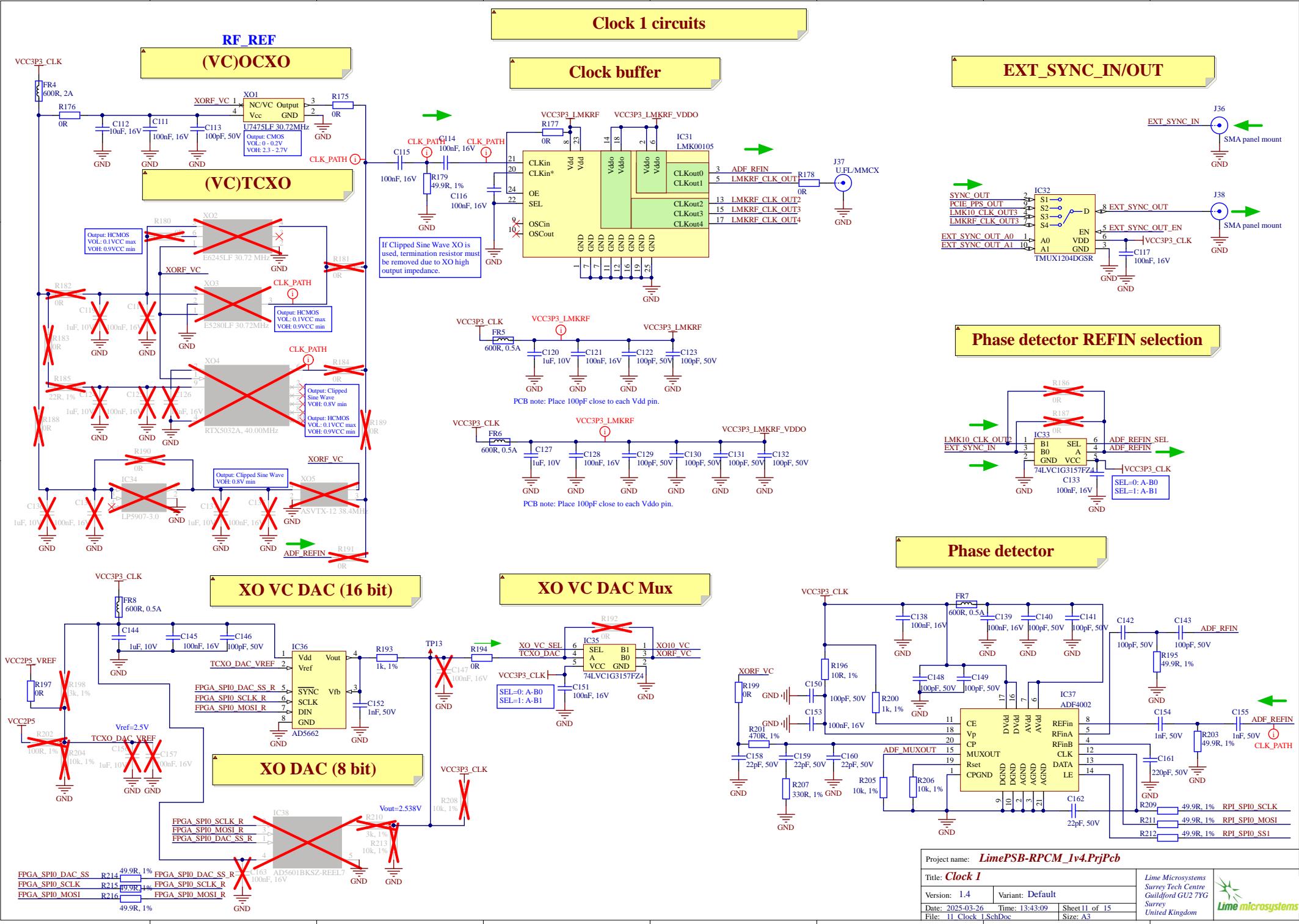


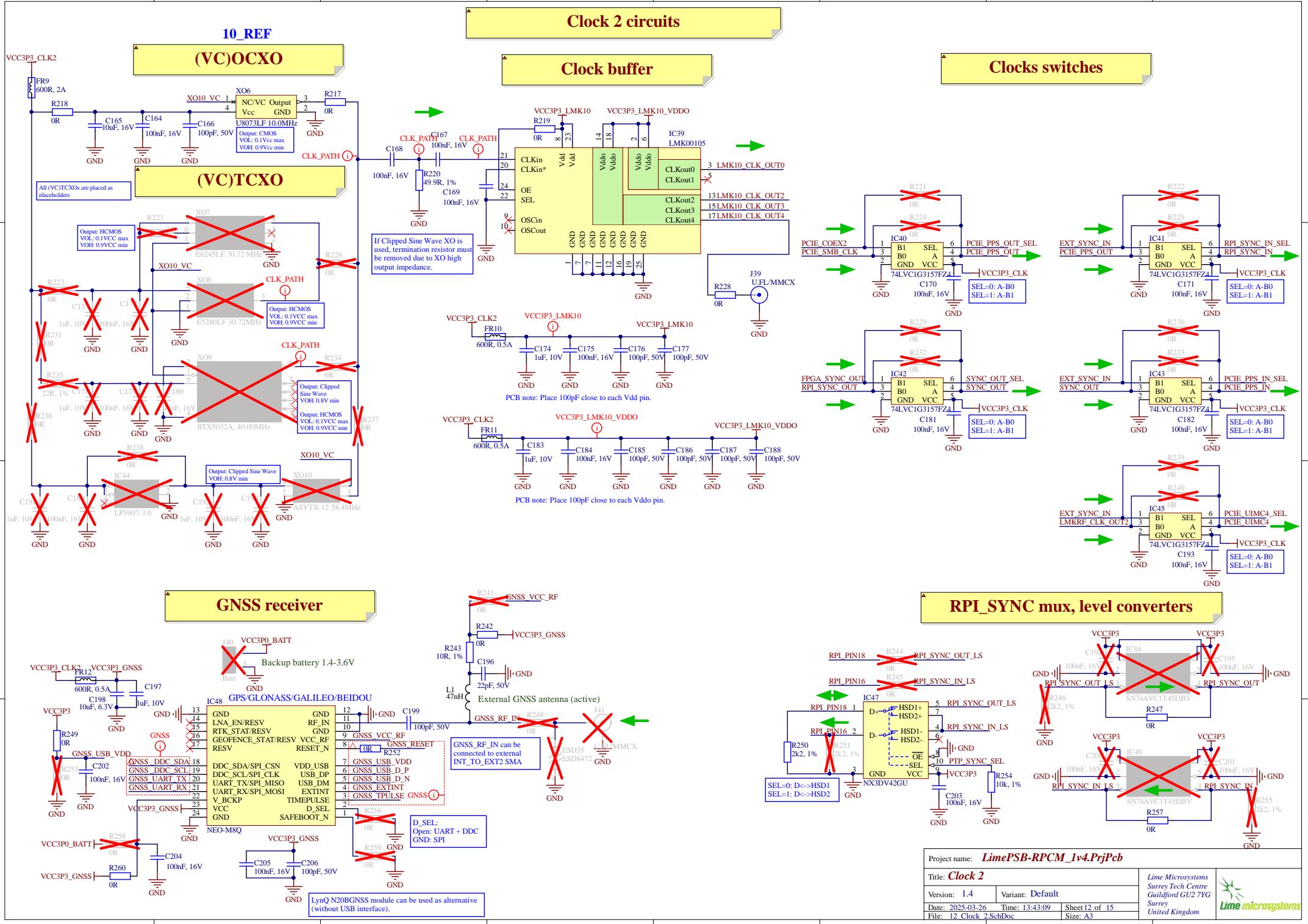
Project name: **LimePSB-RPCM_1v4.PrjPcb**

Title: *USB and HDMI sockets*

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Guildford GU2 7YG
Surrey
United Kingdom*

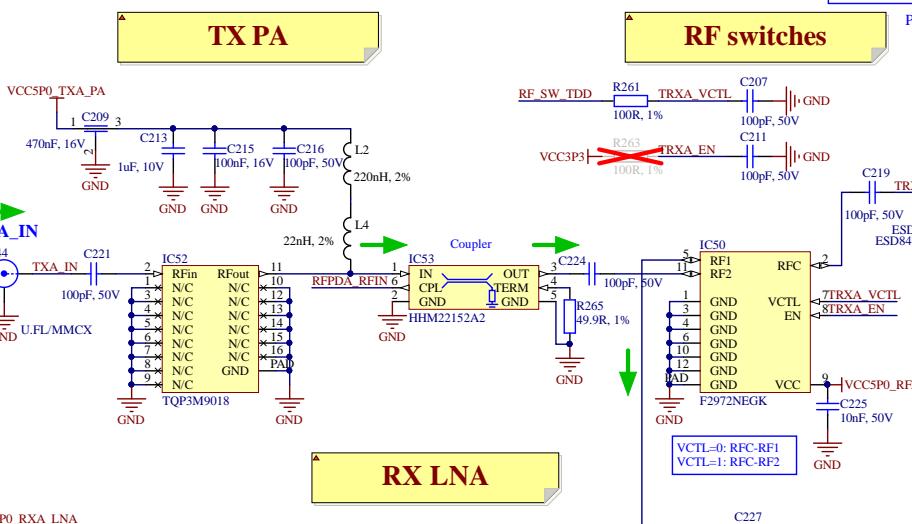




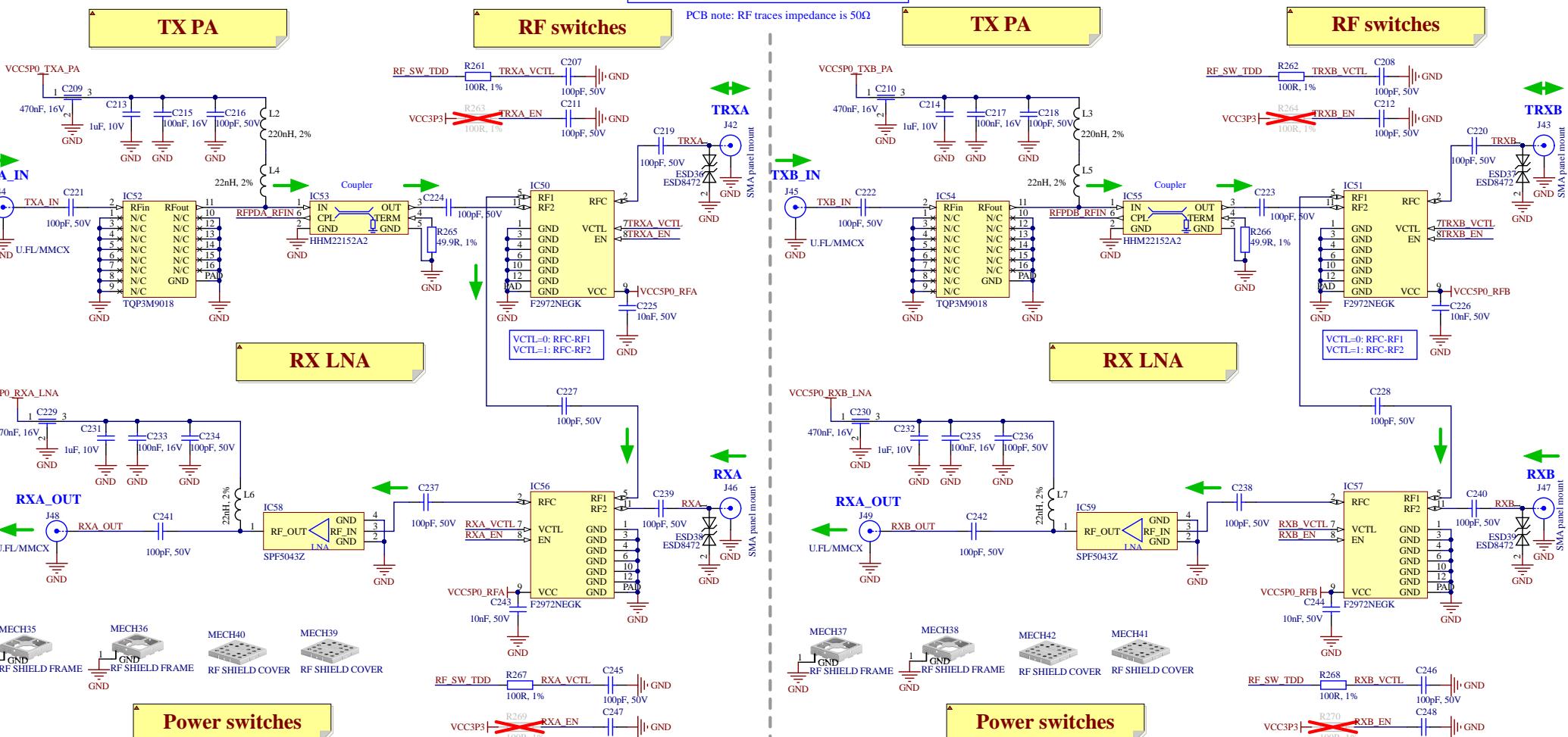


RF front end

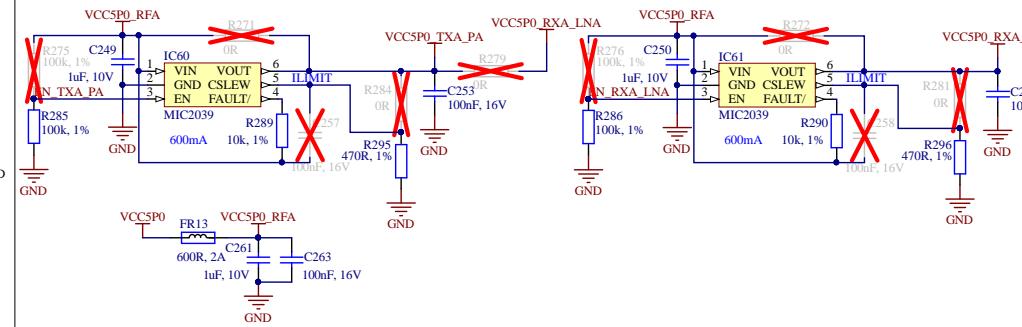
Channel A



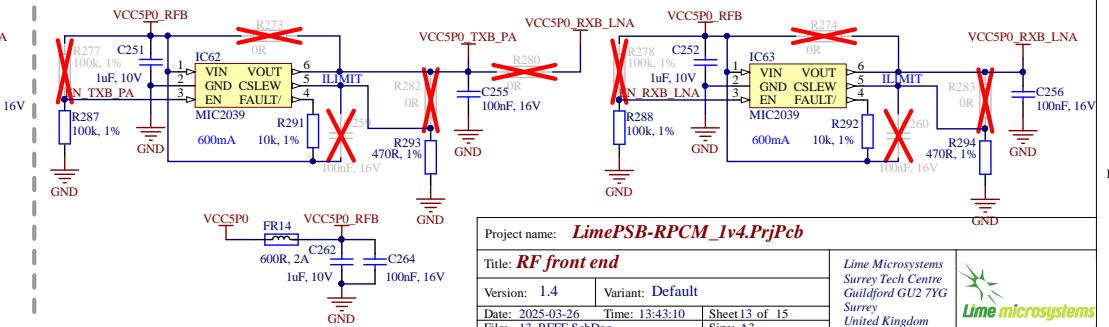
Channel B



Power switches



Power switches



Project name: LimePSB-RPCM_Jv4.PrcPcb

Title: RF front end

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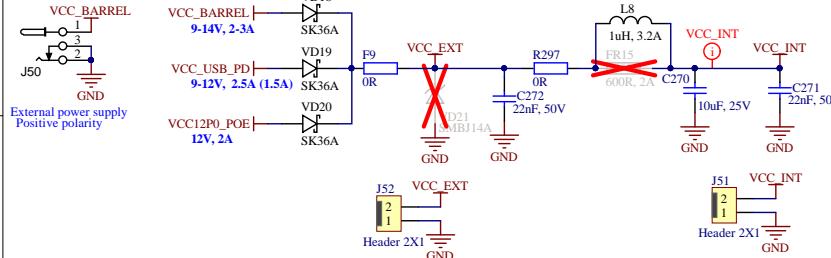
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Date: 2025-03-26 Time: 13:43:10 Sheet 13 of 15
File: 13_RFPE.SchDoc Size: A3

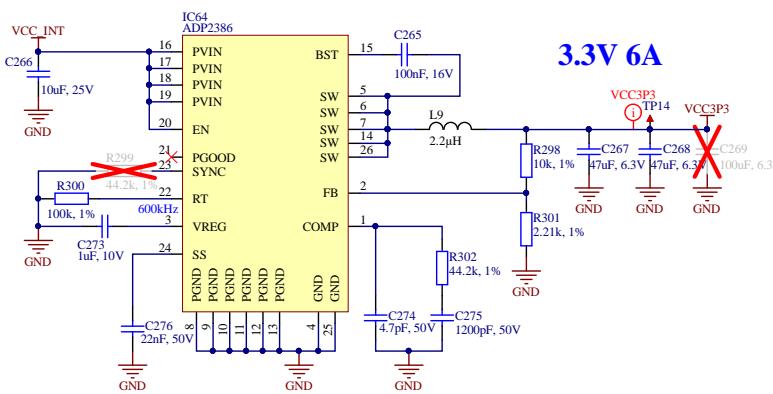


Board power circuits

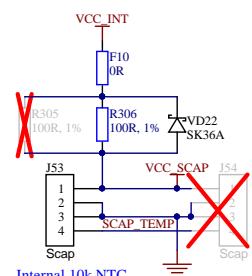
Power input



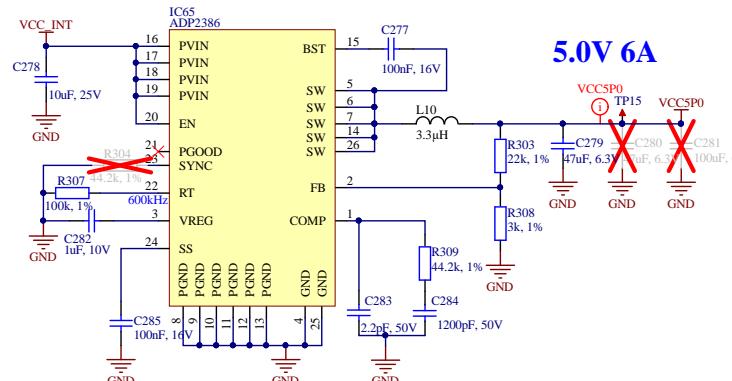
Switching regulators



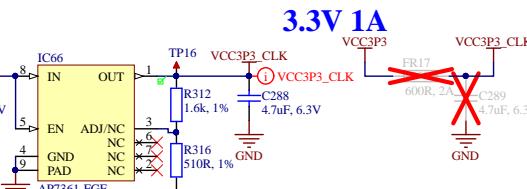
Supercapacitor



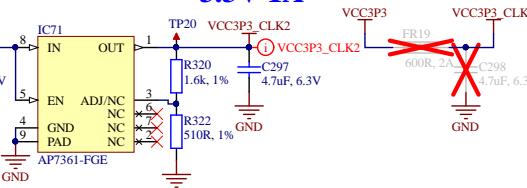
5.0V 6A



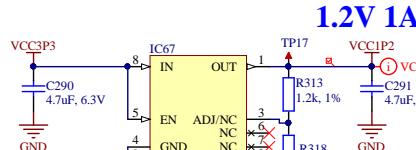
Linear regulators



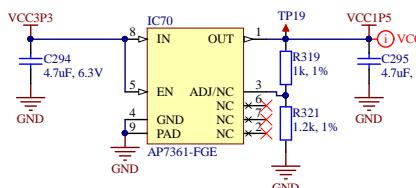
3.3V 1A



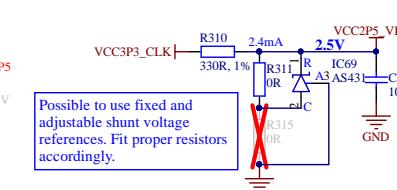
1.2V 1A



5V 1A



Voltage reference (2.5V)



Alternatives for protection of XODAC and ADPC

Optional 2.5V regulator for FPGA NVCM
programming/configuration and X0/DAC reference