

ne microsustems

LimeKEY RPCM v1.0

Lin	ne microsystems												
CONTROLLED IMPEDANCE				STACKUP AND LAYER DESCRIPTION									
GENERAL PARAMETERS													
Parameter Layer/Layers Value													
Сорг	per foil thickness	Тор	17.5um										
Diel	ectric thickness between layers	Top-L2	173um (6.8 mils)										
Diel	ectric permittivity between layers (Er)	<u> </u>	4.2										
	per foil thickness	Bottom	17.5um										
	ectric thickness between layers	Bottom-L5	173um (6.8 mils)	GERBER LAYER N	AMEC.				TH vi	a			
niei	ectric permittivity between layers (Er)		4.2	GTP Top solder paste					Top-B	ot			
	CALCULATIONS			GTO Silkscreen GTS Soldermask (halogen free)	PP 6.8mil (173um) IT180A: 1086X1+2113X1						ELECTRICAL LAYERS:		
	Target impedance Single-ended 50R		G∣∟ 0.5oz+plating						·	Top: RF//PWR/GND			
	Additional comments Top layer, no side GND plane		G1 1oz (35um) G2 1oz (35um)	CORE 10mil (250	CORE 10mil (250um) IT180A: 2116X2				L2: GN	L2: GND L3: Signal/PWR/GND L4: PWR/Signal/GND			
(Top)			G3 1oz (35um) PP 18mil (4										
	Track width Top layer copper foil thickness	0.325 mm (12.795 mils) 173um (6.8 mils)		G4 1oz (35um)	CORE 10mil (250um) IT180A: 2116X2 PP 6.8mil (173um) IT180A: 1086X1+2113X1					L5: GN			
 	Dielectric thickness between layers	17 30111	173um (6.8 mils)	GBL 0.5oz+plating GBS Soldermask (halogen free)	PP 6.8m11 (17)	OMII (1/3UM) IIIOUM: IUSOXI+ZII3XI				Bottom	Bottom: RF/Signal/PWR/GND		
	Dielectric permittivity between layers (Er)	Top-L2	GL	GBO (halogen free) GBO Silkscreen GBP Bottom solder pa							ADDITIONAL LAYERS:		
	Approximate microstrip line impedance	49.99 Ohms (+/	49.99 Ohms (+/- 10% tolerance)		Total PCB thicknes: 1.6mm +/- 10%. Via type #1				0.2mm dr 0.4mm ri	111	Mechanical 1: Board cutout ASM TOP: Assembly top ASM BOT: Assembly bottom Mechanical 13: Component 3D body		
	Target impedance	Differential 100R		1									
	Additional comments		Top layer, no side GND plane								Notes: Board shape and frame		
HDMI (Top)	Top layer copper foil thickness	17.5 um 0.2 mm (7.874 mils) 0.14 mm (5.511 mils)											
	Track width			1									
	Track spacing			1									
	Top layer copper foil thickness	173um ((6.8 mils)	1									
	Dielectric thickness between layers	Tan-1 2	173um (6.8 mils)	1									
	Dielectric permittivity between layers (Er)	Top-L2	4.2										
	Approximate microstrip line impedance	100.6 Ohms (+/- 10% tolerance)		1									
				VERY IMPORTA									
			GENERAL PO				ADDITIONAL			REQUIREMENTS			
				Minimum copper to copper spacing Minimum track width		O.1mm (3.9mil) O.1mm (3.9mil)		● Electrical test : 100 % netlist.					
				PCB thickness									
				PUB thickness		1.6mm +/-10%. IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)		 Boards are to be individually bagged. PCB vendor to silkscreen UL and RoHS complication 			ually bagged.		
				PCB material							nd RoHS compliance marks, vendor		
						External layer 0.5 oz+plating		_	and date code oill be placed		bottom where shown (ignore if none of th		
				Copper weight		Internal layer 1 oz Assemb		ssembly note: Assembly house MUST provide notes in					
						DARK BLUE					were any changes during assembly and the 100% according to BOM and P&P files.		
					Solder mask				ote example: Initial BOM C		`urrent		
		Solder mask		Halogen fre	e	Part		PCB status	Comment				
						Glossy finish (NO		R1 IC5	FIT FIT	1	Not mounted due to bad footprin		
						White epoxy :		100		INF	Not mounted due to part shortage		
Si		Silkscreen		Both sides Halogen fre									
							n pads						
Но			Hole types on the PCB and information		Hole diameters are f manufactured diamete								
	Ro		Route process			b route 🔀							
					V-score and tab route								
			Panel		Yes HASL lead free	No 🔀							
			Surface finish (both sides)		HASL with lead Immersion gold 0.05-0.10um 2.50-5.00um	of gold over							
			og race itilizii (DO(U	or face fillish (Doth Sides)		of nickel							
						OSP Hard gold							