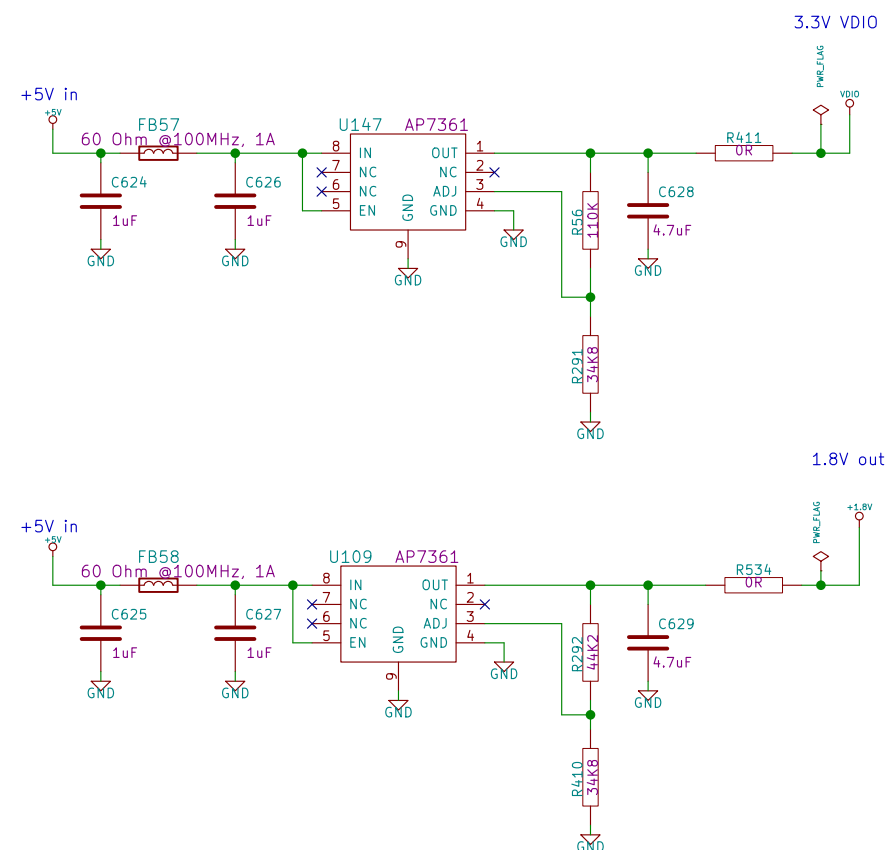
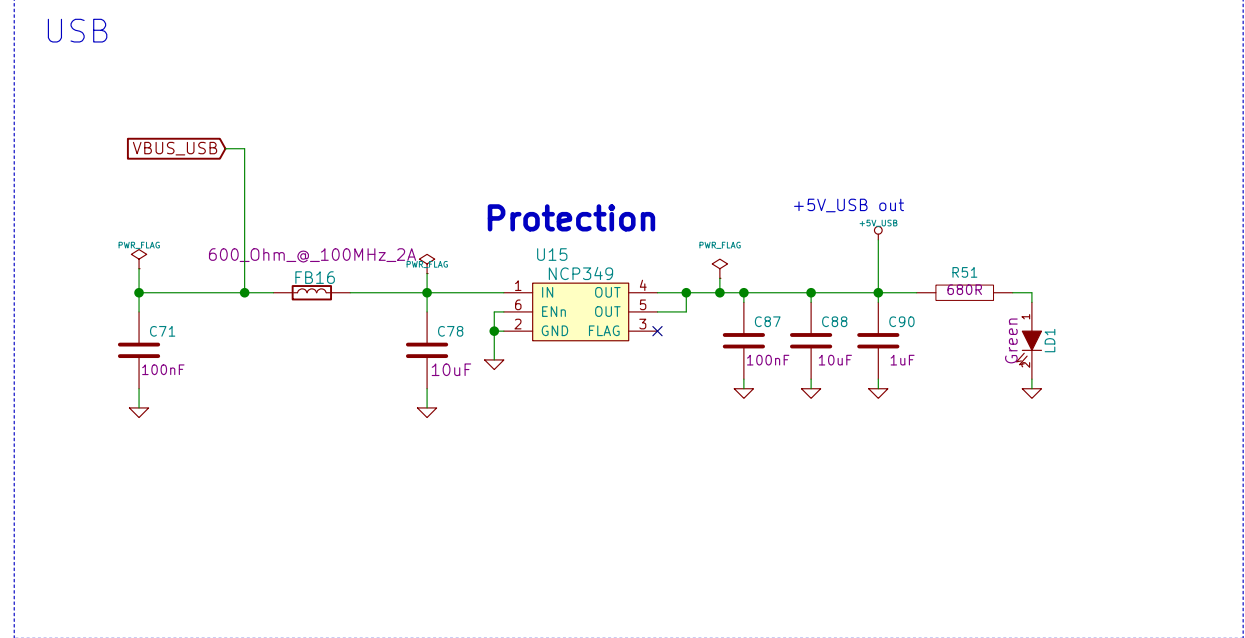
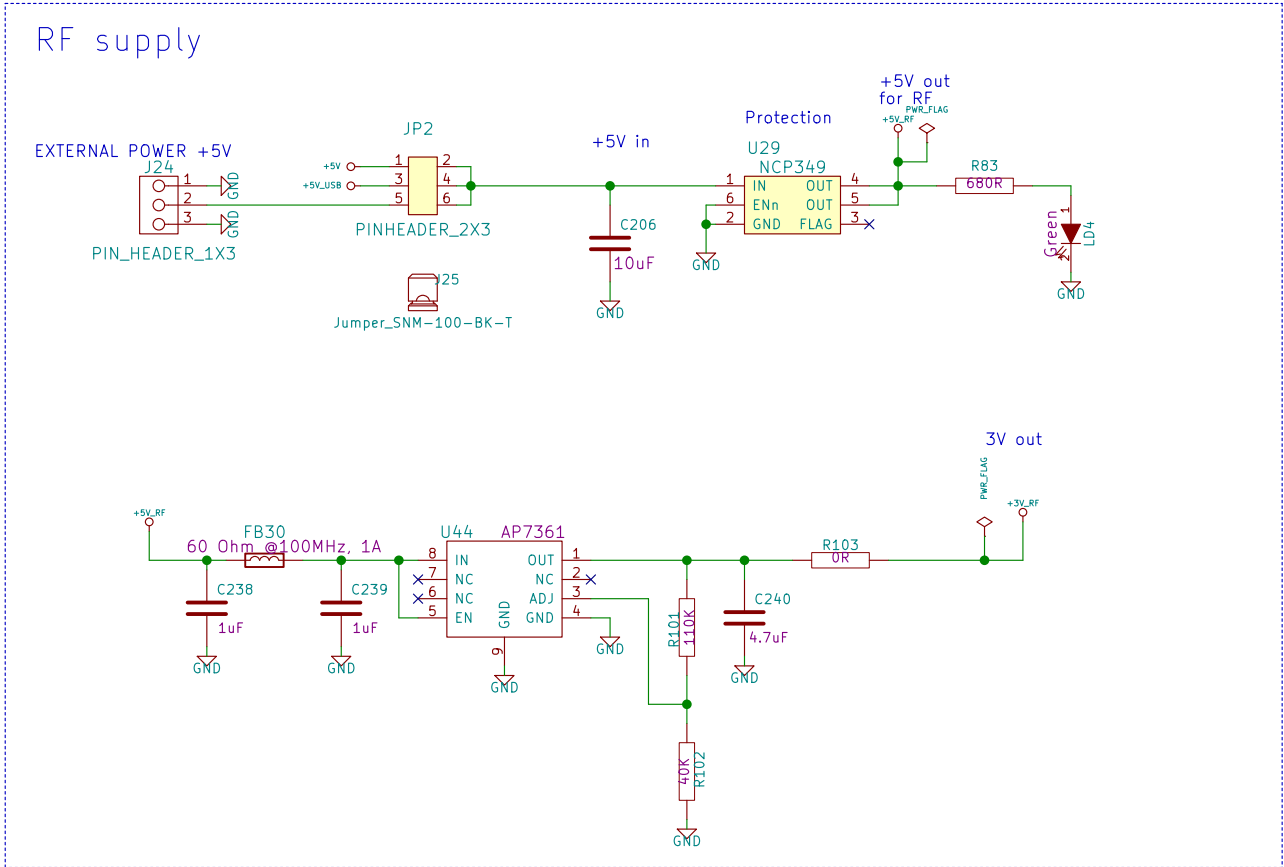
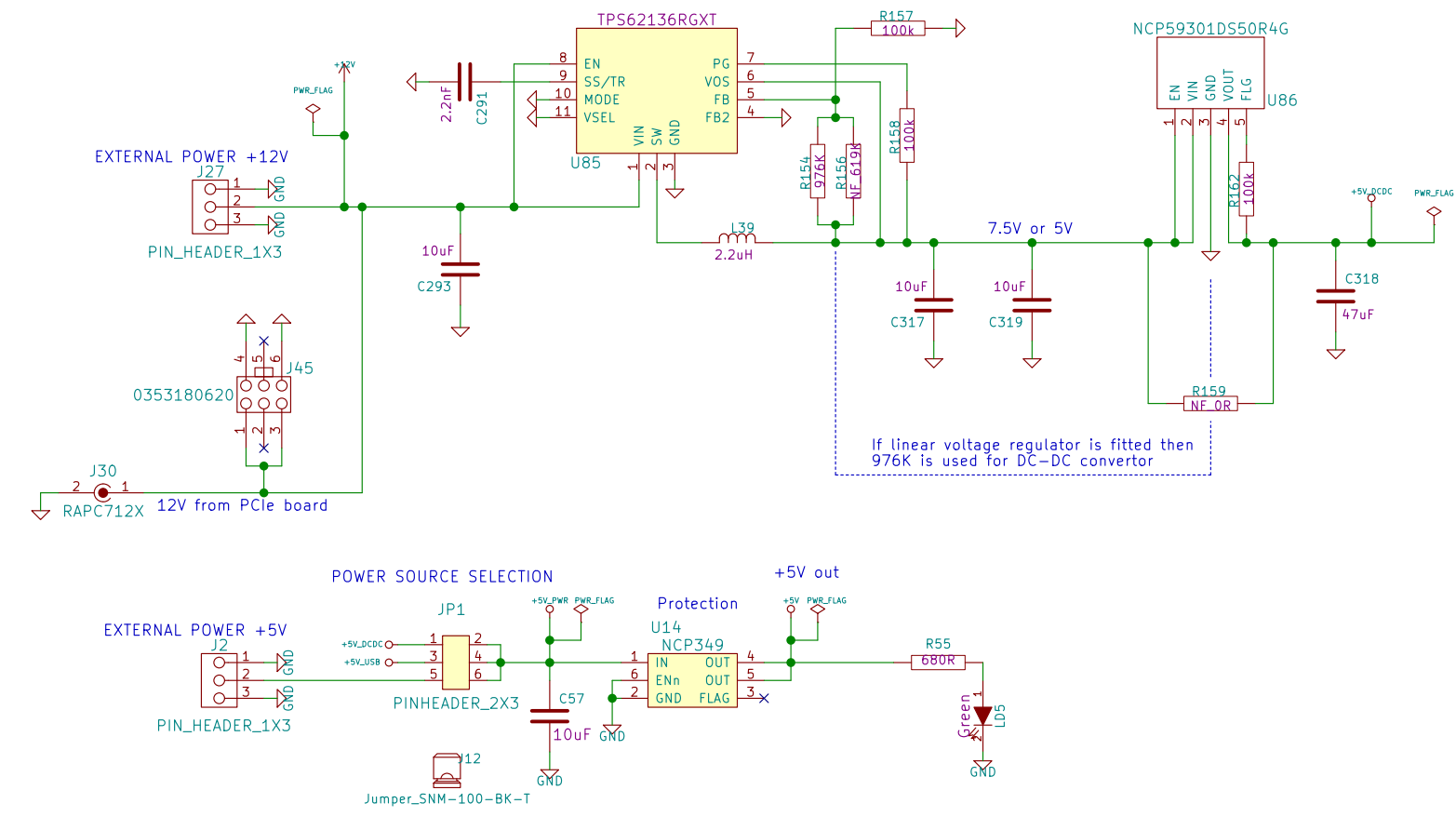


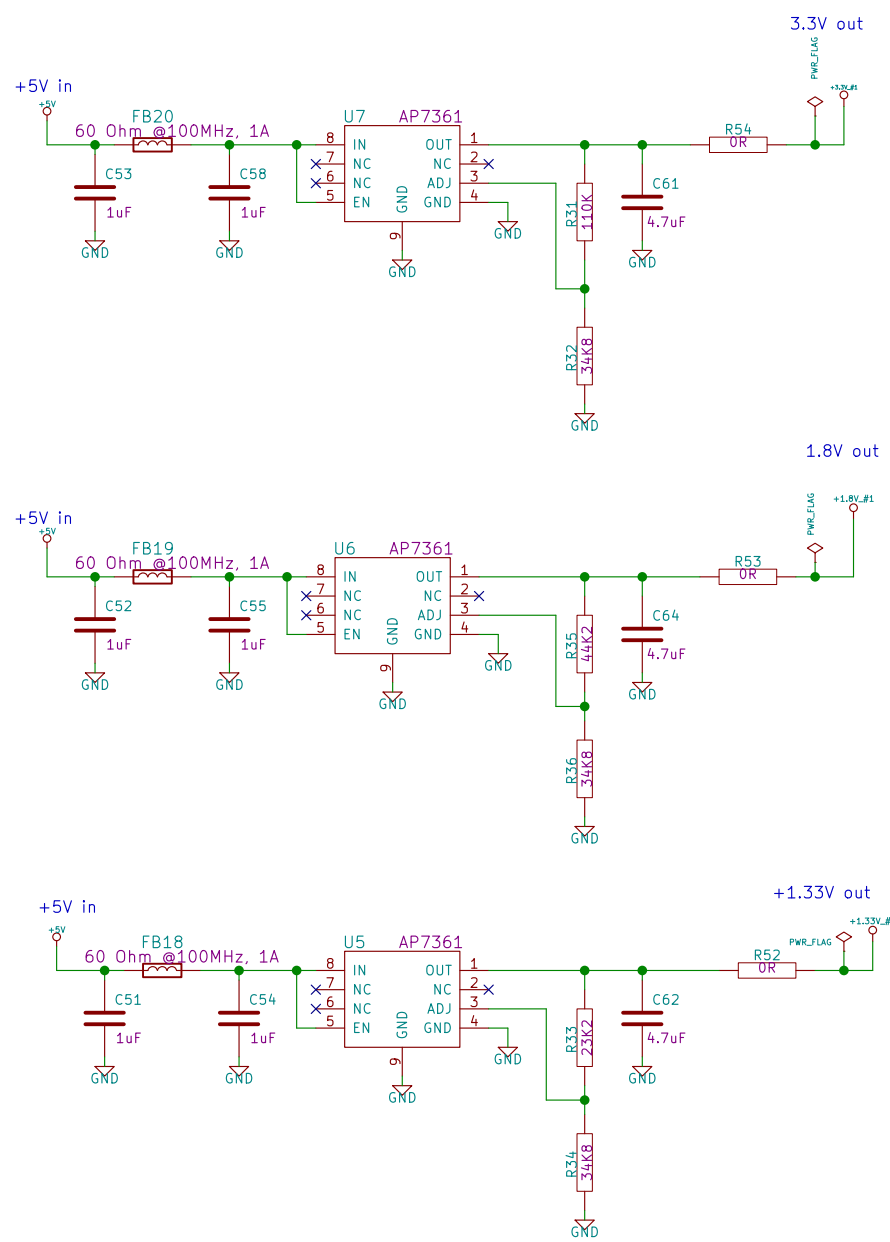
LMS8001 #1

LMS8001 #2

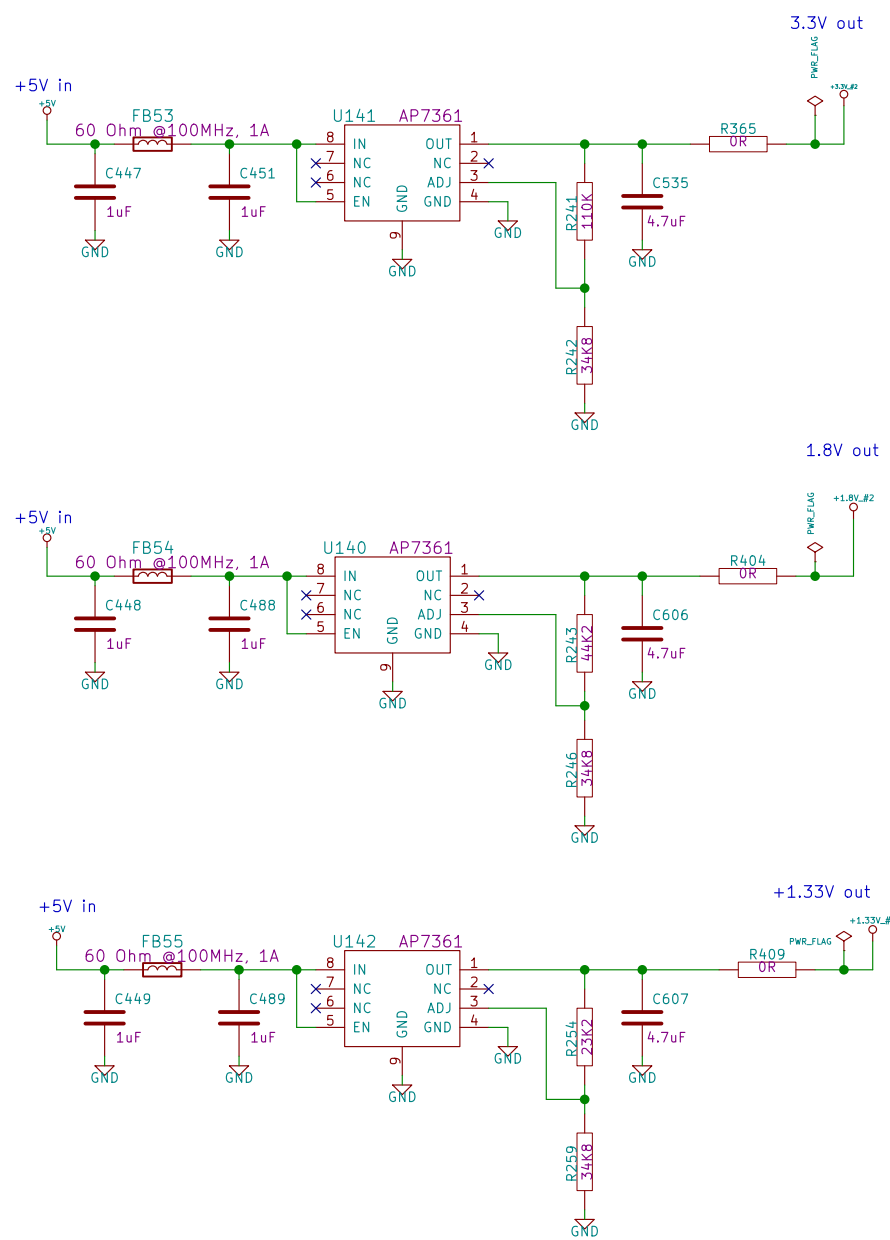
For DRC pass
PWR_FLAG



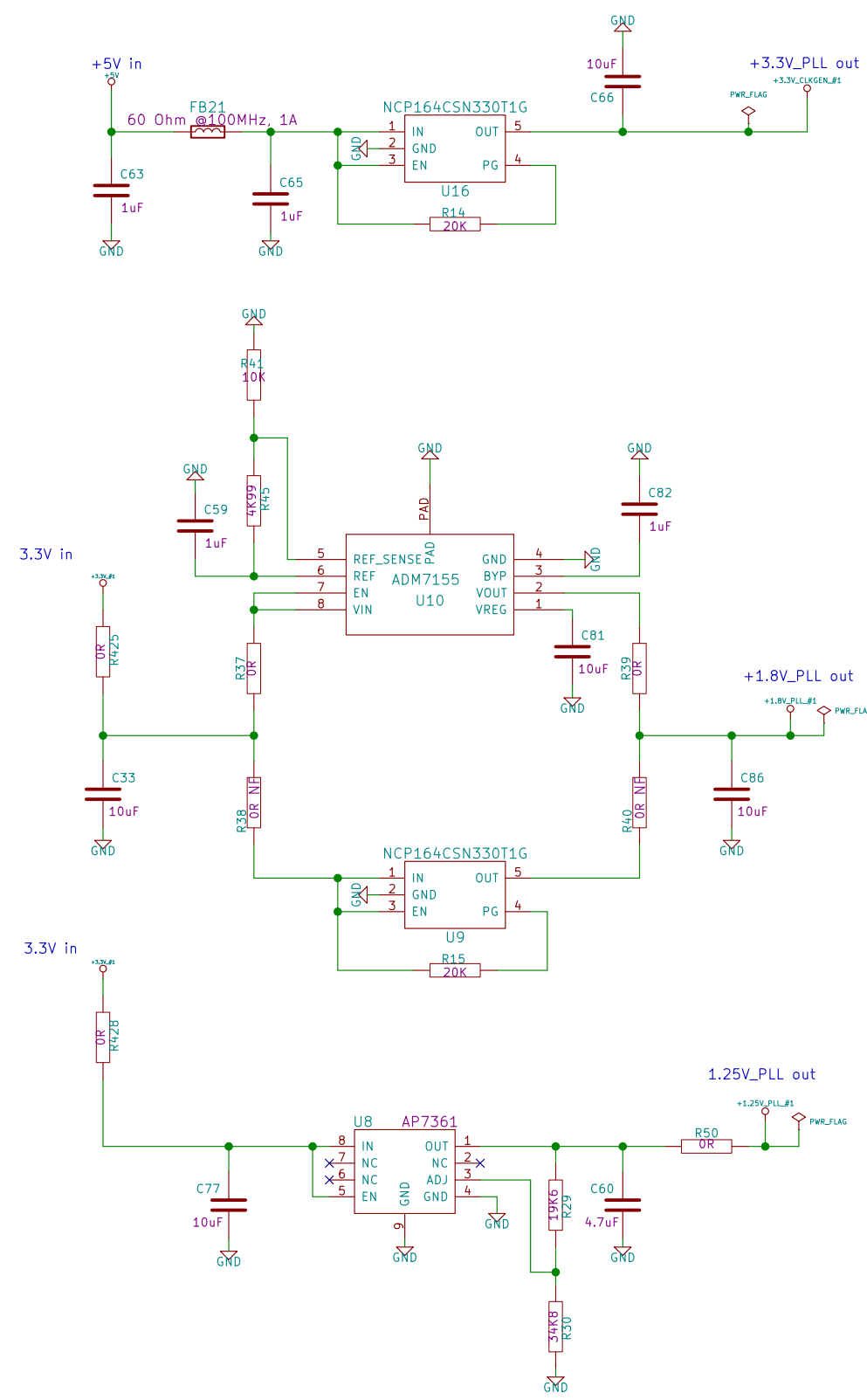
LMS8001_#1 supply



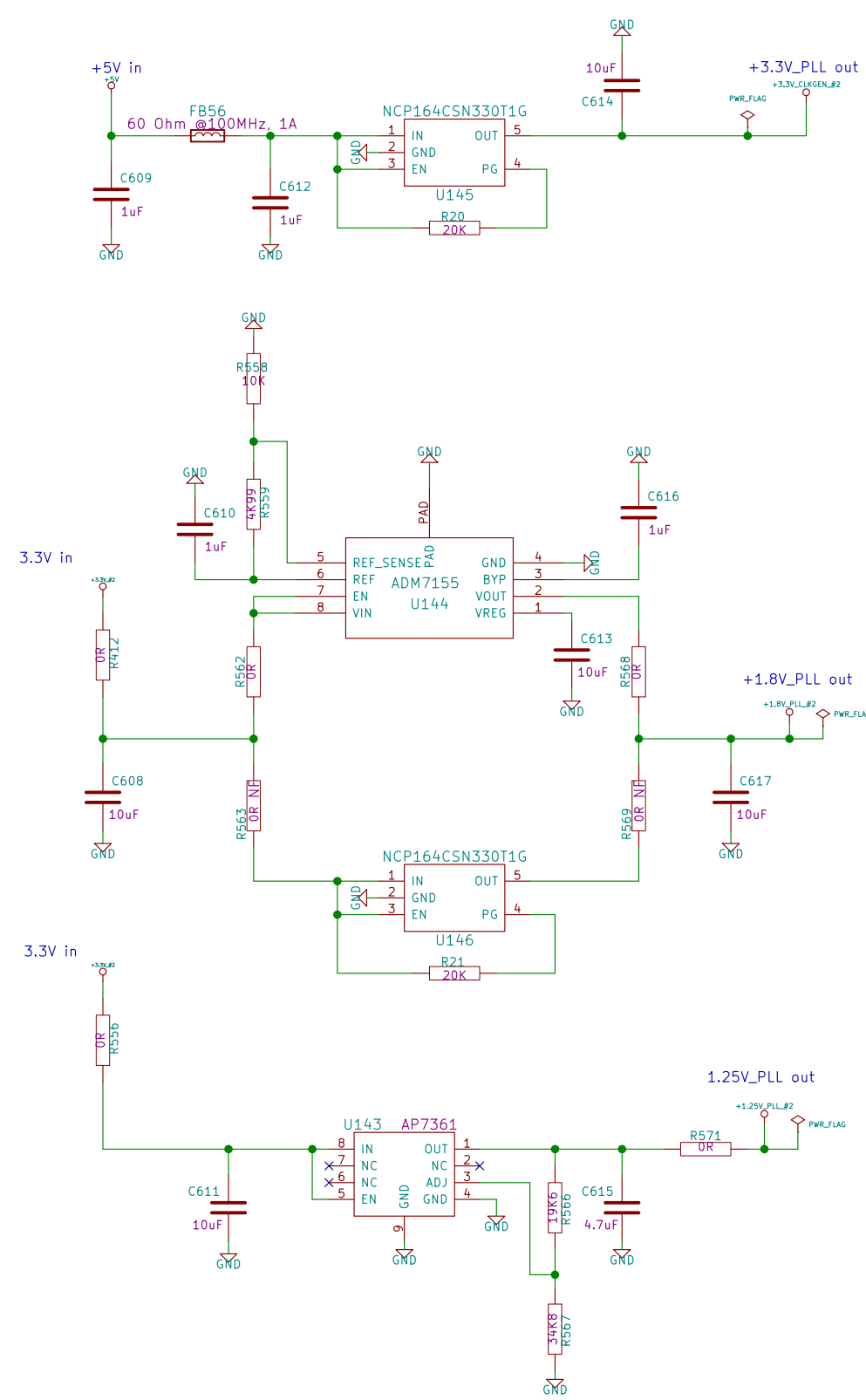
LMS8001_#2 supply



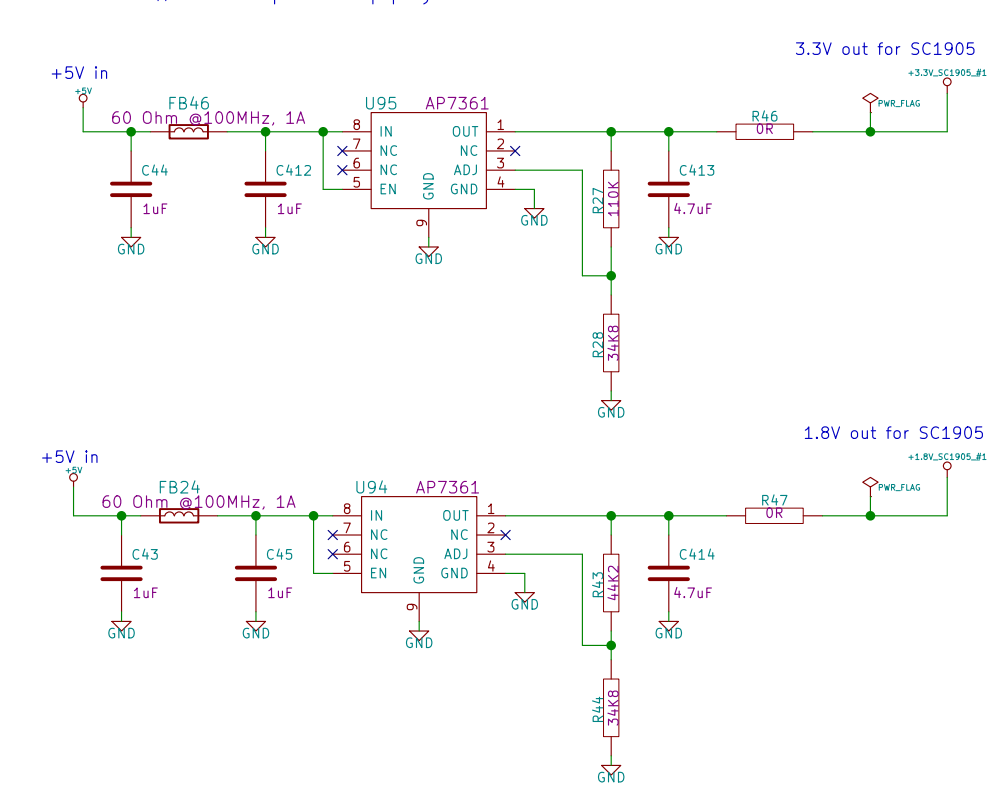
PLL Supply



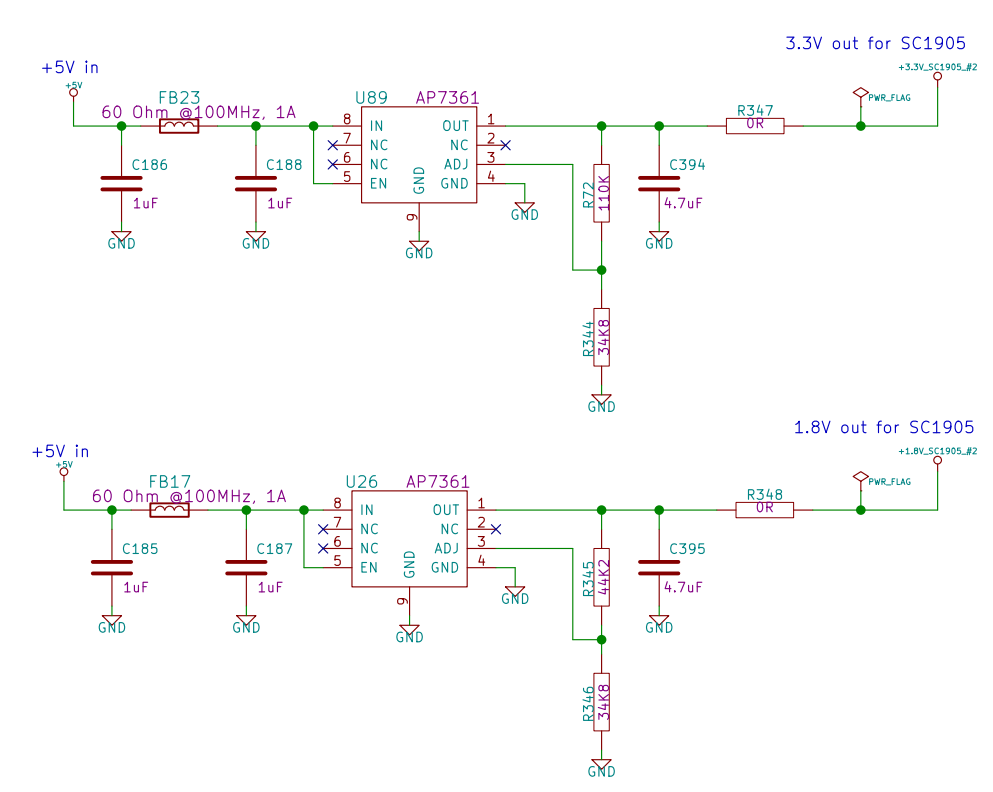
PLL Supply



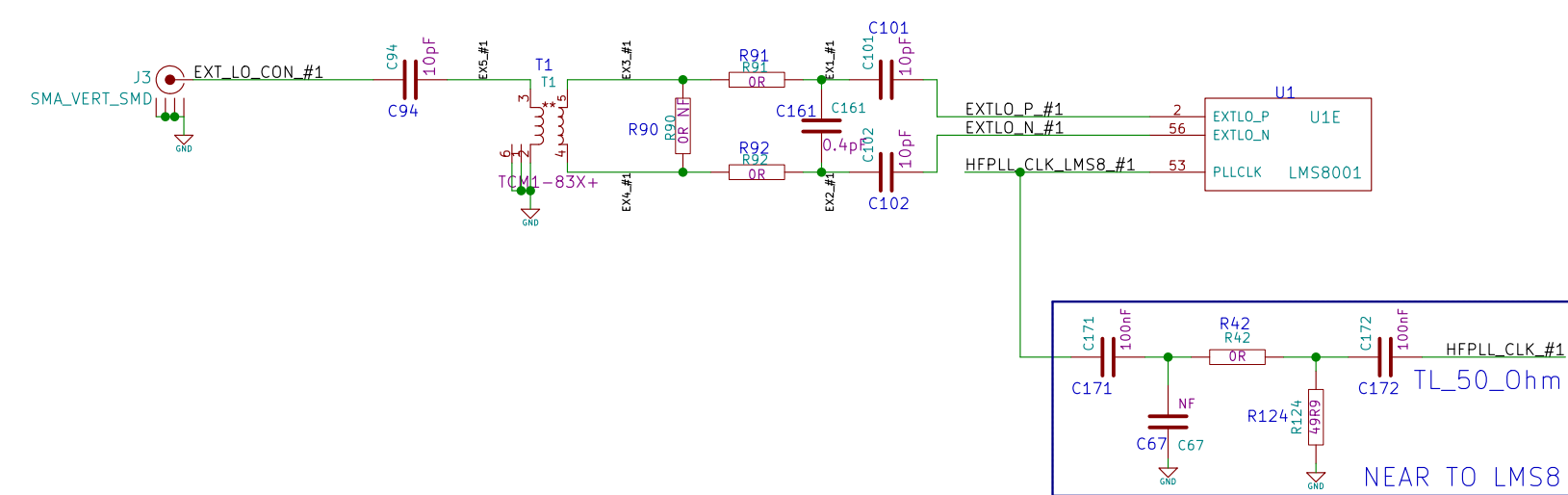
SC1905_#1 Chips Supply



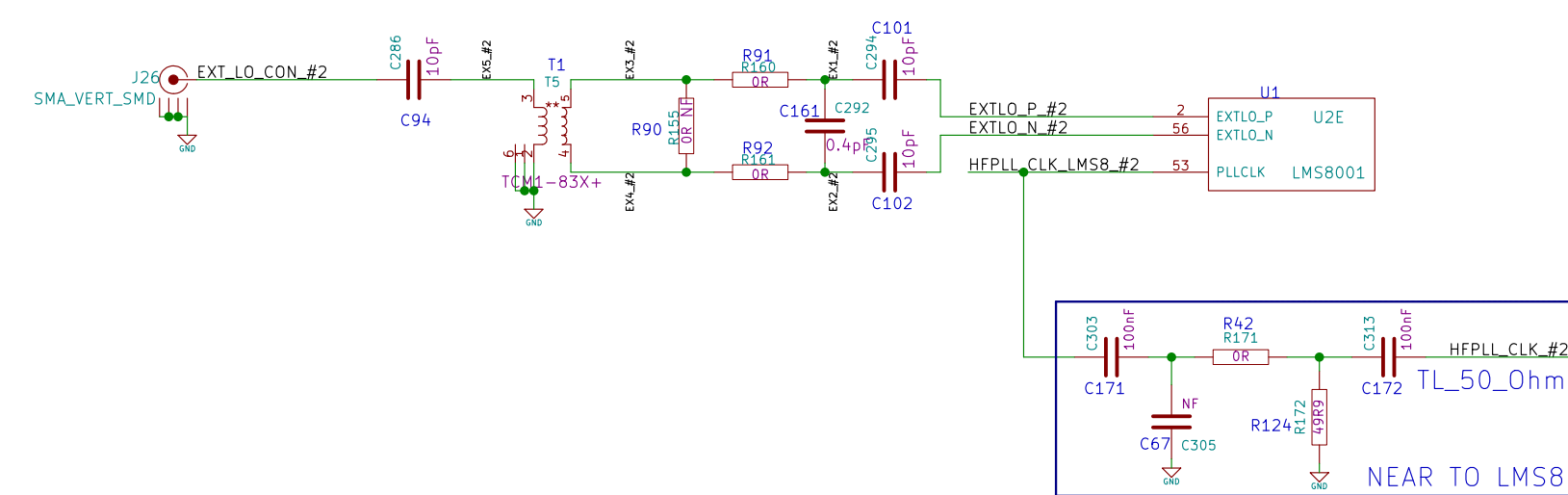
SC1905_#2 Chips Supply



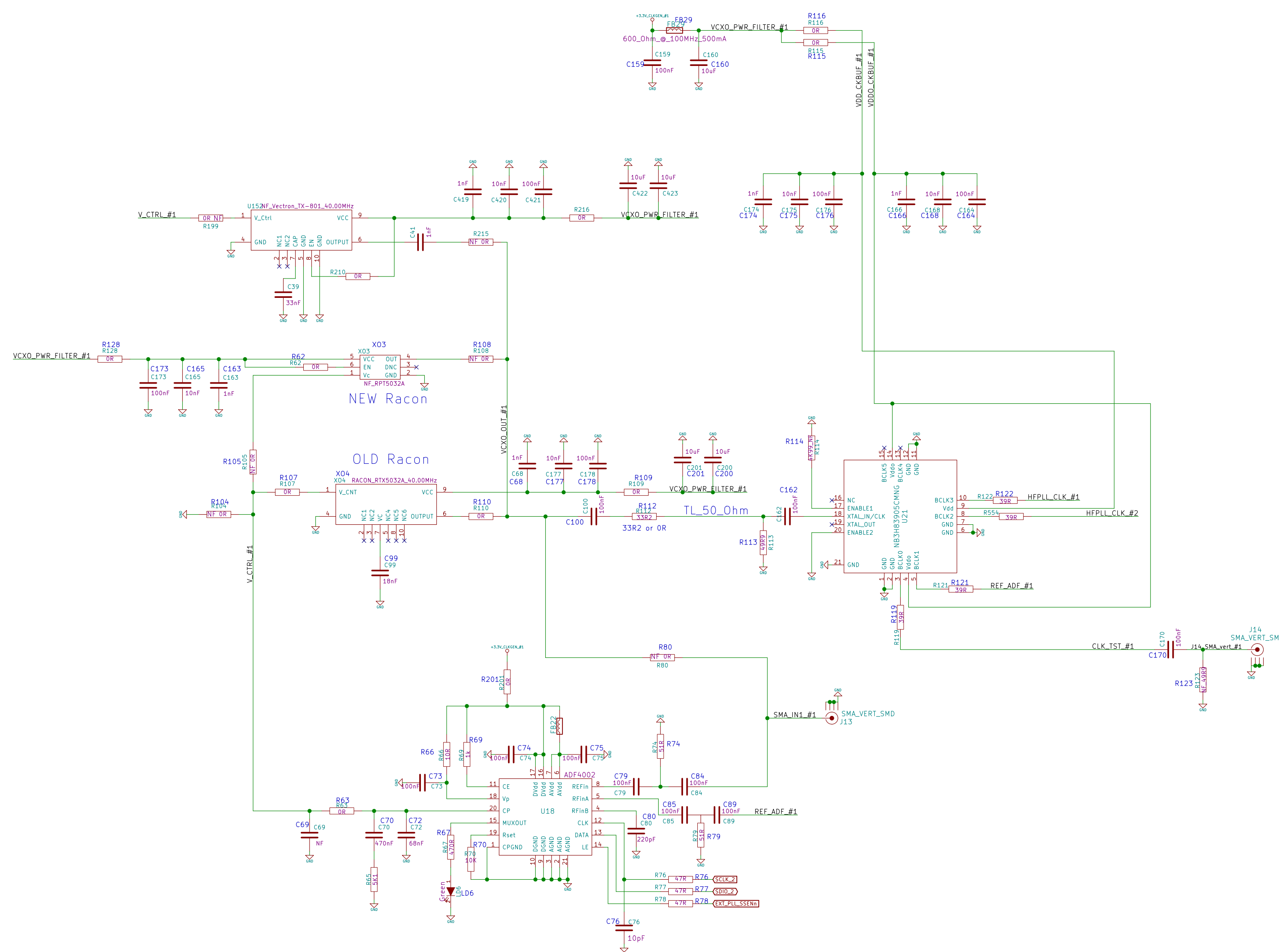
LMS8001 #1

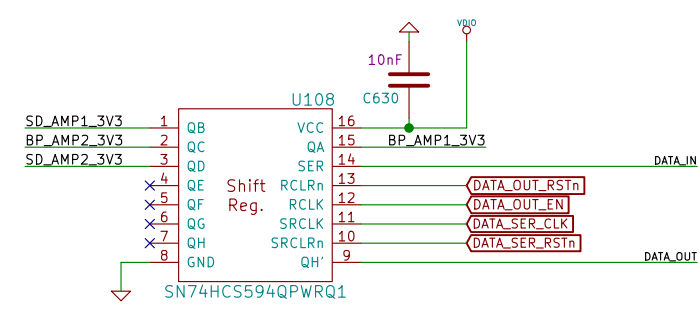
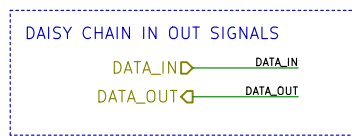


LMS8001 #2

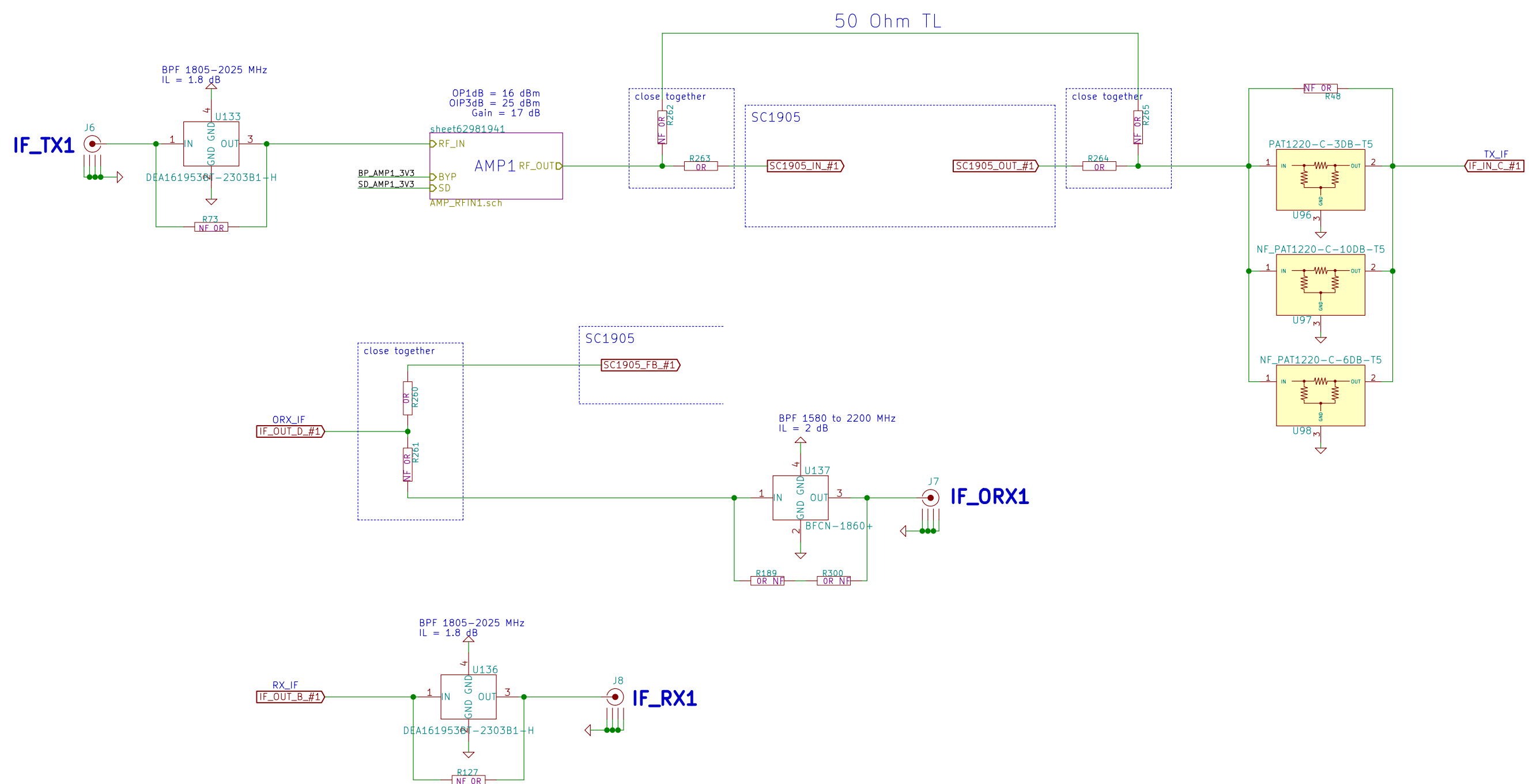
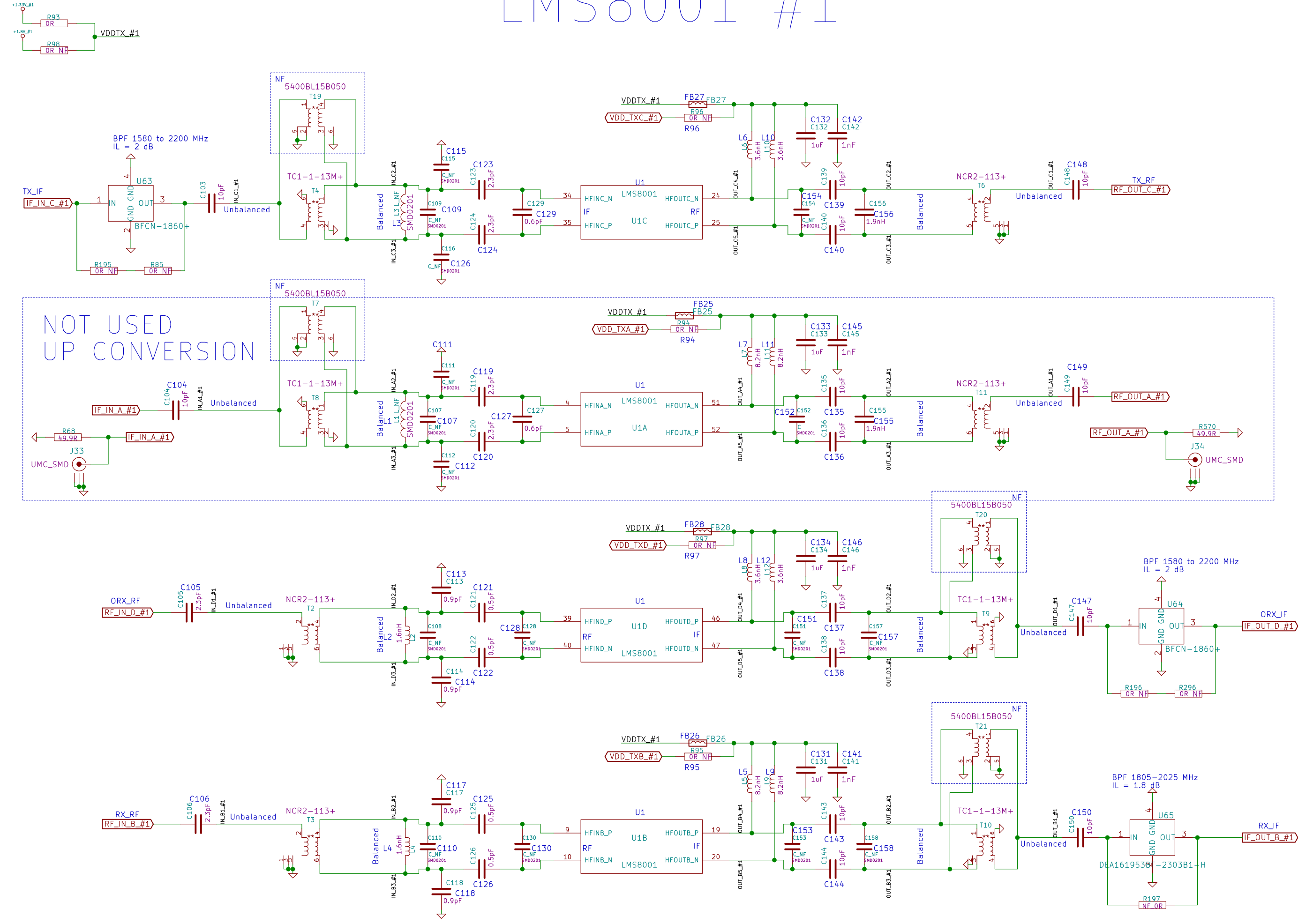


Deleted

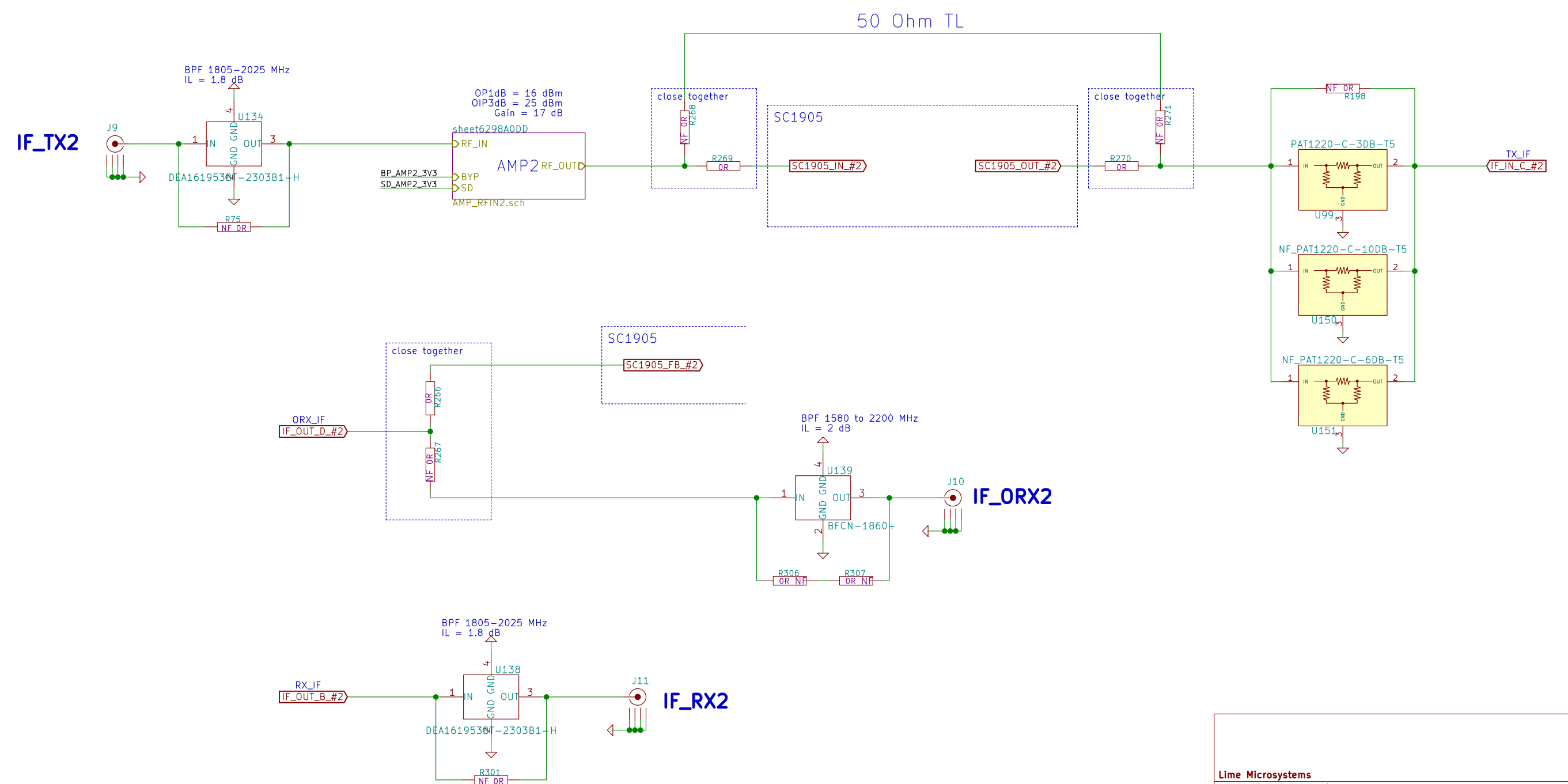
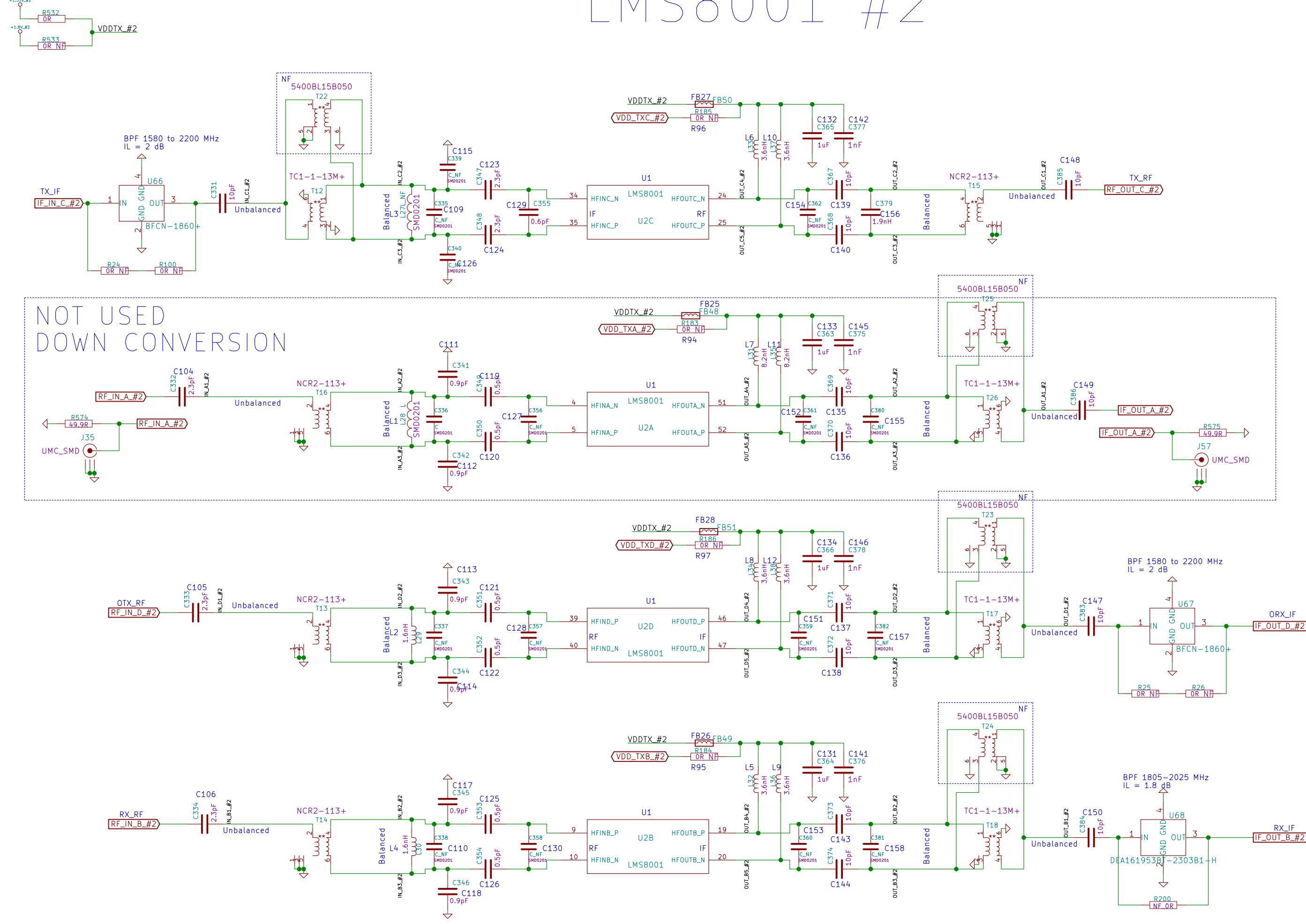


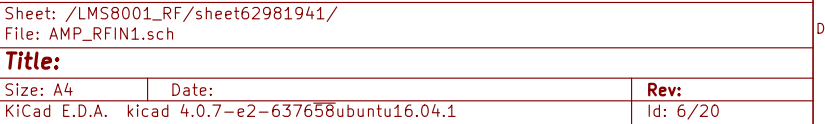


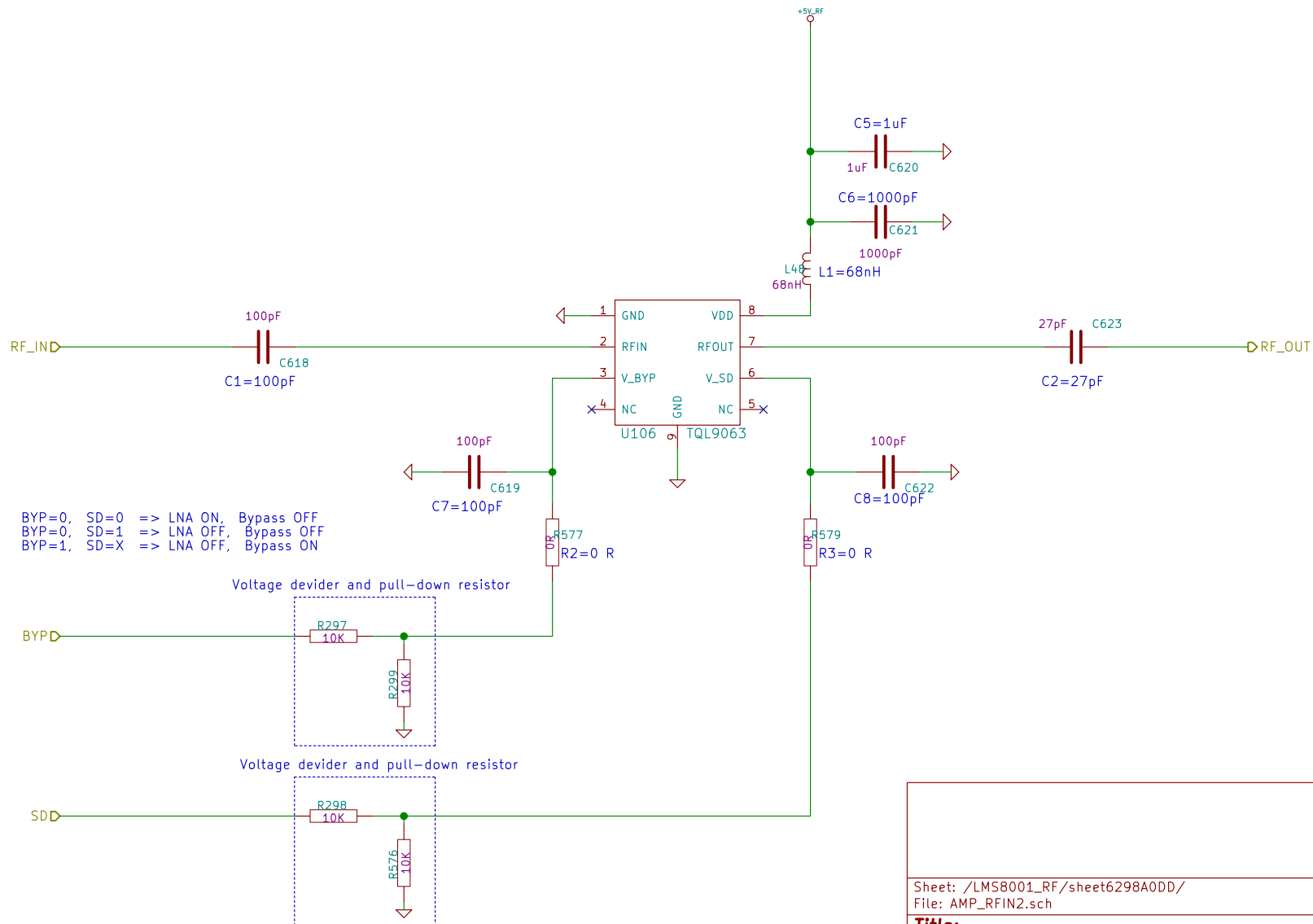
LMS8001 #1



LMS8001 #2







Sheet: /LMS8001_RF/sheet6298A0DD/
File: AMP_RFIN2.sch

Title:

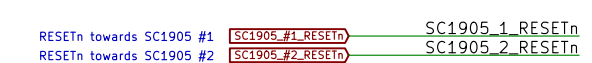
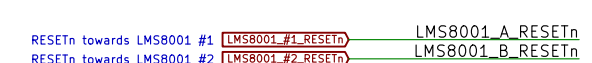
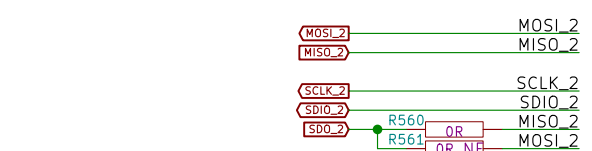
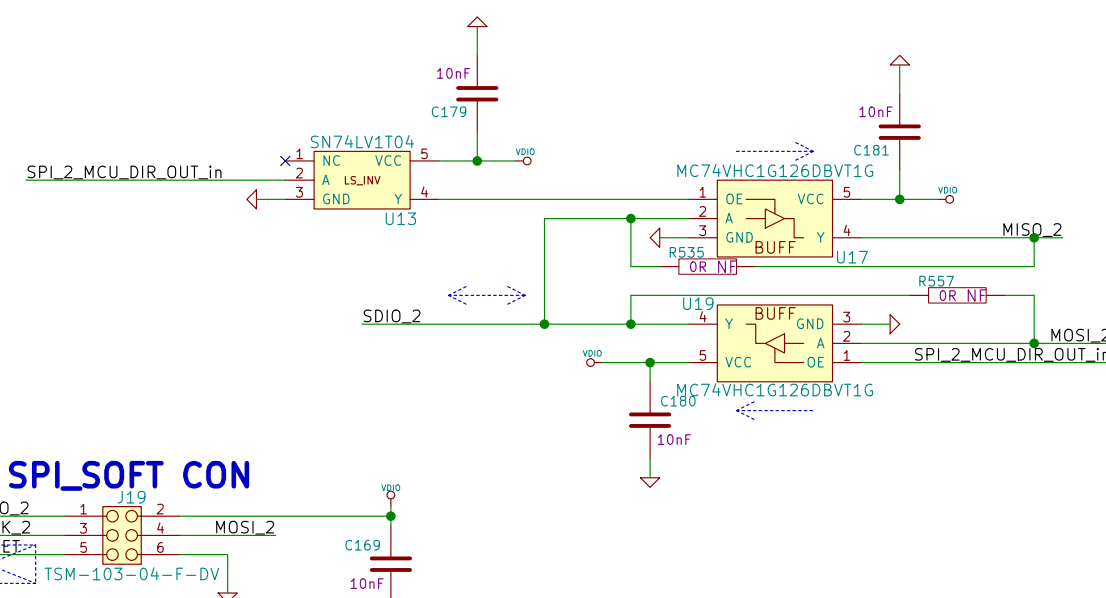
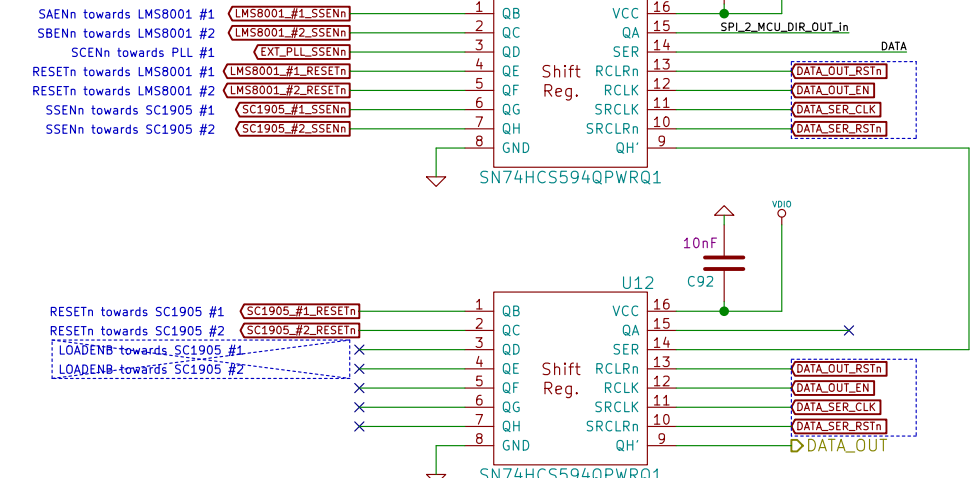
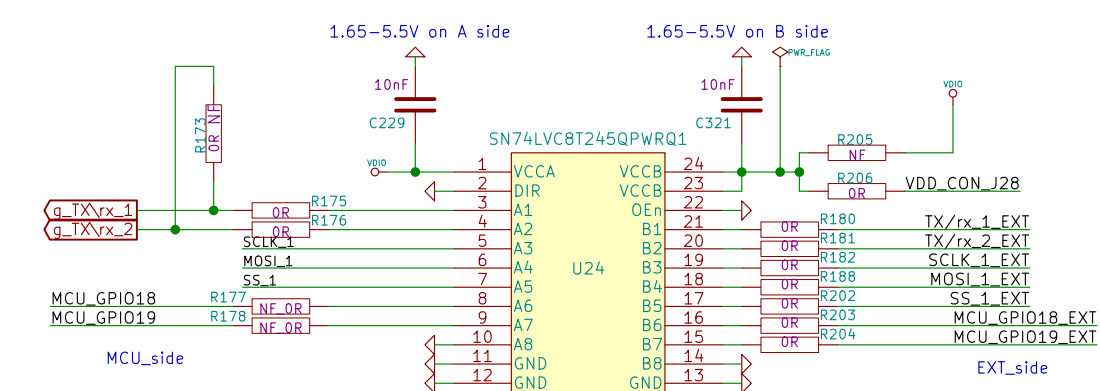
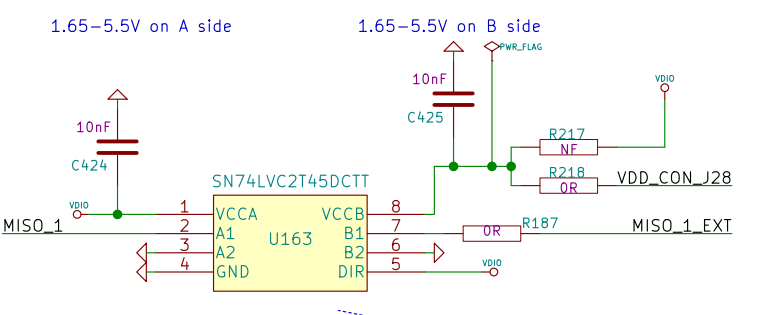
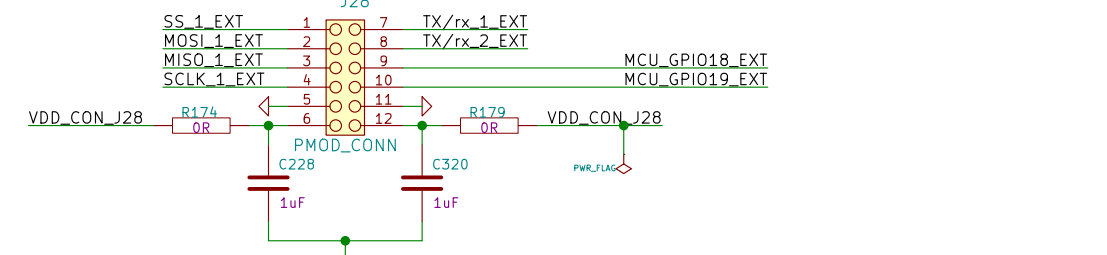
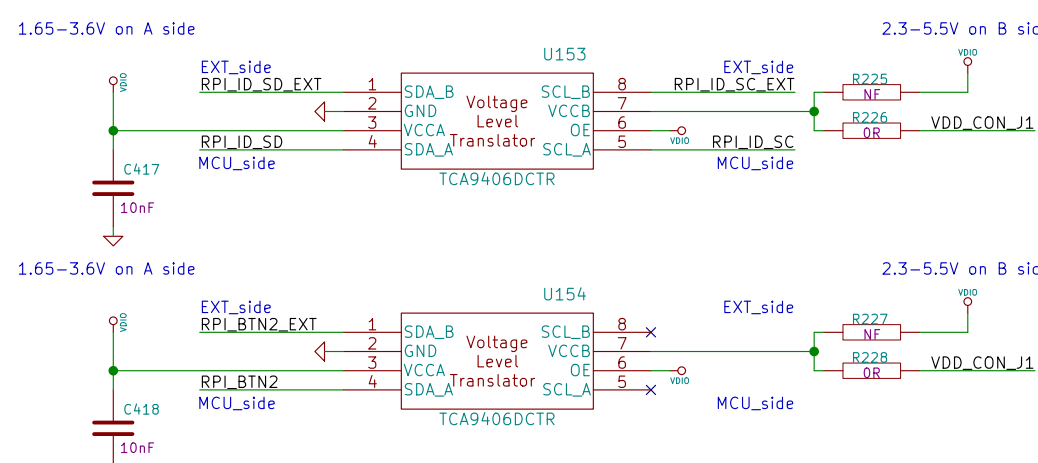
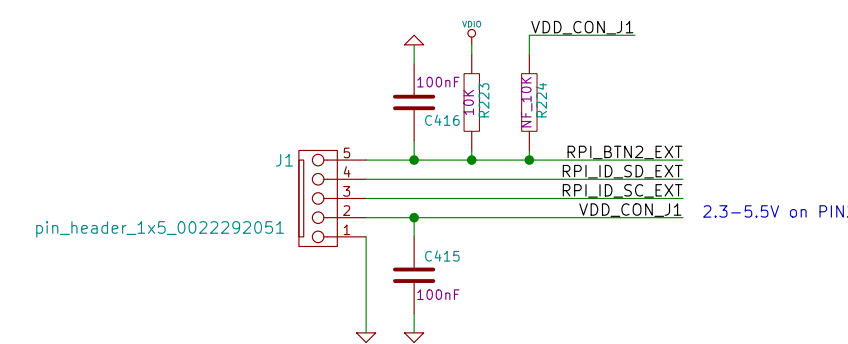
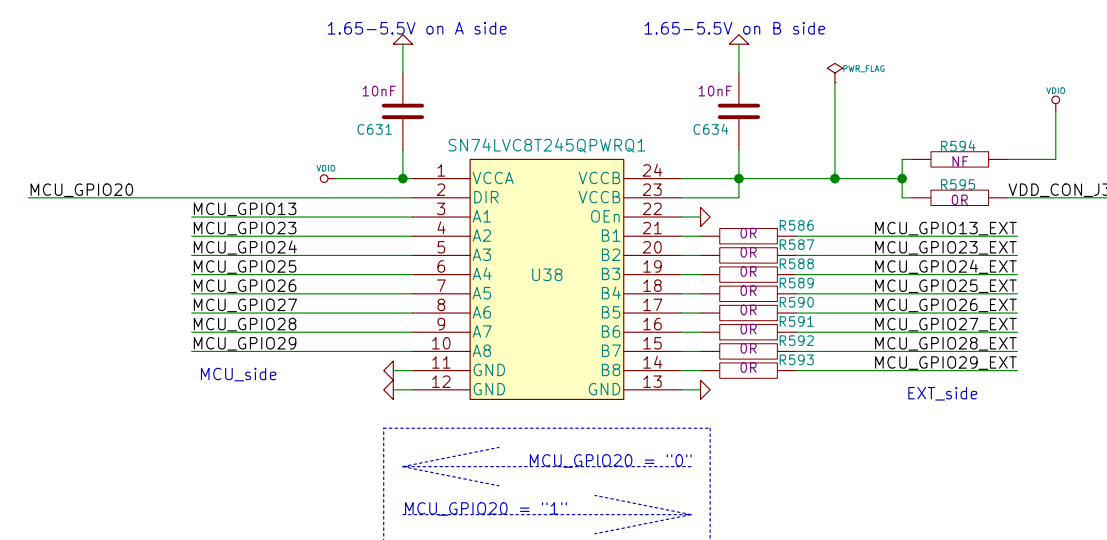
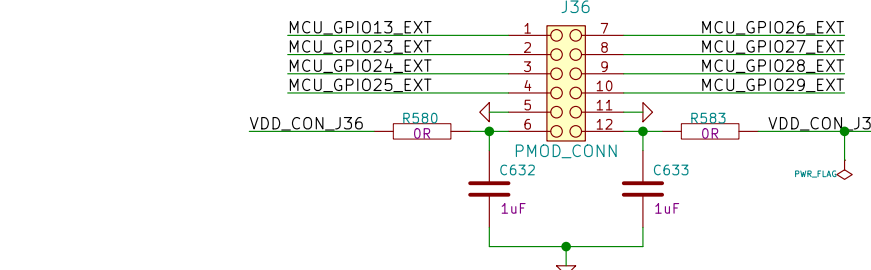
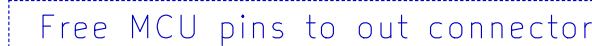
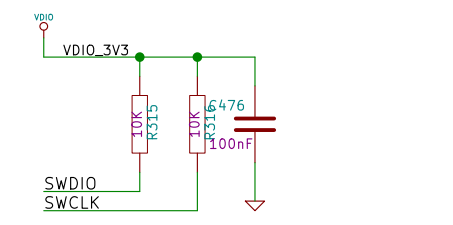
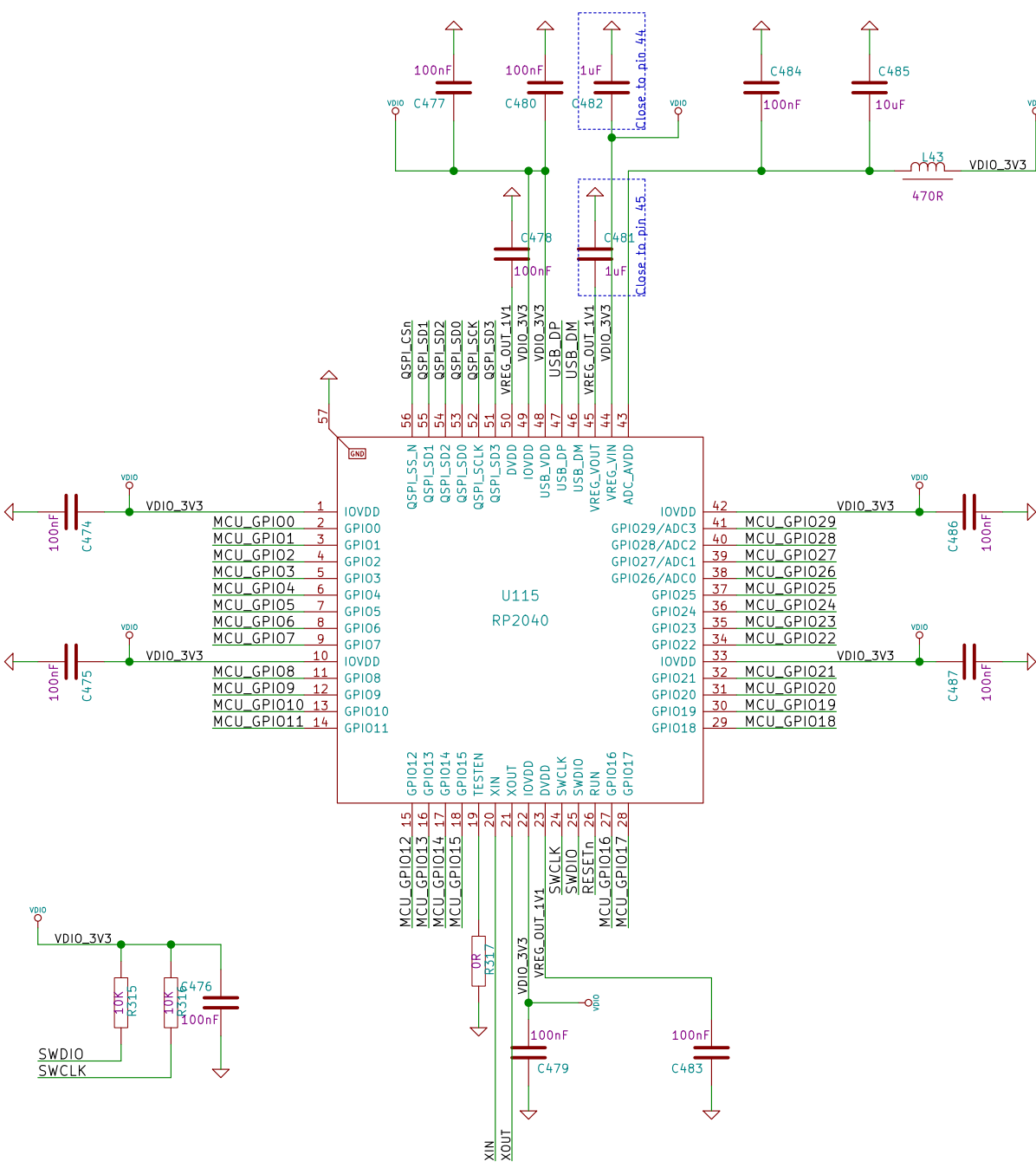
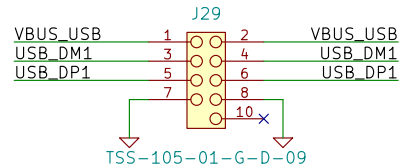
Size: A4

Date:

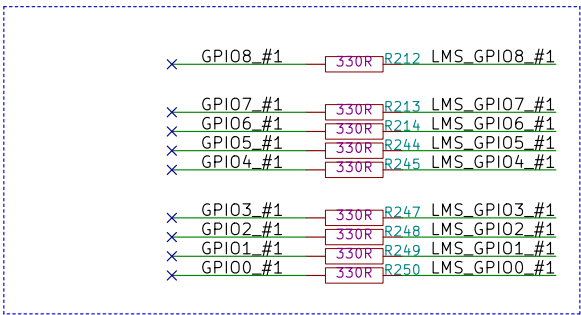
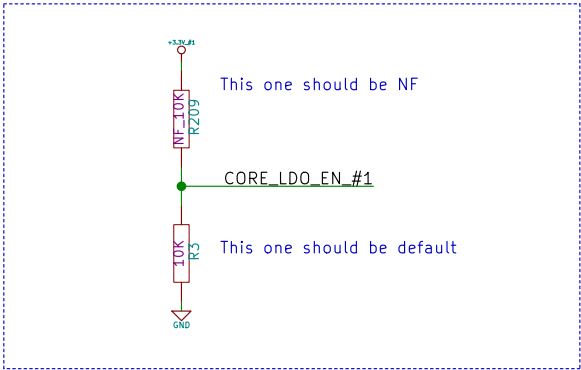
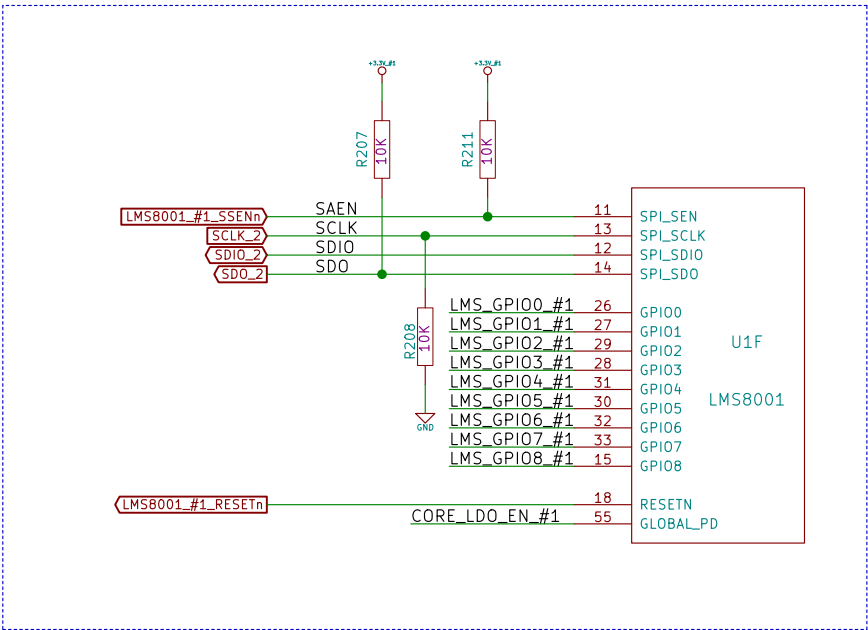
Rev:

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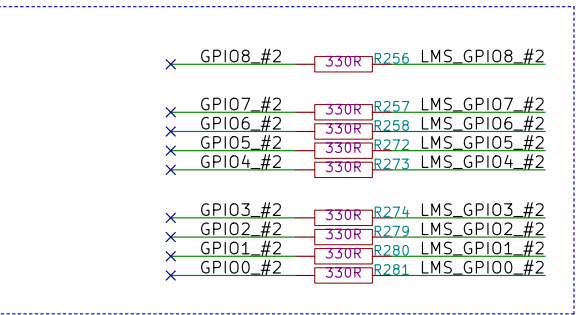
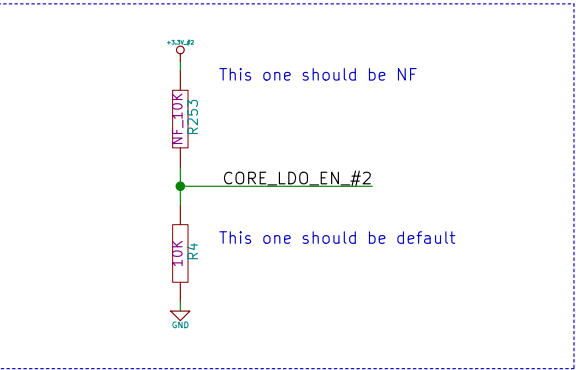
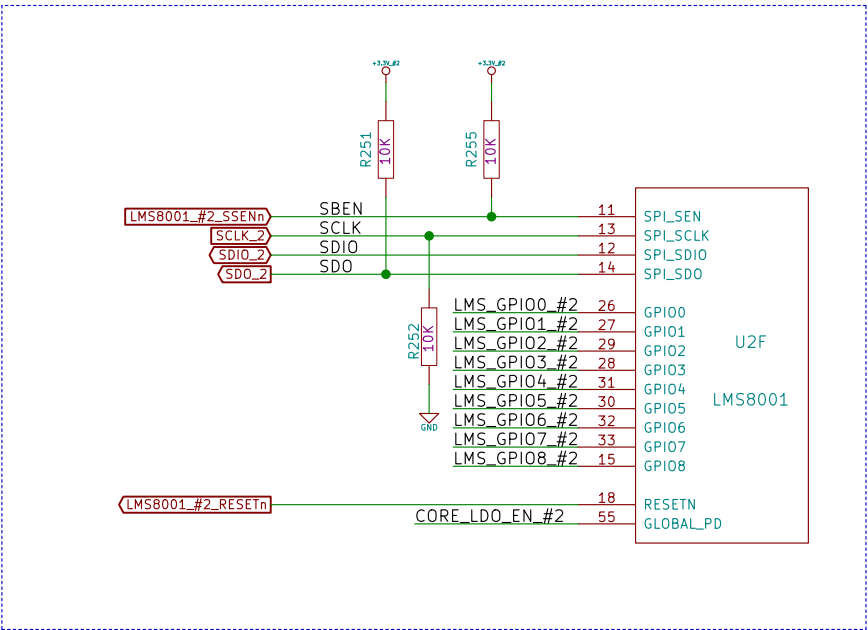
Id: 7/20



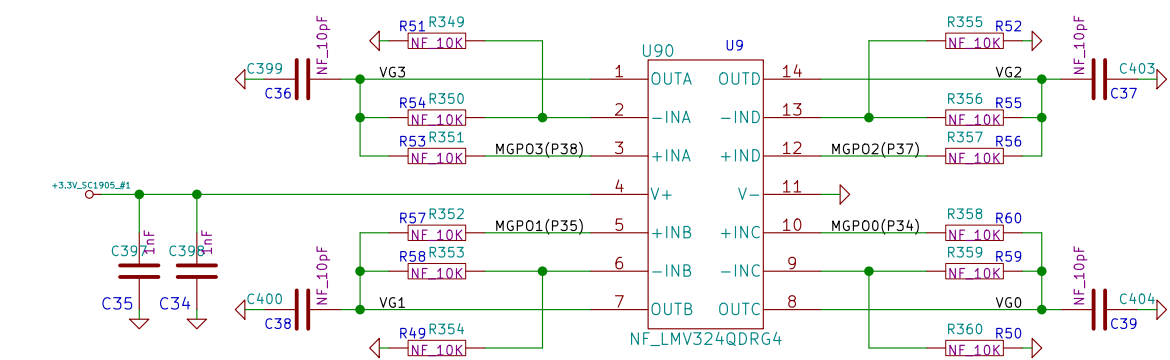
LMS8001 #1



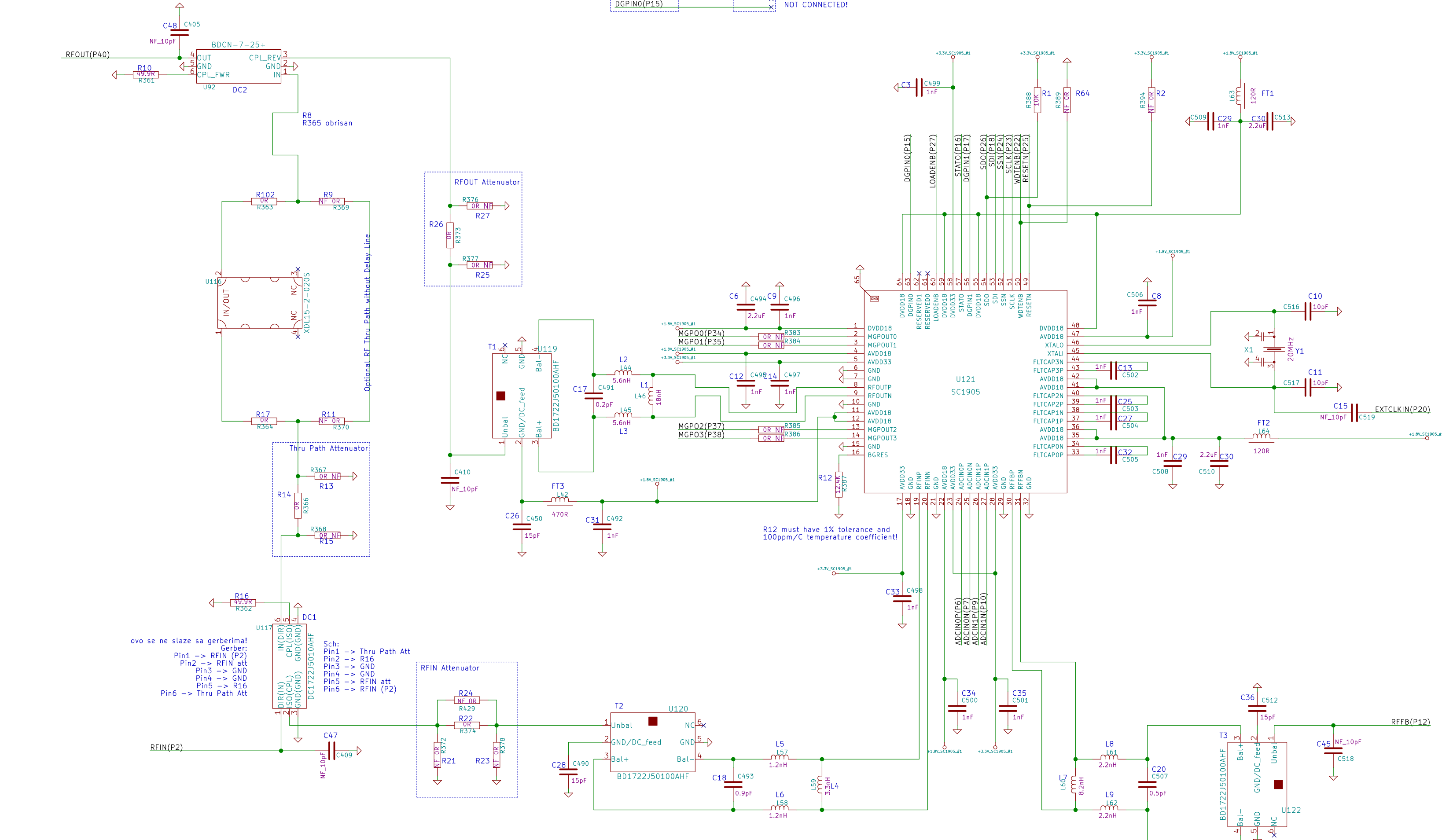
LMS8001 #2

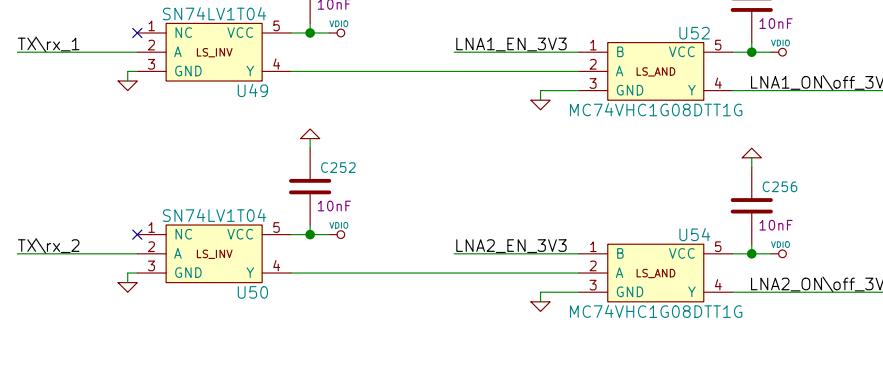
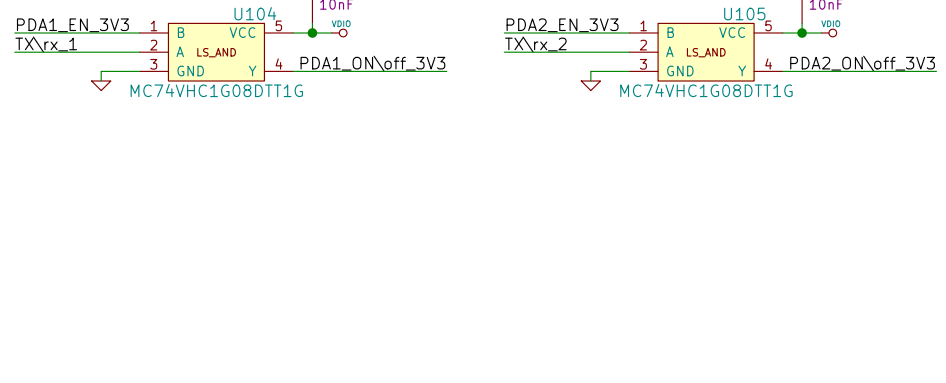
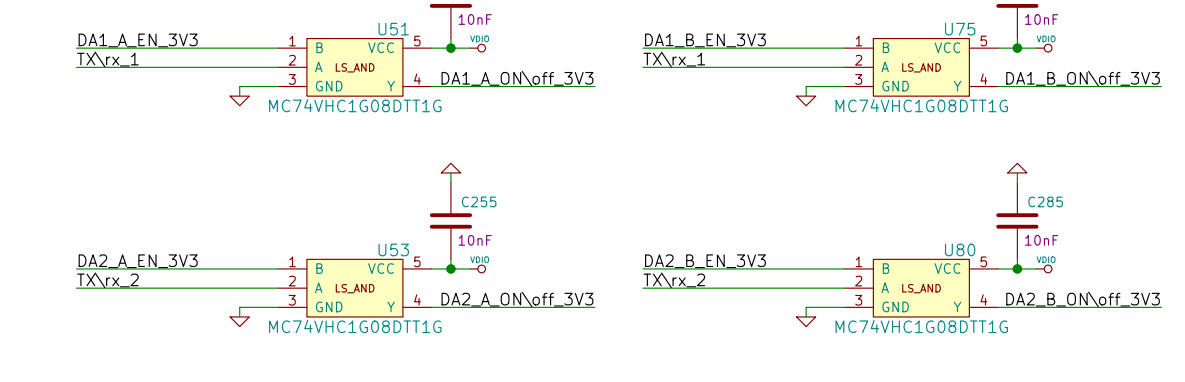
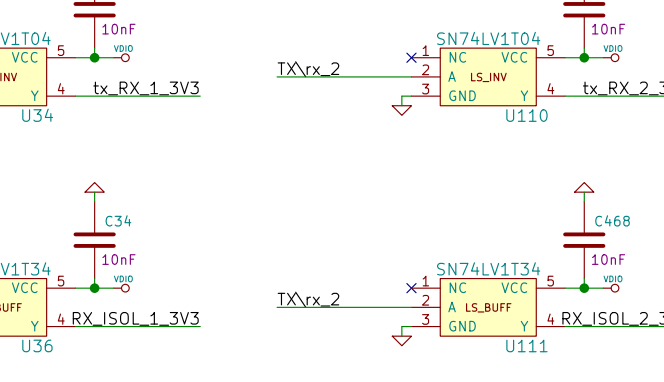
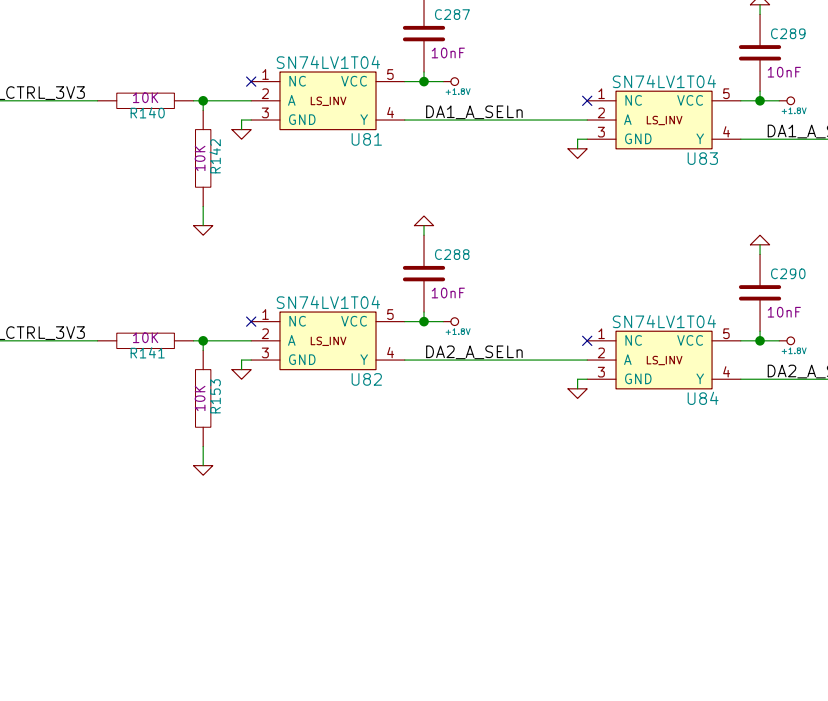
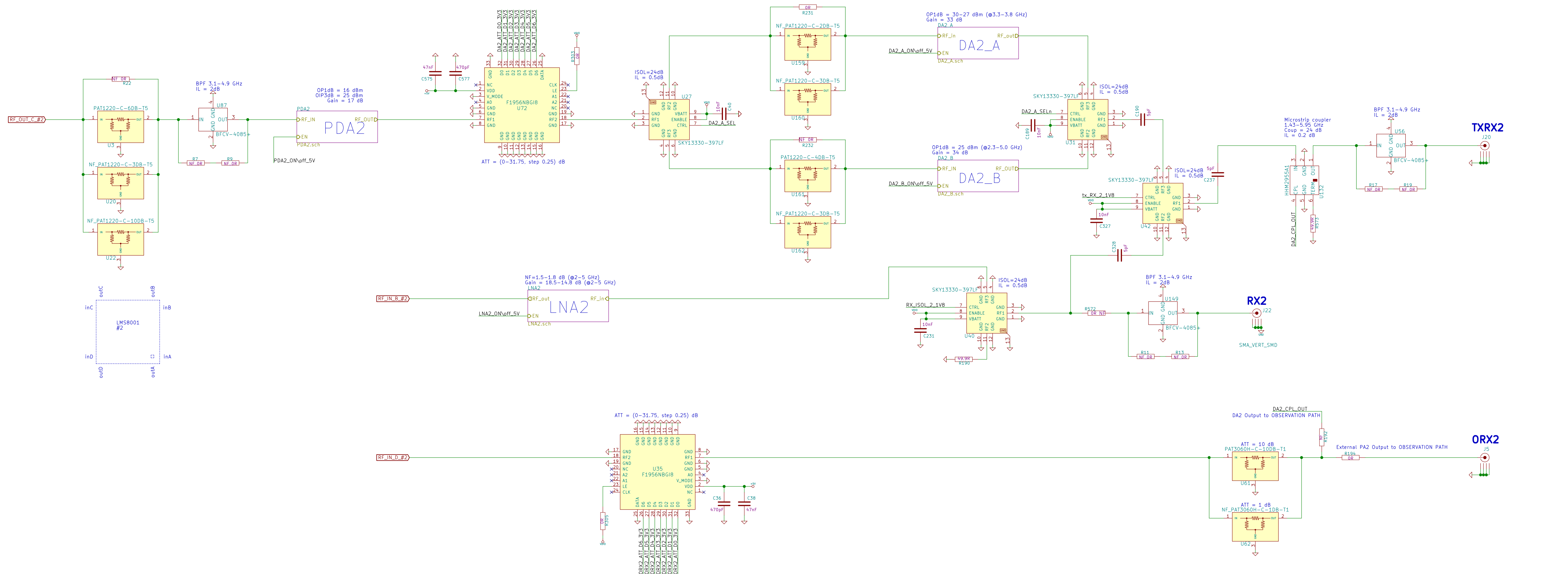
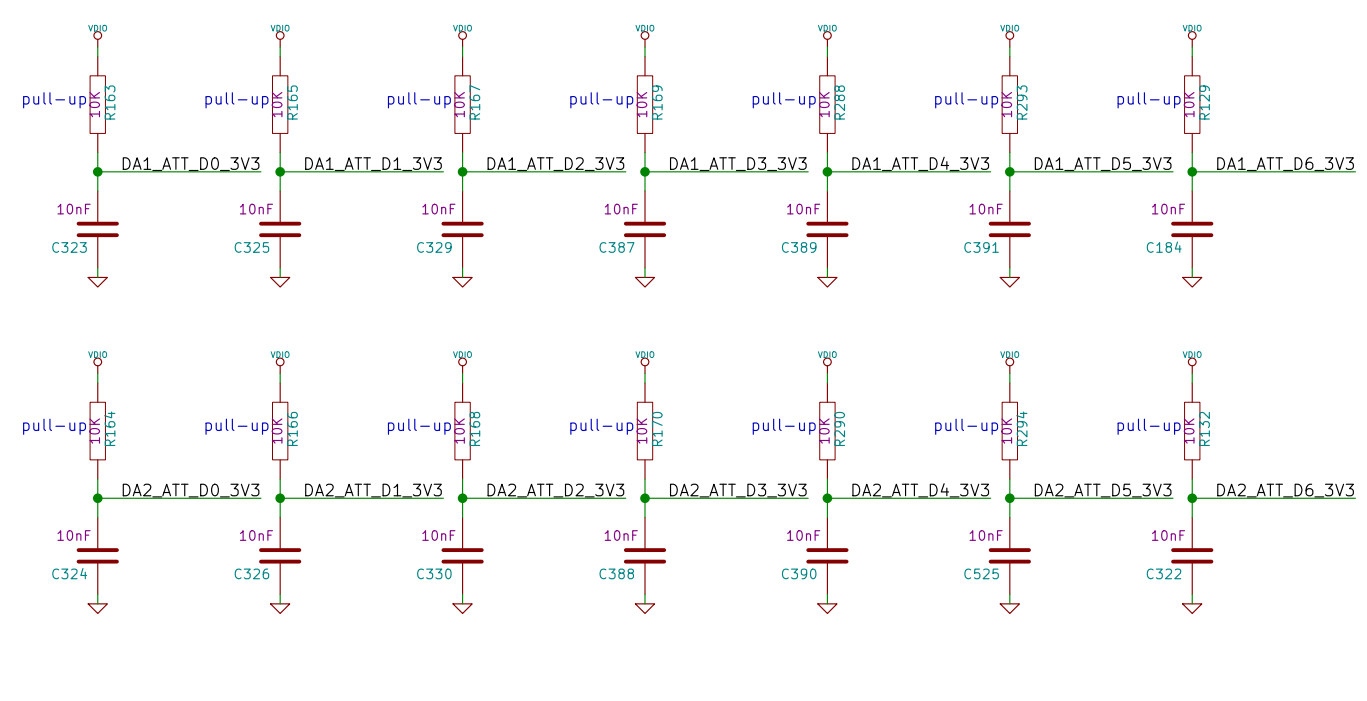
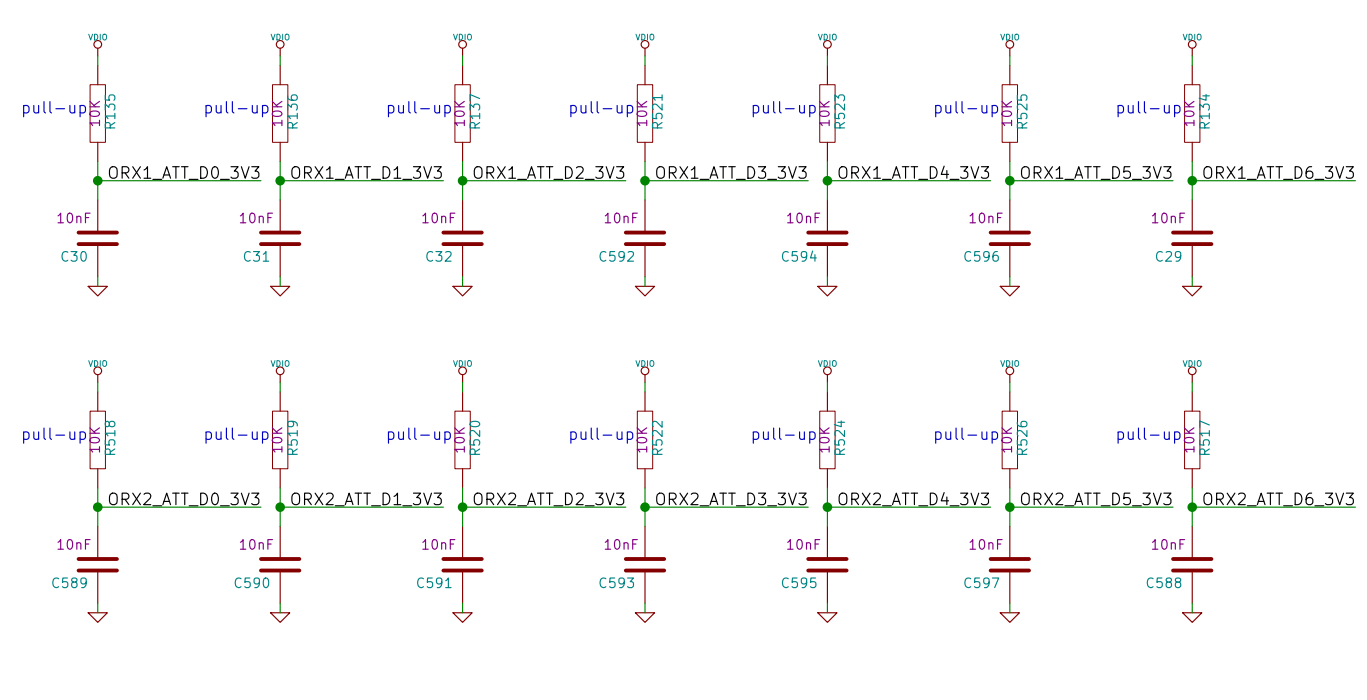
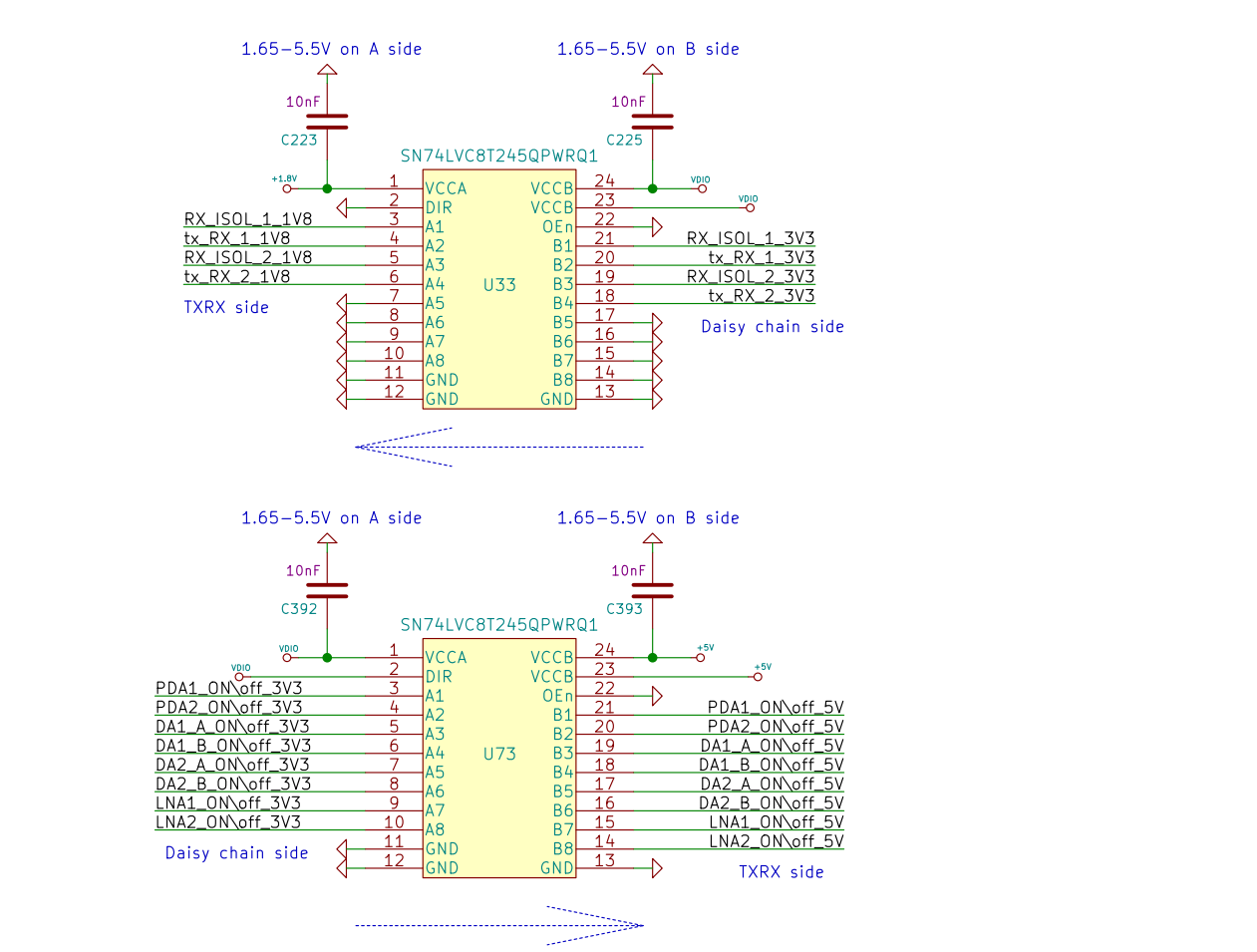


Buffers for MGPOUT 0-3
Not Fitted



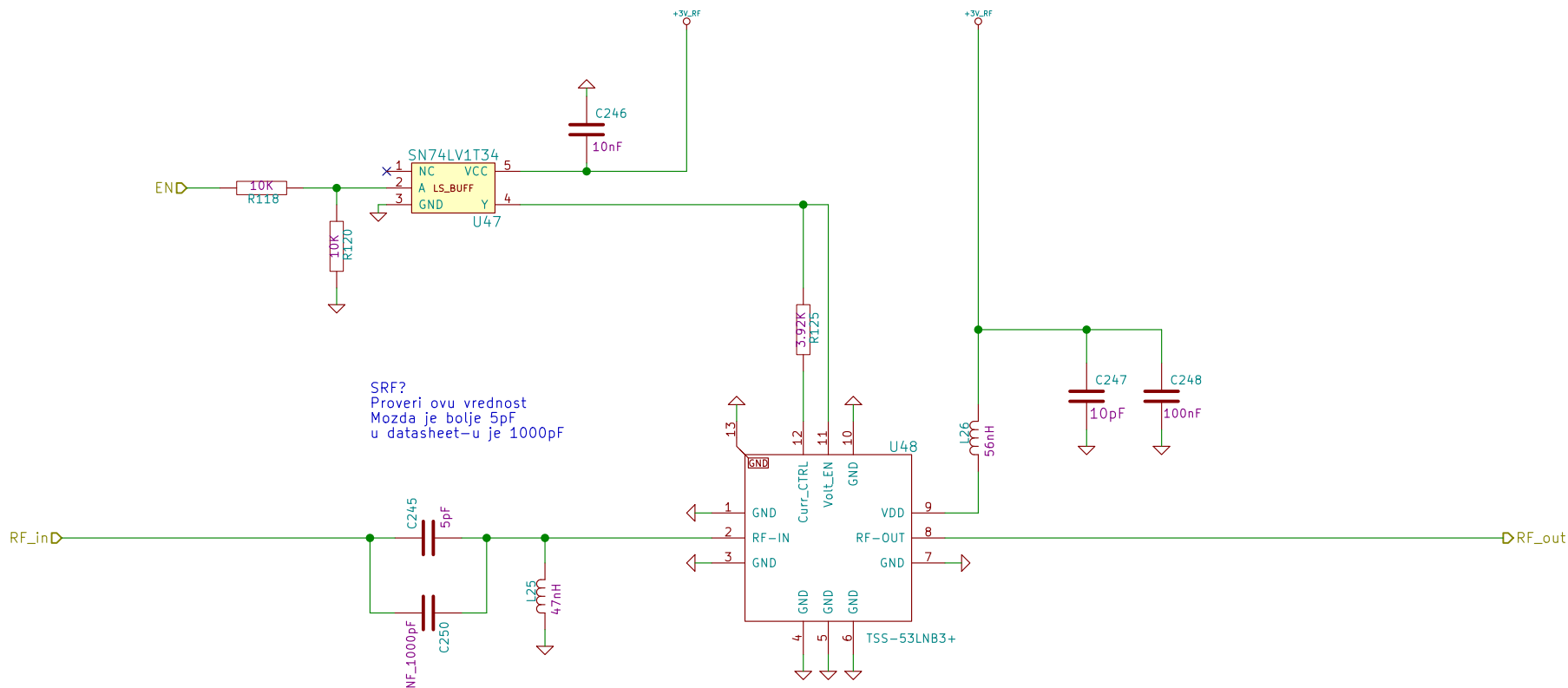
Master Board	EVK1905 board	
STATO(P16)	STATO	CONNECTED TO Q2
RESIN(P25)	RESIN	
SSM(P24)	SSM	
SOP(P10)	SOP	
SOP(P26)	SOP	
SCLK(P23)	SCLK	
WDIENB(P22)	WDIENB	CONNECTED TO R389
LOADENB(P27)	LOADENB	NOT CONNECTED!
DGPIN(P15)	DGPIN	NOT CONNECTED!







Lime Microsystems	
Sheet: /RF/LNA1/	
File: LNA1.sch	
Title: FrontEnd_5G	
Size: A4	Date: 10 Feb 2022
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	Rev: 1v0
	Id: 13/20



Lime Microsystems

Sheet: /RF/LNA2/

File: LNA2.sch

Title: FrontEnd_5G

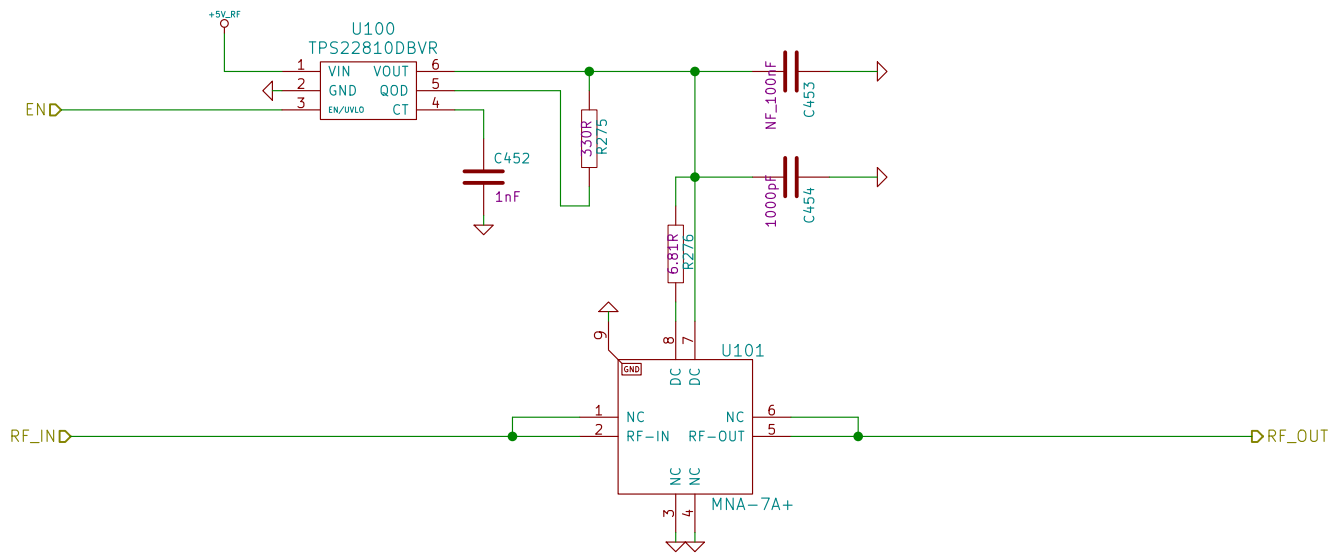
Size: A4

Date: 10 Feb 2022

Rev: 1v0

KiCad E.D.A. kicad 4.0.7-e2-637658ubuntu16.04.1

Id: 14/20



Lime Microsystems

Sheet: /RF/PDA1/

File: PDA1.sch

Title: FrontEnd_5G

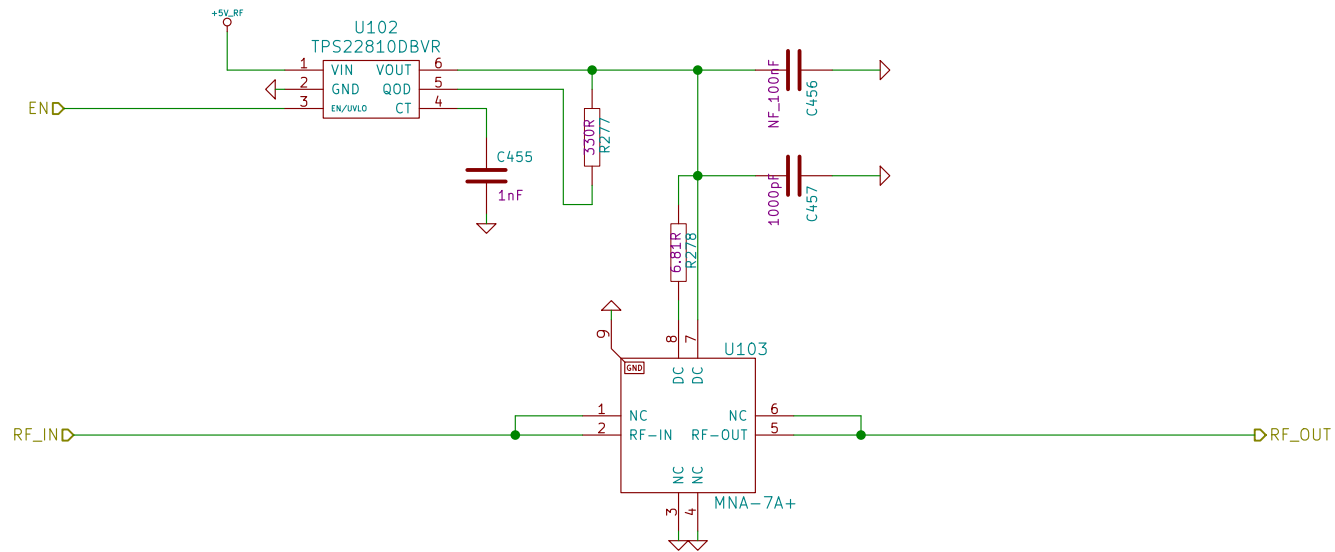
Size: A4

Date: 10 Feb 2022

Rev: 1v0

KiCad E.D.A. kicad 4.0.7-e2-637658ubuntu16.04.1

Id: 15/20



Lime Microsystems

Sheet: /RF/PDA2/
File: PDA2.sch

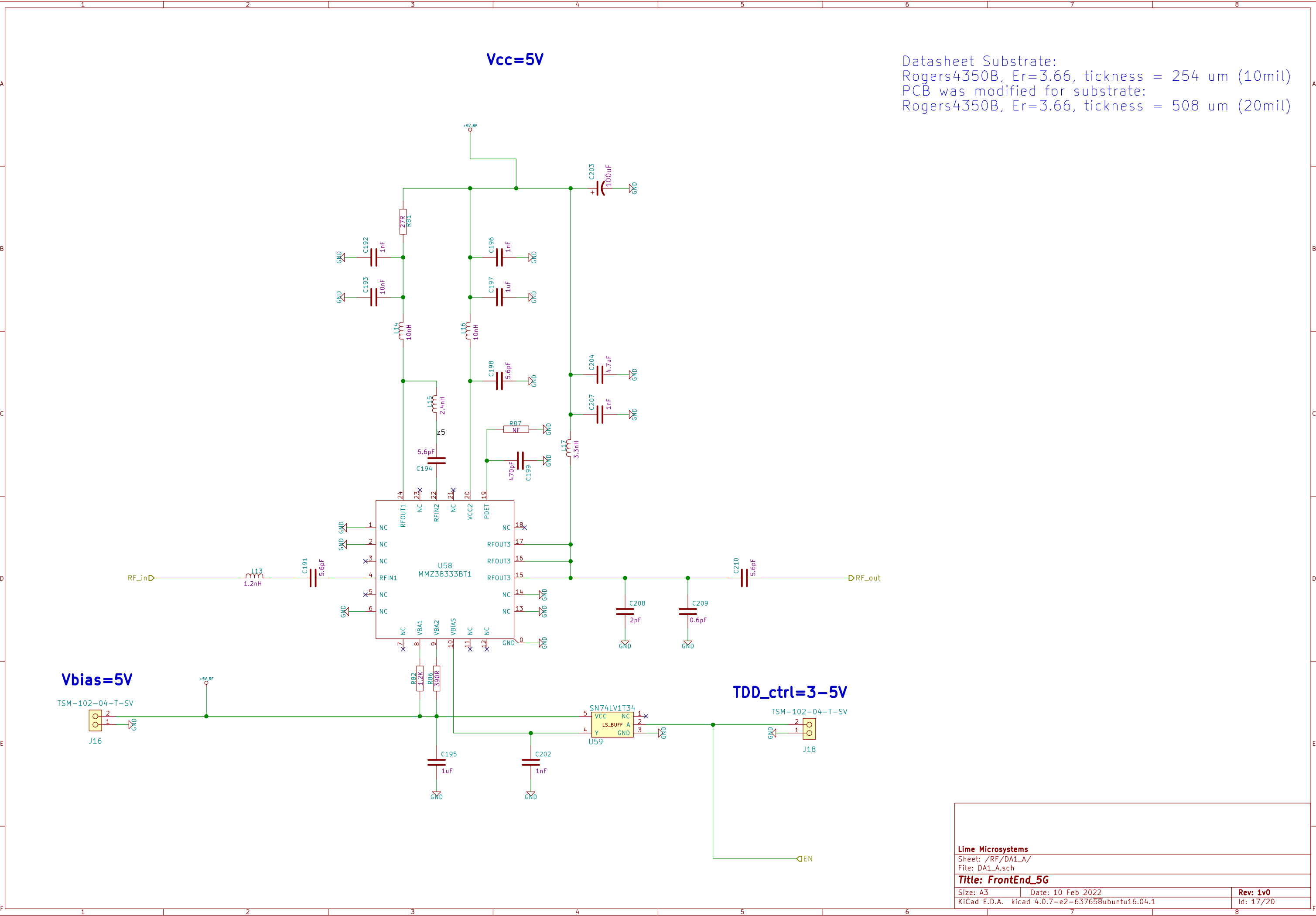
Title: FrontEnd_5G

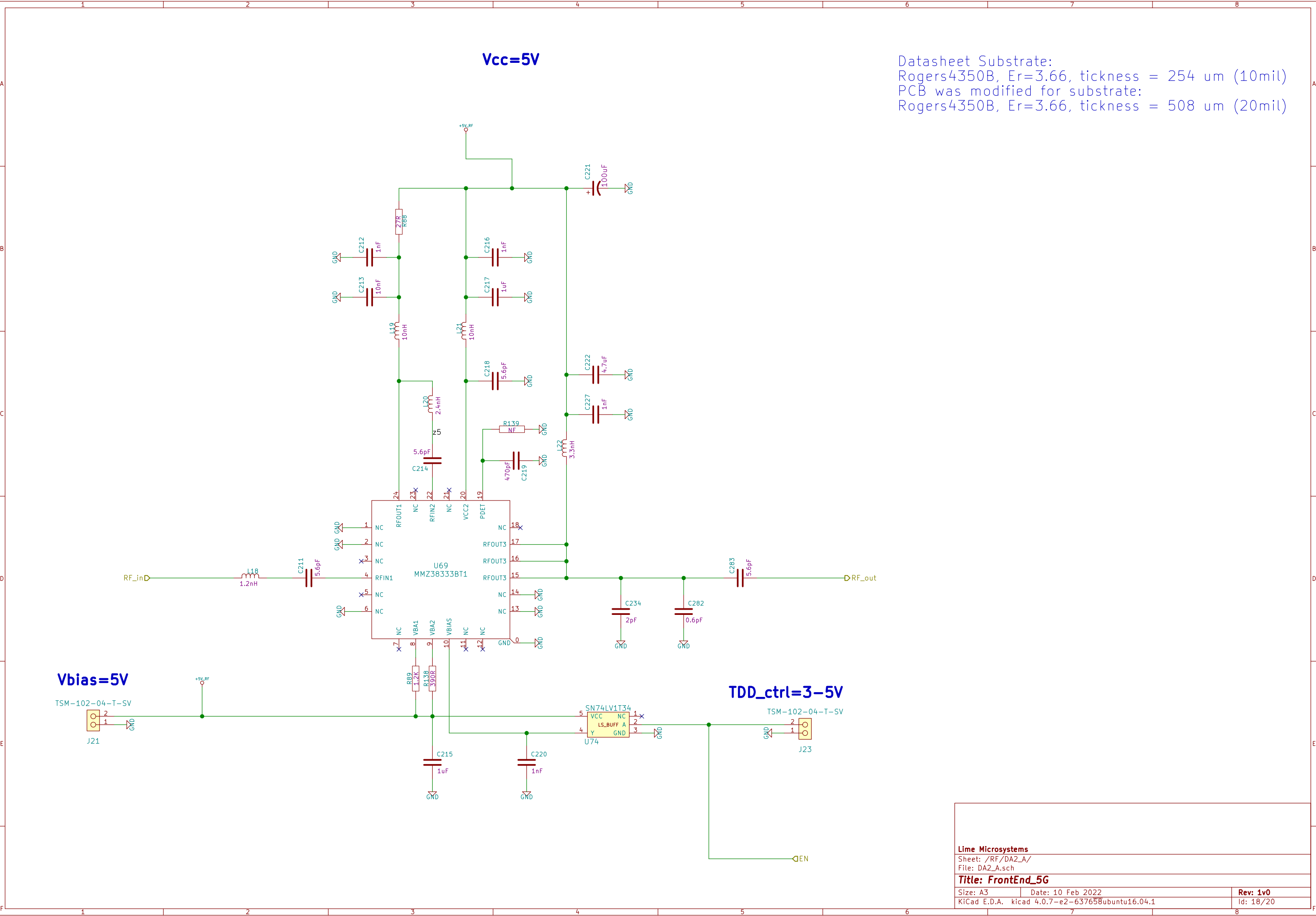
Size: A4
KiCad E.D.A. kicad 4.0.7-e2-637658ubuntu16.04.1

Date: 10 Feb 2022

Rev: 1v0

Id: 16/20





The diagram shows a PCB layout for a 5G front-end circuit. The main components are:

- PA_IN**: Input signal from the RF_IN pin of the QPA9122M PA.
- PA_OUT**: Output signal from the RF_OUT/Vcc3 pin of the QPA9122M PA.
- QPA9122M**: A 5G PA module with pins for RF_IN, RF_OUT/Vcc3, Vcc1/Vcc2, Vpd, and Vbias.
- SN74LV1T34**: A 1.8V CMOS buffer (U76) used to drive the Vpd pin.
- Power and Biasing**:
 - Vpd=1.8V**: Provided by a 1.8V regulator (TSM-102-04-T-SV) and a 10nF capacitor (C296).
 - Vcc1/Vcc2=5V**: Provided by a 5V regulator and a 10uF capacitor (C299).
 - Vcc3/Vbias=5V**: Provided by a 5V regulator and a 10uF capacitor (C302).
- Matching and Tuning**: Various capacitors (C297, C298, C299, C300, C301, C302, C304, C306) and an inductor (L40) are used for impedance matching and tuning.

The layout includes a title block in the bottom right corner:

Lime Microsystems		
Sheet: /RF/DA1_B/		
File: DA1_B.sch		
Title: FrontEnd_5G		
Size: A3	Date: 10 Feb 2022	Rev: 1v0
KiCad E.D.A. kicad 4.0.7-e2-637658ubuntu16.04.1		Id: 19/20

Sheet: /RF/DA1_B/
File: DA1_B.sch

FILE: F001210_00

Size: A3	Date: 10 Feb 2022
KiCad E.D.A. kicad 4.0.7-e2-637658ubuntu16.04.1	

Rev: 1v0
Id: 19/20

Roger 4350B, Er = 3.66, tickness = 508 um (20 mil)

